Didar Kozhikov

ROBT Homework 4.

2.

11001010 —SL→ 10010100

11001010 —SR→ 01100101

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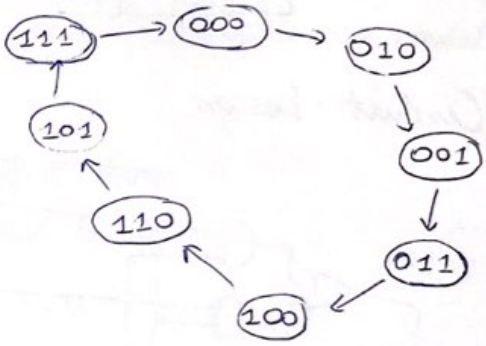
4. The desired sequence is 0 2 1 3 4 6 5 7

Converting to binary we get:

0 → 000	4 → 100
2 → 010	6 → 110
1 → 001	5 → 101
3 → 011	7 → 111

State Diagram.

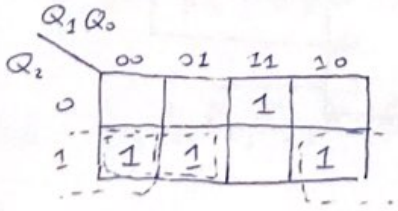


Now state table by state diagram:

Present State			Next State			Flip-flop input		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	1
0	1	0	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0
1	0	0	1	1	0	1	1	0
1	0	1	1	1	1	1	1	1
1	1	0	1	0	1	1	0	1
1	1	1	0	0	0	0	0	0

Applying Karnaugh's Map, we get:

D_2

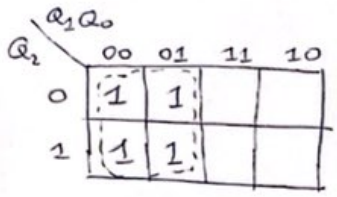


$$\rightarrow D_2 = Q_2\bar{Q}_1 + Q_2\bar{Q}_0 + Q_1Q_0 =$$

$$= Q_2(\bar{Q}_1 + \bar{Q}_0) + Q_1Q_0 = Q_2 + Q_1Q_0$$

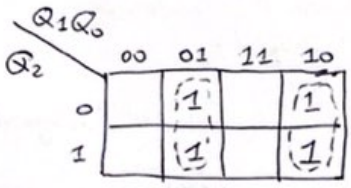
4 (continued):

D_1



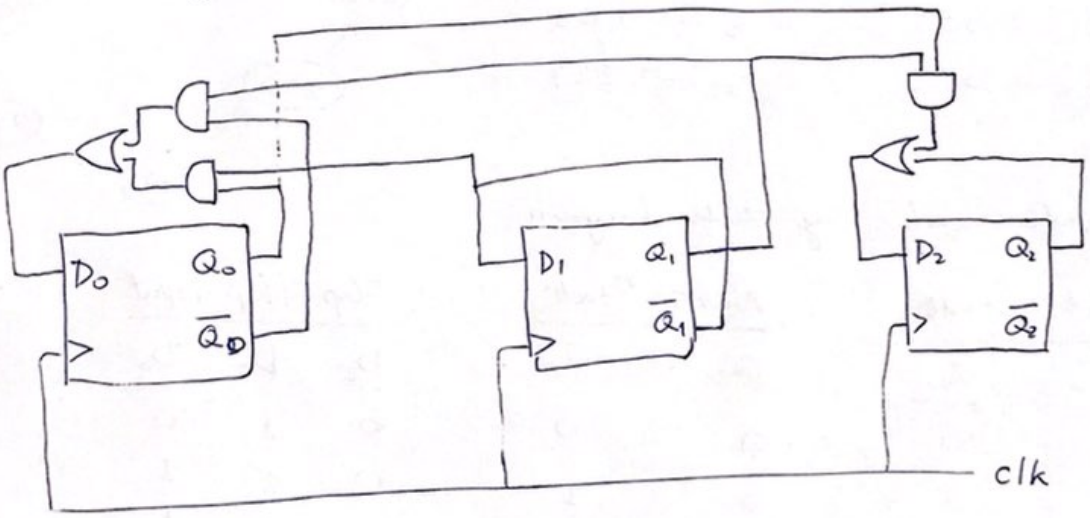
$\rightarrow \quad D_1 = \overline{Q_1}$

D_0

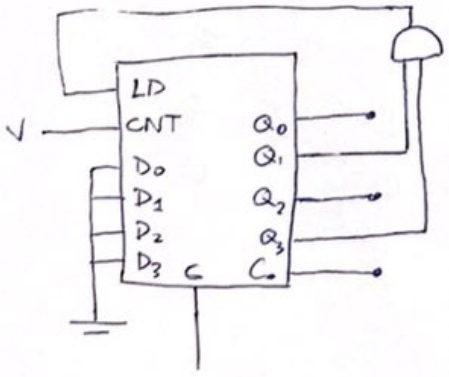


$\rightarrow \quad D_0 = \overline{Q_1} Q_0 + Q_1 \overline{Q_0}$

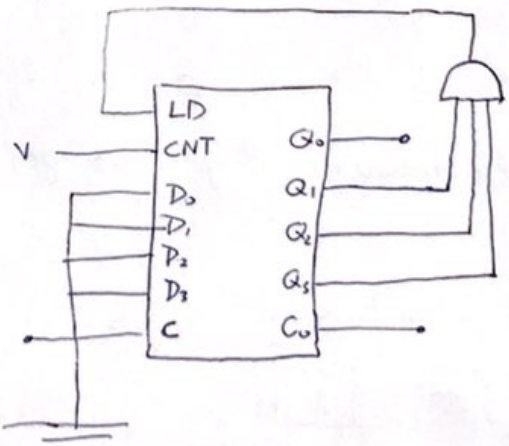
Circuit Design:



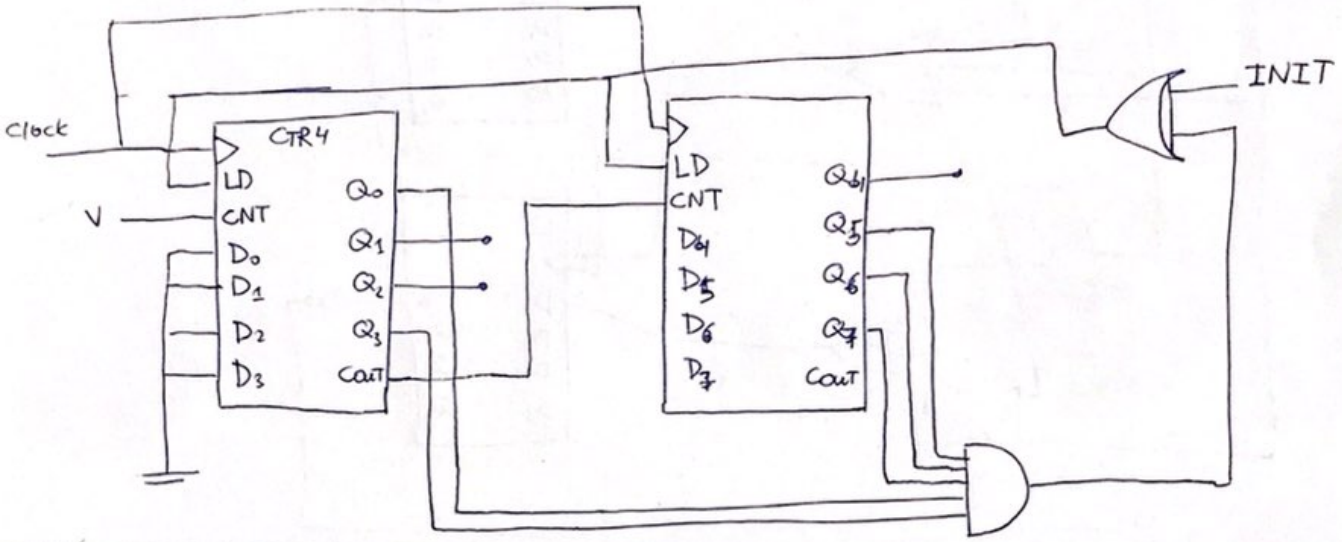
5a) Counter that counts from 0000 through 1010



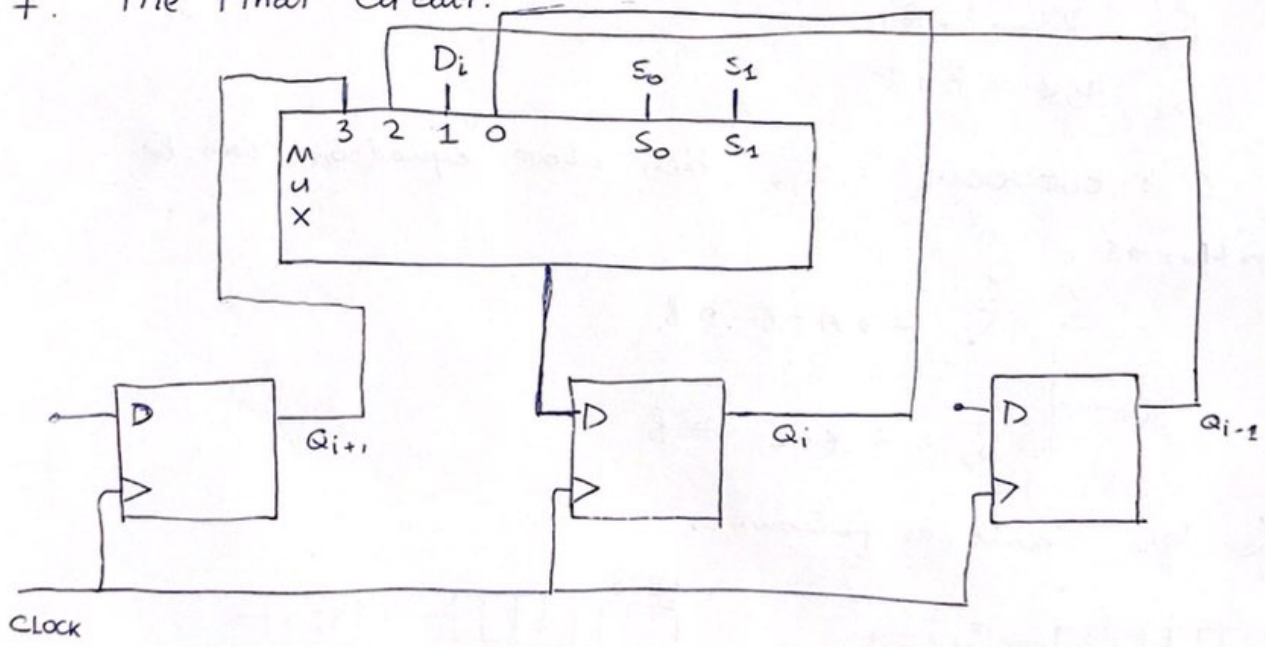
b) Counter from 0000 to 1100.



6. First we need connect the cout from the first counter to the other counter and match their clocks. Then, we using OR gate to INIT input, and the output of that gate loads the both counters. So the circuit will be as follows:

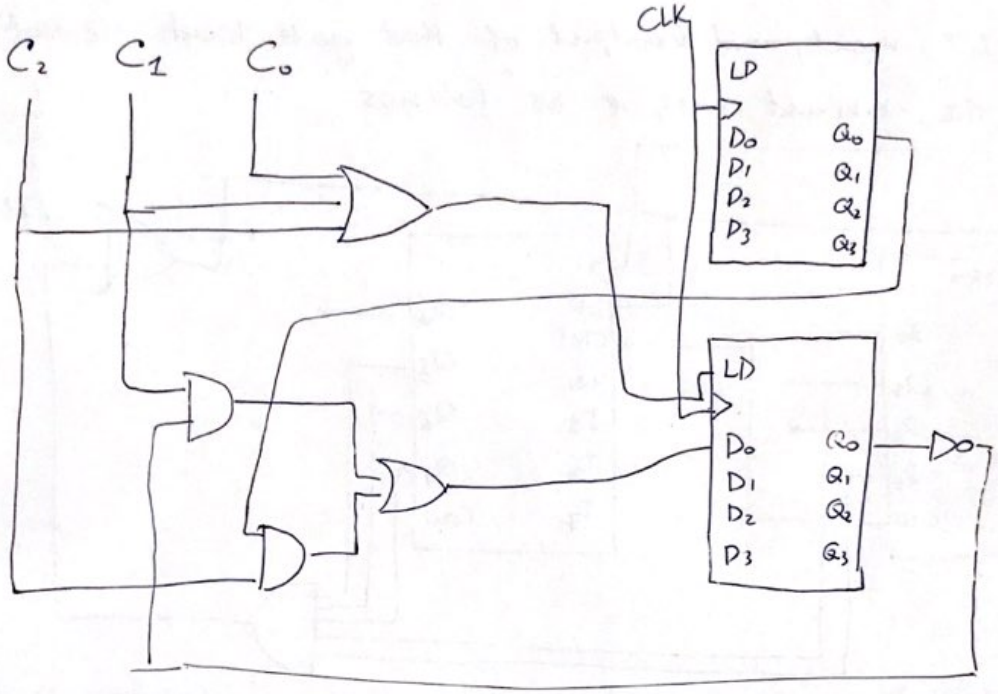


7. The Final Circuit:



Changes :
- D_i connected to Mux Data 1.
- Q_{i-1} connected to Mux Data 2.
- Q_{i+1} connected to Mux Data 3.

8. C_0: $R_2 \leftarrow 0$ C_1: $R_2 \leftarrow \overline{R_2}$ C_2: $R_2 \leftarrow R_1$



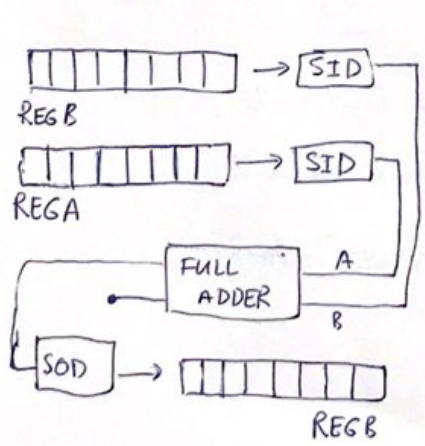
9. S_1 : $B \leftarrow B + A$

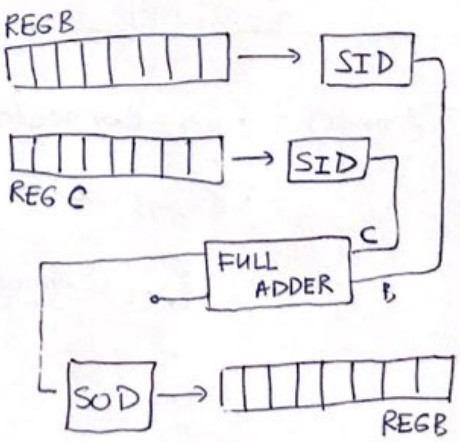
S_2 : $B \leftarrow B + 1$

Let $C = 00000001 = 1_{10}$, then above equation can be rewritten as

$$S \begin{cases} S_1 \rightarrow A + B \rightarrow B \\ S_2 \rightarrow B + C \rightarrow B \end{cases}$$

The logic circuit as follows:

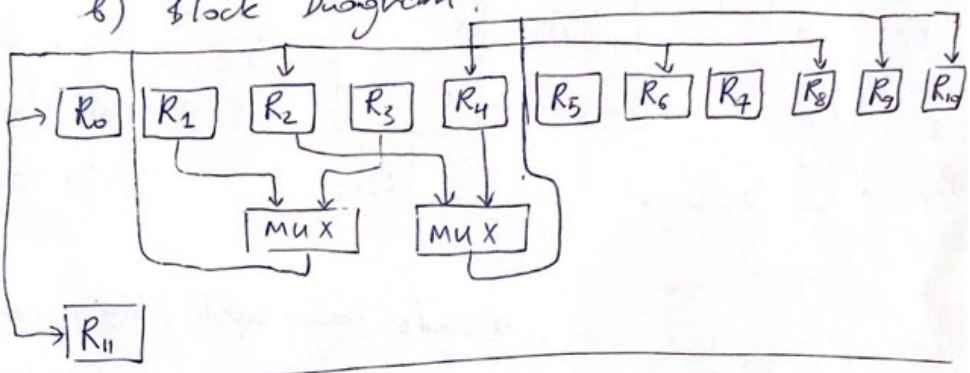




10. $R_0 \leftarrow R_1$
$R_5 \leftarrow R_1$
$R_6 \leftarrow R_2$
$R_7 \leftarrow R_3$
$R_8 \leftarrow R_3$
$R_9 \leftarrow R_4$
$R_{10} \leftarrow R_4$
$R_{11} \leftarrow R_1$

a) Using two clock cycles, the minimum number of such buses is 2.

b) Block Diagram:



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11. How many address lines and input-output data lines are needed in each case?

a) 48K × 8 ⟶ The number of address lines is 16
Data lines needed is 8.

b) 512K × 32 ⟶ Address lines = 19
Data lines = 32.

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12. a) $\frac{2\,MB}{128K \cdot 16} = \frac{2\,MB}{256\,KB} = 8$

b) with 2 byte/word, $2MB/2B = 2^{20}$, so Add bits = 20.
128K addresses per chip implies 17 address bits.

c) 3 address lines to decoder, decoder is 3-to-8 line.

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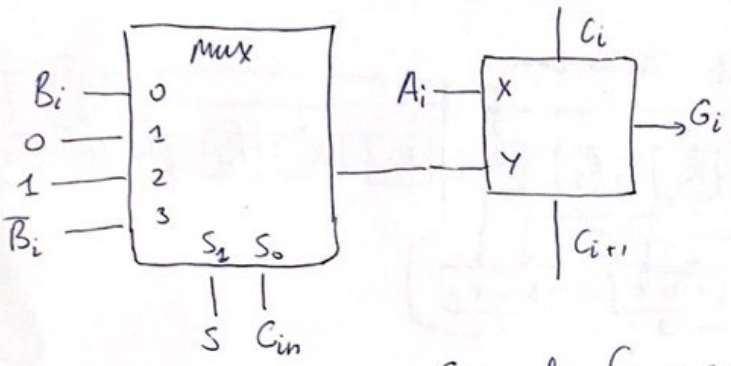
18. $R_3 \leftarrow R_3 + R_1$; $R_3 = 01100111$
$R_4 \leftarrow R_4 \wedge R_1$; $R_4 = 01110100$
$R_5 \leftarrow R_5 \oplus R_1$; $R_5 = 01101100$
$R_1 \leftarrow \overline{R_1}$; $R_1 = 11011111$

$R_1 \leftarrow R_1 + 1$; $R_1 = 11000000$
$R_6 \leftarrow R_6 + \overline{R_1} + 1$; $R_6 = 0110 \cdot 0001$
$R_7 \leftarrow R_7 + \overline{R_1} + 1$; $R_7 = 01101001$
$R_1 \leftarrow R_7$; $R_1 = 01101001$

$\{R_1, R_2, R_3, R_4, R_5, R_6, R_7\} = \{i, D, g, t, l, a, i\} \Longrightarrow$ Digital.

14.



00: $G = A + B$ (Add)

01: $G = A + 1$ (Increment)

10: $G = A - 1$ (Decrement)

11: $G = A + \overline{B} + 1$ (Substract)

Cascade four such stages, connecting the carries

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15. Output for a) 110101 is 1010

b) 101011 is 1110.

16.

	DA	AA	BA	MB	FS	MD	RW
a)	101	000	000	0	1010	0	1
b)	100	–	101	0	1110	0	1
c)	111	–	–	–	–	1	1
e)	001	001	–	1	0101	0	1
g)	010	001	011	0	1010	0	1

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17. a) $R_5 \leftarrow R_4 \wedge R_5$ $R_5 = 0000\ 0100$

b) $R_6 \leftarrow R_2 + R_4 + 1$ $R_6 = 1111\ 1110$

c) $R_5 \leftarrow R_0$ $R_5 = 0000\ 0000$