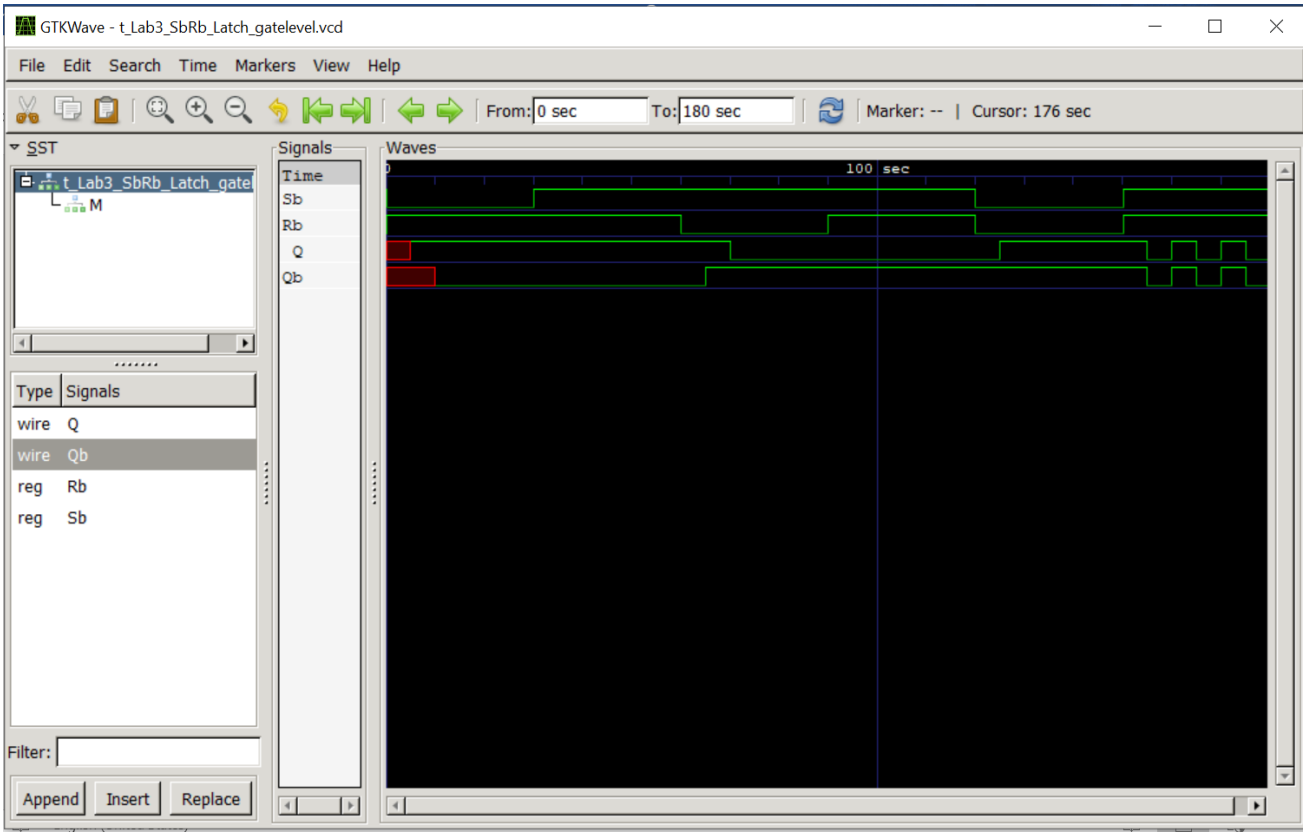
Digital Circuit Design Lab3 Report

1. S'R'- Latch

Waveform



Correctness of the waveform

I used the values on the waveform to form a function table attached below to detect the correctness of the waveform. From the function table, we can see that its result is identical with the characteristic table of $\bar{S}\bar{R}$-Latch (also attached below).

Since there's an input of 0 at the beginning for Q, the NAND gate can generate value by only having one input. Therefore, the delay will be the delay time of only one NAND gate, which is 5 time-units, proving that the delay time for Q is correct. Different from Q, the input for $\bar{Q}$ is 1, so the gate needs two input values to generate output $\bar{Q}$, which is 10 time-units.

Function Table

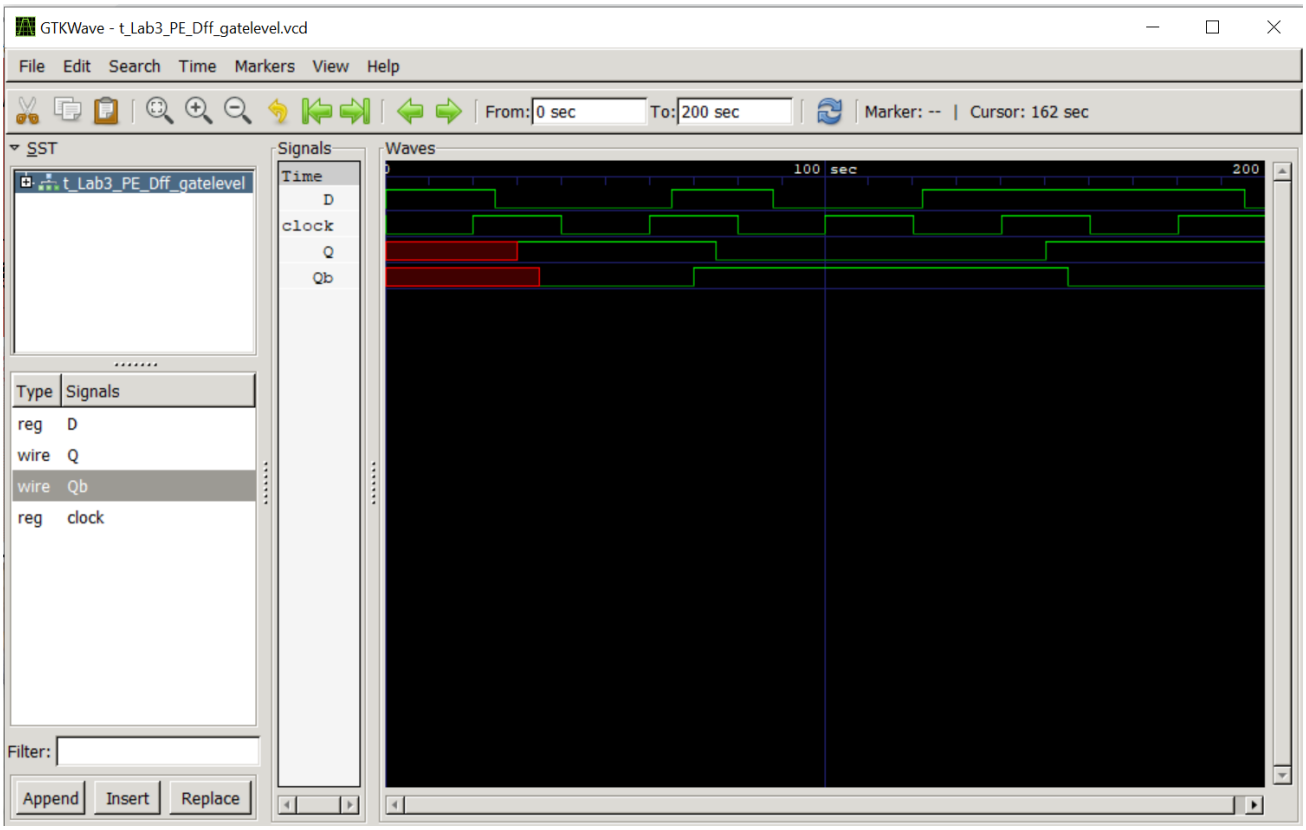
$\bar{S}\,\bar{R}$	$Q\,\bar{Q}$	$Q^+\,\bar{Q}^+$
0 1	-	1 0
1 1	1 0	1 0
1 0	1 0	0 1
1 1	0 1	0 1
0 0	0 1	1 1 -> Forbidden
1 1	1 1	Undefined

Characteristic Table

$\bar{S}$	$\bar{R}$	$Q^+\,\bar{Q}^+$
1	1	No Change ($Q^+ = Q$)
1	0	Reset ($Q^+ = 0$)
0	1	Set ($Q^+ = 1$)
0	0	Indeterminate

2. D-Type Positive Edge Trigger Flip-Flop

Waveform



Correctness of the waveform

The waveform generated above is correct since the function table derived from it is equivalent to the result of the characteristic table of D flip-flop (both tables are attached below).

For the propagation delay, the delay time for the outputs is time length before the positive edge and the holding time plus the propagation delay of the $\bar{S}\bar{R}$-Latch. The holding time equals to the delay time of an NAND gate (5 time-units). Moreover, the propagation delay of Q and $\bar{Q}$ are different in the $\bar{S}\bar{R}$-Latch explained in the previous question. Therefore, the propagation delay time for Q and $\bar{Q}$ are 20 + 5 + 5 = 30 and 20 + 5 + 10 = 35 time-units.

Function Table

D	Q^+ $\bar{Q}^+$
1	1 0
0	0 1
1	1 0
0	0 1
1	1 0
0	0 1

Characteristic Table

D	Q^+
1	1
0	0

2. Mealy-Type Synchronous Sequential Circuit

Design Process

From the given state diagram and state table, we can first derive the Transition table. Next, we can generate the Flip-Flop input equations together with the output equations by the K-Map method. Lastly, the sequential circuit can be derived. The details are as below.

(1) Transition Table

Present State	Next State		Output Z	
$A_2A_1A_0$	x = 0	x = 1	x = 0	x = 1
0 0 0	0 0 1	1 0 0	0	0
0 0 1	0 0 1	0 1 0	0	0
0 1 0	0 1 1	1 0 0	1	0
0 1 1	1 0 1	0 1 0	0	0
1 0 0	0 1 1	1 0 0	0	0
1 0 1	0 0 1	0 1 0	0	1

(2) Derived K-Maps

D_2

$A_2A_1\backslash A_0x$				
		1		
		1		1
	x	x	x	x
		1		

D_1

$A_2A_1\backslash A_0x$				
			1	
	1		1	
	x	x	x	x
	1		1	

D_0

$A_2A_1\backslash A_0x$				
	1			1
	1			1
	x	x	x	x
	1			1

Z

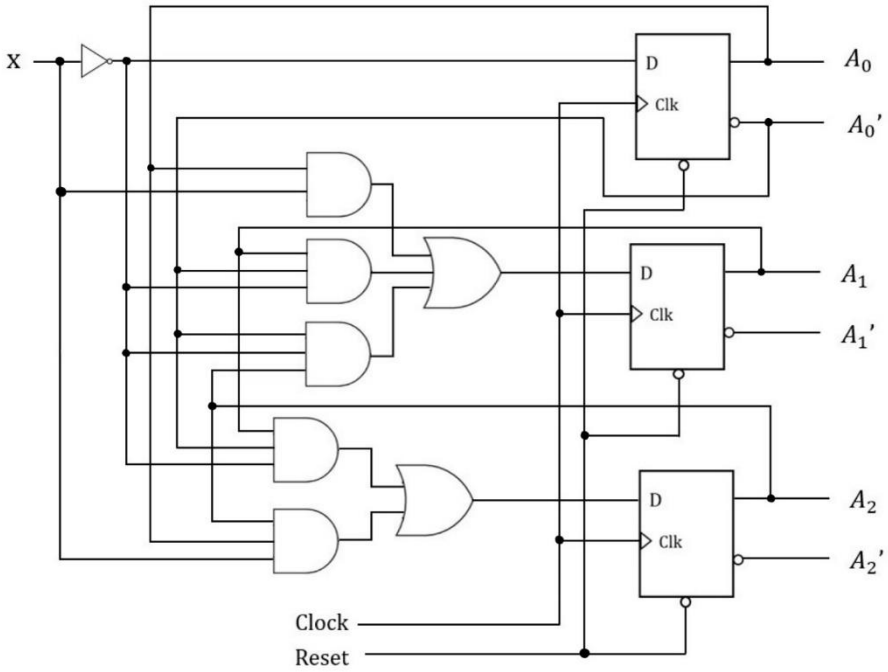
$A_2A_1\backslash A_0x$				
	1			
	x	x	x	x
			1	

(3) Flip-Flop Input Equations & Output Equations

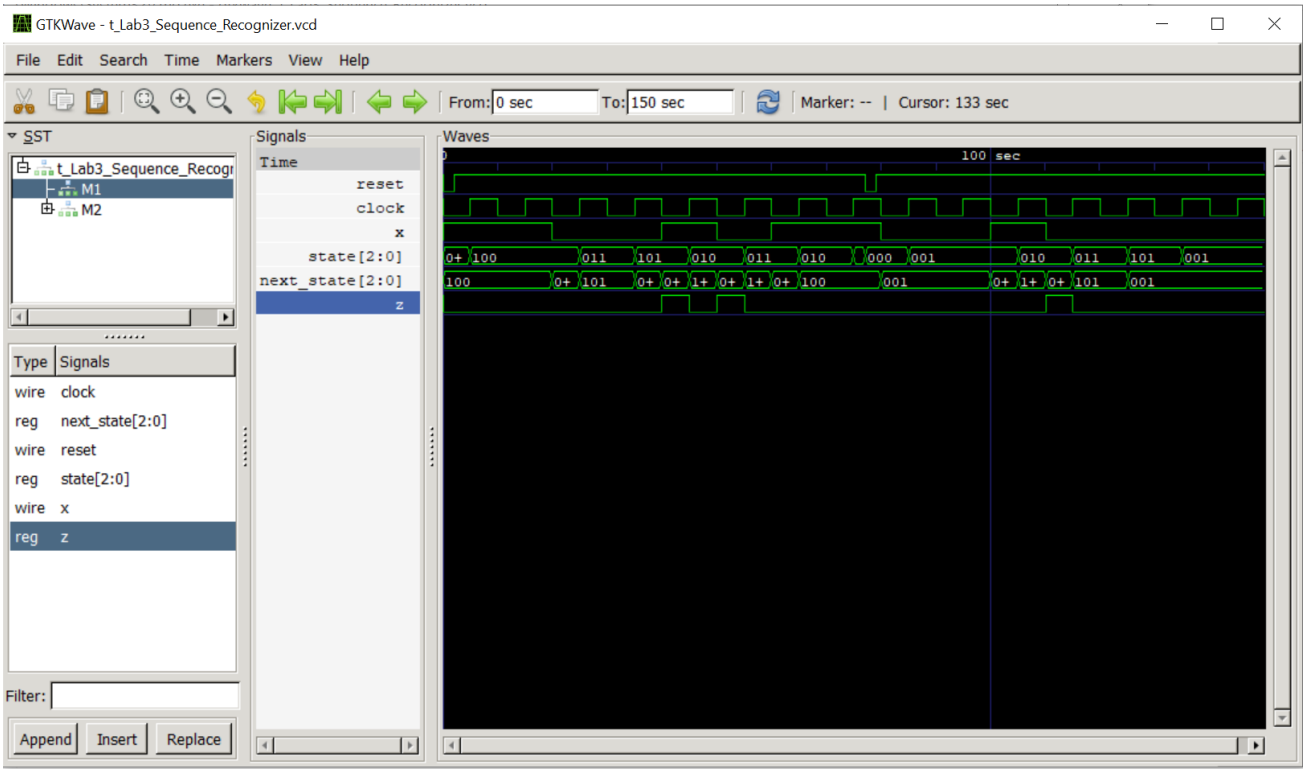
$$D_2 = A_2{}^+ = A_0{}'x + A_1A_0x' \qquad D_0 = A_0{}^+ = x'$$

$$D_1 = A_1{}^+ = A_0x + A_1A_0{}'x + A_2A_0{}'x' \qquad Z = A_1A_0{}'x' + A_2A_0x$$

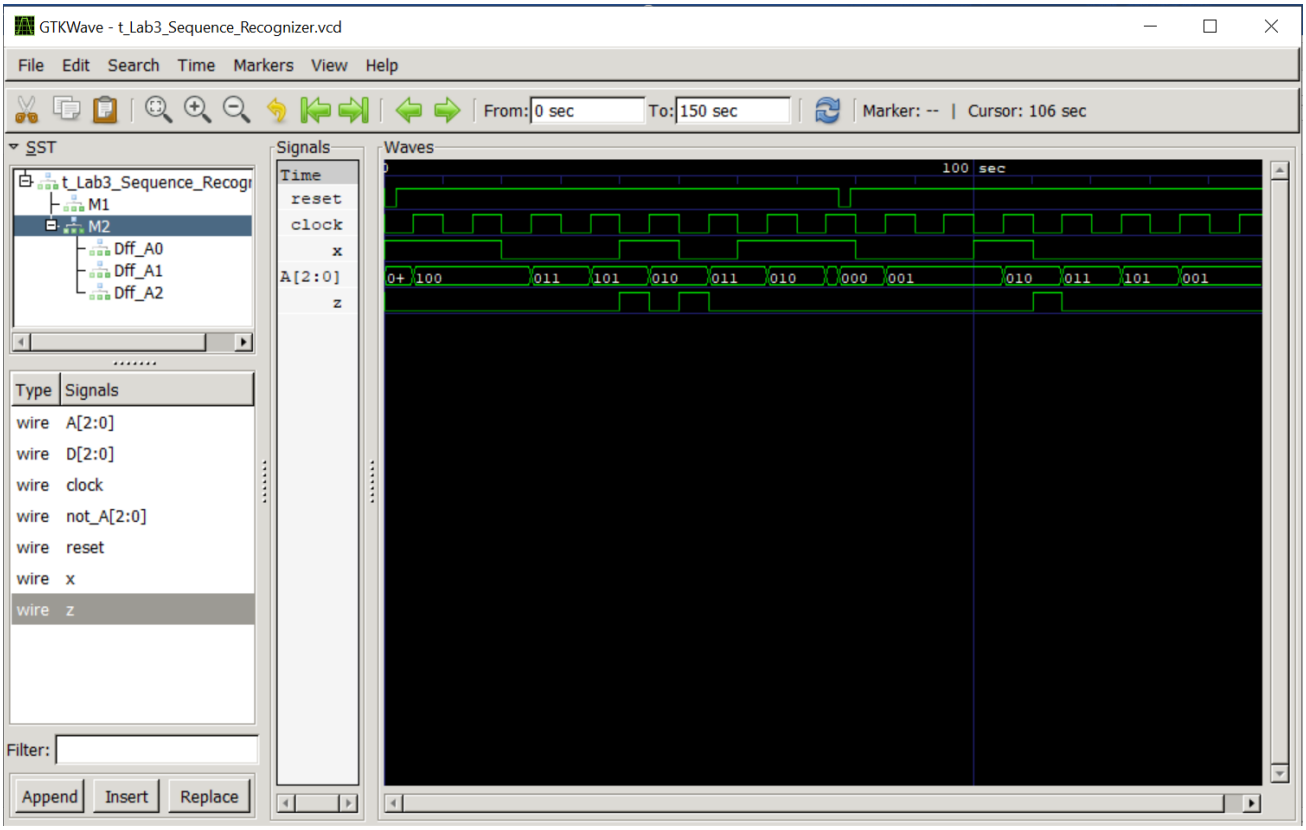
(4) Sequential Circuit



Waveform of the state diagram model



Waveform of the structural model



Testbench Design

I design the testbench by going through two paths of the state diagram:

Path1: S0 – S4 – S4 – S3 – S5 – S2 – S3 – S2 – S4

Path2: S0 – S1 – S1 – S2 – S3 – S5 – S1

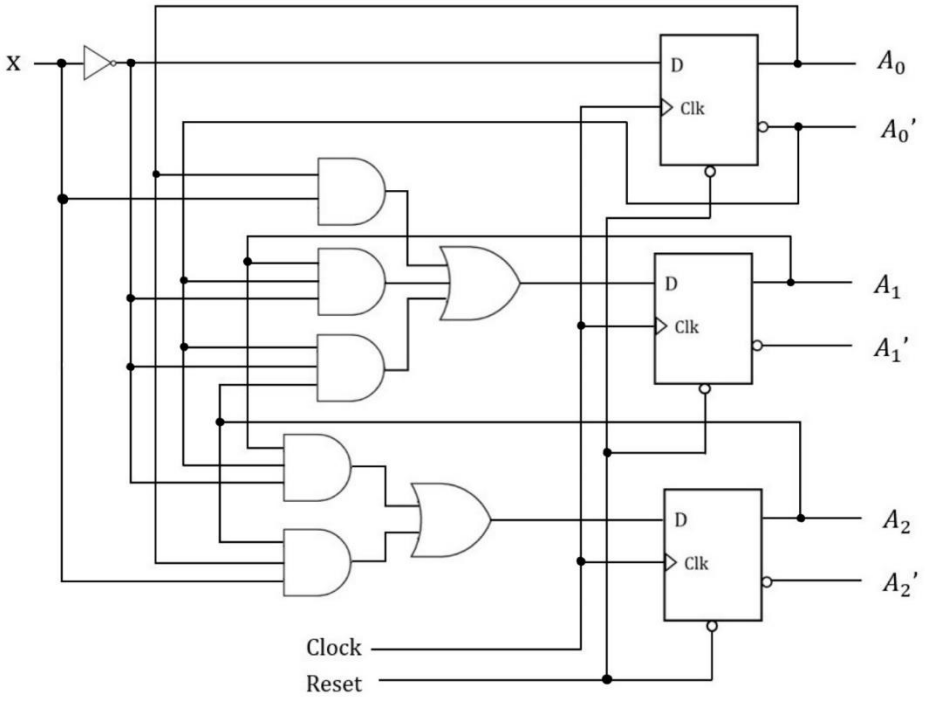
The period of the clock is set to be 10 time-units

Correctness of the waveforms

The first waveform is correct because the results of state and next state are equivalent to the state diagram given and the derived transition table. The second waveform is correct since the output z equals to 1 as the sequence of x appears 010 and 1001.

4. Reflection

Throughout this lab experience, I get to really implement sequential circuits by HDL. This helps me get more familiar with the mechanisms behind those circuits such as the SR-Latch, D Flip-Flop and so on. Although I spent quite a long time figuring out how the Verilog code works for the Mealy-Type circuit, the overall experience was beneficial to me.


X
D
Clk
A_0
A_0'
D
Clk
A_1
A_1'
D
Clk
A_2
A_2'
Clock
Reset