ECE3390 Assignment 3
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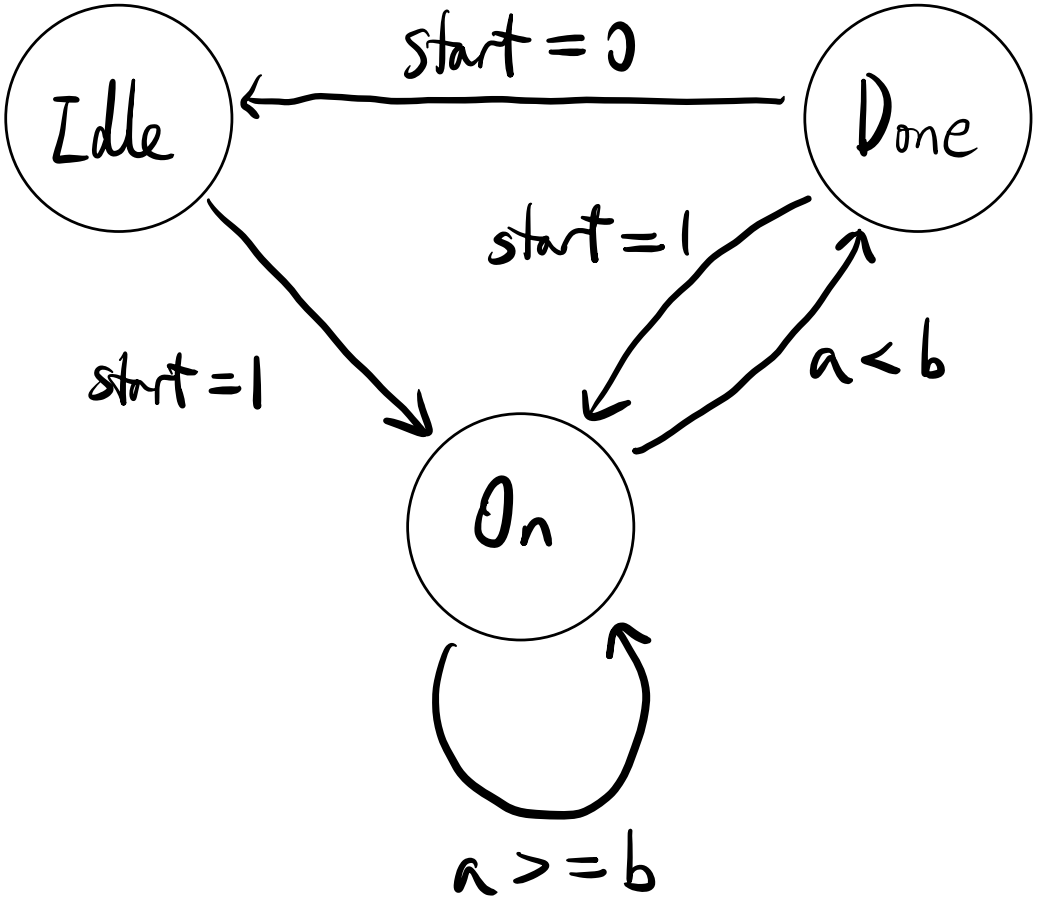
Part4

The state machine

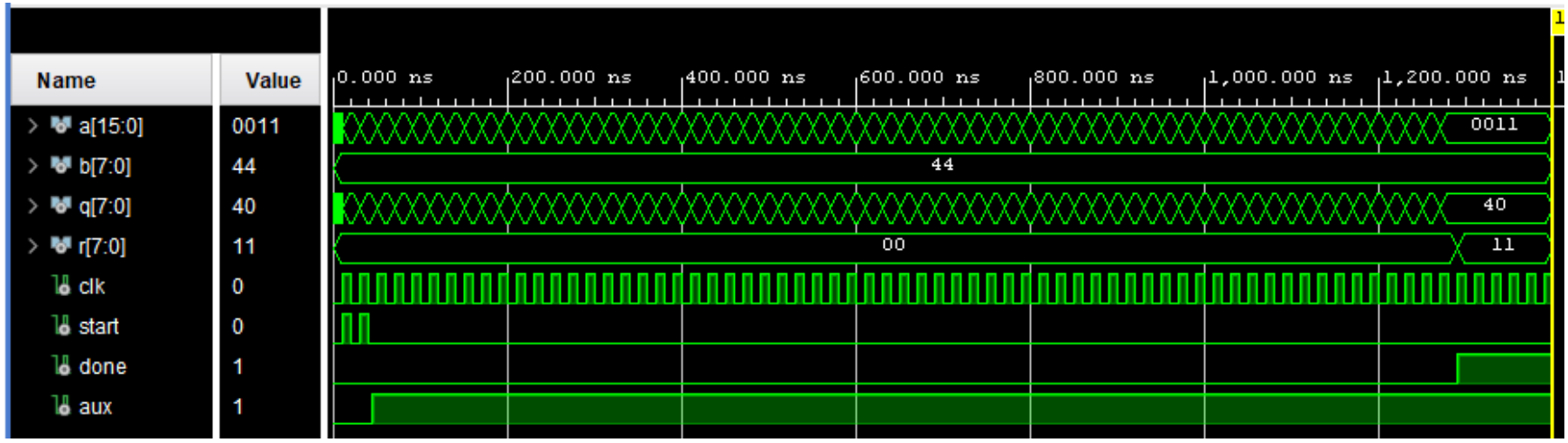


Only in Done state is the output valid

The code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE ieee.numeric_std.ALL;

entity mydivider is
end mydivider;

architecture Behavioral of mydivider is
signal a: unsigned(15 downto 0) := x"1111";
signal b: unsigned(7 downto 0) := x"44";
signal q : unsigned(7 downto 0) := x"00";
signal r : unsigned(7 downto 0) := x"00";
signal clk, start, done, aux : bit :='0';

begin
clk <= not clk after 10 ns;
aux <= '1' after 45 ns;--auxiliary signal used to generate start signal
start <= clk and not aux;
process(clk,start) begin

    if (clk'event and clk='1') then
        if (start='1') then
            r<=x"00";
            q<=x"00";
            done<='0';
        else
            if (a<b)then
                r<=a(7 downto 0);
                done<='1';
            else
                a<=a-b;
                q<=q+1;
            end if;
        end if;
    end if;
end process;
END;
```

The waveform



computes 1111/44=40…11