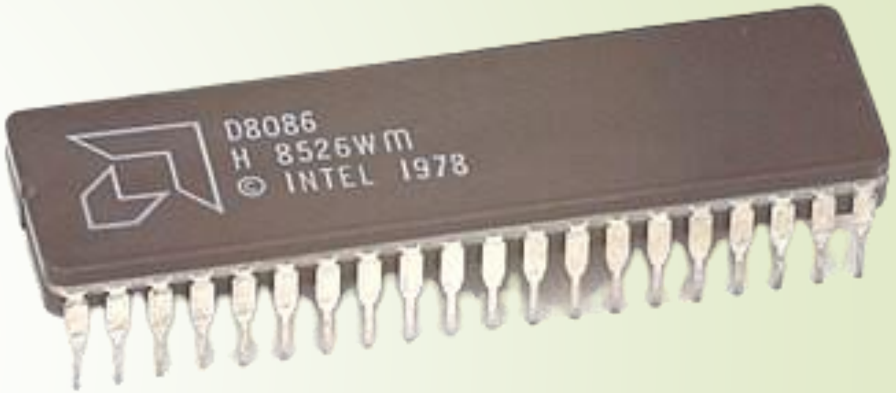
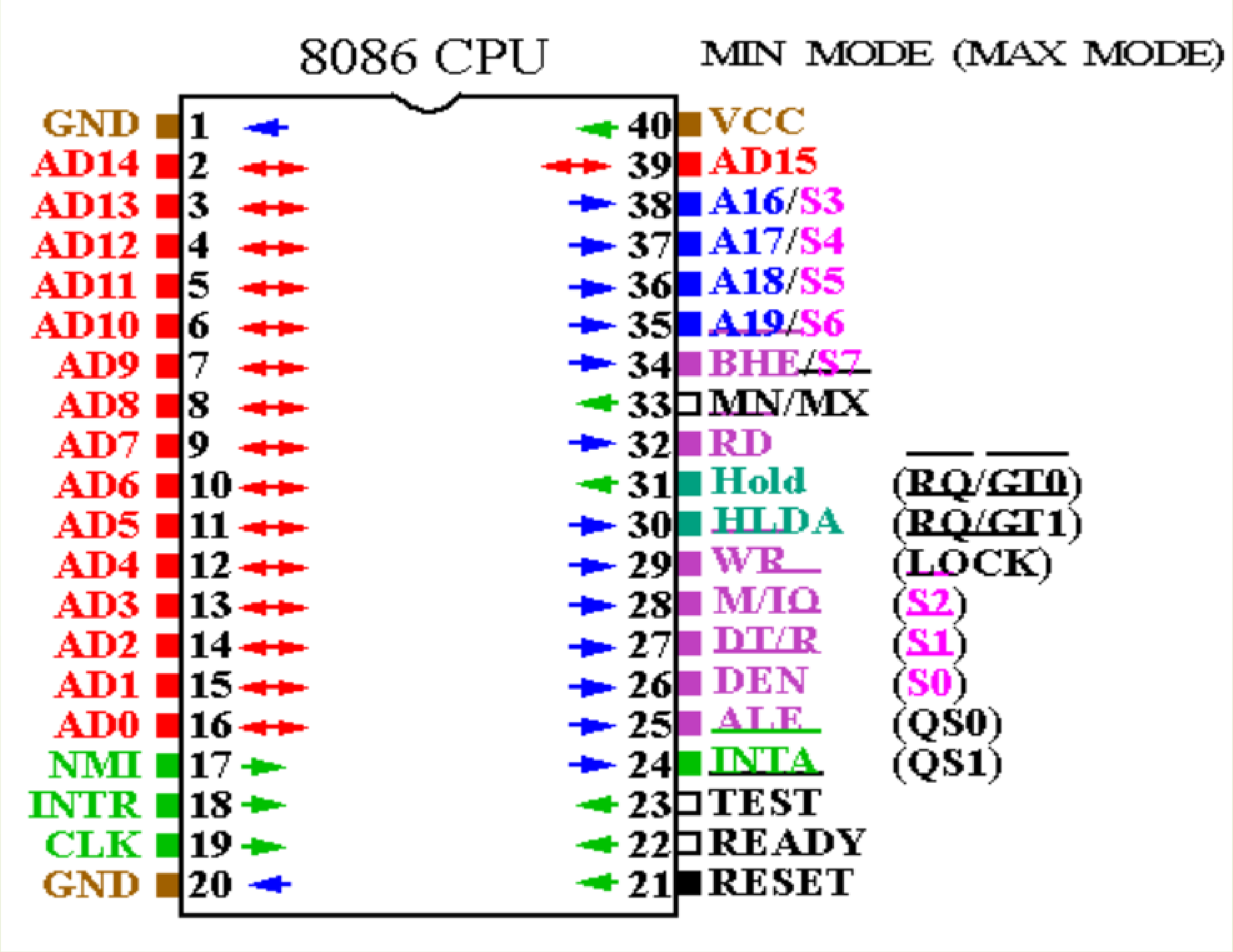
Chapter Two

The 8086 Microprocessor and Its Architecture



8086 Hardware Specifications

- **Pin Diagram and Pin description of 8086:** Figure below illustrates the pin diagram of the 8086 microprocessors.
- The 8086 is Packaged in 40-pin **dual in-line** packages (DIPs).



Cont'd…

Power Supply Requirements

- The 8086 microprocessors require +5.0V with a supply voltage tolerance of ±10 percent.
- The 8086 uses a maximum supply current of **360 mA**
- The microprocessor operate in ambient temperatures of between 32° F and 180° F.

DC Characteristics

- It is impossible to connect anything to the pins of the microprocessor without knowing the input current requirement for an input pin and the output current drive capability for an output pin.
- This knowledge allows the hardware designer to select the proper interface components for use with the microprocessor without the fear of damaging anything.

Cont'd…

Input Characteristics.

- The input characteristics of these microprocessors are compatible with all the standard logic components available today.

- Table below depicts the input voltage levels and the input current requirements for any input pin on either microprocessor.
- The input current levels are very small because the inputs are the gate connections of MOSFETs and represent only leakage currents.

Logic Level	**Voltage**	**Current**
0	0.8 V maximum	±10 μA maximum
1	2.0 V minimum	±10 μA maximum

Cont’d…

Output Characteristics.

- Table below illustrates the output characteristics of all the output pins of these microprocessors.
- The logic 1 voltage level of the 8086 is compatible with that of most standard logic families, but the logic 0 level is not.
- Standard logic circuits have a maximum logic 0 voltage of **0.4V**, and the 8086 has a maximum of **0.45V**.
- Thus, there is a difference of **0.05V**.
- This difference reduces the noise immunity from a standard level of 400 mV (0.8V – 0.45V) to 350mV.
- The noise immunity is the difference between the logic 0 output voltage and the logic 0 input voltage levels.

Logic Level	Voltage	Current
0	0.45 V maximum	2.0 mA maximum
1	2.4 V minimum	-400 µA maximum

Cont'd…

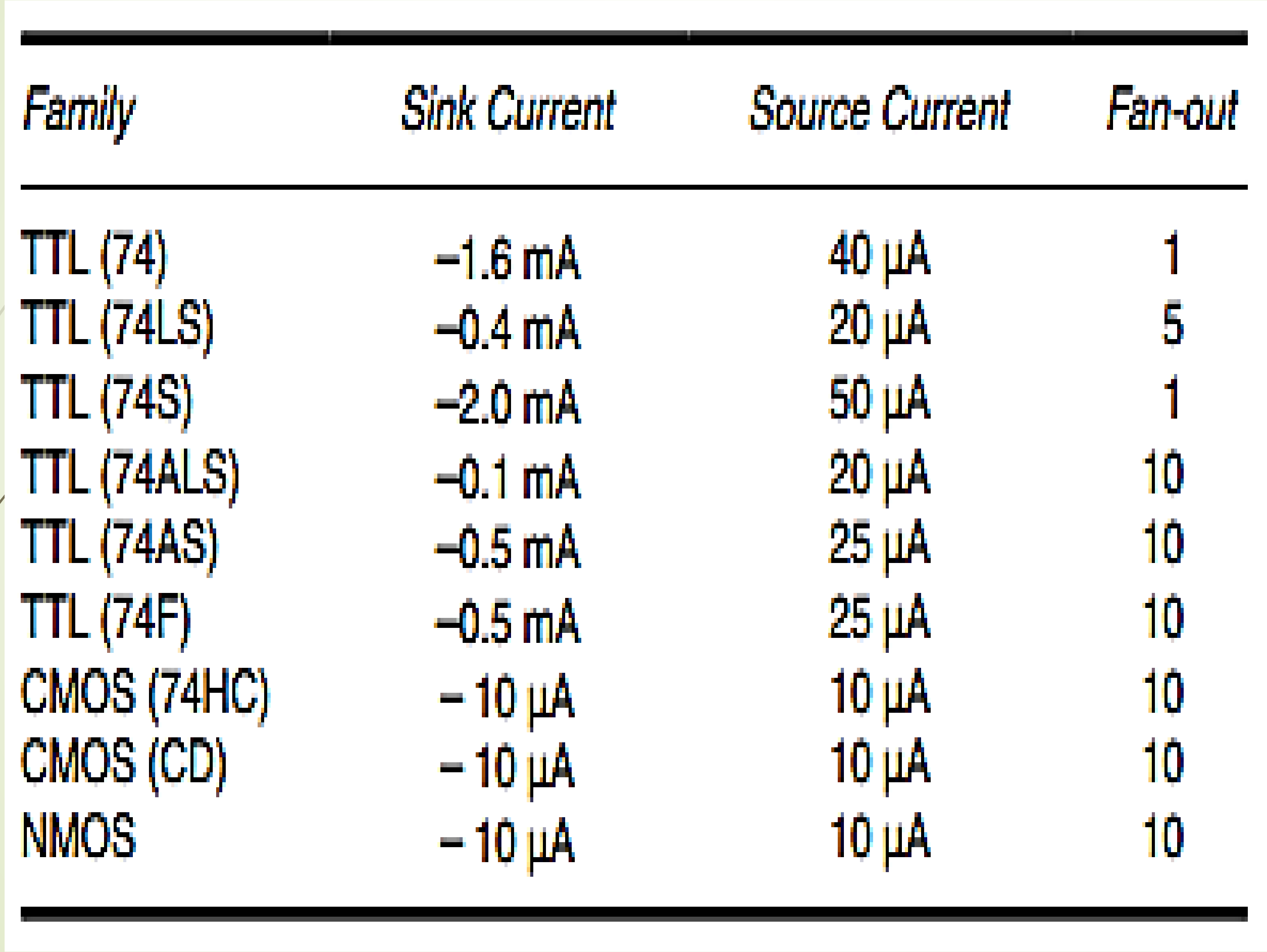
- The reduction in noise immunity may result in problems with long wire connections or too many loads.
- It is therefore recommended that no more than 10 loads of any type or combination be connected to an output pin without buffering.
- If this loading factor is exceeded, noise will begin to take its toll in timing problems.

- Table below lists some of the more common logic families and the recommended fan-out from the 8086.
- The best choice of component types for the connection to an 8086 output pin is an LS, 74ALS, or 74HC logic component.

Fan-out

- Note that some of the fan-out currents calculate to more than 10-unit loads.
- It is therefore recommended that if a fan-out of more than 10-unit loads is required, the system should be buffered.

Cont'd...



Family	*Sink Current*	*Source Current*	*Fan-out*
TTL (74)	−1.6 mA	40 µA	1
TTL (74LS)	−0.4 mA	20 µA	5
TTL (74S)	−2.0 mA	50 µA	1
TTL (74ALS)	−0.1 mA	20 µA	10
TTL (74AS)	−0.5 mA	25 µA	10
TTL (74F)	−0.5 mA	25 µA	10
CMOS (74HC)	− 10 µA	10 µA	10
CMOS (CD)	− 10 µA	10 µA	10
NMOS	− 10 µA	10 µA	10

Pin Connections

AD15–AD8 :

- The 8086 **address/data bus** lines compose the upper multiplexed address/data bus on the 8086.
- These lines contain address bits A15–A8 whenever ALE is a logic 1, and data bus connections D15–D8 when ALE is a logic 0.

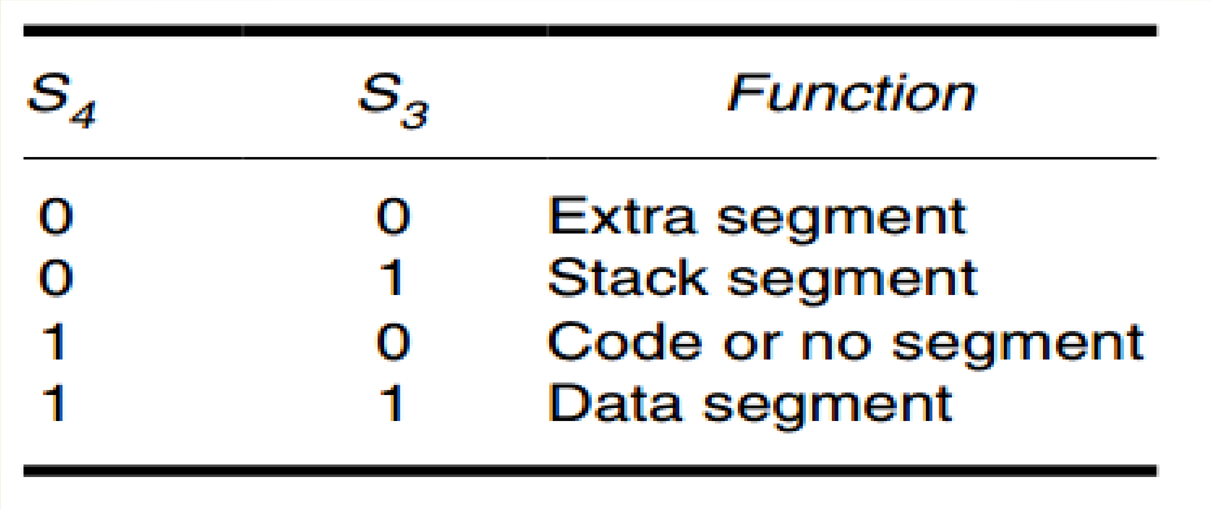
- These pins enter a high-impedance state when a hold acknowledge occurs.

A19/S6–A16/S3

- The **address/status bus** bits are multiplexed to provide address signals A19–A16 and status bits S6–S3.
- These pins also attain a high-impedance state during the hold acknowledge.
- Status bit S6 is always a logic 0, bit S5 indicates the condition of the IF flag bit, and S4 and S3 show which segment is accessed during the current bus cycle.

Cont'd…

- These two status bits could be used to address four separate 1M byte memory banks by decoding them as A21 and A20.
- Function of status bits S3 and S4 is shown in the table below.



S_4	S_3	*Function*
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment

NMI

- The **non-maskable interrupt** input is like INTR except that the NMI interrupt does not check to see whether the IF flag bit is a logic 1.
- If NMI is activated, this interrupt input uses interrupt vector 2.

Cont'd…

$\overline{RD}$

- Whenever the **read signal** is **a logic 0**, the data bus is receptive to data from the memory or I/O devices connected to the system.
- This pin floats to its high-impedance state during a hold acknowledge.

READY

- The **READY** input is controlled to insert wait states into the timing of the microprocessor.
- If the READY pin is placed at a **logic 0 level**, the micro processor enters wait states and remains idle.
- If the READY pin is placed at a **logic 1 level**, it has no effect on the operation of the microprocessor.

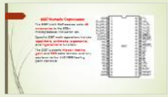
INTR

- **Interrupt request** is used to request a hardware interrupt.
- If INTR is held high when IF = 1, the 8086 enters an interrupt acknowledge cycle ($\overline{INTA}$ becomes active) after the current instruction has completed execution.

Cont’d…

$\overline{TEST}$

- The **Test** pin is an input that is tested by the WAIT instruction.
- If $\overline{TEST}$ is a logic 0, the WAIT instruction functions as an NOP and if $\overline{TEST}$ is a logic 1, the WAIT instruction waits for $\overline{TEST}$ to become a logic 0.
- The $\overline{TEST}$ pin is most often connected to the 8087 numeric coprocessor.



RESET

- The **reset** input causes the microprocessor to reset itself if this pin is held high for a minimum of four clocking periods.
- Whenever the 8086 is reset, it begins executing instructions at memory location FFFFOH and disables future interrupts by clearing the IF flag bit.

$\overline{BHE}$/S7

- The **bus high enable** pin is used in the 8086 to enable the most-significant data bus bits (D15–D8) during a read or a write operation.
- The state of S7 is always a logic 1.

Cont'd…

CLK

- The **clock** pin provides the basic timing signal to the microprocessor.
- The clock signal must have a duty cycle of 33 % (high for one third of the clocking period and low for two thirds) to provide proper internal timing for the 8086.

VCC

- This **power supply** input provides a +5.0 V, ±10 % signal to the microprocessor.

GND

- The **ground** connection is the return for the power supply.
- The 8086 microprocessors have two pins labeled GND—both must be connected to ground for proper operation.

MN/$\overline{MX}$

- The **minimum/maximum** mode pin selects either minimum mode or maximum mode operation for the microprocessor.
- If minimum mode is selected, the **MN/$\overline{MX}$** pin must be connected directly to +5.0 V.

Minimum Mode Pins.

- Minimum mode operation of the 8086 is obtained by connecting the **MN**/$\overline{\boldsymbol{MX}}$ pin directly to +5.0 V.
- Do not connect this pin to +5.0 V through a pull-up register, or it will not function correctly.

M/$\overline{\boldsymbol{IO}}$

- The **M**/$\overline{\boldsymbol{IO}}$ pin selects memory or I/O.
- This pin indicates that the microprocessor address bus contains either a memory address or an I/O port address.
- This pin is at its high-impedance state during a hold acknowledge.

$\overline{\boldsymbol{WR}}$

- The **write line** is a strobe that indicates that the 8086 is outputting data to a memory or I/O device.
- During the time that the $\overline{\boldsymbol{WR}}$ is a logic 0, the data bus contains valid data for memory or I/O.
- This pin floats to a high impedance during a hold acknowledge.

Cont'd...

$\overline{INTA}$

- The **interrupt acknowledge** signal is a response to the INTR input pin.
- The $\overline{INTA}$ pin is normally used to gate the interrupt vector number onto the data bus in response to an interrupt request.

ALE

- **Address latch enable** shows that the 8086 address/data bus contains address information.
- This address can be a memory address or an I/O port number.
- The ALE signal does not float during a hold acknowledge.

DT/ $\overline{R}$

- The **data transmit/receive** signal shows that the microprocessor data bus is transmitting (**DT/$\overline{R}$=1**) or receiving (**DT/$\overline{R}$=0**) data.
- This signal is used to enable external data bus buffers.

$\overline{DEN}$

- **Data bus enable** activates external data bus buffers.

Cont'd...

HOLD

- The **hold input** requests a direct memory access (DMA).
  - Direct Memory Access is a feature of computer systems that allows certain hardware subsystems to access main system memory independently of the central processing unit (CPU)
- If the HOLD signal is a logic 1, the microprocessor stops executing software and places its address, data, and control bus at the high-impedance state.
- If the HOLD pin is a logic 0, the microprocessor executes software normally.

HLDA

- **Hold acknowledge** indicates that the 8086 has entered the hold state.

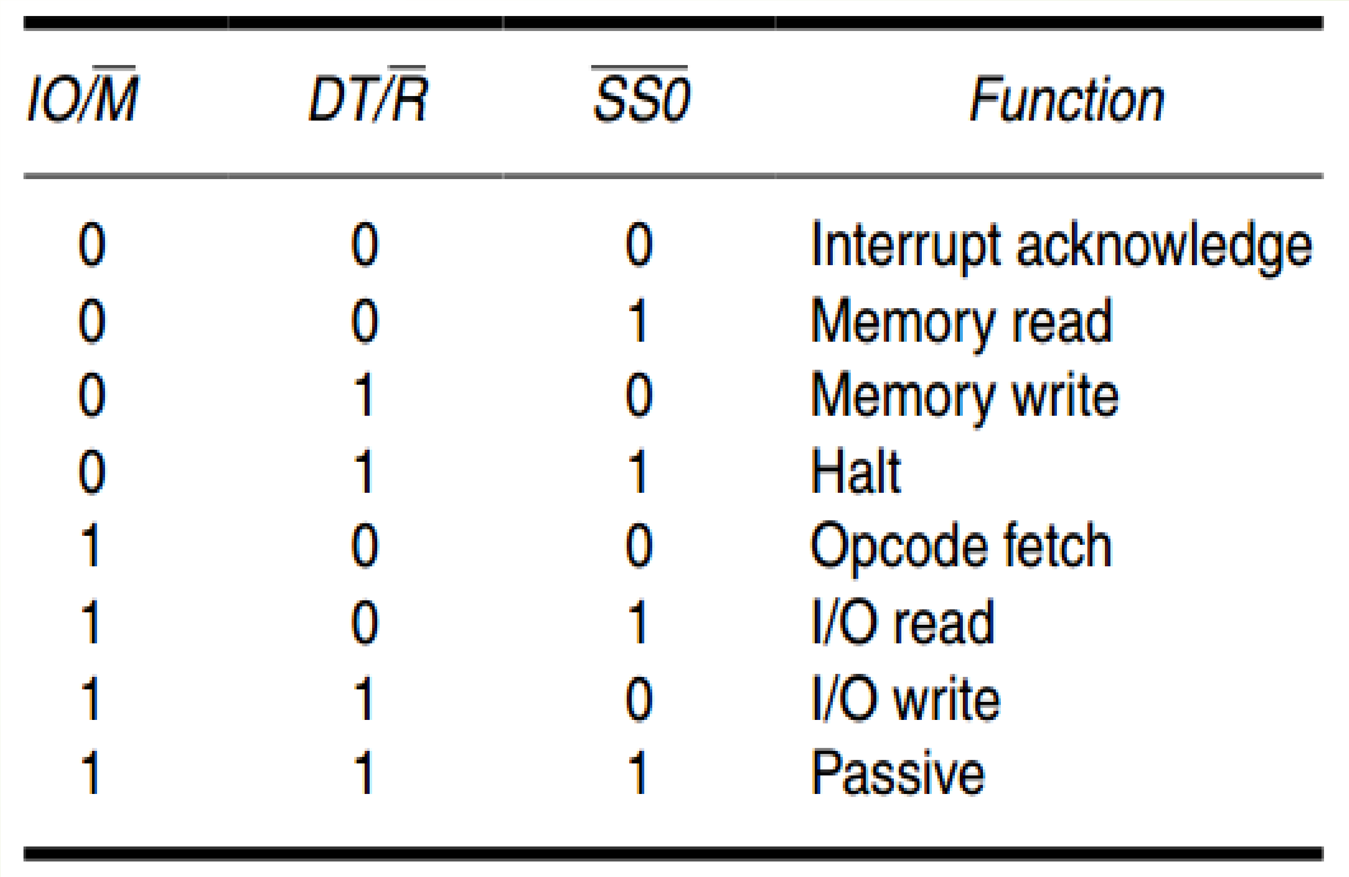
$\overline{SS0}$

- The $\overline{SS0}$ status line is equivalent to the S0 pin in maximum mode operation of the microprocessor.
- This signal is combined with **IO/** $\overline{M}$ and **DT/** $\overline{R}$ to decode the function of the current bus cycle (see Table on the next slide).

Cont’d...

- The bus cycle is also named as machine cycle.
- Bus cycle of 8086 is used to access memory, peripheral devices (Input/Output devices), and Interrupt controller.
- Bus cycle corresponds to a sequence of events that starts with an address being output on system address bus followed by a write or read data transfer

Bus cycle status using $\overline{\boldsymbol{SS0}}$



$IO/\overline{M}$	$DT/\overline{R}$	$\overline{SS0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive

Maximum Mode Pins

- In order to achieve maximum mode for use with external coprocessors, connect the MN/$\overline{\boldsymbol{MX}}$ pin to ground.

$\overline{S2}$, $\overline{S1}$ and $\overline{S0}$

- The **status bits** indicate the function of the current bus cycle.
- These signals are normally decoded by the 8288 bus controller.

Table on the next slide shows the function of these three status bits in the maximum mode.

$\overline{RQ}/\overline{GT1}$ and $\overline{RQ}/\overline{GT0}$

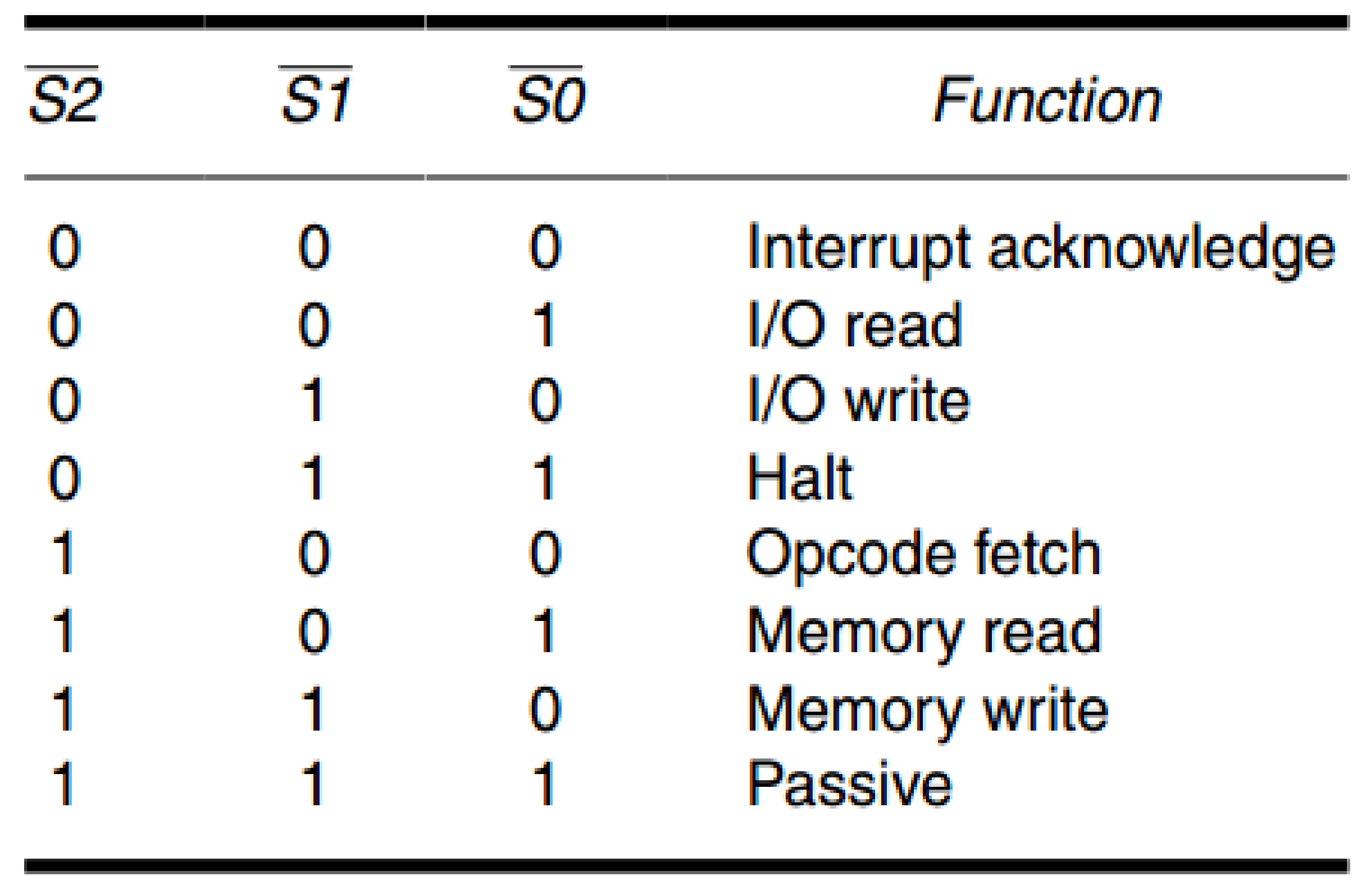
- The **request/grant** pins request direct memory accesses (DMA) during maximum mode operation.
- These lines are bidirectional and are used to both request and grant a DMA operation.

$\overline{LOCK}$

- The **lock** output is used to lock peripherals off the system.
- This pin is activated by using the LOCK: prefix on any instruction.

Cont'd…

- Bus control function generated by the bus controller (8288).

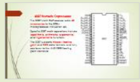


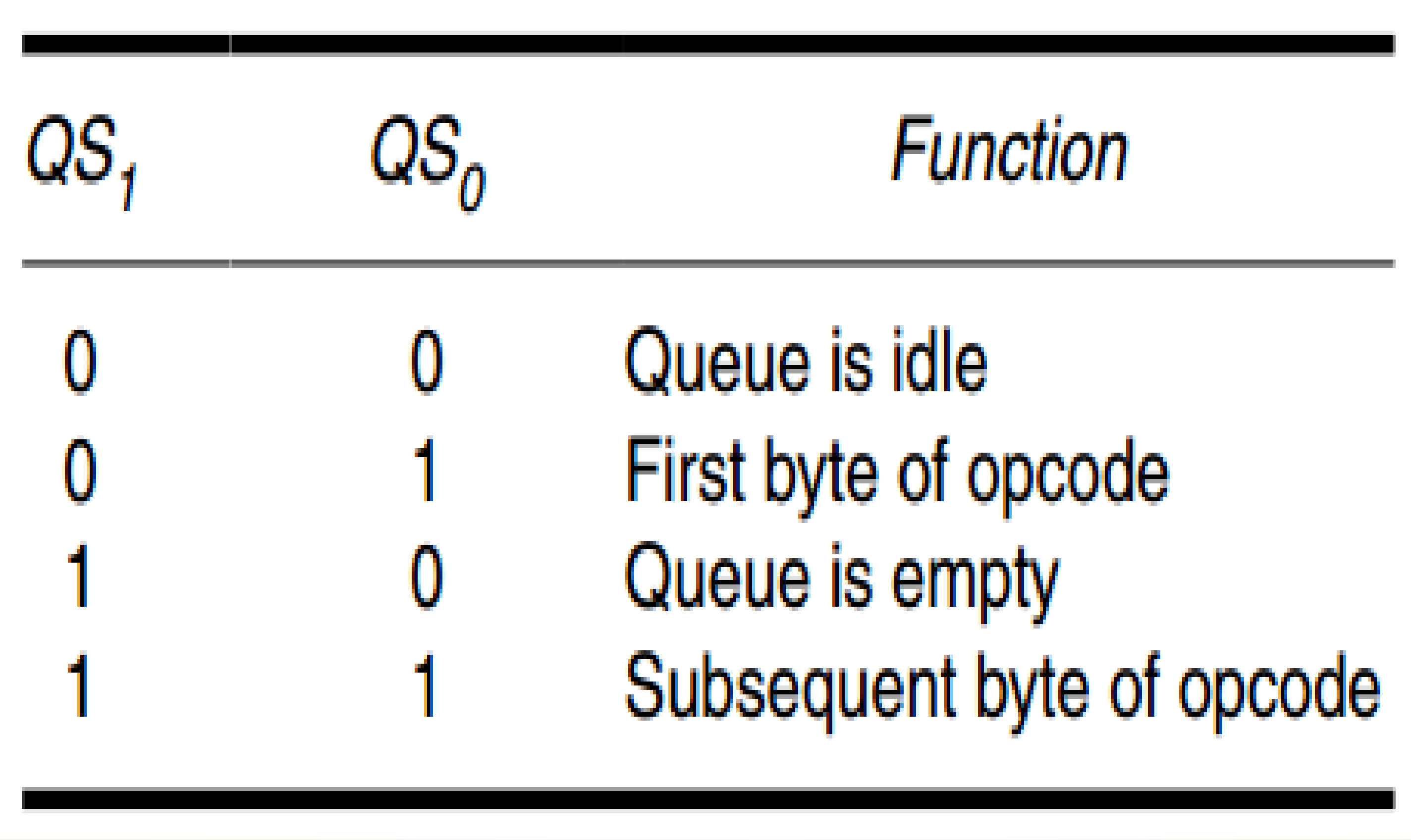
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	*Function*
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive

Cont'd…

QS1 and QS0

- The **queue status** bits show the status of the internal instruction queue.
- These pins are provided for access by the numeric coprocessor (8087).
- Table below shows for the operation of the queue status bits.

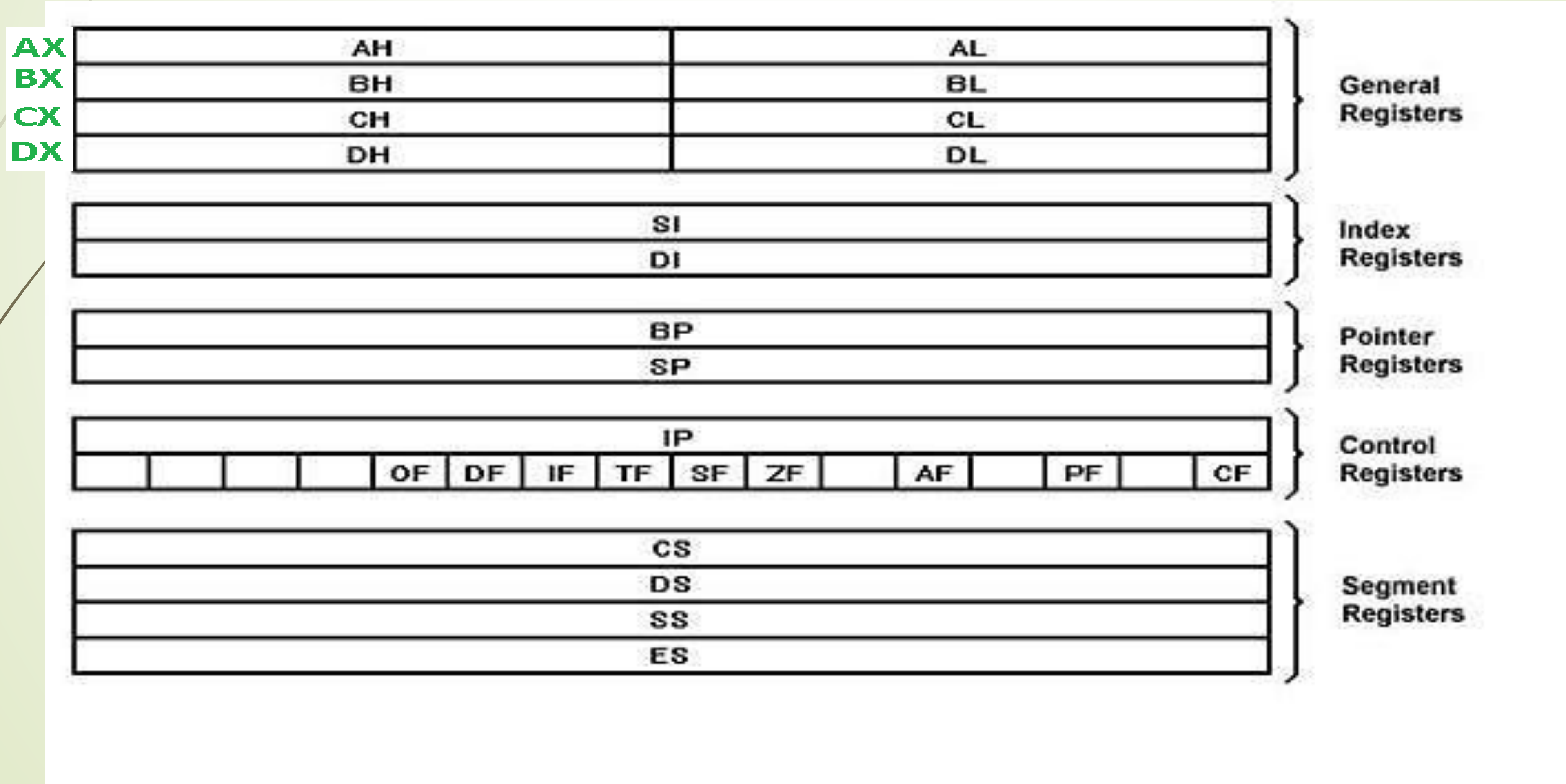




QS_1	*QS_0*	*Function*
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Registers in 8086 Microprocessor

- All the registers of 8086 are 16-bit registers. The general-purpose registers can be used as either 8-bit registers or 16-bit registers.
- The register set of 8086 can be categorized into **5** different categories:



General purpose Register

- The registers *AX*, *BX*,*CX* and *DX* are the general purpose 16-bit registers.
- Each of these registers is a combination of two 8-bit registers which are separately accessible as AL, BL, CL, DL (the "low" bytes) and AH, BH, CH, and DH (the "high" bytes).
- **Accumulator register (AX):** some of the operations, such as MUL and DIV, require that one of the operands be in the accumulator.
- Some other operations, such as ADD and SUB, may be applied to any of the registers (that is, any of the eight general- and special-purpose registers) but are more efficient when working with the accumulator.
- **Base register (BX**): it is the only general-purpose register which may be used for **indirect addressing**. For example, the instruction MOV [BX], AX causes the contents of AX to be stored in the memory location whose address is given in BX.

Cont'd…

- **Count register (CX):** The looping instructions (LOOP, LOOPE, and LOOPNE), the shift and rotate instructions (RCL, RCR, ROL, ROR, SHL, SHR, and SAR), and the string instructions (with the prefixes REP, REPE, and REPNE) all use the count register to determine how many times they will repeat.

- **Data register (DX**): it is used together with AX for the word-size MUL and DIV operations, and it can also hold the port number for the IN and OUT instructions, but it is mostly available as a convenient place to store data, as are all the other general-purpose registers.

Index Registers

- **Source Index register (SI):** it is used as a pointer to the current character being read in a string instruction (LODS, MOVS, or CMPS).
- It is also available as an offset to add to BX or BP when doing indirect addressing; for example, the instruction MOV [BX+SI], AX copies the contents of AX into the memory location whose address is the sum of the contents of BX and SI.
- **Destination Index register (DI):** it is used as a pointer to the current character being written or compared in a string instruction (MOVS, STOS, CMPS, or SCAS).
- It is also available as an **offset**, just like SI.

Pointer Registers

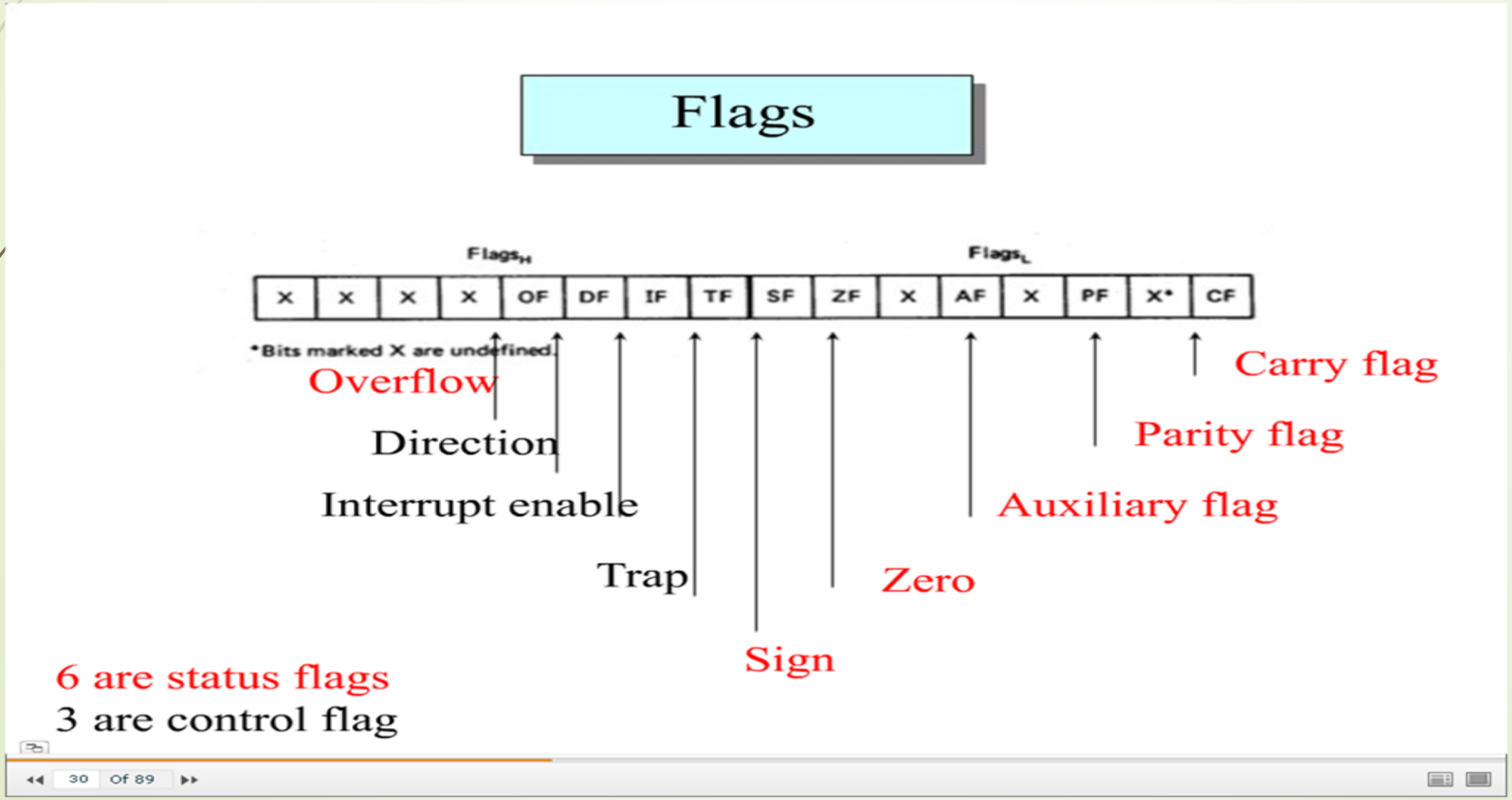
- **Stack Pointer (SP):** it is used for indicating the current position of the top of the stack.
- You should generally never modify this directly, since the subroutine and interrupt call-and-return mechanisms depend on the contents of the stack.
- **Base Pointer (BP):** it can be used for indirect addressing similar to BX.
- **Instruction Pointer (IP):** gives the address of the *next* instruction to be executed, relative to the code segment.
- The only way to modify this is with a branch instruction.

Segment Registers

- **Code segment register (CS)**: is used for addressing memory location in the code segment of the memory, where the **executable program is stored.**
- **Data segment register (DS):** points to the data segment of the memory where the data is stored.
- **Extra Segment Register (ES)** : also refers to a segment in the memory which is another data segment in the memory.
- **Stack Segment Register (SS):** is used for addressing stack segment of the memory.
- The stack segment is segment of memory which is used to store stack data.

Flag Registers

- **Flag Registers:** The 8086 Flag register contents indicate the results of computation in the *ALU*.



Flags

Flags_H Flags_L

X	X	X	X	OF	DF	IF	TF	SF	ZF	X	AF	X	PF	X*	CF

*Bits marked X are undefined.

Overflow

Direction

Interrupt enable

Trap

Sign

Zero

Auxiliary flag

Parity flag

Carry flag

6 are status flags

3 are control flag

Status Flags

- **Sign Flag (SF):** It shows the sign of the result of an arithmetic operation. This flag is set according to the sign of a data item following the arithmetic operation. The sign is indicated by the high-order of left most bit. A positive result clears the value of SF to 0 and negative result sets it to 1.

- **Zero Flag (ZF):** It indicates the result of an arithmetic or comparison operation. A nonzero result clears the zero flag to 0, and a zero result sets it to 1.

- **Auxiliary Carry Flag (AF):** It contains the carry from bit 3 to bit 4 following an arithmetic operation; used for specialized arithmetic. The AF is set when a 1-byte arithmetic operation causes a carry from bit 3 into bit 4.

Cont’d…

- **Parity Flag (PF):** It indicates the total number of 1-bits in the result obtained from an arithmetic operation. An even number of 1-bits clears the parity flag to 0 and an odd number of 1-bits sets the parity flag to 1.

- **Carry Flag (CF):** It contains the carry of 0 or 1 from a high-order bit (leftmost) after an arithmetic operation. It also stores the contents of last bit of a shift or rotate operation.

- **Overflow Flag (OF):** It indicates the overflow of a high-order bit (leftmost bit) of data after a signed arithmetic operation

Control Flags

- **Direction Flag (DF):** It determines left or right direction for moving or comparing string data. When the DF value is 0, the string operation takes left-to-right direction and when the value is set to 1, the string operation takes right-to-left direction.

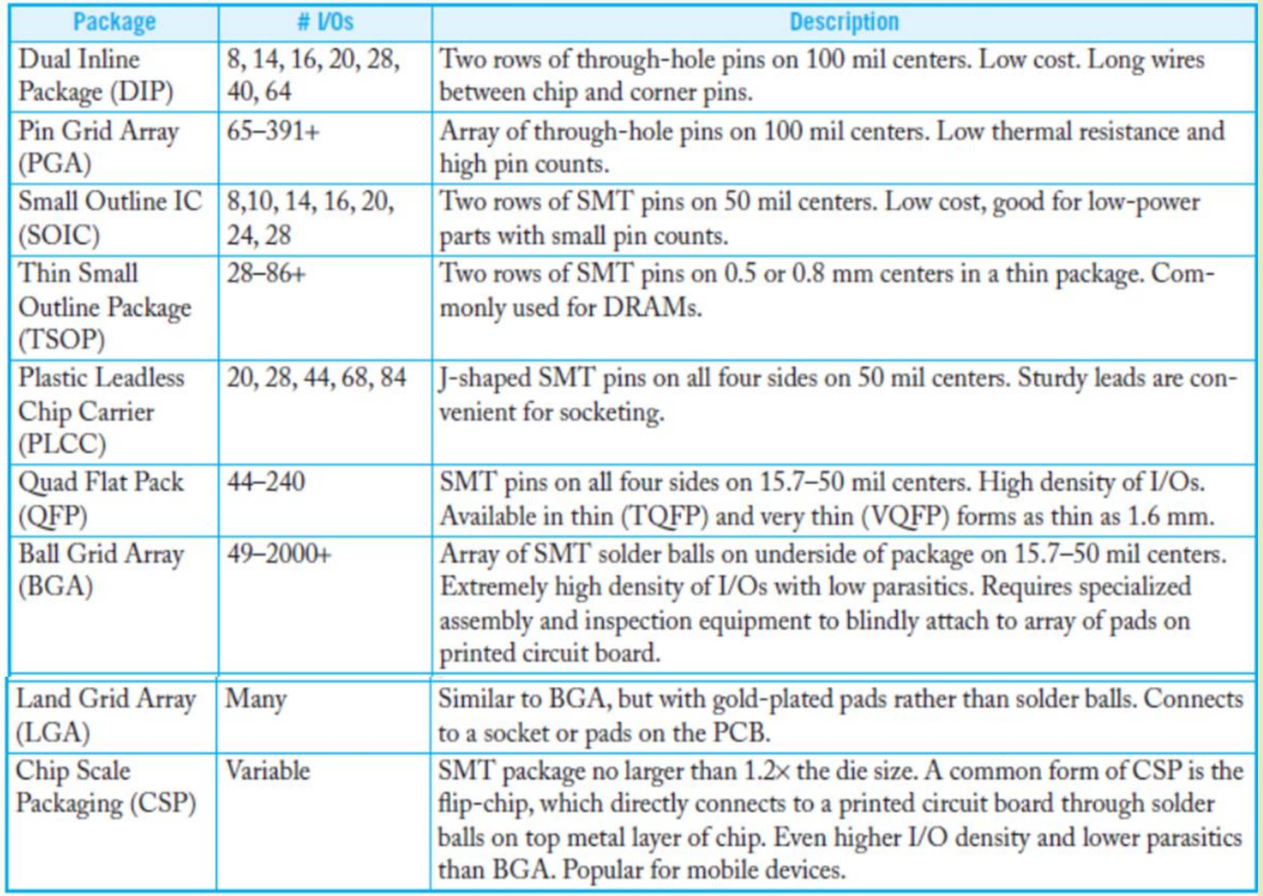
- **Interrupt Flag (IF):** It determines whether the external interrupts like keyboard entry, etc., are to be ignored or processed. It disables the external interrupt when the value is 0 and enables interrupts when set to 1.

- **Trap Flag (TF):** It allows setting the operation of the processor in single-step mode. The DEBUG program we used sets the trap flag, so we could step through the execution one instruction at a time.

Integrated Circuit (IC) Packaging

- It is the final stage of semiconductor device fabrication, in which the die is encapsulated in a supporting case that prevents physical damage and corrosion.
- The case, known as a "package", supports the electrical contacts which connect the device to a circuit board.
- A die, in the context of integrated circuits, is a small block of semiconducting material on which a given functional circuit is fabricated
- The materials of the package are either plastic (thermoset or thermoplastic), metal (commonly Kovar) or ceramic.

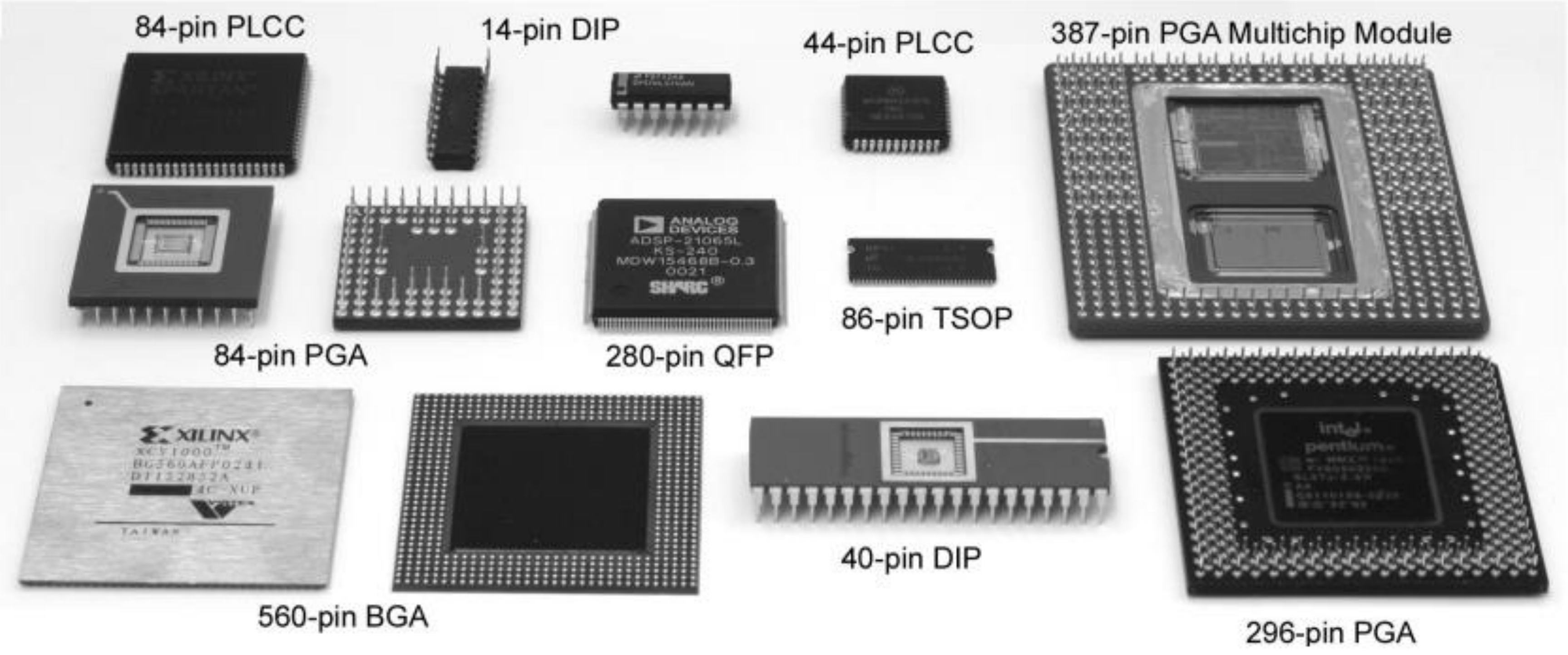
Different types of packaging options are:



Package	# I/Os	Description
Dual Inline Package (DIP)	8, 14, 16, 20, 28, 40, 64	Two rows of through-hole pins on 100 mil centers. Low cost. Long wires between chip and corner pins.
Pin Grid Array (PGA)	65–391+	Array of through-hole pins on 100 mil centers. Low thermal resistance and high pin counts.
Small Outline IC (SOIC)	8,10, 14, 16, 20, 24, 28	Two rows of SMT pins on 50 mil centers. Low cost, good for low-power parts with small pin counts.
Thin Small Outline Package (TSOP)	28–86+	Two rows of SMT pins on 0.5 or 0.8 mm centers in a thin package. Commonly used for DRAMs.
Plastic Leadless Chip Carrier (PLCC)	20, 28, 44, 68, 84	J-shaped SMT pins on all four sides on 50 mil centers. Sturdy leads are convenient for socketing.
Quad Flat Pack (QFP)	44–240	SMT pins on all four sides on 15.7–50 mil centers. High density of I/Os. Available in thin (TQFP) and very thin (VQFP) forms as thin as 1.6 mm.
Ball Grid Array (BGA)	49–2000+	Array of SMT solder balls on underside of package on 15.7–50 mil centers. Extremely high density of I/Os with low parasitics. Requires specialized assembly and inspection equipment to blindly attach to array of pads on printed circuit board.
Land Grid Array (LGA)	Many	Similar to BGA, but with gold-plated pads rather than solder balls. Connects to a socket or pads on the PCB.
Chip Scale Packaging (CSP)	Variable	SMT package no larger than 1.2× the die size. A common form of CSP is the flip-chip, which directly connects to a printed circuit board through solder balls on top metal layer of chip. Even higher I/O density and lower parasitics than BGA. Popular for mobile devices.

Examples

Through-hole vs. surface mount

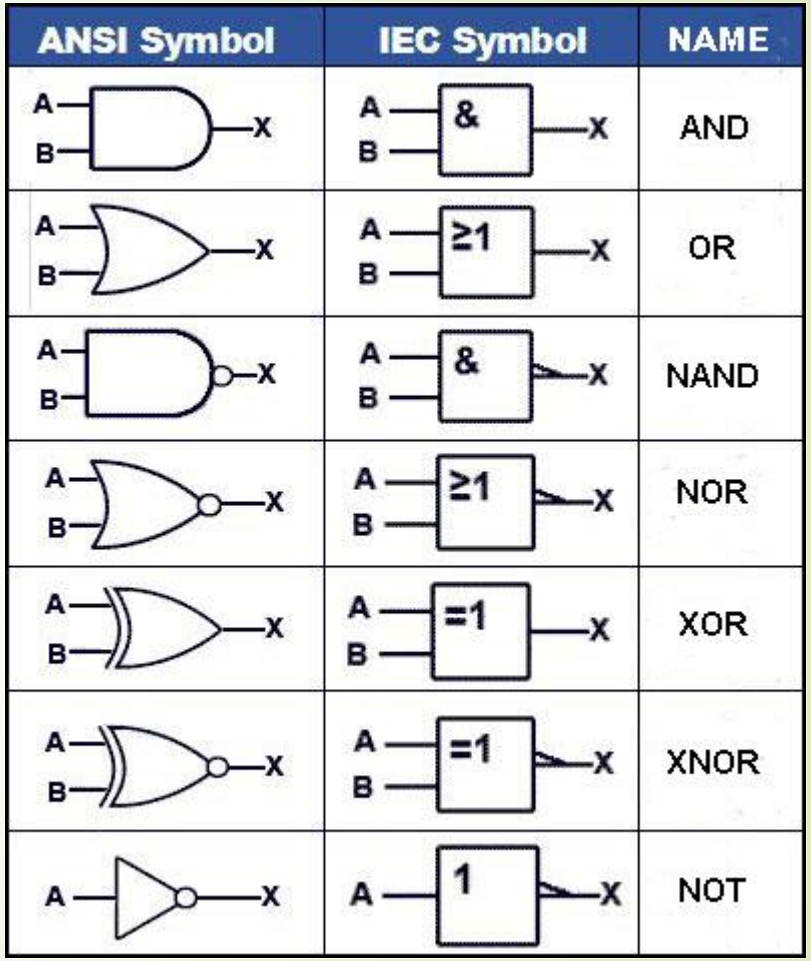


Standard Logic Circuits

Standard logic devices are generic logic functions that comply with the original classic 7400 series logic family.

This was a series of **transistor-to-transistor logic** (**TTL**) that included devices with functions like:

- **logic gates**,
- flip-flops,
- counters,
- bus transceivers.
- Multiplexers
- registers
- arithmetic logic units (ALUs)
- computer memory
- **Logic gates** are fundamental building blocks of digital circuits and are used in a variety of electronic devices and applications.



ANSI Symbol	IEC Symbol	NAME
	&	AND
	≥1	OR
	&	NAND
	≥1	NOR
	=1	XOR
	=1	XNOR
	1	NOT

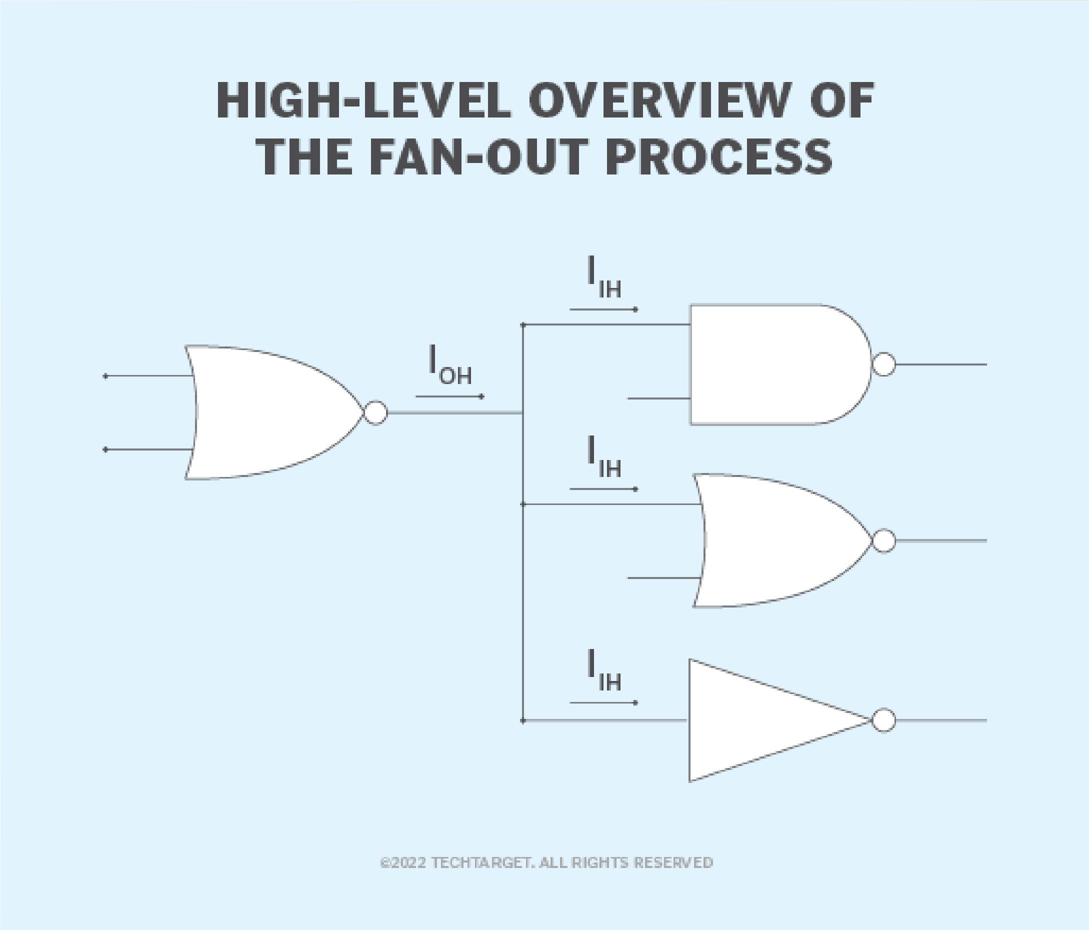
Fan-out

In digital circuitry, fan-out is a measure of the maximum number of digital inputs that the output of a single logic gate can feed without disrupting the circuitry's operations.

Most transistor-to-transistor logic (TTL) gates can support **up to 10** other digital gates or devices.

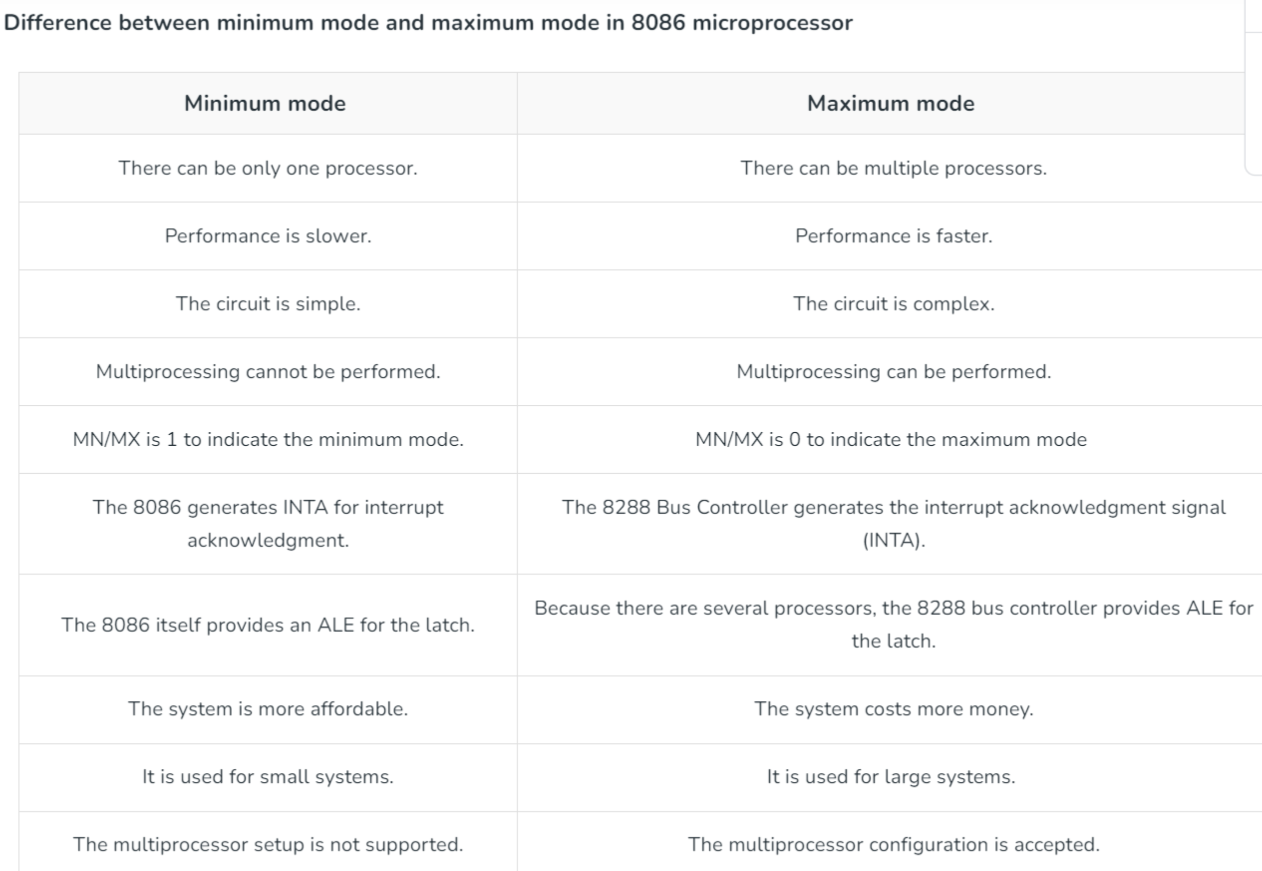
Thus, a typical TTL gate has a fan-out of 10.

In contrast, complementary metal oxide semiconductor (**CMOS**) gates can support over 50 connected devices, giving them a fan-out rate of greater than 50.


HIGH-LEVEL OVERVIEW OF THE FAN-OUT PROCESS
I_{OH}
I_{IH}
I_{IH}
I_{IH}
©2022 TECHTARGET. ALL RIGHTS RESERVED

Minimum and Maximum Mode of 8086

- In the 8086 microprocessor, there are two modes of operation: minimum mode and maximum mode.
- Minimum mode is used when the 8086 microprocessor is operating as a **standalone** processor without any **external coprocessors** or **support chips**. In this mode, the 8086 uses a single 8-bit bus for both data and instructions, and a single 20-bit address bus. The minimum mode requires a minimum set of support chips, such as clock generator, address latch, and bus controller.
- Maximum mode is used when the 8086 microprocessor is operating with one or more external coprocessors or support chips.
- In this mode, the 8086 uses a multiplexed bus for data and instructions, and a 20-bit address bus.
- The maximum mode requires additional support chips, such as a bus controller, a clock generator, and a data buffer.

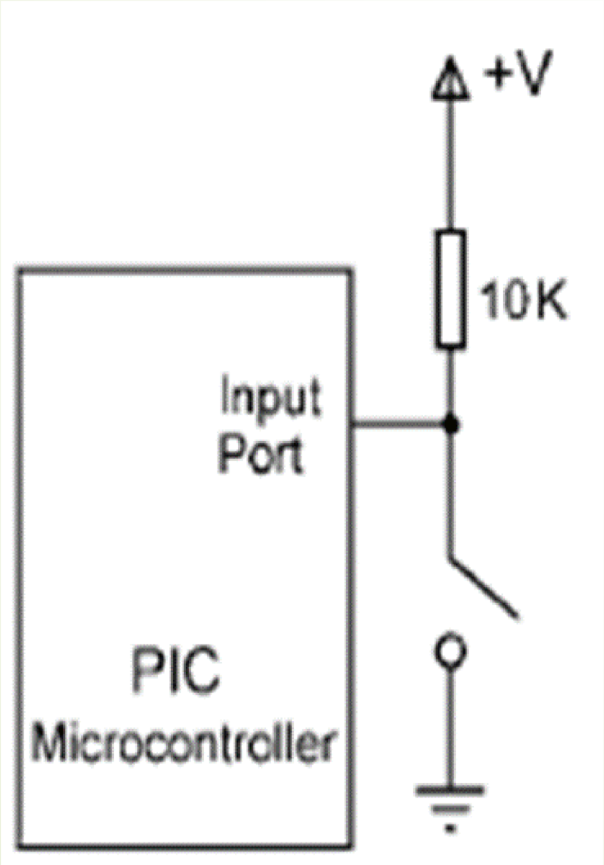


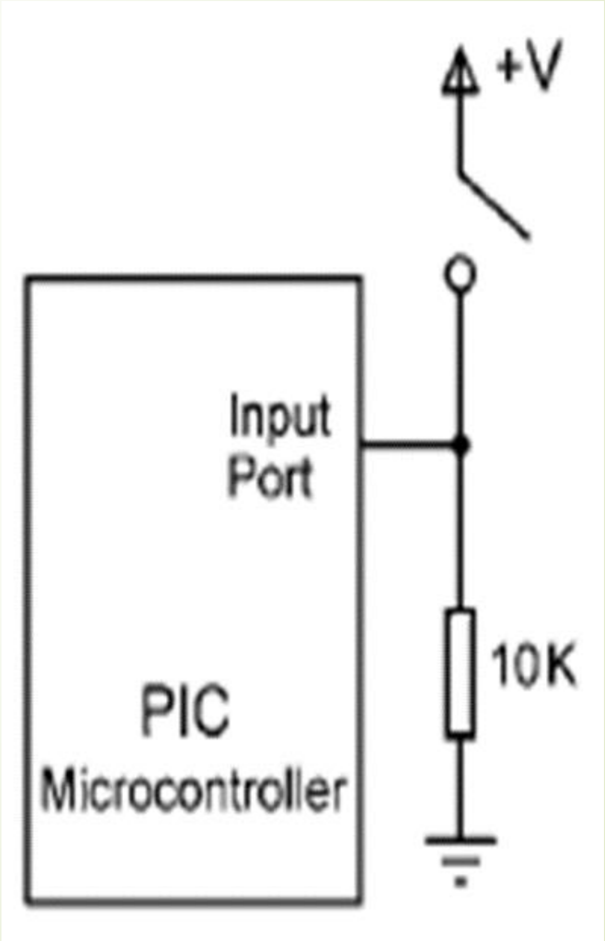
Difference between minimum mode and maximum mode in 8086 microprocessor

Minimum mode	Maximum mode
There can be only one processor.	There can be multiple processors.
Performance is slower.	Performance is faster.
The circuit is simple.	The circuit is complex.
Multiprocessing cannot be performed.	Multiprocessing can be performed.
MN/MX is 1 to indicate the minimum mode.	MN/MX is 0 to indicate the maximum mode
The 8086 generates INTA for interrupt acknowledgment.	The 8288 Bus Controller generates the interrupt acknowledgment signal (INTA).
The 8086 itself provides an ALE for the latch.	Because there are several processors, the 8288 bus controller provides ALE for the latch.
The system is more affordable.	The system costs more money.
It is used for small systems.	It is used for large systems.
The multiprocessor setup is not supported.	The multiprocessor configuration is accepted.

ACTIVE LOW Mode (PULL UP RESISTER)

ACTIVE HIGH Mode (PULL DOWN RESISTER)



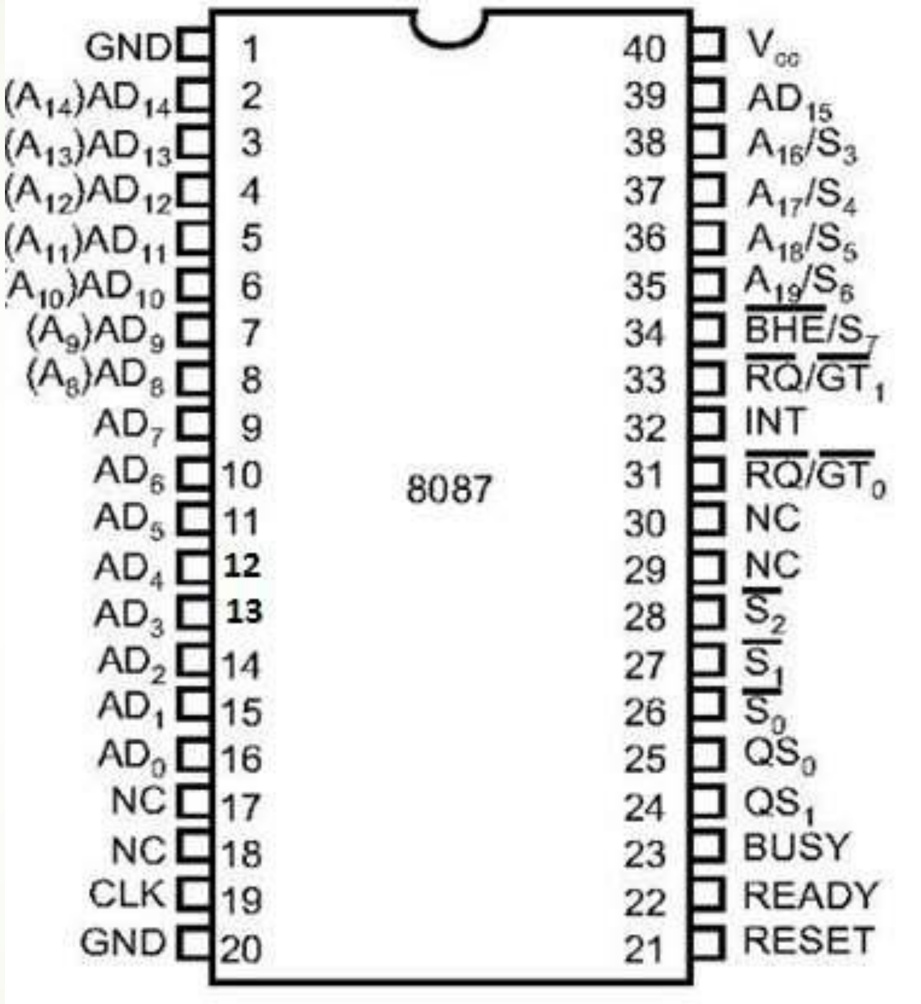


8087 Numeric Coprocessor

The 8087 Math CoProcessor adds 68 mnemonics to the 8086-microprocessor instruction set.

Specific 8087 math operations include logarithmic, arithmetic, exponential, and trigonometric functions.

The 8087 supports integer, floating point and BCD data formats, and fully conforms to the ANSI/IEEE floating point standard



8288 - bus controller

- The Intel 8288 is a bus controller designed for Intel 8086/8087/8088/8089.
- The chip is supplied in 20-pin DIP package.
- The 8086 (and 8088) operate in maximum mode, so they are configured primarily for multiprocessor operation or for working with coprocessors.
- Necessary control signals are generated by the 8288.
- It was used in the IBM PC, XT and its clones. IBM PC AT used its successor Intel 82288.

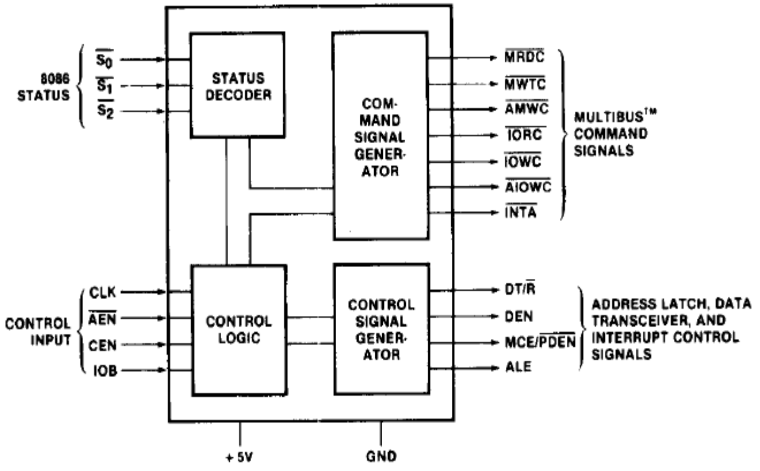
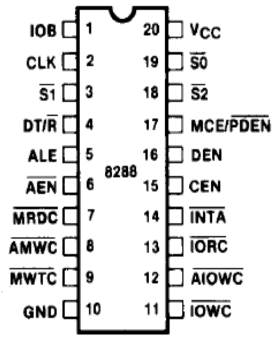


Figure 1. Block Diagram



8288
IOB 1
CLK 2
$\overline{S_1}$ 3
DT/$\overline{\text{R}}$ 4
ALE 5
$\overline{\text{AEN}}$ 6
$\overline{\text{MRDC}}$ 7
$\overline{\text{AMWC}}$ 8
$\overline{\text{MWTC}}$ 9
GND 10
20 V_{CC}
19 $\overline{S_0}$
18 $\overline{S_2}$
17 MCE/$\overline{\text{PDEN}}$
16 DEN
15 CEN
14 $\overline{\text{INTA}}$
13 $\overline{\text{IORC}}$
12 $\overline{\text{AIOWC}}$
11 $\overline{\text{IOWC}}$

Figure 2. Pin Configuration