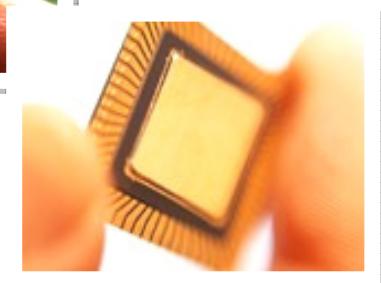
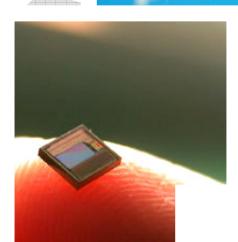


Raydium

瑞鼎科技股份有限公司
Rydium Semiconductor Corporation



RM68130 Data Sheet

Single Chip Driver with 262K color

for 176RGBx220 a-Si TFT LCD

Revision : 0.2

Date : Jul. 25, 2011

Revision History :

Revision	Description Of Change	Date
0.1	New creation	2011/7/15
0.2	Update R0Bh RTN[3:0] default values	2011/7/25

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1. General Description

The RM68130 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising 87,120 bytes RAM for a maximum 176 RGB x 220 dots graphics display, a 528-channel source driver, a 220-channel gate driver and power supply circuit. For efficient data transfer, the RM68130 supports high-speed interface via 8-/9-/16-/18-bit ports as i80/M68-system interface to the microcomputer and high-speed RAM write function. As moving picture interface, the RM68130 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB17:0).

Also, the RM68130 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The RM68130's power management functions such as 8-color display and power operation mode such as deep standby mode and standby mode make this LSI a perfect driver for the medium or small sized portable products with color display systems such as digital cellular phones or hand-held devices with outstanding battery consistency.

2. Features

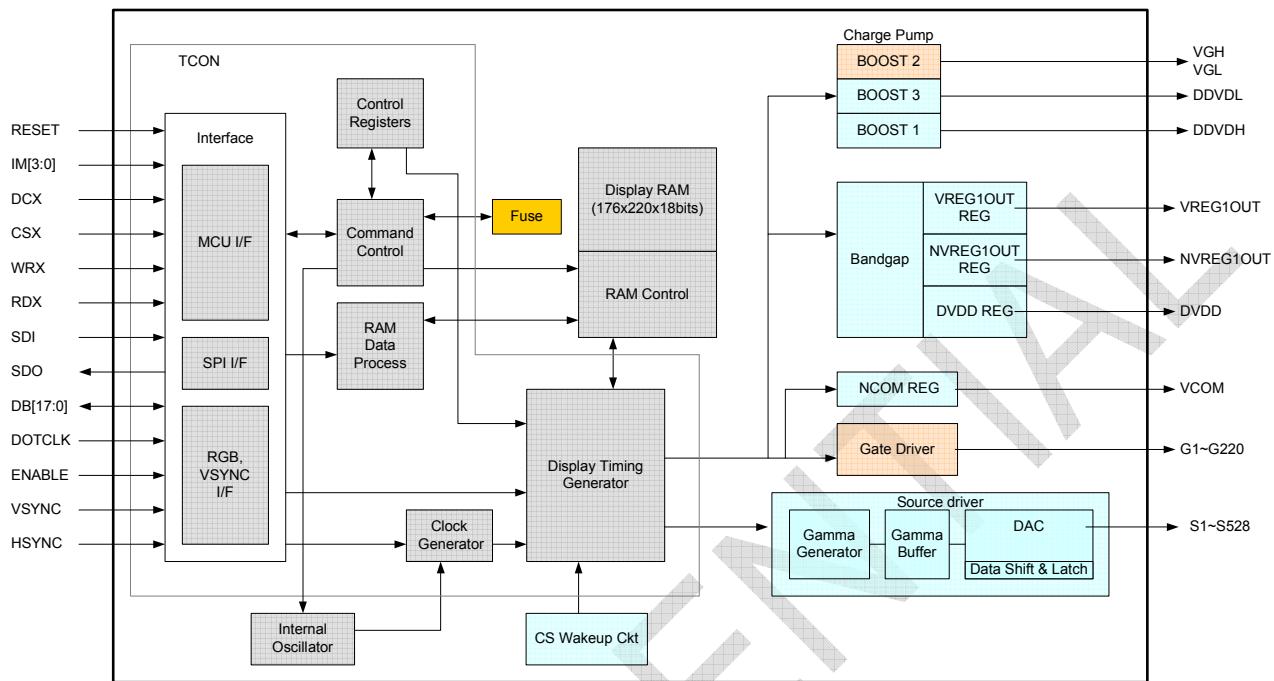
- Single chip solution for a liquid crystal QCIF+ TFT LCD display
- 176RGBx220-dot resolution capable of graphics display in 262,144 color
- Incorporate 528-channel source driver and 220-channel gate driver
- Internal 87,120 bytes graphic RAM
- System interface
 - 1. i80/M68 system interface with 8-/ 9-/16-/18-bit bus width (with two different data bus formats)
 - 2. Serial Peripheral Interface (24-bit 4 wires, 3-wire 9-bit and 4-wire 8-bit)
 - 3. RGB interface with 6-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
 - 4. VSYNC interface (System interface + VSYNC)
- Internal oscillator and hardware reset
- Reversible source/gate driver shift direction

- Window address function to specify a rectangular area for internal GRAM access
- Abundant functions for color display control
 - γ-correction function enabling display in 262,144 colors
 - Line-unit vertical scrolling function
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Power saving functions
 - 8-color mode
 - sleep mode
 - standby mode
 - deep standby mode
- Low -power consumption architecture
 - Low operating power supplies:
 - ◆ VDDI = 1.65V ~ 3.3 V (interface I/O)
 - ◆ VCI = 2.5V ~ 3.3 V (analog)
- LCD Voltage drive:
 - Source driver output voltage
 - ◆ Source Voltage (GVDD to AGND) : 3.15V ~ 4.7 V
 - Gate driver output voltage
 - ◆ VGH - GND = VCIx4, x5, x6
 - ◆ VGL – GND = VCIx-3, x-4
 - VCOM driver output voltage
 - ◆ VCOM – AGND = -0.425V~ -2V
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the glass substrate
- Internal NVM: VCOM level adjustment, 6 bits x 3 sets

Table 1 Power Supply Specifications

No.	Item	RM68130
1	TFT data lines	528 output
2	TFT gate lines	220 output
3	Liquid crystal drive output	S1~S528 V0~V63 grayscales
		G1~G220 VGH-VGL
		VCOM -0.425V~-2V
4	Input voltage (interface voltage)	1.65V~3.30V Power supply to IM0/ID, IM1-3, CSX, RS, WRX_SCL, RDX, RESET, DB17-0, SDI_SDA, SDO, DOTCLK, VSYNC, HSYNC, ENABLE, FMARK, M, CL1. Connect to VCI and VCI on the FPC when the electrical potentials are the same.
		2.50V~3.30V Connect to VDDI and VCI on the FPC when the electrical potentials are the same.
5	Internal step-up circuits	DDVDH VCIx2
		VGH VCIx4, x5, x6
		VGL VCIx-3, x-4
		DDVDL VCIx-2

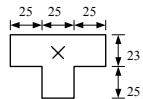
3. Block Diagram



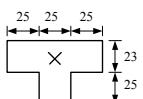
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4. Pin Diagram

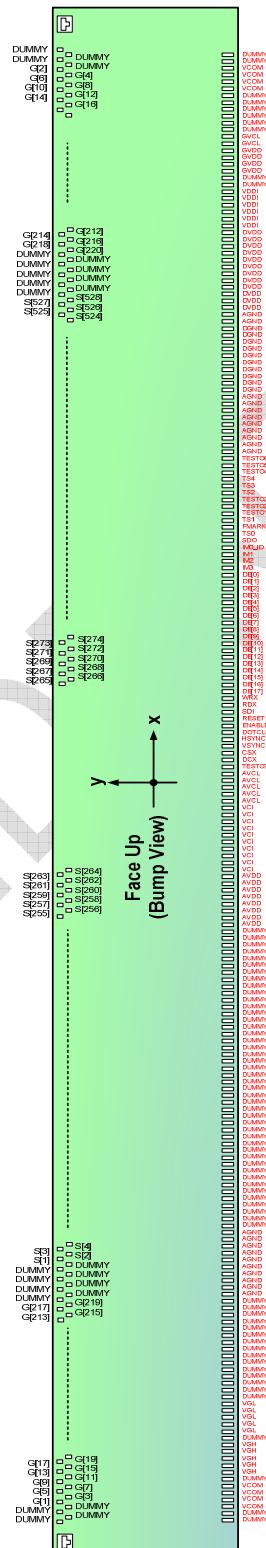
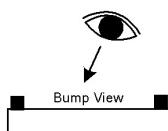
Alignment Mark(left): (X,Y)=(-6852.5,266.5)



Alignment Mark(right): (X,Y)=(6852.5,266.5)



Unit: μm



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- Chip size: 14 mm x 0.66 mm (Include sealing and scribe line)
- Chip thickness: 280 um (typ.)
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size

16um x 85um: Output Pads to Panel

40um x 46um: Input Pads

- Au bump pitch: (16um) See PAD coordinates table
- Au bump height: 12um (typ.)
- Alignment mark

Alignment mark shape	X	Y
Type A	-6852.5	266.5
	6852.5	266.5

Pad Coordinate (Unit: um)

No.	Name	X	Y	No.	Name	X	Y
1	DUMMY	-6695	-251	56	DUMMY	-3395	-251
2	DUMMY	-6635	-251	57	DUMMY	-3335	-251
3	VCOM	-6575	-251	58	DUMMY	-3275	-251
4	VCOM	-6515	-251	59	DUMMY	-3215	-251
5	VCOM	-6455	-251	60	DUMMY	-3155	-251
6	VCOM	-6395	-251	61	DUMMY	-3095	-251
7	DUMMY	-6335	-251	62	DUMMY	-3035	-251
8	VGH	-6275	-251	63	DUMMY	-2975	-251
9	VGH	-6215	-251	64	DUMMY	-2915	-251
10	VGH	-6155	-251	65	DUMMY	-2855	-251
11	VGH	-6095	-251	66	DUMMY	-2795	-251
12	VGH	-6035	-251	67	DUMMY	-2735	-251
13	DUMMY	-5975	-251	68	DUMMY	-2675	-251
14	VGL	-5915	-251	69	DUMMY	-2615	-251
15	VGL	-5855	-251	70	DUMMY	-2555	-251
16	VGL	-5795	-251	71	DUMMY	-2495	-251
17	VGL	-5735	-251	72	DUMMY	-2435	-251
18	VGL	-5675	-251	73	DUMMY	-2375	-251
19	DUMMY	-5615	-251	74	DUMMY	-2315	-251
20	DUMMY	-5555	-251	75	DUMMY	-2255	-251
21	DUMMY	-5495	-251	76	DUMMY	-2195	-251
22	DUMMY	-5435	-251	77	DUMMY	-2135	-251
23	DUMMY	-5375	-251	78	DUMMY	-2075	-251
24	DUMMY	-5315	-251	79	DUMMY	-2015	-251
25	DUMMY	-5255	-251	80	DUMMY	-1955	-251
26	DUMMY	-5195	-251	81	DUMMY	-1895	-251
27	DUMMY	-5135	-251	82	DUMMY	-1835	-251
28	DUMMY	-5075	-251	83	DUMMY	-1775	-251
29	DUMMY	-5015	-251	84	DUMMY	-1715	-251
30	DUMMY	-4955	-251	85	DUMMY	-1655	-251
31	DUMMY	-4895	-251	86	DUMMY	-1595	-251
32	DUMMY	-4835	-251	87	DUMMY	-1535	-251
33	DUMMY	-4775	-251	88	AVDD	-1475	-251
34	AGND	-4715	-251	89	AVDD	-1415	-251
35	AGND	-4655	-251	90	AVDD	-1355	-251
36	AGND	-4595	-251	91	AVDD	-1295	-251
37	AGND	-4535	-251	92	AVDD	-1235	-251
38	AGND	-4475	-251	93	AVDD	-1175	-251
39	AGND	-4415	-251	94	AVDD	-1115	-251
40	AGND	-4355	-251	95	AVDD	-1055	-251
41	AGND	-4295	-251	96	VCI	-995	-251
42	AGND	-4235	-251	97	VCI	-935	-251
43	AGND	-4175	-251	98	VCI	-875	-251
44	DUMMY	-4115	-251	99	VCI	-815	-251
45	DUMMY	-4055	-251	100	VCI	-755	-251
46	DUMMY	-3995	-251	101	VCI	-695	-251
47	DUMMY	-3935	-251	102	VCI	-635	-251
48	DUMMY	-3875	-251	103	VCI	-575	-251
49	DUMMY	-3815	-251	104	VCI	-515	-251
50	DUMMY	-3755	-251	105	VCI	-455	-251
51	DUMMY	-3695	-251	106	AVCL	-395	-251
52	DUMMY	-3635	-251	107	AVCL	-335	-251
53	DUMMY	-3575	-251	108	AVCL	-275	-251
54	DUMMY	-3515	-251	109	AVCL	-215	-251
55	DUMMY	-3455	-251	110	AVCL	-155	-251

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No.	Name	X	Y	No.	Name	X	Y
111	TEST07	-95	-251	169	DGND	3935	-251
112	DCX	-35	-251	170	DGND	3995	-251
113	CSX	25	-251	171	DGND	4055	-251
114	VSYNC	85	-251	172	DGND	4115	-251
115	HSYNC	145	-251	173	DGND	4175	-251
116	DOTCLK	205	-251	174	DGND	4235	-251
117	ENABLE	265	-251	175	DGND	4295	-251
118	RESET	325	-251	176	AGND	4355	-251
119	SDI	385	-251	177	AGND	4415	-251
120	RDX	445	-251	178	DVDD	4475	-251
121	WRX	505	-251	179	DVDD	4535	-251
122	DB[17]	565	-251	180	DVDD	4595	-251
123	DB[16]	650	-251	181	DVDD	4655	-251
124	DB[15]	735	-251	182	DVDD	4715	-251
125	DB[14]	820	-251	183	DVDD	4775	-251
126	DB[13]	905	-251	184	DVDD	4835	-251
127	DB[12]	990	-251	185	DVDD	4895	-251
128	DB[11]	1075	-251	186	DVDD	4955	-251
129	DB[10]	1160	-251	187	DVDD	5015	-251
130	DB[9]	1245	-251	188	DVDD	5075	-251
131	DB[8]	1330	-251	189	DVDD	5135	-251
132	DB[7]	1415	-251	190	VDDI	5195	-251
133	DB[6]	1500	-251	191	VDDI	5255	-251
134	DB[5]	1585	-251	192	VDDI	5315	-251
135	DB[4]	1670	-251	193	VDDI	5375	-251
136	DB[3]	1755	-251	194	VDDI	5435	-251
137	DB[2]	1840	-251	195	VDDI	5495	-251
138	DB[1]	1925	-251	196	DUMMY	5555	-251
139	DB[0]	2010	-251	197	DUMMY	5615	-251
140	IM3	2095	-251	198	GVDD	5675	-251
141	IM2	2155	-251	199	GVDD	5735	-251
142	IM1	2215	-251	200	GVDD	5795	-251
143	IMO_ID	2275	-251	201	GVDD	5855	-251
144	SDO	2335	-251	202	GVCL	5915	-251
145	TS0	2420	-251	203	GVCL	5975	-251
146	FMARK	2505	-251	204	DUMMY	6035	-251
147	TS1	2590	-251	205	DUMMY	6095	-251
148	TEST01	2675	-251	206	DUMMY	6155	-251
149	TEST02	2735	-251	207	DUMMY	6215	-251
150	TEST03	2795	-251	208	DUMMY	6275	-251
151	TS2	2855	-251	209	DUMMY	6335	-251
152	TS3	2915	-251	210	VCOM	6395	-251
153	TS4	2975	-251	211	VCOM	6455	-251
154	TEST04	3035	-251	212	VCOM	6515	-251
155	TEST05	3095	-251	213	VCOM	6575	-251
156	TEST06	3155	-251	214	DUMMY	6635	-251
157	AGND	3215	-251	215	DUMMY	6695	-251
158	AGND	3275	-251	216	DUMMY	6772	230
159	AGND	3335	-251	217	DUMMY	6756	77
160	AGND	3395	-251	218	DUMMY	6740	230
161	AGND	3455	-251	219	DUMMY	6724	77
162	AGND	3515	-251	220	G[2]	6708	230
163	AGND	3575	-251	221	G[4]	6692	77
164	AGND	3635	-251	222	G[6]	6676	230
165	AGND	3695	-251	223	G[8]	6660	77
166	DGND	3755	-251	224	G[10]	6644	230
167	DGND	3815	-251	225	G[12]	6628	77
168	DGND	3875	-251	226	G[14]	6612	230

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No.	Name	X	Y	No.	Name	X	Y
227	G[16]	6596	77	285	G[132]	5668	77
228	G[18]	6580	230	286	G[134]	5652	230
229	G[20]	6564	77	287	G[136]	5636	77
230	G[22]	6548	230	288	G[138]	5620	230
231	G[24]	6532	77	289	G[140]	5604	77
232	G[26]	6516	230	290	G[142]	5588	230
233	G[28]	6500	77	291	G[144]	5572	77
234	G[30]	6484	230	292	G[146]	5556	230
235	G[32]	6468	77	293	G[148]	5540	77
236	G[34]	6452	230	294	G[150]	5524	230
237	G[36]	6436	77	295	G[152]	5508	77
238	G[38]	6420	230	296	G[154]	5492	230
239	G[40]	6404	77	297	G[156]	5476	77
240	G[42]	6388	230	298	G[158]	5460	230
241	G[44]	6372	77	299	G[160]	5444	77
242	G[46]	6356	230	300	G[162]	5428	230
243	G[48]	6340	77	301	G[164]	5412	77
244	G[50]	6324	230	302	G[166]	5396	230
245	G[52]	6308	77	303	G[168]	5380	77
246	G[54]	6292	230	304	G[170]	5364	230
247	G[56]	6276	77	305	G[172]	5348	77
248	G[58]	6260	230	306	G[174]	5332	230
249	G[60]	6244	77	307	G[176]	5316	77
250	G[62]	6228	230	308	G[178]	5300	230
251	G[64]	6212	77	309	G[180]	5284	77
252	G[66]	6196	230	310	G[182]	5268	230
253	G[68]	6180	77	311	G[184]	5252	77
254	G[70]	6164	230	312	G[186]	5236	230
255	G[72]	6148	77	313	G[188]	5220	77
256	G[74]	6132	230	314	G[190]	5204	230
257	G[76]	6116	77	315	G[192]	5188	77
258	G[78]	6100	230	316	G[194]	5172	230
259	G[80]	6084	77	317	G[196]	5156	77
260	G[82]	6068	230	318	G[198]	5140	230
261	G[84]	6052	77	319	G[200]	5124	77
262	G[86]	6036	230	320	G[202]	5108	230
263	G[88]	6020	77	321	G[204]	5092	77
264	G[90]	6004	230	322	G[206]	5076	230
265	G[92]	5988	77	323	G[208]	5060	77
266	G[94]	5972	230	324	G[210]	5044	230
267	G[96]	5956	77	325	G[212]	5028	77
268	G[98]	5940	230	326	G[214]	5012	230
269	G[100]	5924	77	327	G[216]	4996	77
270	G[102]	5908	230	328	G[218]	4980	230
271	G[104]	5892	77	329	G[220]	4964	77
272	G[106]	5876	230	330	DUMMY	4948	230
273	G[108]	5860	77	331	DUMMY	4932	77
274	G[110]	5844	230	332	DUMMY	4916	230
275	G[112]	5828	77	333	DUMMY	4900	77
276	G[114]	5812	230	334	DUMMY	4884	230
277	G[116]	5796	77	335	DUMMY	4868	77
278	G[118]	5780	230	336	DUMMY	4852	230
279	G[120]	5764	77	337	DUMMY	4836	77
280	G[122]	5748	230	338	DUMMY	4820	230
281	G[124]	5732	77	339	S[528]	4804	77
282	G[126]	5716	230	340	S[527]	4788	230
283	G[128]	5700	77	341	S[526]	4772	77
284	G[130]	5684	230	342	S[525]	4756	230

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No.	Name	X	Y	No.	Name	X	Y
343	S[524]	4740	77	401	S[466]	3812	77
344	S[523]	4724	230	402	S[465]	3796	230
345	S[522]	4708	77	403	S[464]	3780	77
346	S[521]	4692	230	404	S[463]	3764	230
347	S[520]	4676	77	405	S[462]	3748	77
348	S[519]	4660	230	406	S[461]	3732	230
349	S[518]	4644	77	407	S[460]	3716	77
350	S[517]	4628	230	408	S[459]	3700	230
351	S[516]	4612	77	409	S[458]	3684	77
352	S[515]	4596	230	410	S[457]	3668	230
353	S[514]	4580	77	411	S[456]	3652	77
354	S[513]	4564	230	412	S[455]	3636	230
355	S[512]	4548	77	413	S[454]	3620	77
356	S[511]	4532	230	414	S[453]	3604	230
357	S[510]	4516	77	415	S[452]	3588	77
358	S[509]	4500	230	416	S[451]	3572	230
359	S[508]	4484	77	417	S[450]	3556	77
360	S[507]	4468	230	418	S[449]	3540	230
361	S[506]	4452	77	419	S[448]	3524	77
362	S[505]	4436	230	420	S[447]	3508	230
363	S[504]	4420	77	421	S[446]	3492	77
364	S[503]	4404	230	422	S[445]	3476	230
365	S[502]	4388	77	423	S[444]	3460	77
366	S[501]	4372	230	424	S[443]	3444	230
367	S[500]	4356	77	425	S[442]	3428	77
368	S[499]	4340	230	426	S[441]	3412	230
369	S[498]	4324	77	427	S[440]	3396	77
370	S[497]	4308	230	428	S[439]	3380	230
371	S[496]	4292	77	429	S[438]	3364	77
372	S[495]	4276	230	430	S[437]	3348	230
373	S[494]	4260	77	431	S[436]	3332	77
374	S[493]	4244	230	432	S[435]	3316	230
375	S[492]	4228	77	433	S[434]	3300	77
376	S[491]	4212	230	434	S[433]	3284	230
377	S[490]	4196	77	435	S[432]	3268	77
378	S[489]	4180	230	436	S[431]	3252	230
379	S[488]	4164	77	437	S[430]	3236	77
380	S[487]	4148	230	438	S[429]	3220	230
381	S[486]	4132	77	439	S[428]	3204	77
382	S[485]	4116	230	440	S[427]	3188	230
383	S[484]	4100	77	441	S[426]	3172	77
384	S[483]	4084	230	442	S[425]	3156	230
385	S[482]	4068	77	443	S[424]	3140	77
386	S[481]	4052	230	444	S[423]	3124	230
387	S[480]	4036	77	445	S[422]	3108	77
388	S[479]	4020	230	446	S[421]	3092	230
389	S[478]	4004	77	447	S[420]	3076	77
390	S[477]	3988	230	448	S[419]	3060	230
391	S[476]	3972	77	449	S[418]	3044	77
392	S[475]	3956	230	450	S[417]	3028	230
393	S[474]	3940	77	451	S[416]	3012	77
394	S[473]	3924	230	452	S[415]	2996	230
395	S[472]	3908	77	453	S[414]	2980	77
396	S[471]	3892	230	454	S[413]	2964	230
397	S[470]	3876	77	455	S[412]	2948	77
398	S[469]	3860	230	456	S[411]	2932	230
399	S[468]	3844	77	457	S[410]	2916	77
400	S[467]	3828	230	458	S[409]	2900	230

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No.	Name	X	Y	No.	Name	X	Y
459	S[408]	2884	77	517	S[350]	1906	77
460	S[407]	2868	230	518	S[349]	1890	230
461	S[406]	2852	77	519	S[348]	1874	77
462	S[405]	2836	230	520	S[347]	1858	230
463	S[404]	2820	77	521	S[346]	1842	77
464	S[403]	2804	230	522	S[345]	1826	230
465	S[402]	2788	77	523	S[344]	1810	77
466	S[401]	2772	230	524	S[343]	1794	230
467	S[400]	2756	77	525	S[342]	1778	77
468	S[399]	2740	230	526	S[341]	1762	230
469	S[398]	2724	77	527	S[340]	1746	77
470	S[397]	2708	230	528	S[339]	1730	230
471	S[396]	2642	77	529	S[338]	1714	77
472	S[395]	2626	230	530	S[337]	1698	230
473	S[394]	2610	77	531	S[336]	1682	77
474	S[393]	2594	230	532	S[335]	1666	230
475	S[392]	2578	77	533	S[334]	1650	77
476	S[391]	2562	230	534	S[333]	1634	230
477	S[390]	2546	77	535	S[332]	1618	77
478	S[389]	2530	230	536	S[331]	1602	230
479	S[388]	2514	77	537	S[330]	1586	77
480	S[387]	2498	230	538	S[329]	1570	230
481	S[386]	2482	77	539	S[328]	1554	77
482	S[385]	2466	230	540	S[327]	1538	230
483	S[384]	2450	77	541	S[326]	1522	77
484	S[383]	2434	230	542	S[325]	1506	230
485	S[382]	2418	77	543	S[324]	1490	77
486	S[381]	2402	230	544	S[323]	1474	230
487	S[380]	2386	77	545	S[322]	1458	77
488	S[379]	2370	230	546	S[321]	1442	230
489	S[378]	2354	77	547	S[320]	1426	77
490	S[377]	2338	230	548	S[319]	1410	230
491	S[376]	2322	77	549	S[318]	1394	77
492	S[375]	2306	230	550	S[317]	1378	230
493	S[374]	2290	77	551	S[316]	1362	77
494	S[373]	2274	230	552	S[315]	1346	230
495	S[372]	2258	77	553	S[314]	1330	77
496	S[371]	2242	230	554	S[313]	1314	230
497	S[370]	2226	77	555	S[312]	1298	77
498	S[369]	2210	230	556	S[311]	1282	230
499	S[368]	2194	77	557	S[310]	1266	77
500	S[367]	2178	230	558	S[309]	1250	230
501	S[366]	2162	77	559	S[308]	1234	77
502	S[365]	2146	230	560	S[307]	1218	230
503	S[364]	2130	77	561	S[306]	1202	77
504	S[363]	2114	230	562	S[305]	1186	230
505	S[362]	2098	77	563	S[304]	1170	77
506	S[361]	2082	230	564	S[303]	1154	230
507	S[360]	2066	77	565	S[302]	1138	77
508	S[359]	2050	230	566	S[301]	1122	230
509	S[358]	2034	77	567	S[300]	1106	77
510	S[357]	2018	230	568	S[299]	1090	230
511	S[356]	2002	77	569	S[298]	1074	77
512	S[355]	1986	230	570	S[297]	1058	230
513	S[354]	1970	77	571	S[296]	1042	77
514	S[353]	1954	230	572	S[295]	1026	230
515	S[352]	1938	77	573	S[294]	1010	77
516	S[351]	1922	230	574	S[293]	994	230

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No.	Name	X	Y	No.	Name	X	Y
575	S[292]	978	77	633	S[234]	-1034	77
576	S[291]	962	230	634	S[233]	-1050	230
577	S[290]	946	77	635	S[232]	-1066	77
578	S[289]	930	230	636	S[231]	-1082	230
579	S[288]	914	77	637	S[230]	-1098	77
580	S[287]	898	230	638	S[229]	-1114	230
581	S[286]	882	77	639	S[228]	-1130	77
582	S[285]	866	230	640	S[227]	-1146	230
583	S[284]	850	77	641	S[226]	-1162	77
584	S[283]	834	230	642	S[225]	-1178	230
585	S[282]	818	77	643	S[224]	-1194	77
586	S[281]	802	230	644	S[223]	-1210	230
587	S[280]	786	77	645	S[222]	-1226	77
588	S[279]	770	230	646	S[221]	-1242	230
589	S[278]	754	77	647	S[220]	-1258	77
590	S[277]	738	230	648	S[219]	-1274	230
591	S[276]	722	77	649	S[218]	-1290	77
592	S[275]	706	230	650	S[217]	-1306	230
593	S[274]	690	77	651	S[216]	-1322	77
594	S[273]	674	230	652	S[215]	-1338	230
595	S[272]	658	77	653	S[214]	-1354	77
596	S[271]	642	230	654	S[213]	-1370	230
597	S[270]	626	77	655	S[212]	-1386	77
598	S[269]	610	230	656	S[211]	-1402	230
599	S[268]	594	77	657	S[210]	-1418	77
600	S[267]	578	230	658	S[209]	-1434	230
601	S[266]	562	77	659	S[208]	-1450	77
602	S[265]	546	230	660	S[207]	-1466	230
603	S[264]	-554	77	661	S[206]	-1482	77
604	S[263]	-570	230	662	S[205]	-1498	230
605	S[262]	-586	77	663	S[204]	-1514	77
606	S[261]	-602	230	664	S[203]	-1530	230
607	S[260]	-618	77	665	S[202]	-1546	77
608	S[259]	-634	230	666	S[201]	-1562	230
609	S[258]	-650	77	667	S[200]	-1578	77
610	S[257]	-666	230	668	S[199]	-1594	230
611	S[256]	-682	77	669	S[198]	-1610	77
612	S[255]	-698	230	670	S[197]	-1626	230
613	S[254]	-714	77	671	S[196]	-1642	77
614	S[253]	-730	230	672	S[195]	-1658	230
615	S[252]	-746	77	673	S[194]	-1674	77
616	S[251]	-762	230	674	S[193]	-1690	230
617	S[250]	-778	77	675	S[192]	-1706	77
618	S[249]	-794	230	676	S[191]	-1722	230
619	S[248]	-810	77	677	S[190]	-1738	77
620	S[247]	-826	230	678	S[189]	-1754	230
621	S[246]	-842	77	679	S[188]	-1770	77
622	S[245]	-858	230	680	S[187]	-1786	230
623	S[244]	-874	77	681	S[186]	-1802	77
624	S[243]	-890	230	682	S[185]	-1818	230
625	S[242]	-906	77	683	S[184]	-1834	77
626	S[241]	-922	230	684	S[183]	-1850	230
627	S[240]	-938	77	685	S[182]	-1866	77
628	S[239]	-954	230	686	S[181]	-1882	230
629	S[238]	-970	77	687	S[180]	-1898	77
630	S[237]	-986	230	688	S[179]	-1914	230
631	S[236]	-1002	77	689	S[178]	-1930	77
632	S[235]	-1018	230	690	S[177]	-1946	230

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No.	Name	X	Y	No.	Name	X	Y
691	S[176]	-1962	77	749	S[118]	-2940	77
692	S[175]	-1978	230	750	S[117]	-2956	230
693	S[174]	-1994	77	751	S[116]	-2972	77
694	S[173]	-2010	230	752	S[115]	-2988	230
695	S[172]	-2026	77	753	S[114]	-3004	77
696	S[171]	-2042	230	754	S[113]	-3020	230
697	S[170]	-2058	77	755	S[112]	-3036	77
698	S[169]	-2074	230	756	S[111]	-3052	230
699	S[168]	-2090	77	757	S[110]	-3068	77
700	S[167]	-2106	230	758	S[109]	-3084	230
701	S[166]	-2122	77	759	S[108]	-3100	77
702	S[165]	-2138	230	760	S[107]	-3116	230
703	S[164]	-2154	77	761	S[106]	-3132	77
704	S[163]	-2170	230	762	S[105]	-3148	230
705	S[162]	-2186	77	763	S[104]	-3164	77
706	S[161]	-2202	230	764	S[103]	-3180	230
707	S[160]	-2218	77	765	S[102]	-3196	77
708	S[159]	-2234	230	766	S[101]	-3212	230
709	S[158]	-2250	77	767	S[100]	-3228	77
710	S[157]	-2266	230	768	S[99]	-3244	230
711	S[156]	-2282	77	769	S[98]	-3260	77
712	S[155]	-2298	230	770	S[97]	-3276	230
713	S[154]	-2314	77	771	S[96]	-3292	77
714	S[153]	-2330	230	772	S[95]	-3308	230
715	S[152]	-2346	77	773	S[94]	-3324	77
716	S[151]	-2362	230	774	S[93]	-3340	230
717	S[150]	-2378	77	775	S[92]	-3356	77
718	S[149]	-2394	230	776	S[91]	-3372	230
719	S[148]	-2410	77	777	S[90]	-3388	77
720	S[147]	-2426	230	778	S[89]	-3404	230
721	S[146]	-2442	77	779	S[88]	-3420	77
722	S[145]	-2458	230	780	S[87]	-3436	230
723	S[144]	-2474	77	781	S[86]	-3452	77
724	S[143]	-2490	230	782	S[85]	-3468	230
725	S[142]	-2506	77	783	S[84]	-3484	77
726	S[141]	-2522	230	784	S[83]	-3500	230
727	S[140]	-2538	77	785	S[82]	-3516	77
728	S[139]	-2554	230	786	S[81]	-3532	230
729	S[138]	-2570	77	787	S[80]	-3548	77
730	S[137]	-2586	230	788	S[79]	-3564	230
731	S[136]	-2602	77	789	S[78]	-3580	77
732	S[135]	-2618	230	790	S[77]	-3596	230
733	S[134]	-2634	77	791	S[76]	-3612	77
734	S[133]	-2650	230	792	S[75]	-3628	230
735	S[132]	-2716	77	793	S[74]	-3644	77
736	S[131]	-2732	230	794	S[73]	-3660	230
737	S[130]	-2748	77	795	S[72]	-3676	77
738	S[129]	-2764	230	796	S[71]	-3692	230
739	S[128]	-2780	77	797	S[70]	-3708	77
740	S[127]	-2796	230	798	S[69]	-3724	230
741	S[126]	-2812	77	799	S[68]	-3740	77
742	S[125]	-2828	230	800	S[67]	-3756	230
743	S[124]	-2844	77	801	S[66]	-3772	77
744	S[123]	-2860	230	802	S[65]	-3788	230
745	S[122]	-2876	77	803	S[64]	-3804	77
746	S[121]	-2892	230	804	S[63]	-3820	230
747	S[120]	-2908	77	805	S[62]	-3836	77
748	S[119]	-2924	230	806	S[61]	-3852	230

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No.	Name	X	Y	No.	Name	X	Y
807	S[60]	-3868	77	865	S[2]	-4796	77
808	S[59]	-3884	230	866	S[1]	-4812	230
809	S[58]	-3900	77	867	DUMMY	-4828	77
810	S[57]	-3916	230	868	DUMMY	-4844	230
811	S[56]	-3932	77	869	DUMMY	-4860	77
812	S[55]	-3948	230	870	DUMMY	-4876	230
813	S[54]	-3964	77	871	DUMMY	-4892	77
814	S[53]	-3980	230	872	DUMMY	-4908	230
815	S[52]	-3996	77	873	DUMMY	-4924	77
816	S[51]	-4012	230	874	DUMMY	-4940	230
817	S[50]	-4028	77	875	G[219]	-4956	77
818	S[49]	-4044	230	876	G[217]	-4972	230
819	S[48]	-4060	77	877	G[215]	-4988	77
820	S[47]	-4076	230	878	G[213]	-5004	230
821	S[46]	-4092	77	879	G[211]	-5020	77
822	S[45]	-4108	230	880	G[209]	-5036	230
823	S[44]	-4124	77	881	G[207]	-5052	77
824	S[43]	-4140	230	882	G[205]	-5068	230
825	S[42]	-4156	77	883	G[203]	-5084	77
826	S[41]	-4172	230	884	G[201]	-5100	230
827	S[40]	-4188	77	885	G[199]	-5116	77
828	S[39]	-4204	230	886	G[197]	-5132	230
829	S[38]	-4220	77	887	G[195]	-5148	77
830	S[37]	-4236	230	888	G[193]	-5164	230
831	S[36]	-4252	77	889	G[191]	-5180	77
832	S[35]	-4268	230	890	G[189]	-5196	230
833	S[34]	-4284	77	891	G[187]	-5212	77
834	S[33]	-4300	230	892	G[185]	-5228	230
835	S[32]	-4316	77	893	G[183]	-5244	77
836	S[31]	-4332	230	894	G[181]	-5260	230
837	S[30]	-4348	77	895	G[179]	-5276	77
838	S[29]	-4364	230	896	G[177]	-5292	230
839	S[28]	-4380	77	897	G[175]	-5308	77
840	S[27]	-4396	230	898	G[173]	-5324	230
841	S[26]	-4412	77	899	G[171]	-5340	77
842	S[25]	-4428	230	900	G[169]	-5356	230
843	S[24]	-4444	77	901	G[167]	-5372	77
844	S[23]	-4460	230	902	G[165]	-5388	230
845	S[22]	-4476	77	903	G[163]	-5404	77
846	S[21]	-4492	230	904	G[161]	-5420	230
847	S[20]	-4508	77	905	G[159]	-5436	77
848	S[19]	-4524	230	906	G[157]	-5452	230
849	S[18]	-4540	77	907	G[155]	-5468	77
850	S[17]	-4556	230	908	G[153]	-5484	230
851	S[16]	-4572	77	909	G[151]	-5500	77
852	S[15]	-4588	230	910	G[149]	-5516	230
853	S[14]	-4604	77	911	G[147]	-5532	77
854	S[13]	-4620	230	912	G[145]	-5548	230
855	S[12]	-4636	77	913	G[143]	-5564	77
856	S[11]	-4652	230	914	G[141]	-5580	230
857	S[10]	-4668	77	915	G[139]	-5596	77
858	S[9]	-4684	230	916	G[137]	-5612	230
859	S[8]	-4700	77	917	G[135]	-5628	77
860	S[7]	-4716	230	918	G[133]	-5644	230
861	S[6]	-4732	77	919	G[131]	-5660	77
862	S[5]	-4748	230	920	G[129]	-5676	230
863	S[4]	-4764	77	921	G[127]	-5692	77
864	S[3]	-4780	230	922	G[125]	-5708	230

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No.	Name	X	Y
923	G[123]	-5724	77
924	G[121]	-5740	230
925	G[119]	-5756	77
926	G[117]	-5772	230
927	G[115]	-5788	77
928	G[113]	-5804	230
929	G[111]	-5820	77
930	G[109]	-5836	230
931	G[107]	-5852	77
932	G[105]	-5868	230
933	G[103]	-5884	77
934	G[101]	-5900	230
935	G[99]	-5916	77
936	G[97]	-5932	230
937	G[95]	-5948	77
938	G[93]	-5964	230
939	G[91]	-5980	77
940	G[89]	-5996	230
941	G[87]	-6012	77
942	G[85]	-6028	230
943	G[83]	-6044	77
944	G[81]	-6060	230
945	G[79]	-6076	77
946	G[77]	-6092	230
947	G[75]	-6108	77
948	G[73]	-6124	230
949	G[71]	-6140	77
950	G[69]	-6156	230
951	G[67]	-6172	77
952	G[65]	-6188	230
953	G[63]	-6204	77
954	G[61]	-6220	230
955	G[59]	-6236	77
956	G[57]	-6252	230
957	G[55]	-6268	77
958	G[53]	-6284	230
959	G[51]	-6300	77
960	G[49]	-6316	230
961	G[47]	-6332	77
962	G[45]	-6348	230
963	G[43]	-6364	77
964	G[41]	-6380	230
965	G[39]	-6396	77
966	G[37]	-6412	230
967	G[35]	-6428	77
968	G[33]	-6444	230
969	G[31]	-6460	77
970	G[29]	-6476	230
971	G[27]	-6492	77
972	G[25]	-6508	230
973	G[23]	-6524	77
974	G[21]	-6540	230
975	G[19]	-6556	77
976	G[17]	-6572	230
977	G[15]	-6588	77
978	G[13]	-6604	230
979	G[11]	-6620	77
980	G[9]	-6636	230

No.	Name	X	Y
981	G[7]	-6652	77
982	G[5]	-6668	230
983	G[3]	-6684	77
984	G[1]	-6700	230
985	DUMMY	-6716	77
986	DUMMY	-6732	230
987	DUMMY	-6748	77
988	DUMMY	-6764	230

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5. Pin Function

Table 2 Interface

Signal	I/O	Connect to	Function						When not in use	
IM3-1, IM0/ID	I	GND or VDDI	Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.						-	
			IM3	IM2	IM1	IM0	Interface Mode	DB Pin in use		
			0	0	0	0	M68-system 16-bit interface	DB[17:10], DB[8:1]		
			0	0	0	1	M68-system 8-bit interface	DB[17:10]		
			0	0	1	0	i80-system 16-bit interface	DB[17-10], DB[8-1]		
			0	0	1	1	i80-system 8-bit interface	DB[17-10]		
			0	1	0	(ID)	24-bit 4 wires Serial Peripheral Interface (SPI)	SDI, SDO, SCL, CSX		
			0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, CSX		
			0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, CSX, RS(DCX)		
			1	0	0	0	M68-system 18-bit interface	DB[17-0]		
			1	0	0	1	M68-system 9-bit interface	DB[17-9]		
			1	0	1	0	i80-system 18-bit interface	DB[17-0]		
			1	0	1	1	i80-system 9-bit interface	DB[17-9]		
			1	1	*	*	Setting disabled	-		
			When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.							
CSX	I	MPU	Chip select signal. Amplitude: VDDI-GND Low: the RM68130 is selected and accessible High: the RM68130 is not selected and not accessible.						GND	
RS(DCX)	I	MPU	Register select signal. Amplitude: VDDI-GND Low: select Index or status register High: select control register Fix to either VDDI or DGND when not in use						VDDI	

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WRX/SCL	I	MPU	In 68-system mode, this is used to select operation, read or write. (RW) In 80-system mode, this serves as a write strobe signal (WRX) and enables write operation when WRX is low. In SPI mode, it serves as a synchronous clock (SCL). Amplitude: VDDI -GND	VDDI
RDX	I	MPU	In 68-system mode, this serves as write/read enable strobe (E). In 80-system mode, this serves as a read strobe signal. (RDX) and enables read operation when RDX is low. Must be fixed to GND level when SPI mode. Amplitude: VDDI -GND	VDDI
RESET	I	MPU	Reset signal. Initializes the RM68130 when it is low. Make sure to execute a power-on reset when turning on power supply. Amplitude: VDDI-IOGND.	-
SDI_SDA	I/O	MPU	Serial data input (SDI) pin in serial interface operation. The data is inputted and latched on the rising edge of the SCL signal. In the 24-bit 4 wires serial peripheral interface, this pin is used as input pin. In the 8/9-bit SPI, this pin is a bi-directional data pin. Amplitude: VDDI -GND	GND
SDO	O	MPU	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: VDDI -GND	Open
DB0-DB17	I/O	MPU	18-bit parallel bi-directional data bus for 80/68-system interface operation. Amplitude: VDDI-GND. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-DB1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation. Amplitude: VDDI-GND. 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used. Unused pins must be fixed to GND level.	GND or VDDI

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ENABLE	I	MPU	Data enable signal for RGB interface operation. Low: accessible (select) High: Not accessible (Not select) The EPL bit inverts the polarity of the ENABLE signal. Amplitude: VDDI-GND.	GND or VDDI
VSYNC	I	MPU	Frame synchronous signal for RGB interface operation.. VSPL = "0": Active low. VSPL = "1": Active high. The VSPL bit inverts the polarity of the VSYNC signal. Amplitude: VDDI-GND.	GND or VDDI
H SYNC	I	MPU	Line synchronous signal for RGB interface operation. HSPL = "0": Active low. HSPL = "1": Active high. The HSPL bit inverts the polarity of the HSYNC signal. Amplitude: VDDI-GND.	GND or VDDI
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. Amplitude: VDDI -GND. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK	GND or VDDI
FMARK	O	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: VDDI -GND).	Open

Table 3 Power supply

Signal	I/O	Connect to	Function	When not in use
AVDD	O		Output pin of the X2 charge pump. This pin is also the power input for VGH and VGL charge pump.	
AVCL	O		Output pin of the X(-2) charge pump. This pin is also the power input for generating GVCL.	
VGH	O		Power supply for gate driver.	-

VGL	O		Power supply (negative) for gate driver.	-
GVDD	O		source driver (positive) grayscale reference voltage level	-
GVCL	O		source driver (negative) grayscale reference voltage level	-
DVDD	O		internal logic regulator output, which is used as the power supply to internal logic.	-
VDDI	I	VDDI	Power supply for I/O system.	
VCI	I	VCI	Power supply for analog system.	
DGND	I	GND	System ground for I/O system and digital system.	
AGND	I	GND	System ground for analog system.	

Table 4 LCD drive

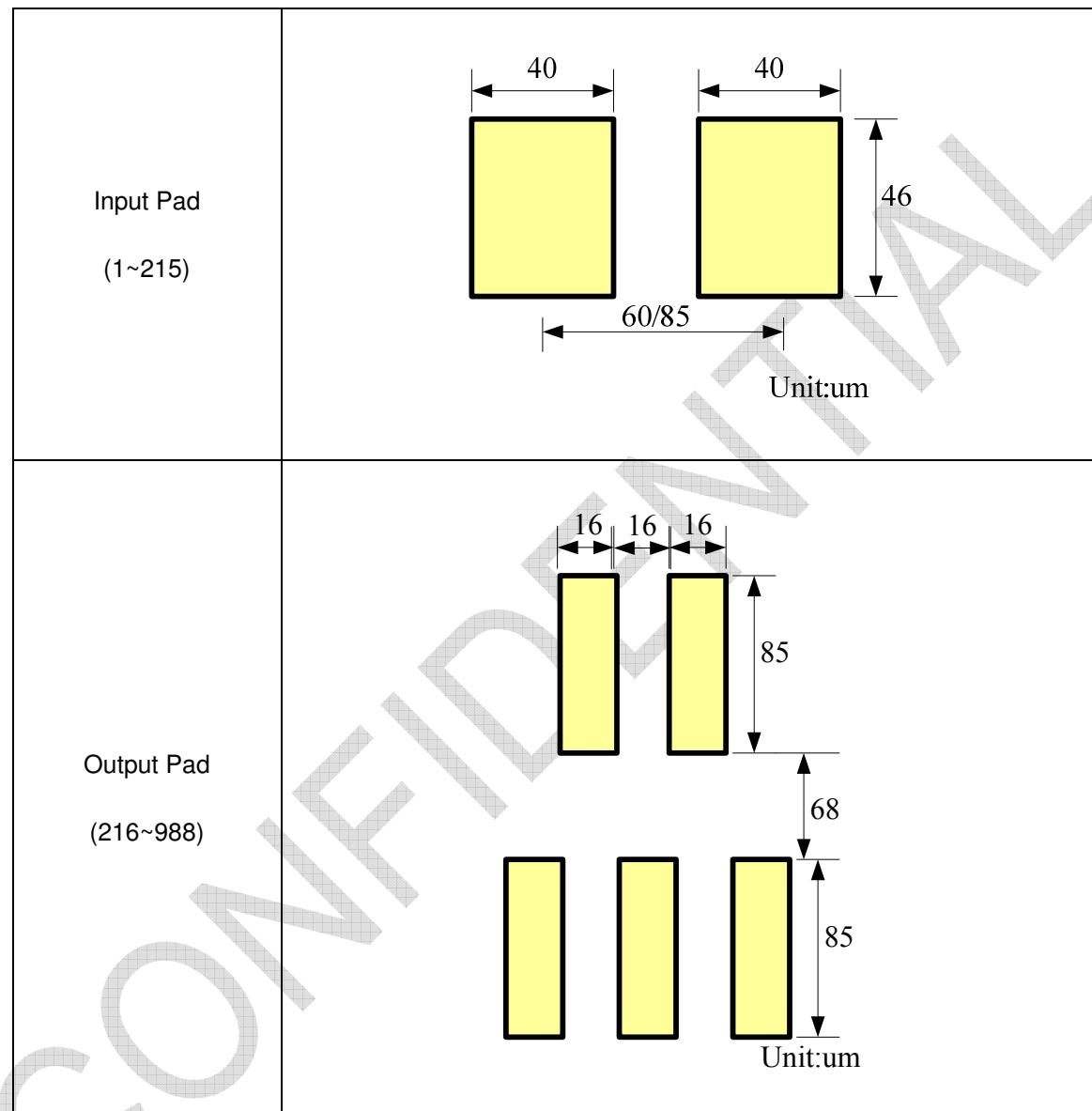
Signal	I/ O	Connect to	Function	When not in use
VCOM	O	TFT panel common electrode	A power supply for the TFT-LCD common electrode.	
S1~S528	O	LCD	Source driver output pins.	
G1~G220	O	LCD	Gate driver output pins.	

Table 5 Others (test, dummy pins)

Signal	I/O	Connect to	Function	When not in use
DUMMY	-	Open	Dummy pad and no output	Open
TEST01-7	O	Open	Test pins. If this is not used. Tie DGND/VDDI.	DGND/VDDI
TS4-0	I	Open	Test pins. Leave them open.	Open GND

6. Bump Arrangement

BUMP Size



7. Function Description

7.1 System Interface

The RM68130 supports 80/68-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The RM68130 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information about control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the RM68130 performs the first read operation from the internal GRAM. Valid data is read out when the RM68130 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 6 Register Selection (80/68-system 8/9/16/18-bit Parallel Interface)

WRX	RDX	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 7 Register Selection (Clock synchronous serial interface)

Start byte		Function
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 8 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	0	68-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	0	1	68-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	1	1	80-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	*	Clock synchronous serial interface	(SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	1	0	9-bit 3-wire SPI	SDA, SCL, CSX	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	Single transfer (8 bits)
0	1	1	1	8-bit 4-wire SPI	SDA, SCL, CSX, RS(DCX)	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	Single transfer (8 bits)
1	0	0	0	68-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	0	1	68-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	0	1	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	1	1	80-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	*	*	Setting disabled	-	-	-

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7.2 External Display Interface (RGB, VSYNC interfaces)

The RM68130 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display interface” section.

The RM68130 allows switching interface by instruction according to the still and/or moving pictures display required. Via the RGB interface, the RM68130 writes all display data to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display.

7.3 Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the RM68130 writes data to the internal GRAM, the address in the AC is automatically increased or decreased one step. The window address function enables writing data only within the rectangular area specified in the GRAM.

7.4 Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 87,120 (176RGB x 220 x18/8) bytes with 18 bits per pixel.

7.5 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal driving voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

7.6 Timing Generator

The timing generator produces timing signals for the operations of internal circuits such as the internal GRAM, source driver, etc. The timing signals for display operations such as RAM read operation and the timing signals for internal operations such as RAM access from the MPU are generated separately in order to avoid mutual interference.

7.7 Oscillator (OSC)

The RM68130 generates the RC oscillation clock by internal RC oscillator circuit. The frame rate is adjusted by the register setting.

7.8 Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the RM68130 consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). The display pattern data is latched when 528 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for each LCD module.

7.9 Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

8. GRAM Address Map and Read/Write

Table 9 GRAM address and display position on the panel (SS = 0, BGR = 0)

GS=0		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	WD[17:0]																								
G1	G220	h0000		h0001		h0002		h0003			h00AC		h00AD		h00AE		h00AF								
G2	G219	h0100		h00101		h0102		h0103			h01AC		h01AD		h01AE		h01AF								
G3	G218	h0200		h0201		h0202		h0203			h02AC		h02AD		h02AE		h02AF								
G4	G217	h0300		h0301		h0302		h0303			h03AC		h03AD		h03AE		h03AF								
G5	G216	h0400		h0401		h0402		h0403			h04AC		h04AD		h04AE		h04AF								
G6	G215	h0500		h0501		h0502		h0503			h05AC		h05AD		h05AE		h05AF								
G7	G214	h0600		h0601		h0602		h0603			h06AC		h06AD		h06AE		h06AF								
G8	G213	h0700		h0701		h0702		h0703			h07AC		h07AD		h07AE		h07AF								
G9	G212	h0800		h0801		h0802		h0803			h08AC		h08AD		h08AE		h08AF								
G10	G211	h0900		h0901		h0902		h0903			h09AC		h09AD		h09AE		h09AF								
G11	G210	h0A00		h0A01		h0A02		h0A03			h0AAC		h0AAD		h0AAE		h0AAF								
G12	G209	h0B00		h0B01		h0B02		h0B03			h0BAC		h0BAD		h0BAE		h0BAF								
G209	G12	hD000		hD001		hD002		hD003			hD0AC		hD0AD		hD0AE		hD0AF								
G210	G11	hD100		hD101		hD102		hD103			hD1AC		hD1AD		hD1AE		hD1AF								
G211	G10	hD200		hD201		hD202		hD203			hD2AC		hD2AD		hD2AE		hD2AF								
G212	G9	hD300		hD301		hD302		hD303			hD3AC		hD3AD		hD3AE		hD3AF								
G213	G8	hD400		hD401		hD402		hD403			hD4AC		hD4AD		hD4AE		hD4AF								
G214	G7	hD500		hD501		hD502		hD503			hD5AC		hD5AD		hD5AE		hD5AF								
G215	G6	hD600		hD601		hD602		hD603			hD6AC		hD6AD		hD6AE		hD6AF								
G216	G5	hD700		hD701		hD702		hD703			hD7AC		hD7AD		hD7AE		hD7AF								
G217	G4	hD800		hD801		hD802		hD803			hD8AC		hD8AD		hD8AE		hD8AF								
G218	G3	hD900		hD901		hD902		hD903			hD9AC		hD9AD		hD9AE		hD9AF								
G219	G2	hDA00		hDA01		hDA02		hDA03			hDAAC		hDAAD		hDAAE		hDAAF								
G220	G1	hDB00		hDB01		hDB02		hDB03			hDBAC		hDBAD		hDBAE		hDBAF								

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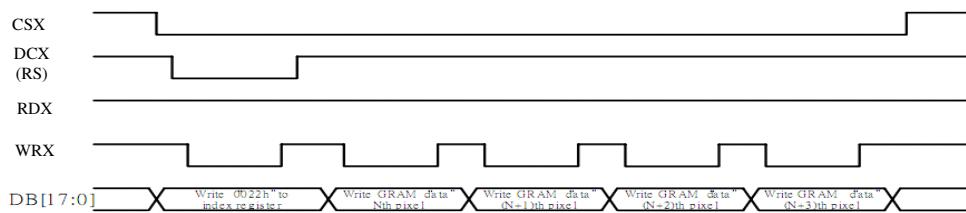
Table 10 GRAM address and display position on the panel (SS = 1, BGR = 1)

GS=0		S5 ₈ S5 ₂₇ S5 ₂₆	S5 ₂₅ S5 ₂₄ S5 ₂₃	S5 ₂₂ S5 ₂₁ S5 ₂₀	S5 ₁₉ S5 ₁₈ S5 ₁₇	S1 ₂ S1 ₁ S1 ₀	S9 S8 S7	S6 S5 S4	S3 S2 S1
GS=0	GS=1	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]
G1	G220	h0000	h0001	h0002	h0003	h00AC	h00AD	h00AE	h00AF
G2	G219	h0100	h00101	h0102	h0103	h01AC	h01AD	h01AE	h01AF
G3	G218	h0200	h0201	h0202	h0203	h02AC	h02AD	h02AE	h02AF
G4	G217	h0300	h0301	h0302	h0303	h03AC	h03AD	h03AE	h03AF
G5	G216	h0400	h0401	h0402	h0403	h04AC	h04AD	h04AE	h04AF
G6	G215	h0500	h0501	h0502	h0503	h05AC	h05AD	h05AE	h05AF
G7	G214	h0600	h0601	h0602	h0603	h06AC	h06AD	h06AE	h06AF
G8	G213	h0700	h0701	h0702	h0703	h07AC	h07AD	h07AE	h07AF
G9	G212	h0800	h0801	h0802	h0803	h08AC	h08AD	h08AE	h08AF
G10	G211	h0900	h0901	h0902	h0903	h09AC	h09AD	h09AE	h09AF
G11	G210	h0A00	h0A01	h0A02	h0A03	h0AAC	h0AAD	h0AAE	h0AAF
G12	G209	h0B00	h0B01	h0B02	h0B03	h0BAC	h0BAD	h0BAE	h0BAF
.....
G209	G12	hD000	hD001	hD002	hD003	hD0AC	hD0AD	hD0AE	hD0AF
G210	G11	hD100	hD101	hD102	hD103	hD1AC	hD1AD	hD1AE	hD1AF
G211	G10	hD200	hD201	hD202	hD203	hD2AC	hD2AD	hD2AE	hD2AF
G212	G9	hD300	hD301	hD302	hD303	hD3AC	hD3AD	hD3AE	hD3AF
G213	G8	hD400	hD401	hD402	hD403	hD4AC	hD4AD	hD4AE	hD4AF
G214	G7	hD500	hD501	hD502	hD503	hD5AC	hD5AD	hD5AE	hD5AF
G215	G6	hD600	hD601	hD602	hD603	hD6AC	hD6AD	hD6AE	hD6AF
G216	G5	hD700	hD701	hD702	hD703	hD7AC	hD7AD	hD7AE	hD7AF
G217	G4	hD800	hD801	hD802	hD803	hD8AC	hD8AD	hD8AE	hD8AF
G218	G3	hD900	hD901	hD902	hD903	hD9AC	hD9AD	hD9AE	hD9AF
G219	G2	hDA00	hDA01	hDA02	hDA03	hDAAC	hDAAD	hDAAE	hDAAF
G220	G1	hDB00	hDB01	hDB02	hDB03	hDBAC	hDBAD	hDBAE	hDBAF

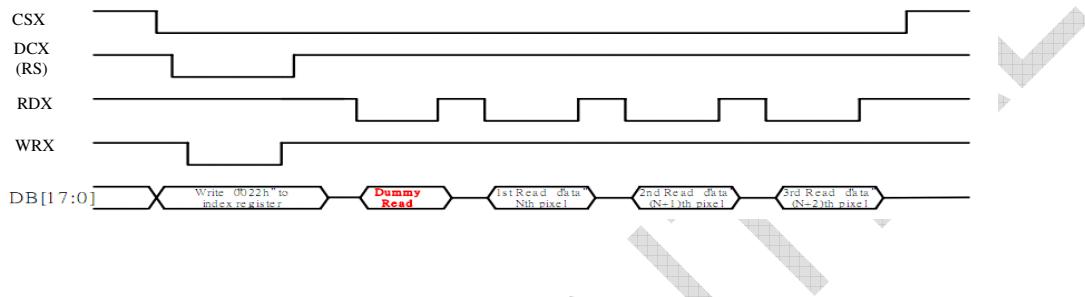
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i80 18-/16-bit System Bus Interface Timing

(a) Write to GRAM

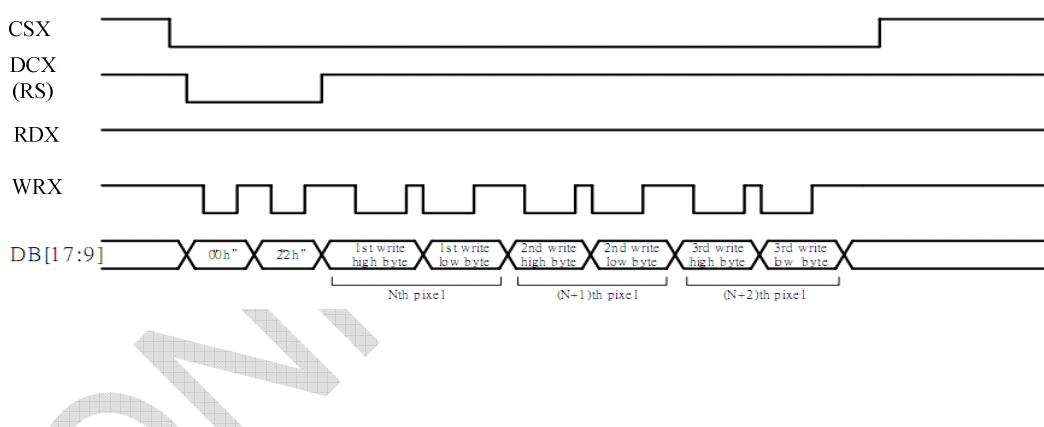


(b) Read from GRAM

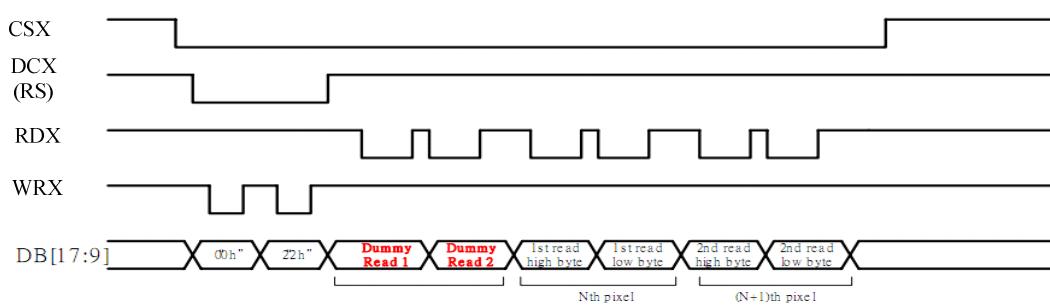


i80 9-/8-bit System Bus Interface Timing

(a) Write to GRAM

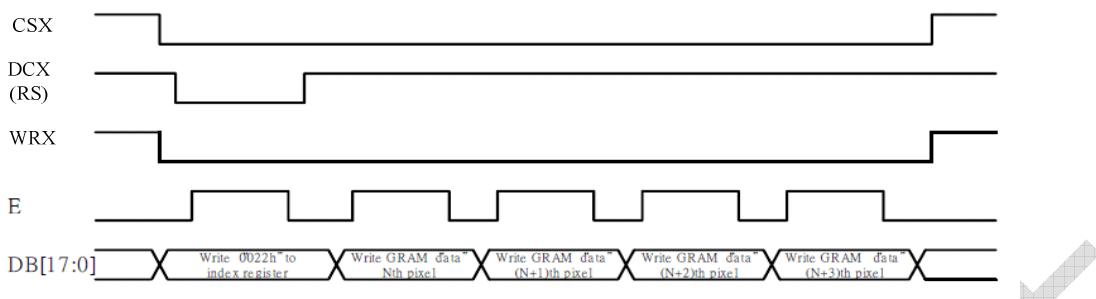


(b) Read from GRAM

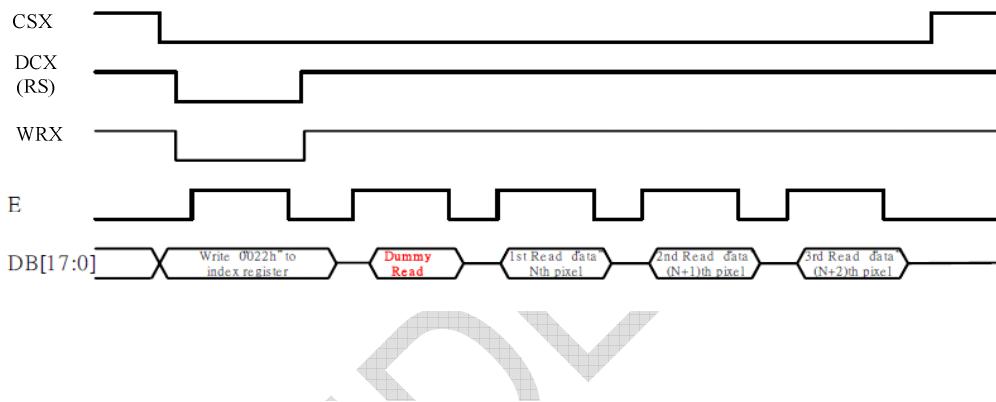


M68 18-/16-bit System Bus Interface Timing

(a) Write to GRAM

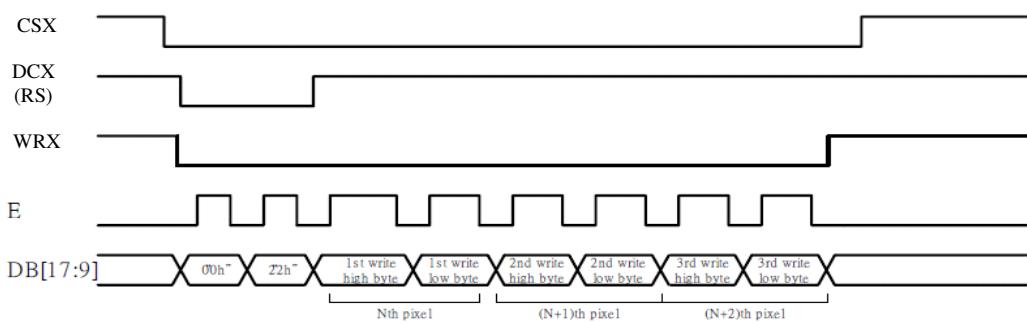


(b) Read from GRAM

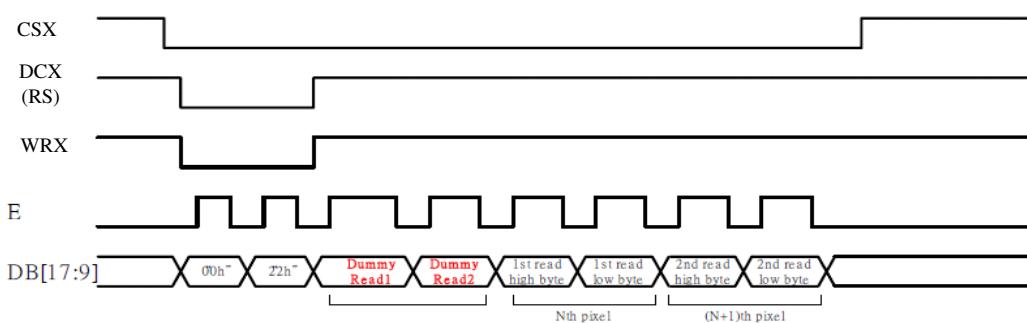


M68 9-/8-bit System Bus Interface Timing

(a) Write to GRAM



(b) Read from GRAM



9. Instruction

9.1 Outline

The RM68130 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. All the functional blocks of RM68130 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (RDX/WRX) and data bus D17-0 are used to read/write the instructions and data of RM68130. When accessing the RM68130's internal RAM, data is processed in units of 18 bits. The following are the categories of instruction in RM68130.

1. Specify the index of register
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. γ -correction
7. Window address control
8. Panel display control

The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the loading on the microcomputer. The RM68130 writes instructions consecutively by executing the instruction within the cycle when it is written, meanwhile, there is no instruction execution time required.

9.2 Instruction Data Format

The data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface. For more details, please refer to section of "System Interface".

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

9.3 Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

9.4 ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	0	1	1	0	1	0	0	0	0	0	0	1	0	0	1	1

The ID code “6813”h is outputted when this register is read.

9.5 Display control

9.5.1 Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0

VSPL: Inverts the polarity of signals from the VSYNC pin.

VSPL = "0" : Low active.

VSPL = "1" : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.

HSPL = "0" : Low active.

HSPL = "1" : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.

DPL = "0" : Data are read on the rising edge of the DOTCLK.

DPL = "1" : Data are read on the falling edge of the DOTCLK.

EPL: Set the polarity of the signal from the ENABLE pin in RGB interface mode. .

EPL = "0":

ENABLE = "Low" / Write data to DB[17:0]

ENABLE = "High" / Inhibit data write operation

EPL = "1":

ENABLE = "High" / Write data to DB[17:0]

ENABLE = "Low" / Inhibit data write operation

The following table shows the relationship between the EPL, ENABLE bits, and RAM access

EPL	Enable	RAM write	Ram address
0	0	Enabled	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enabled	Updated

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S528.

When SS = “1”, the source driver output shift from S528 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S528.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S528.

When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S528 to S1.

When changing the SS or BGR bits, RAM data must be rewritten.

GS: Select the shift direction of outputs from the gate driver. The scan order is changeable in accordance to the scan mode by the gate driver. Select an optimum shift direction for the assembly.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

NL[4:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[4:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[4:0]	Number of Lines	NL[4:0]	Number of Lines	NL[4:0]	Number of Lines
5'h00	reserverd	5'h0A	80	5'h14	160
5'h01	8	5'h0B	88	5'h15	168
5'h02	16	5'h0C	96	5'h16	176
5'h03	24	5'h0D	104	5'h17	184
5'h04	32	5'h0E	112	5'h18	192
5'h05	40	5'h0F	120	5'h19	200
5'h06	48	5'h10	128	5'h1A	208
5'h07	56	5'h11	136	5'h1B	216
5'h08	64	5'h12	144	5'h1C	220
5'h09	72	5'h13	152	Others	Setting inhibited

9.5.2 LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	INV	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

INV: VCOM polarity control

When INV=1, dot inversion enabled.

When INV=0, column inversion enabled.

9.5.3 Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	BGR	0	0	MDT1	MDT0	0	0	I/D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the RM68130 writes data to the internal GRAM.

AM = "0", sets the horizontal direction.

AM = "1", sets the vertical direction.

When making a window address area, the data is written only within the area in the direction determined by I/D[1:0] and AM.

I/D[1:0]: Either increments or decrements the address counter automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]).

BGR: Reverse the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

MDT1: This bit is active on the 80-system of 8-bit bus and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 80-system of 16-bit bus, and the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set in the 8-bit or 16-bit mode, set MDT1 bit to be "0".

MDT0: When 8-bit or 16-bit 80 interface mode and MDT1 bit =1, MDT0 defines color depth for the IC.

Interface Mode	MDT1	MDT0	Write data to GRAM																		
*	0	0	Default transfer value. Multiple data transfer (MDT[1:0]) function is not available. Data transfer is controlled by interface mode.																		
	0	1	Multiple data transfer (MDT[1:0]) function is not available.																		
80-system 8-bit	1	0	Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
		1	GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	1	1	Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
		1	GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Interface Mode	MDT1	MDT0	Write data to GRAM																		
80-system 16-bit	0	1	Input Data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
		1	GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	1	0	Input Data	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2
		1	GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

8-bit (80-system), MDT0 = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)

8-bit (80-system), MDT0 = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

16-bit (80-system), MDT0 = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)

16-bit (80-system), MDT1 = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

9.5.4 Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	TEMON	0	0	0	0	0	0	0	0	CL	REV	D1	D0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: Set D[1:0] = "11" to turn on the display panel, and D[1:0] = "00" to turn off the display panel.

D[1:0]	source output	Gate output	VCOM output	Display	SRAM Read
00	VSS	VGL	VSS	Off	Off
01	VSS	Operate	VSS	Off	Off
10	NW/NB based on NDL setting		Operate	Off	Off
11	Normal Display	Operate	Operate	On	On

Note: data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

CL: When CL = 1, the RM68130 displays in 8-colors with low power consumption.

CL	Display color
0	262,144
1	8

REV: When REV = "1", the grayscale levels can be inverted.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	Negative polarity
0	18'h000000	V63	V0

1	18'h3FFFFF	V0	V63
	18'h000000	V0	V63

	18'h3FFFFF	V63	V0

TEMON:

TEMON = 1, Enable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.

TEMON = 0, Disable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.

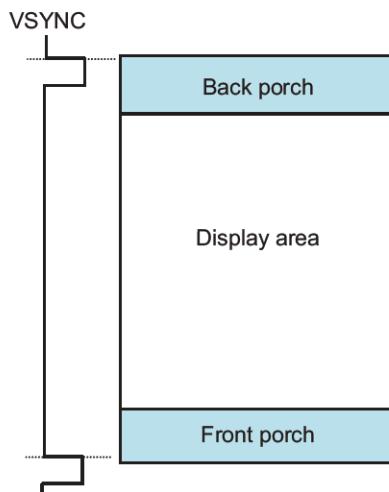
9.5.5 Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [3:0] / BP [3:0]: Sets the number of lines for a front porch period / back porch period (a blank period following the end of display / (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

FP[3:0] BP[3:0]	Front and Back Porch period (Line periods)
4'h00	Setting disabled
4'h01	Setting disabled
4'h02	2 lines
4'h03	3 lines
4'h04	4 lines
4'h05	5 lines
4'h06	6 lines
4'h07	7 lines
4'h08	8 lines
4'h09	9 lines
4'h0A	10 lines
4'h0B	11 lines
4'h0C	12 lines
4'h0D	13 lines
4'h0E	14 lines
4'h0F	Setting disabled



Note : The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

9.5.6 Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTB: When DSTB = 1, the RM68130 enters the deep standby mode, where the power supply for the internal logic is turned off to save more power than the standby mode. Writing the GRAM data or setting any instructions are prohibited during the deep-standby mode and they must be reset after releasing from the deep standby mode.

9.5.7 Frame Cycle Control (R0Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

RTN[3:0]: Set the clock cycle number of one display line.

RTN[3:0]	Clock Cycles per line
4'h0	16 clocks
4'h1	17 clocks
4'h2	18 clocks
4'h3	19 clocks
4'h4	20 clocks
4'h5	21 clocks
4'h6	22 clocks
4'h7	23 clocks
4'h8	24 clocks
4'h9	25 clocks
4'hA	26 clocks
4'hB	27 clocks
4'hC	28 clocks
4'hD	29 clocks
4'hE	30 clocks
4'hF	31 clocks

9.5.8 RGB Input Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format in RGB interface.

RIM[1:0]	RGB interface operation	Display color
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB 11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting disabled	-

Note:

1. Instruction bits are set via system interface.
2. Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

RM	RAM Access Interface
0	System interface / VSYNC interface
1	RGB interface

9.5.9 Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	DIVE 1	DIVE 0	0	0	DIVI 1	DIVI 0	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[7:0]: Sets the output position of frame cycle signal (frame marker). When FMP[7:0] = 8'h00, a high-active pulse FMARK is outputted at the start of back porch period for 1H period .
Make sure the setting restriction $8'h00 \leq FMP \leq BP+NL+FP$.

FMP[7:0]	FMARK output position
8'h00	0
8'h01	1 st line
8'h02	2 nd line
...	...
8'hEA	234 th line
8'hEB	235 th line
8'hEC	236 th line

DIVI[1:0]: Sets the division ratio of the internal clock frequency.

Frame Frequency Calculation

$$\text{Frame frequency} = \frac{f_{osc}}{\text{Clocksper line} \times \text{division ratio} \times (\text{line} + \text{BP} + \text{FP})} [\text{Hz}]$$

fosc : RC oscillation frequency

Line : Number of lines to drive the LCD (NL bits)

Division ratio : DIVI

Clocksper line : RTN

DIV[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

DIVE[1:0]: Sets the division ratio of DOTCLK when RM68130 display operation is synchronized with RGB interface signals.

DIVE[1:0]		Division Ratio	18-bit, 1 transfer		DOTCLK =	6-bit, 3 transfer		DOTCLK =
			RGB interface		5 MHz	RGB interface		15 MHz
2'h0		Setting inhibited	Setting inhibited		-	Setting inhibited		-
2'h1		1/4	4 DOTCLKs		0.8 us	12 DOTCLKs		0.8 us
2'h2		1/8	8 DOTCLKs		1.6 us	24 DOTCLKs		1.6 us
2'h3		1/16	16 DOTCLKs		3.2 us	48 DOTCLKs		3.2 us

9.5.10 Oscillator Control (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSC_EN	
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

OSC_EN: This instruction starts the oscillator from the Halt State in the standby mode. After this instruction, wait at least 10 ms for oscillation to stabilize before giving the next instruction.

OSC_EN	OSC Control
0	OSC. off
1	OSC. on

9.6 Power Control

9.6.1 Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, the RM68130 enters the sleep mode, and the display operation stops except the RC oscillator to reduce the power consumption. No change to the DRAM data and instruction

setting is accepted and the DRAM data and the instruction setting are maintained in SLP mode.

STB: When STB = 1, the RM68130 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal oscillator. Further, no external clock pulses are supplied.

Outputs	Conditions
VCOM	GND
Gate	GND
Source	GND

9.6.2 Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	APO N	0	0	0	0	0	0	0	0	0	0	0	0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the auto booster sequence circuit is stopped. In case of APON=1, booster circuits are automatically and sequentially operated.

9.7 RAM Access Instruction

9.7.1 RAM Address Set (Horizontal Address) (R20h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.7.2 RAM Address Set (Vertical Address) (R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[15:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the RM68130 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note: In RGB interface operation (RM = "1"), the address AD15-0 is set in the address counter every frame on the falling edge of VSYNC.

AD[15:0]	GRAM Data Setting
16'h0000 ~ 16'h00AF	Bitmap data on the 1 st line
16'h0100 ~ 16'h01AF	Bitmap data on the 2 nd line
16'h0200 ~ 16'h02AF	Bitmap data on the 3 rd line
16'h0300 ~ 16'h03AF	Bitmap data on the 4 th line
16'h0400 ~ 16'h04AF	Bitmap data on the 5 th line
..	..
16'hD800 ~ 16'hD8AF	Bitmap data on the 217 th line
16'hD900 ~ 16'hD9AF	Bitmap data on the 218 th line
16'hDA00 ~ 16'hDAAF	Bitmap data on the 219 th line
16'hDB00 ~ 16'hDBAF	Bitmap data on the 220 th line

9.7.3 Write Data to GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1																

RAM write data WD[17:0] is transferred via different data bus in different interface operation.

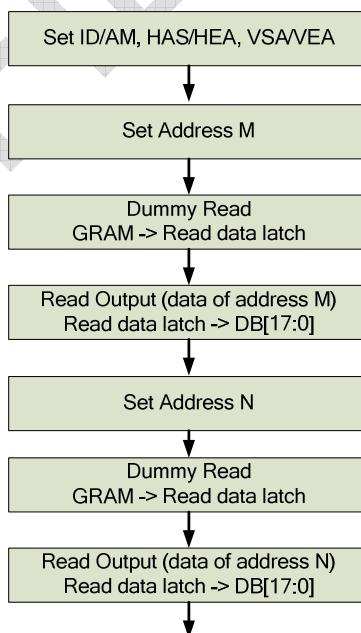
This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

9.7.4 Read Data from GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1																

RAM read data RD[17:0] is transferred via different data bus in different interface operation.

Read 18-bit data from GRAM through the read data register (RDR).



9.8 Software Reset (R28h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	1	1	0	0	1	1	1	0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When Software Reset parameter is 00CEh, it cause a software reset. This register automatically set to Zero after a Software Reset.

9.9 Gate Scan Control (R30H)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
	Default	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN[4:0]: Specifies the gate line where the gate driver starts scan.

SCN[4:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
5'h00	G1	G220	G1	G220
5'h01	G9	G212	G17	G204
5'h02	G17	G204	G33	G188
5'h03	G25	G196	G49	G172
5'h04	G33	G188	G65	G156
5'h05	G41	G180	G81	G140
5'h06	G49	G172	G97	G124
5'h07	G57	G164	G113	G108
5'h08	G65	G156	G129	G92
5'h09	G73	G148	G145	G76
5'h0A	G81	G140	G161	G60
5'h0B	G89	G132	G177	G44
5'h0C	G97	G124	G193	G28
5'h0D	G105	G116	G209	G12
5'h0E	G113	G108	G2	G219
5'h0F	G121	G100	G18	G203
5'h10	G129	G92	G34	G187
5'h11	G137	G84	G50	G171
5'h12	G145	G76	G66	G155
5'h13	G153	G68	G82	G139
5'h14	G161	G60	G98	G123
5'h15	G169	G52	G114	G107
5'h16	G177	G44	G130	G91
5'h17	G185	G36	G146	G75
5'h18	G193	G28	G162	G59
5'h19	G201	G20	G178	G43
5'h1A	G209	G12	G194	G27
5'h1B	G217	G4	G210	G11

9.10 Vertical Scroll Control 1 (R31h, R32h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R31h	W	1	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0
R32h	W	1	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0
R31h	Default	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1

SSA[7:0]: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA[7:0]	Scroll Start Lines
8'h00	0
8'h01	1
8'h02	2
8'h03	3
...	...
8'hD9	217
8'hDA	218
8'hDB	219

SEA[7:0]: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA[7:0]	Scroll End Lines
8'h00	0
8'h01	1
8'h02	2
8'h03	3
...	...
8'hD9	217
8'hDA	218
8'hDB	219

[Note]

Do not set any higher raster-row than 219 ("DB" H).

Set SS17-10 ≤ SSA7-0, if set out of range, SSA7-0 = SS17-10.

Set SE17-10 ≥ SEA7-0, if set out of range, SEA7-0 = SE17-10

9.11 Vertical Scroll Control 2 (R33h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SST[7:0]: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any line from the 1st to 220th can be scrolled for the number of the raster-row. After 219th line is displayed, the display restarts from

the first raster-row. When SST7-0 = 00000000, Vertical Scroll Function is disabled.

SST[7:0]	Scrolling Lines
8'h00	0
8'h01	1
8'h02	2
8'h03	3
...	...
8'hD9	217
8'hDA	218
8'hDB	219

[Note]

Do not set any higher raster-row than 219 ("DB" H).

Set SS17-10 < SSA7-0 + SST7-0 ≤ SEA7-0 ≤ SE17-10, if set out of range, Scroll function is disabled.

9.12 Partial Screen Driving Position (R34h, R35h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R34h	W	1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
R35h	W	1	0	0	0	0	0	0	0	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R34h	Default	0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1
R35h		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SE1[7:0]: Specify the driving end position for the screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For example, when SS1[7:0] = 019h and SE1[7:0] = 029h are set, the LCD driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS1[7:0] ≤ SE1[7:0] ≤ DBh.

SS1[7:0]: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

[Note] : Do not set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.

Ex) SS1[7:0]=07h and SE1[7:0]=10h are performed from G8 to G17.

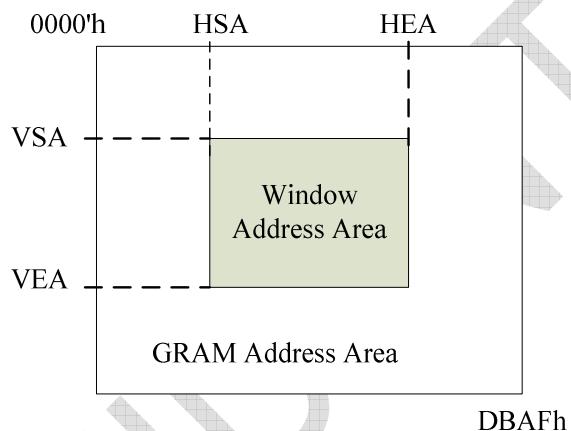
9.13 Window Address Position (R36h/R37h, R38h/R39h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R36h	W	1	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
R37h	W	1	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R38h	W	1	0	0	0	0	0	0	0	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
R39h	W	1	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R36h	Default	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	1
R37h		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R38h		0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	1

R39h		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
------	--	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that $8'h00 \leq \text{HAS} < \text{HEA} \leq 8'hAF$ and $8'h01 \leq \text{HEA} - \text{HSA}$.

VSA[7:0], VEA[7:0]: VSA[7:0] and VEA[7:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[7:0] and VEA[7:0] specify the vertical range to write data. Set VSA[7:0] and VEA[7:0] before starting RAM write operation. In setting, make sure that $8h00 \leq \text{VSA} < \text{VEA} \leq 8'hDB$.



Note: The window address range must be within the GRAM address space.

9.14 γ Control (R50h~R59h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	KP13	KP12	KP11	KP10	0	0	0	0	KP03	KP02	KP01	KP00
R51h	W	1	0	0	0	0	KP33	KP32	KP31	KP30	0	0	0	0	KP23	KP22	KP21	KP20
R52h	W	1	0	0	0	0	KP53	KP52	KP51	KP50	0	0	0	0	KP43	KP42	KP41	KP40
R53h	W	1	0	0	0	0	RP13	RP12	RP11	RP10	0	0	0	0	RP03	RP02	RP01	RP00
R54h	W	1	0	0	0	0	KN13	KN12	KN11	KN10	0	0	0	0	KN03	KN02	KN01	KN00
R55h	W	1	0	0	0	0	KN33	KN32	KN31	KN30	0	0	0	0	KN23	KN22	KN21	KN20
R56h	W	1	0	0	0	0	KN53	KN52	KN51	KN50	0	0	0	0	KN43	KN42	KN41	KN40
R57h	W	1	0	0	0	0	RN13	RN12	RN11	RN10	0	0	0	0	RN03	RN02	RN01	RN00
R58h	W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VRP01	VRP00
R59h	W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00

KP5-0[3:0] / KN5-0[3:0] : γ Fine Adjustment Register for positive/negative polarity

PRP1-0[3:0] / PRN1-0[3:0] : γ Gradient Adjustment Register for positive/negative polarity

VRP1-0[4:0] / VRN1-0[4:0] : γ Amplitude Adjustment Register for positive/negative polarity

9.15 OTP VCM Control

9.15.1 OTP VCM Programming Control 1 (R60h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	NVM_D5	NVM_D4	NVM_D3	NVM_D2	NVM_D1	NVM_D0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NVM_D[5:0]: OTP programming data.

9.15.2 OTP VCM Programming Control 2 (R61h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	VCM_SEL	0	0	0	0	0	0	ID_PGM_EN	VCM_PGM_EN
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.

ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.

VCM_SEL: Select the VCOMH voltage setting.

VCM_SEL	VCM Selection
0	Use the register R14 to adjust the VCOMH voltage (default)
1	Use the NV memory to adjust the VCOMH voltage

Note: When the VCM NV memory had been programmed, the VCM_SEL bit will be set as '1' automatically.

9.15.3 OTP VCM Status (R62h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VMF4	VMF3	VMF2	VMF1	VMF0
R	1	0	0	PGM_CNT1	PGM_CNT0	0	0	0	0	0	VCM_D6	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VMF: VCOM voltage adjustment

VMF[4]	VMF[3:0]	VCOM Output Level
0	0000	"VCOMS"+16d
0	0001	"VCOMS"+15d
0		
0	1110	"VCOMS"+2d
0	1111	"VCOMS"+1d
1	0000	"VCOMS"
1	0001	"VCOMS"-1d
1	0010	"VCOMS"-2d
1		
1	1110	"VCOMS"-14d
1	1111	"VCOMS"-15d

- 1d=25mV, 2d=50mV 3d=75mV....

After VCOM fine tune, user can use OTP programming to recode the fine tune value.

PGM_CNT[1:0]: OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
2'h0	OTP clean
2'h1	OTP programmed 1 time
2'h2	OTP programmed 2 times
2'h3	OTP programmed 3 times

VCM_D[6:0]: OTP VCM data read value. These bits are read only.

9.15.4 OTP Programming ID Key (R63h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data R60h, it must write R63h with 0xAA55 value first to make OTP programming successfully. If R63h is not written with 0xAA55, OTP programming will fail. See OTP Programming flow.

9.15.5 Read ID Code (R65h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	ID_PGM_CNT1	ID_PGM_CNT0	0	0	0	0	0	0	0	0	ID3	ID2	ID1	ID0
	Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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ID[3:0]: This ID code is stored in the VN memory to record the LCM vendor code (read only).

ID_PGM_CNT[1:0]	Description
2'h0	OTP clean
2'h1	OTP programmed 1 time
2'h2	OTP programmed 2 times
2'h3	OTP programmed 3 times

ID_PGM_CNT[1:0]: OTP programmed record. These bits are read only.

9.16 SPI Read/Write Control (R66h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RW
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used.

If users need to read back the register data by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

R/WX	Description
0	Register write mode (default)
1	Register read mode

9.17 Power Control 3 (RB0h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VGLSEL1	VGLSEL0	0	0	VGHBT1	VGHBT0
Default		0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0

VGHBT: VGH Pump voltage selection

VGHBT[1:0]	DDVDH	DDVDL	VGH
00	VClx2	VClx(-2)	VClx4
01	VClx2	VClx(-2)	VClx5
10 (default)	VClx2	VClx(-2)	VClx6
11	VClx2	VClx(-2)	VClx6

VGLSEL: VGL Pump voltage selection.

VGLSEL[1:0]	DDVDH	DDVDL	VGL
00	VClx2	VClx(-2)	VClx(-3)
01 (default)	VClx2	VClx(-2)	VClx(-4)
10	VClx2	VClx(-2)	VClx(-3)
11	VClx2	VClx(-2)	VClx(-4)

VCM: VCOM voltage selection

VCOM voltage setting.

	VCOMS [5:0]	VCOM									
0	000000	-0.425	16	010000	-0.825	32	100000	-1.225	48	110000	-1.625
1	000001	-0.45	17	010001	-0.85	33	100001	-1.25	49	110001	-1.65
2	000010	-0.475	18	010010	-0.875	34	100010	-1.275	50	110010	-1.675
3	000011	-0.5	19	010011	-0.9	35	100011	-1.3	51	110011	-1.7
4	000100	-0.525	20	010100	-0.925	36	100100	-1.325	52	110100	-1.725
5	000101	-0.55	21	010101	-0.95	37	100101	-1.35	53	110101	-1.75
6	000110	-0.575	22	010110	-0.975	38	100110	-1.375	54	110110	-1.775
7	000111	-0.6	23	010111	-1	39	100111	-1.4	55	110111	-1.8
8	001000	-0.625	24	011000	-1.025	40	101000	-1.425	56	111000	-1.825
9	001001	-0.65	25	011001	-1.05	41	101001	-1.45	57	111001	-1.85
10	001010	-0.675	26	011010	-1.075	42	101010	-1.475	58	111010	-1.875
11	001011	-0.7	27	011011	-1.1	43	101011	-1.5	59	111011	-1.9
12	001100	-0.725	28	011100	-1.125	44	101100	-1.525	60	111100	-1.925
13	001101	-0.75	29	011101	-1.15	45	101101	-1.55	61	111101	-1.95
14	001110	-0.775	30	011110	-1.175	46	101110	-1.575	62	111110	-1.975
15	001111	-0.8	31	011111	-1.2	47	101111	-1.6	63	111111	-2

9.18 Power Control 4 (RB1h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	0	0	0	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0

VRHP: VREG1OUT voltage adjustment control.

VRHN: NVREG1OUT voltage adjustment control.

Table 11 VREG1OUT and NVREG1OUT output level mapping (GVDD=VREG1OUT, GVCL=NVREG1OUT)

VRHP[4:0]	GVDD	VRHN[4:0]	GVCL
00000	4.7	00000	-4.7
00001	4.65	00001	-4.65
00010	4.6	00010	-4.6
00011	4.55	00011	-4.55
00100	4.5	00100	-4.5
00101	4.45	00101	-4.45
00110	4.4	00110	-4.4
00111	4.35	00111	-4.35
01000	4.3	01000	-4.3
01001	4.25	01001	-4.25
01010	4.2	01010	-4.2
01011	4.15	01011	-4.15
01100	4.1	01100	-4.1
01101	4.05	01101	-4.05
01110	4	01110	-4
01111	3.95	01111	-3.95
10000	3.9	10000	-3.9
10001	3.85	10001	-3.85
10010	3.8	10010	-3.8
10011	3.75	10011	-3.75
10100	3.7	10100	-3.7
10101	3.65	10101	-3.65
10110	3.6	10110	-3.6
10111	3.55	10111	-3.55
11000	3.5	11000	-3.5
11001	3.45	11001	-3.45
11010	3.4	11010	-3.4
11011	3.35	11011	-3.35
11100	3.3	11100	-3.3
11101	3.25	11101	-3.25
11110	3.2	11110	-3.2
11111	3.15	11111	-3.15

9.19 Power Control 4 (RE8h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	cp_ctrl_en	0	0	0	gamma_en	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

gamma_en : gamma register(R50h~R59h) write enable signal. Must set 1 as enable this function.

CP_ctrl_en : Charge pump control(RB0) enable signal for VGHBT/VGLSEL setting. Must set 1 as enable this function.

10. Instruction List

No.	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	0	0	1	1	0	1	0	0	0	0	0	0	1	0	0	1	1
01h	Driver Output Control 1	W	1	VSP1	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	0	INV	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	0	0	0	BGR	0	0	MDT1	MDT0	0	0	I/D1	I/D0	AM	0	0	0
07h	Display Control 1	W	1	0	0	0	TEMON	0	0	0	0	0	0	0	0	CL	REV	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
0Bh	Frame Cycle Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	RTN3	RTN2	RTN1	RTN0
0Ch	RGB Display Interface Control 1	W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0
0Dh	Frame Maker Position	W	1	0	0	DIVE1	DIVE0	0	0	DIVI1	DIVI0	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	Oscillator Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSC_en
10h	Power Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SLP
11h	Power Control 2	W	1	0	0	0	APON	0	0	0	0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM			RAM write data WD[17:0] / read data RD[17:0] is transferred via different data bus in different interface operation.															
28h	Software Reset	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
30h	Gate Scan Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0
31h	Vertical Scroll Control 1	W	1	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0	

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32h	Vertical Scroll Control 1	W	1	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0		
33h	Vertical Scroll Control 2	W	1	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0		
34h	Partial Screen Driving Position	W	1	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10		
35h	Partial Screen Driving Position	W	1	0	0	0	0	0	0	0	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10		
36h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0		
37h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0		
38h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0		
39h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
50h	Gamma Control 1	W	1	0	0	0	0	KP13	KP12	KP11	KP10	0	0	0	0	KP03	KP02	KP01	KP00	
51h	Gamma Control 2	W	1	0	0	0	0	KP33	KP32	KP31	KP30	0	0	0	0	KP23	KP22	KP21	KP20	
52h	Gamma Control 3	W	1	0	0	0	0	KP53	KP52	KP51	KP50	0	0	0	0	KP43	KP42	KP41	KP40	
53h	Gamma Control 4	W	1	0	0	0	0	RP13	RP12	RP11	RP10	0	0	0	0	RP03	RP02	RP01	RP00	
54h	Gamma Control 5	W	1	0	0	0	0	KN13	KN12	KN11	KN10	0	0	0	0	KN03	KN02	KN01	KN00	
55h	Gamma Control 6	W	1	0	0	0	0	KN33	KN32	KN31	KN30	0	0	0	0	KN23	KN22	KN21	KN20	
56h	Gamma Control 7	W	1	0	0	0	0	KN53	KN52	KN51	KN50	0	0	0	0	KN43	KN42	KN41	KN40	
57h	Gamma Control 8	W	1	0	0	0	0	RN13	RN12	RN11	RN10	0	0	0	0	RN03	RN02	RN01	RN00	
58h	Gamma Control 9	W	1	0	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	VRP04	VRP03	VRP02	VRP01	VRP00
59h	Gamma Control 9	W	1	0	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	VRN04	VRN03	VRN02	VRN01	VRN00
60h	OTP VCM Programming Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	NVM_D5	NVM_D4	NVM_D3	NVM_D2	NVM_D1	NVM_D0
61h	OTP VCM Programming Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ID_PG_M_EN	VCM_PGM_EN
62h	OTP VCM Status	W	1	0	0	0	PGM_CN_T1	PGM_CN_T0	0	0	0	0	0	VCM_D6	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0
63h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0	
65h	Read ID Code	W	1	0	0	ID_PGM_CNT1	ID_PGM_CNT0	0	0	0	0	0	0	0	0	0	ID3	ID2	ID1	ID0
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX	

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B0h	Power Control 3	W	1	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VGLS EL1	VGLS EL0	0	0	VGHB T1	VGHBTO
B1h	Power Control 4	W	1	0	0	0	VRHN4	VRHN3	VRHN2	VRHN1	VRHN0	0	0	0	VRHP4	VRHP3	VRHP2	VRHP1	VRHP0
E8h	Enable control	W	1	0	0	0	cp_ctrl_en	0	0	0	gamma _en	0	0	0	0	0	0	0	0

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11. Interface and Data Format

The RM68130 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The RM68130 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the RM68130 supports RGB interface and VSYNC interface, which enables data rewrite operation without flicker effect of the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the RM68130 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the RM68130's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The RM68130 operates in either one of the following four modes according to the state of the display.

The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes:

1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.

12. System Interface

The following are the kinds of system interfaces available with the RM68130. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

IM3	IM2	IM1	IM0/ID	Interfacing Mode with MPU	DB pins
0	0	0	0	M68-system 16-bit bus interface	DB17-10, DB8-1
0	0	0	1	M68-system 8-bit bus interface	DB17-10
0	0	1	0	i80-system 16-bit bus interface	DB17-10, DB8-1
0	0	1	1	i80-system 8-bit bus interface	DB17-10
0	1	0	ID	Serial Peripheral Interface(SPI)	CSX, SCL, SDI, SDO
0	1	1	0	3-wire 9-bit data serial interface	CSX, SCL, SDA
0	1	1	1	4-wire 8-bit data serial interface	CSX, SCL, SDA, RS(DCX)
1	0	0	0	M68-system 18-bit bus interface	DB17-0
1	0	0	1	M68-system 9-bit bus interface	DB17-9
1	0	1	0	i80-system 18-bit bus interface	DB17-0
1	0	1	1	i80-system 9-bit bus interface	DB17-9
1	1	*	*	Setting Invalid	

12.1 18-bit System Interface

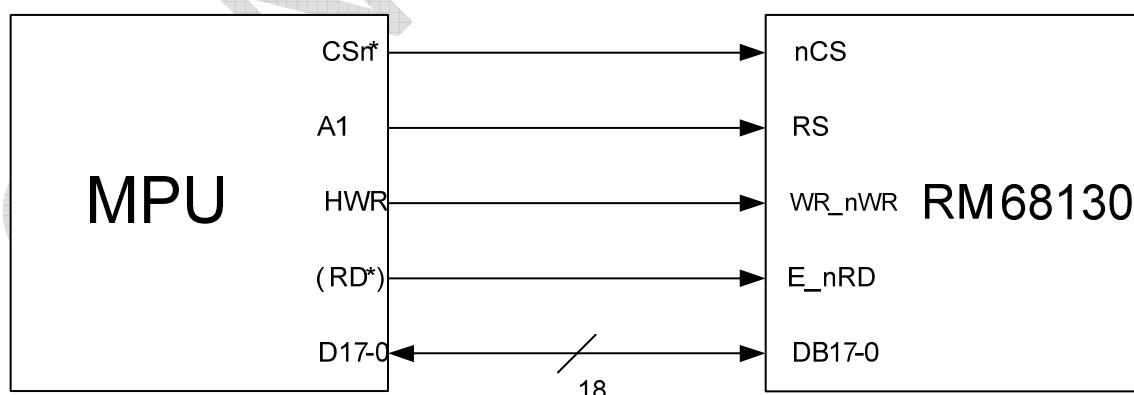
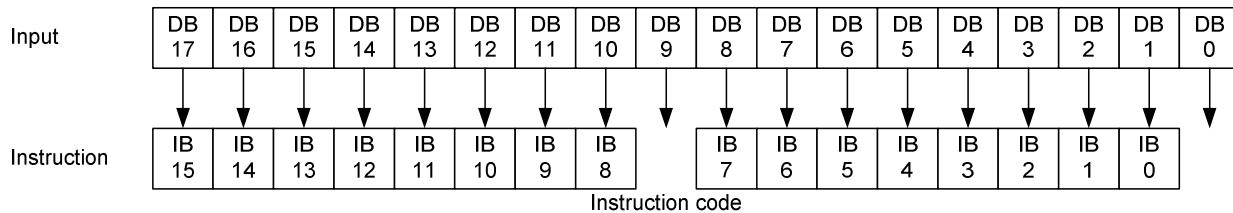


Figure 1 18-bit bus interface for M68/i80-system

Instruction write



Instruction read

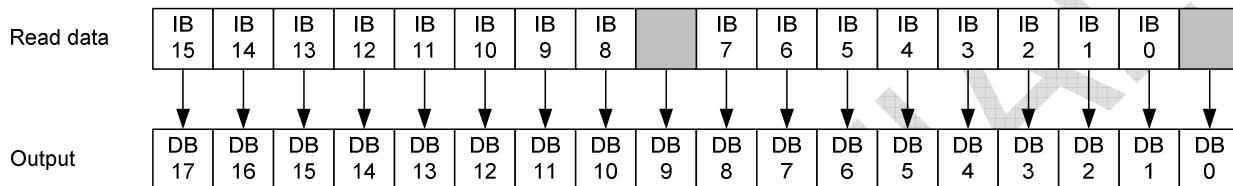
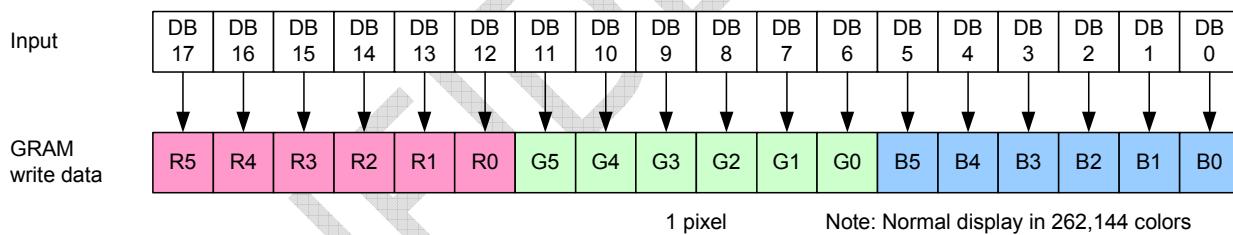


Figure 2 18-bit Interface Data Format (Instruction Write / Instruction Read)

RAM data write



RAM data read

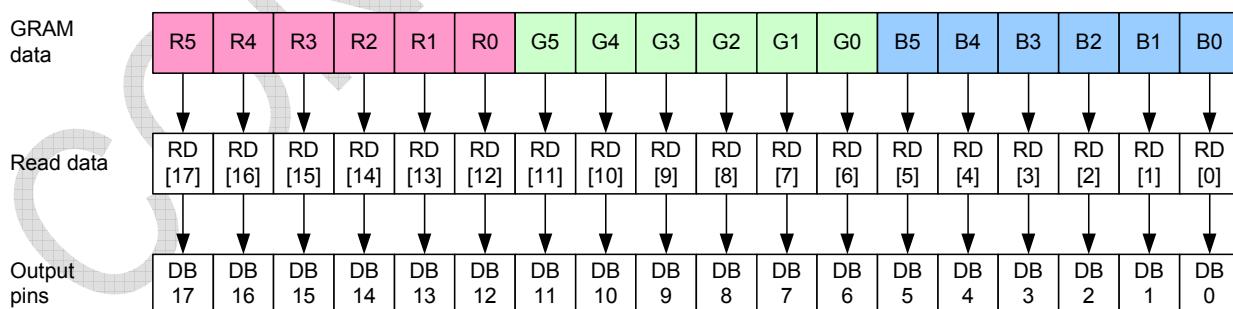


Figure 3 18-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.2 16-bit System Interface

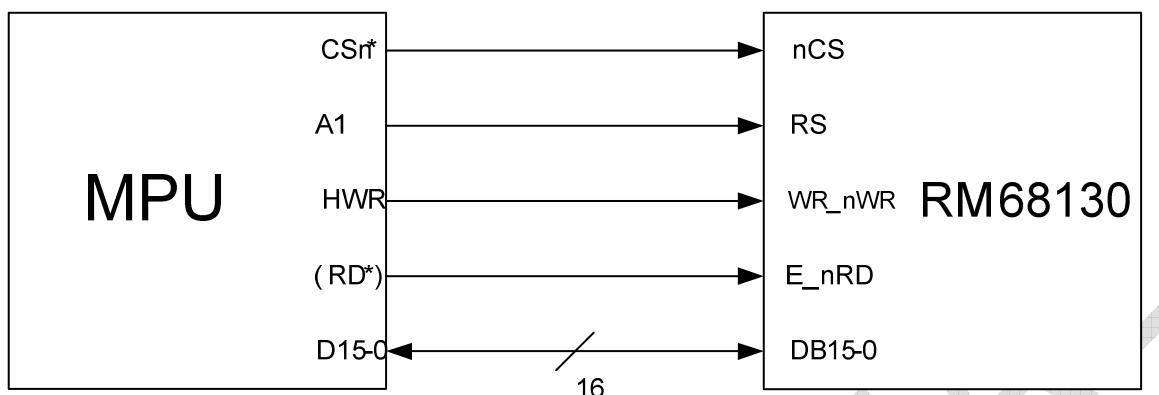
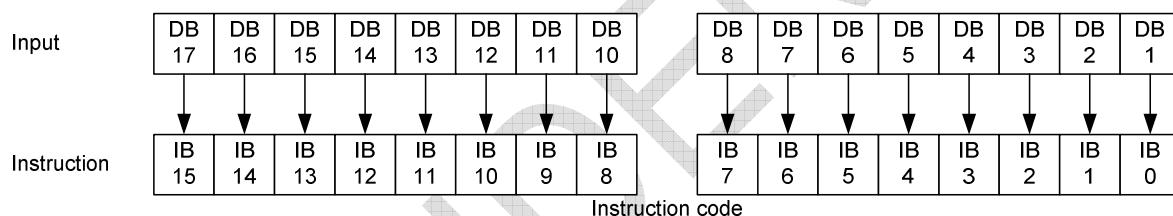
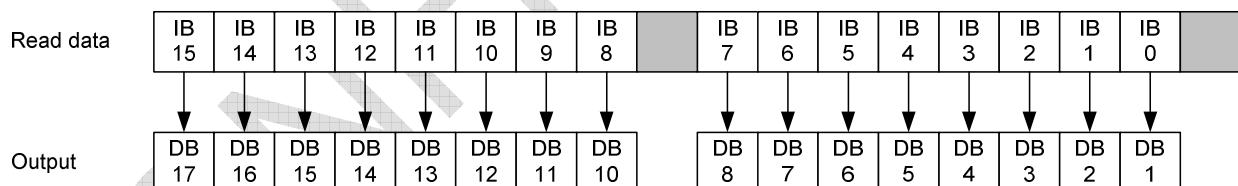


Figure 4 16-bit bus interface for M68/i80-system

Instruction write



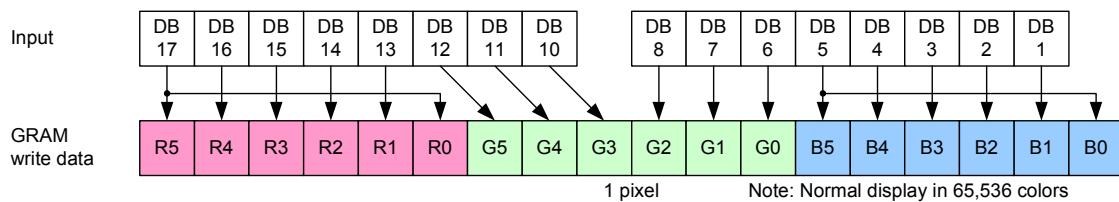
Instruction read



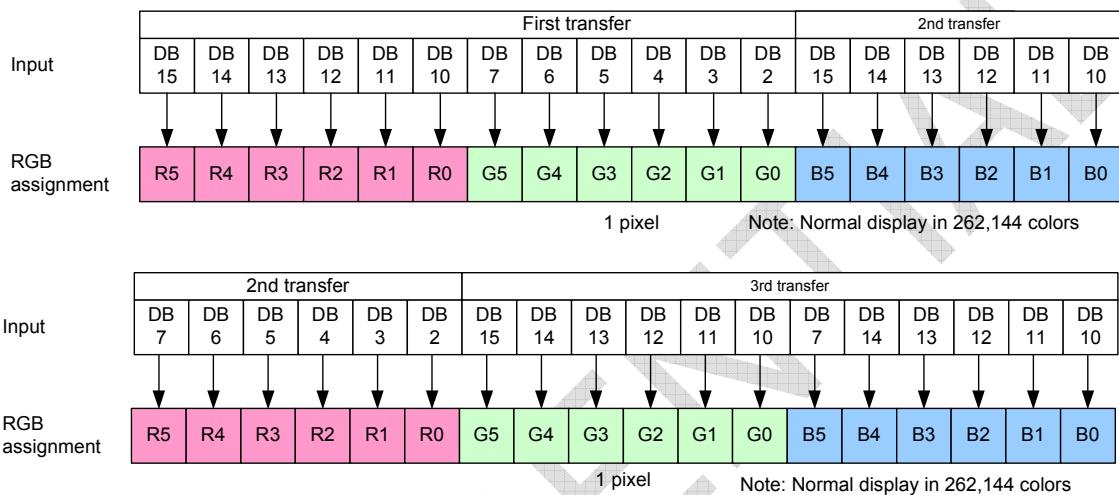
Note: Data cannot be transferred in twice in read operation via 16-bit interface

Figure 5 16-bit Interface Data Format (Instruction Write / Instruction Read)

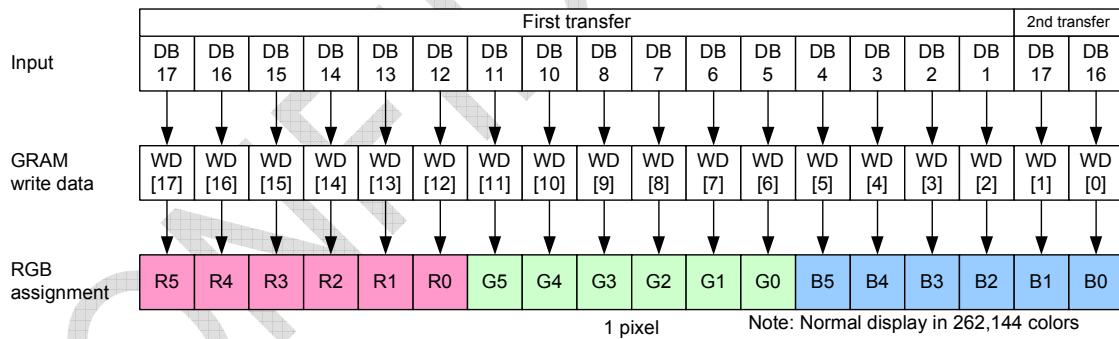
RAM data write (single transfer mode: MDT[1:0] = 2'h0)



RAM data write (2 transfer mode: MDT[1:0]=2'h01)



RAM data write (2 transfer mode: MDT[1:0]=2'h10, MSB mode)



RAM data write (2 transfer mode: MDT[1:0]=2'h11, LSB mode)

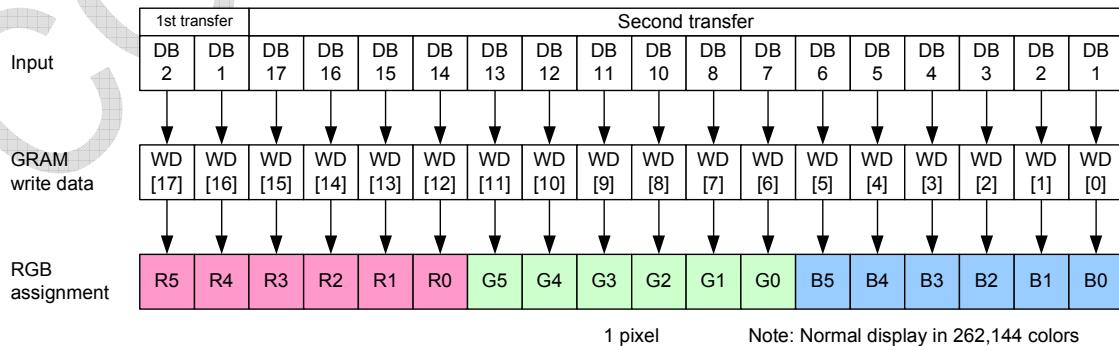


Figure 6 16-bit Interface Data Format (RAM data write)

12.3 9-bit System Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

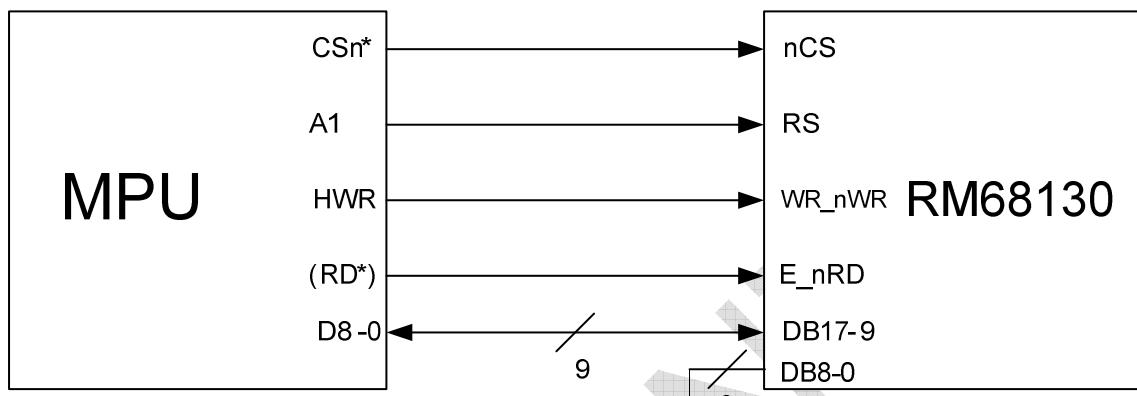
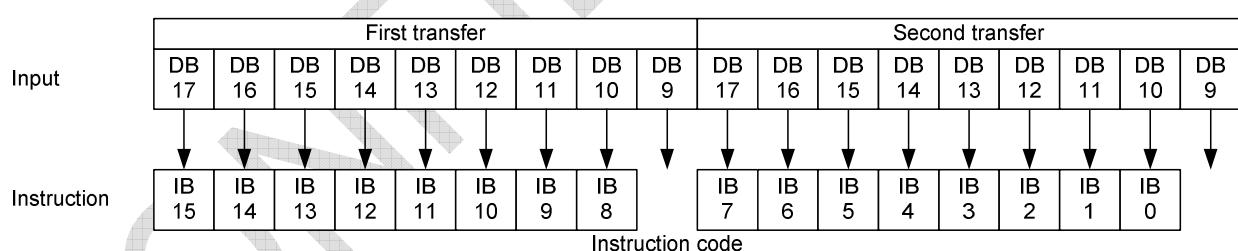


Figure 9 9-bit bus interface for M68/i80-system

Instruction write



Device code read

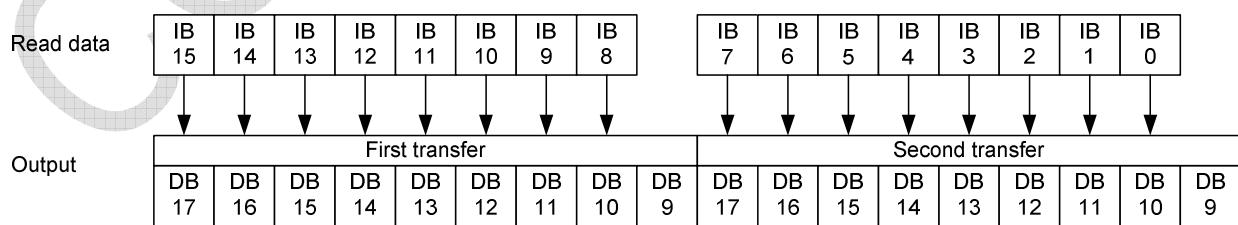
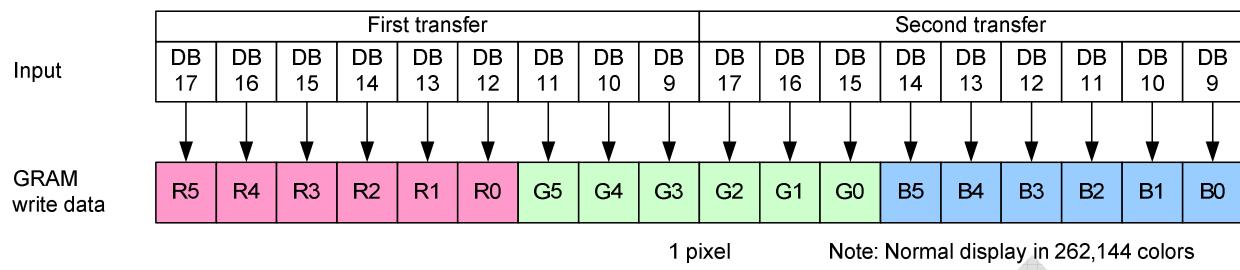


Figure 7 9-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write



RAM data read

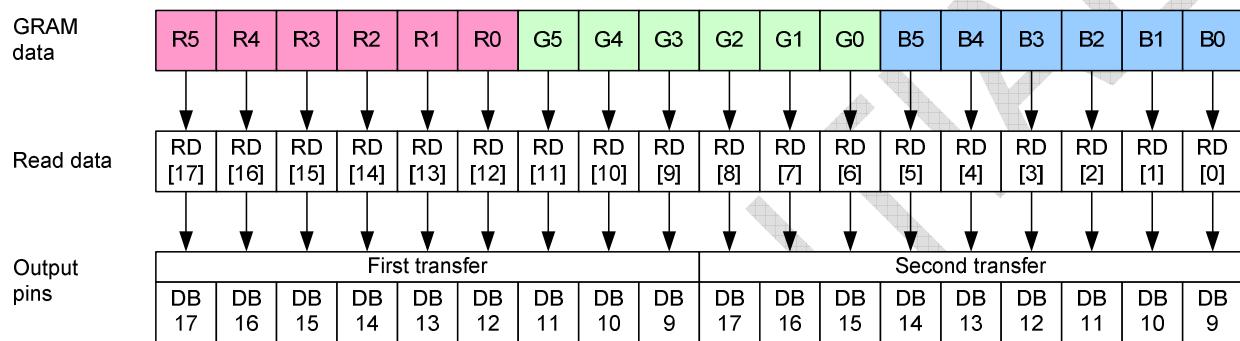


Figure 11 9-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.4 8-bit System Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at GND level. When transferring the index register setting, make sure to write upper byte (8 bits).

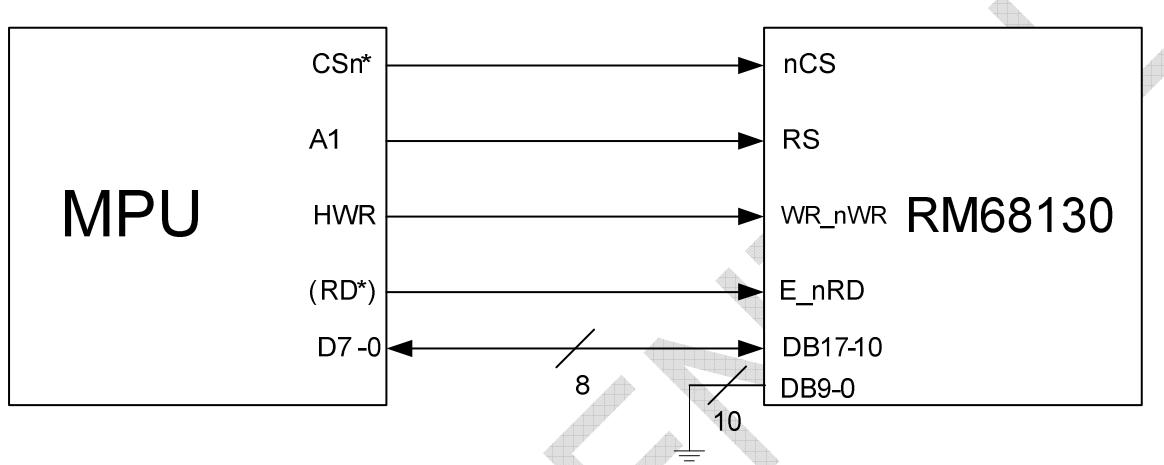
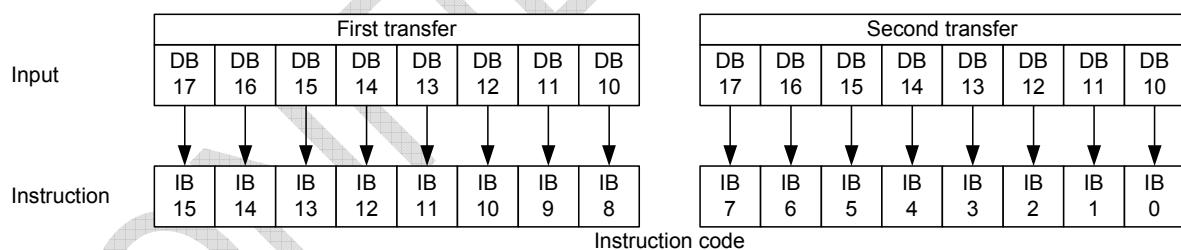


Figure 8 8-bit bus interface for M68/i80-system

Instruction write



Device code read

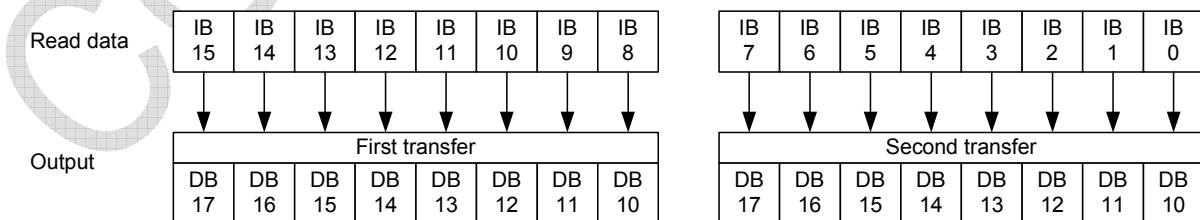
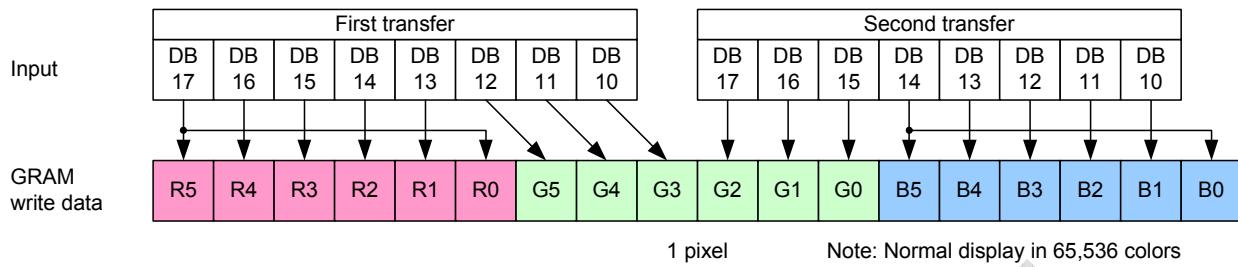
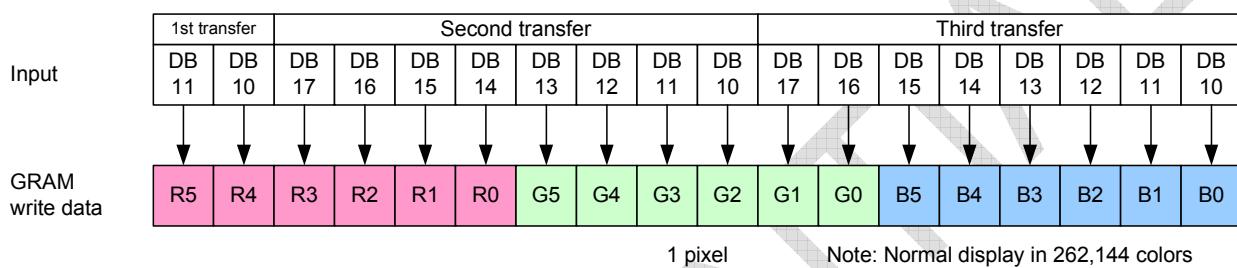


Figure 9 8-bit Interface Data Format (Instruction Write / Device Code Read)

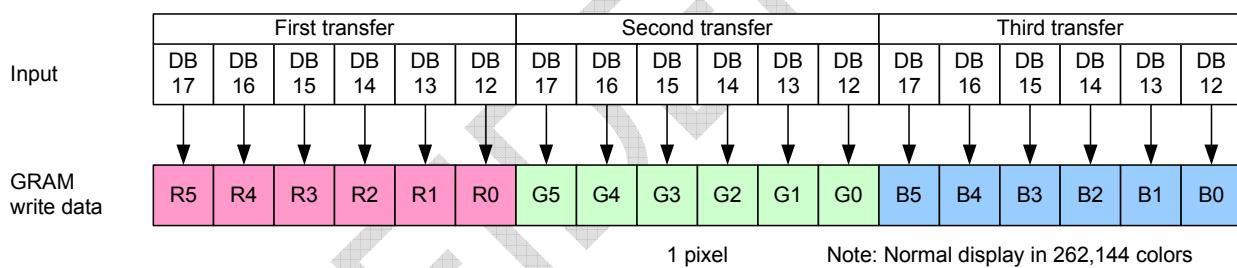
RAM data write (2-transfer mode: MDT[1:0] = 2'h0)



RAM data write (3-transfer mode: MDT[1:0]=2'h01)



RAM data write (3-transfer mode: MDT[1:0] = 2'h10)



RAM data write (3-transfer mode: MDT[1:0] = 2'h11)

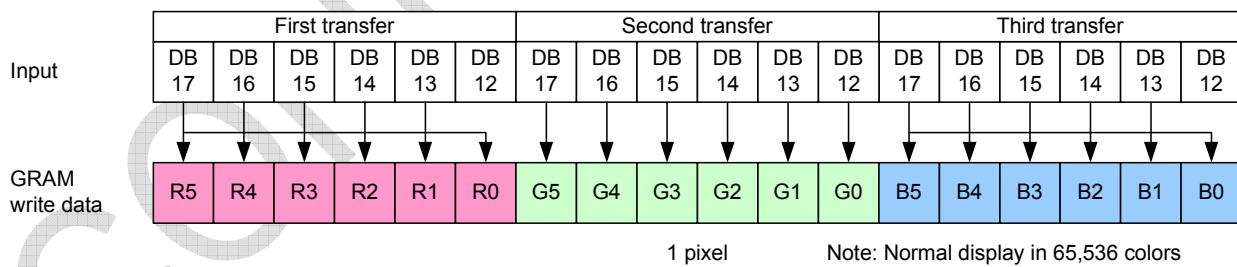


Figure 14 8-bit Interface Data Format (RAM Data Write)

12.5 Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the GND/VDDI/GND levels, respectively. The data is transferred via chip select line (CSX), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID

pin, and the DB17-0 pins, not used in this mode, must be fixed at GND level.

The SPI interface operation enables from the falling edge of CSX and ends of data transfer on the rising edge of CSX. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by RM68130.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, RM68130 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the RM68130 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Table 12 Start Byte Format

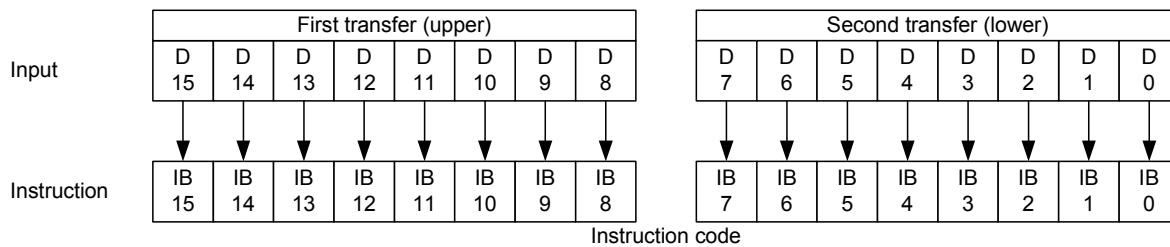
Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start			Device ID code			RS	R/W	

Note: The ID bit is determined by setting the IM0/ID pin.

Table 13 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Read a status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

Instruction



RAM data write

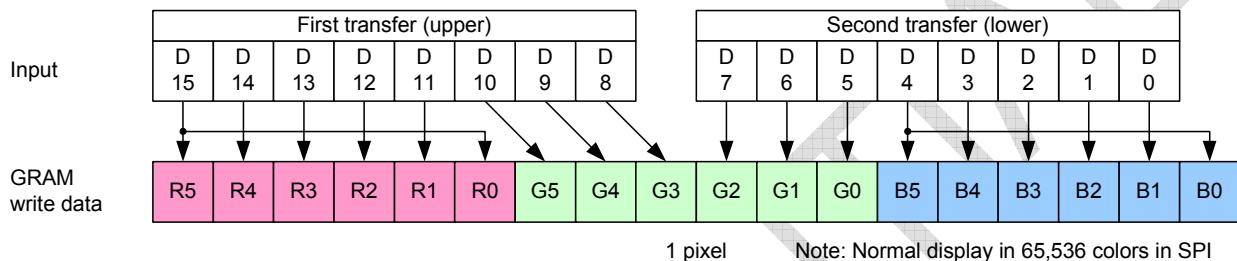
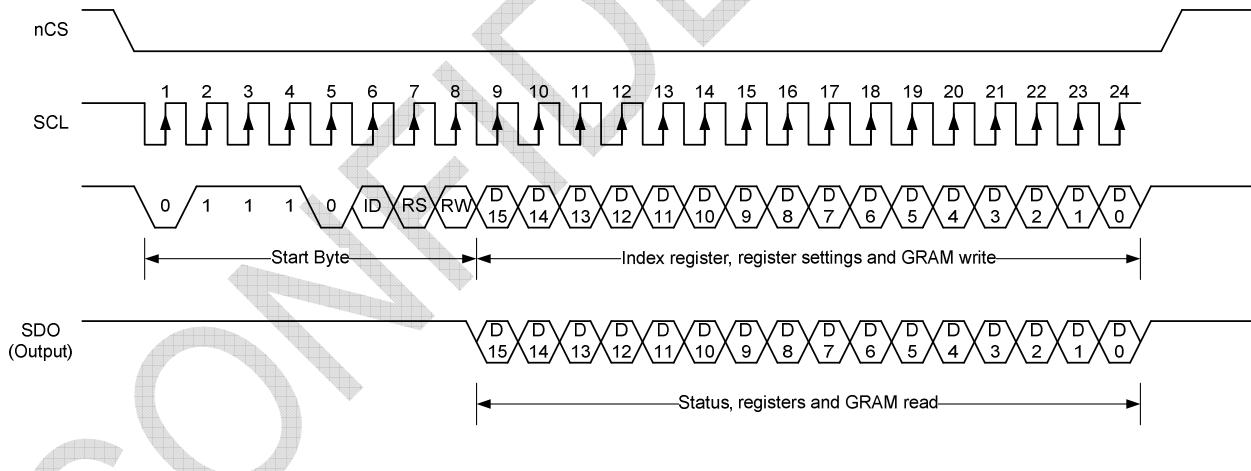
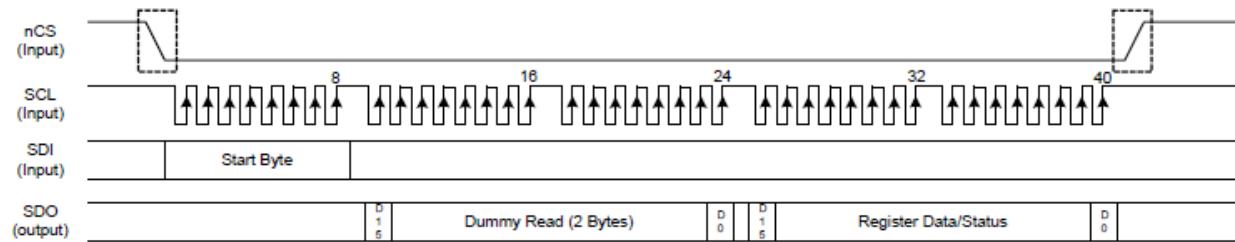


Figure 10 Serial Interface Data Format

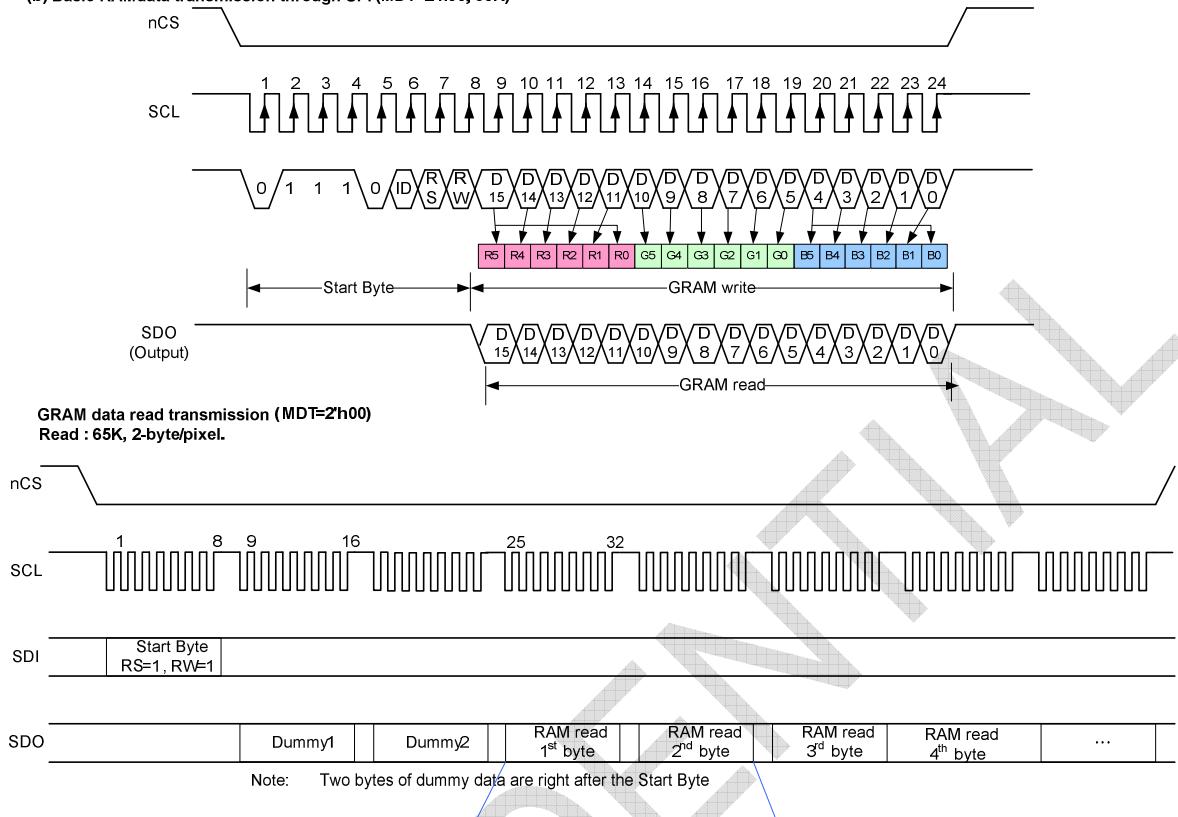
(a) Basic data transmission through SPI



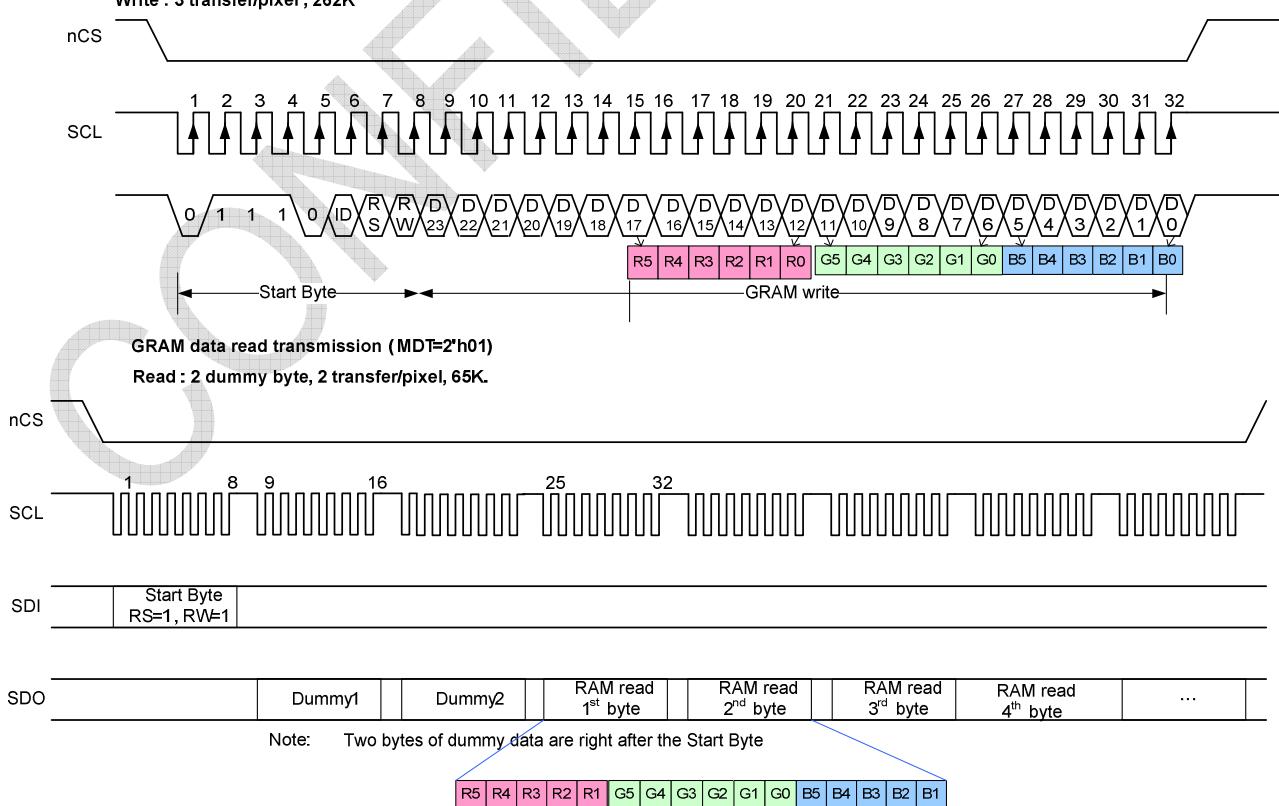
Status/registers read transmission



(b) Basic RAMdata transmission through SPI (MDT=2'h00, 65K)

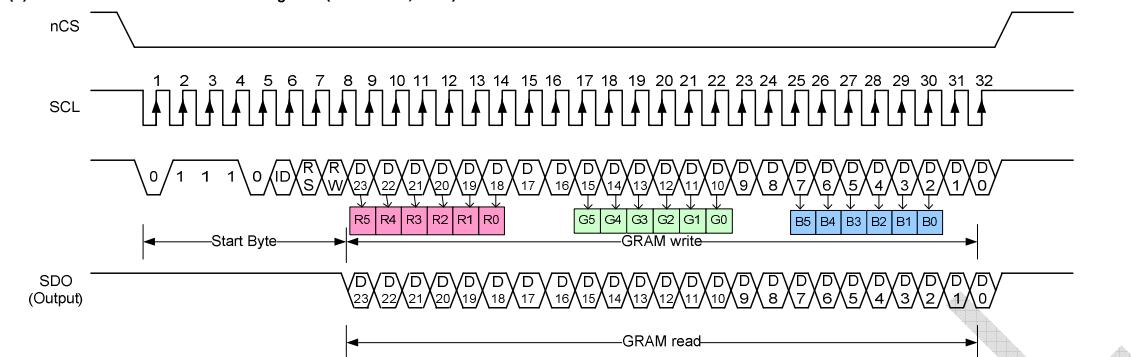


(c) Basic RAMdata transmission through SPI (MDT=2'h01)
Write : 3 transfer/pixel , 262K



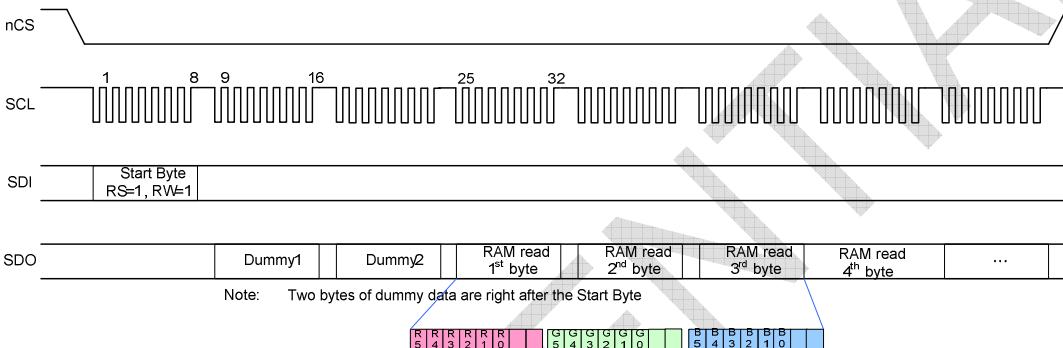
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(d) Basic RAM data transmission through SPI (MDT=2'h10, 262K)

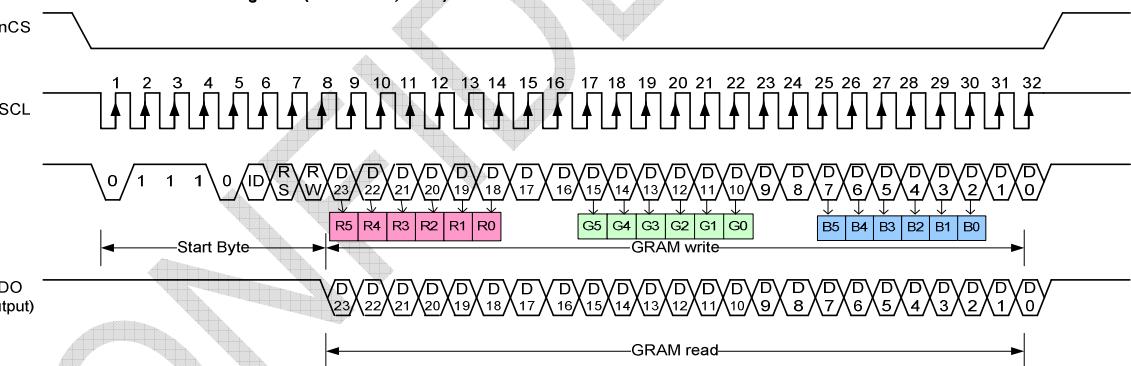


GRAM data read transmission (MDT=2'h10)

Read : 262K, 3-byte/pixel.



(d) Basic RAM data transmission through SPI (MDT=2'h11, 262K)



GRAM data read transmission (MDT=2'h11)

Read : 262K, 3-byte/pixel.

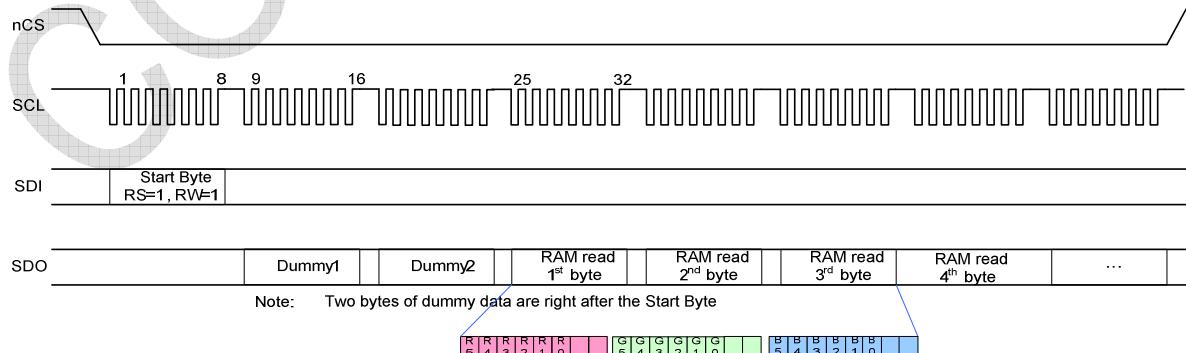


Figure 11 Data Transfer in Serial Interface

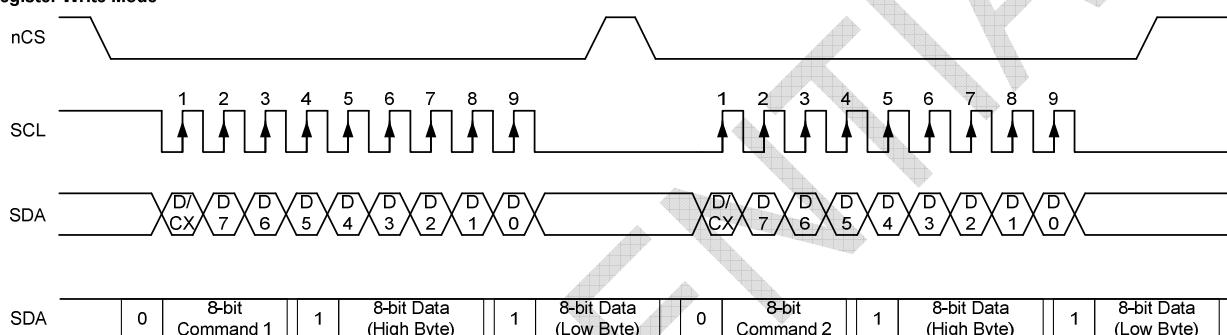
12.6 3-wire 9-bit data Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock and SDA is serial data.

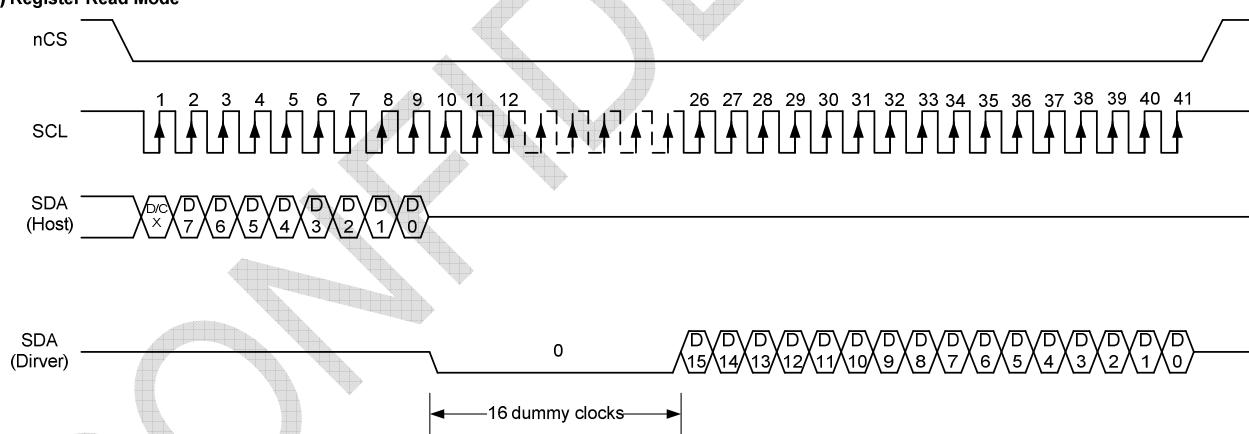
Serial data must be input to SDA in the sequence DCX, D7 to D0. The RM68130 catches the data at the rising edge of SCL signal. The first bit of serial data DCX is data/command flag. DCX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. DCX = "0" indicates that D7 to D0 bits are commands.

When users need to read back the register or GRAM data, the register R66h must be set to "1" first, and then write the register index to read back the register or GRAM data.

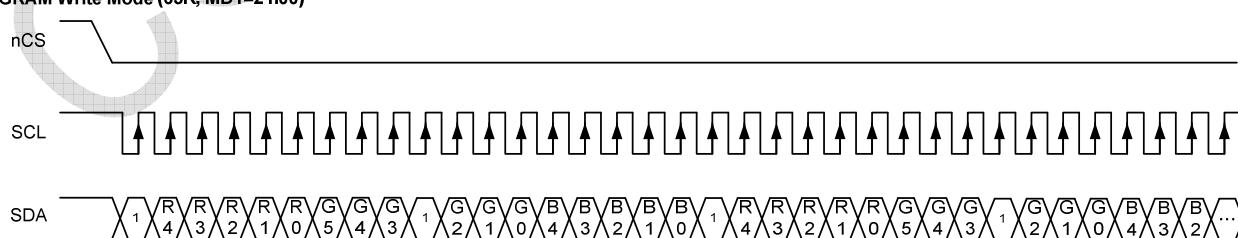
(a) Register Write Mode



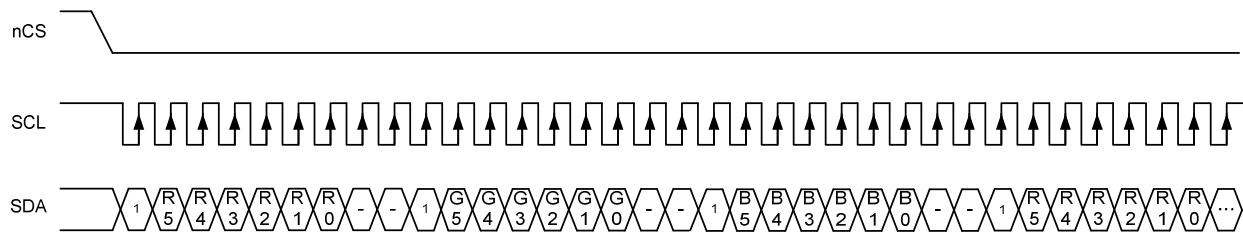
(b) Register Read Mode



(c) GRAM Write Mode (65K, MDT=2'h00)



(d) GRAM Write Mode (262K, MDT=2'h11)



(e) GRAM Read Mode (65K, MDT=2'h00)

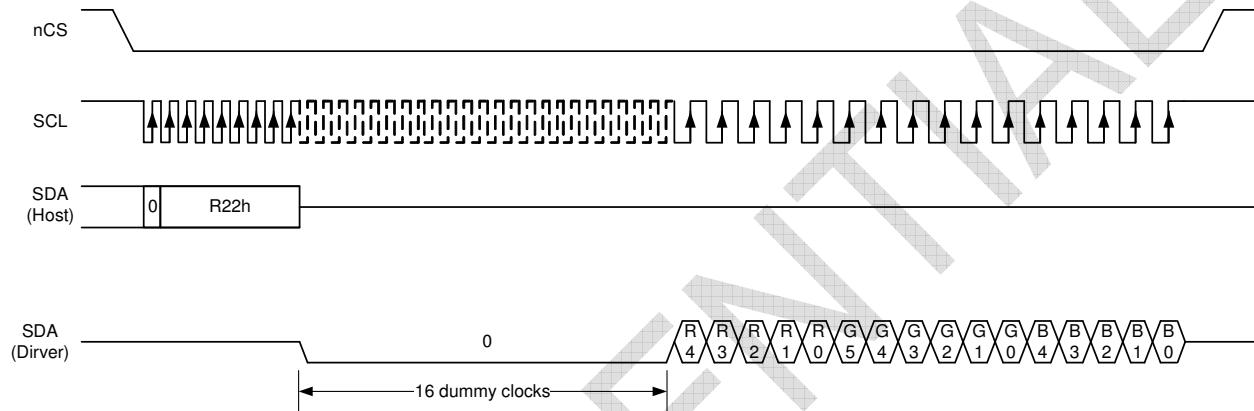


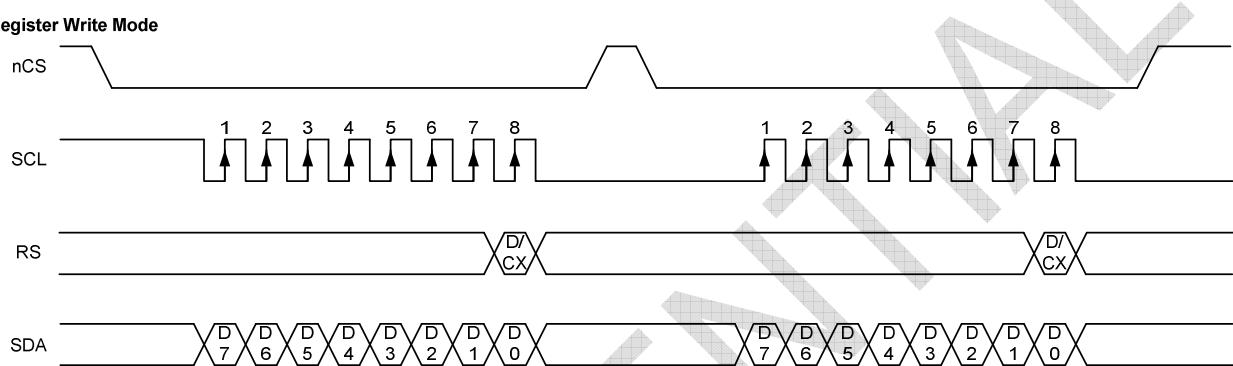
Figure 127 Data Transfer in 3-wire Serial Interface

12.7 4-wire 8-bit data Serial Interface

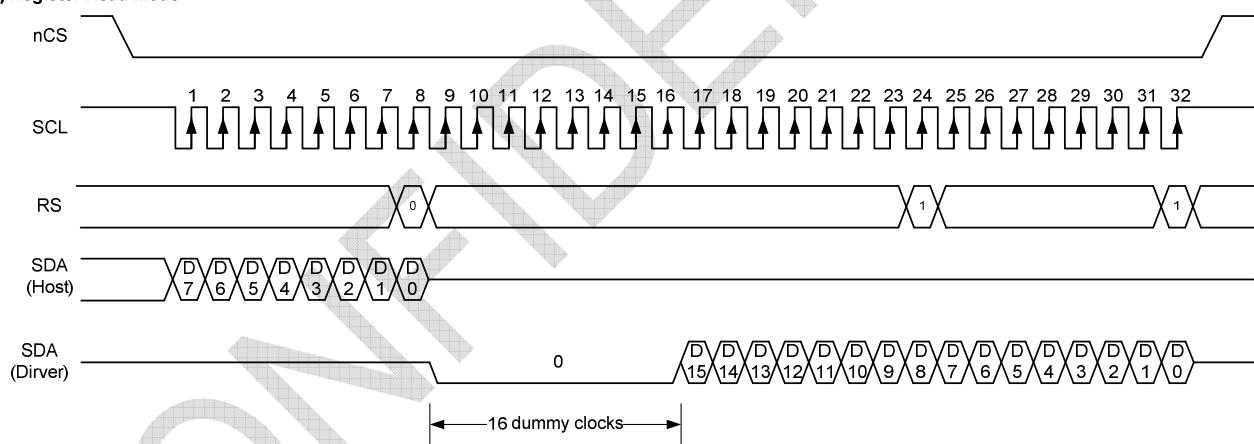
This SPI mode uses a 4-wire 8-bit serial interface. The chip-select CSX (active low) enables and disables the serial interface. DCX (input through RS pin) is the command or data select signal, SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D7 to D0. The RM68130 catches the data at the rising edge of SCL signal. The DCX signal indicates data/command. DCX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. DCX = "0" indicates that D7 to D0 bits are commands.

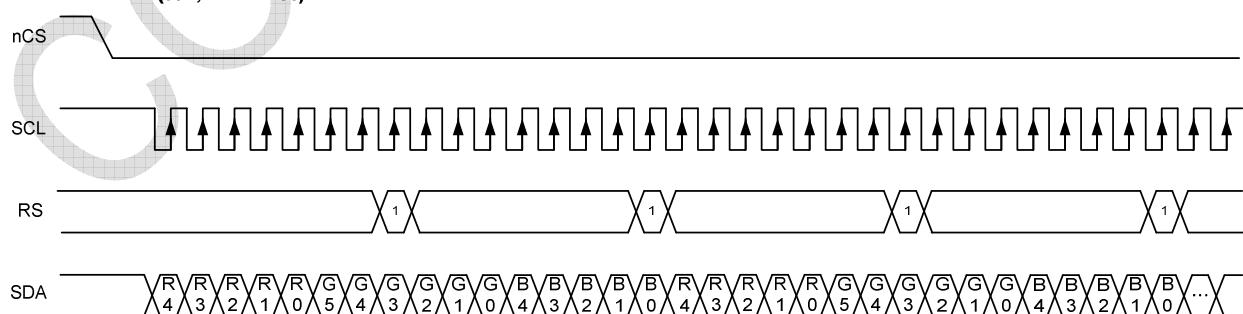
(a) Register Write Mode



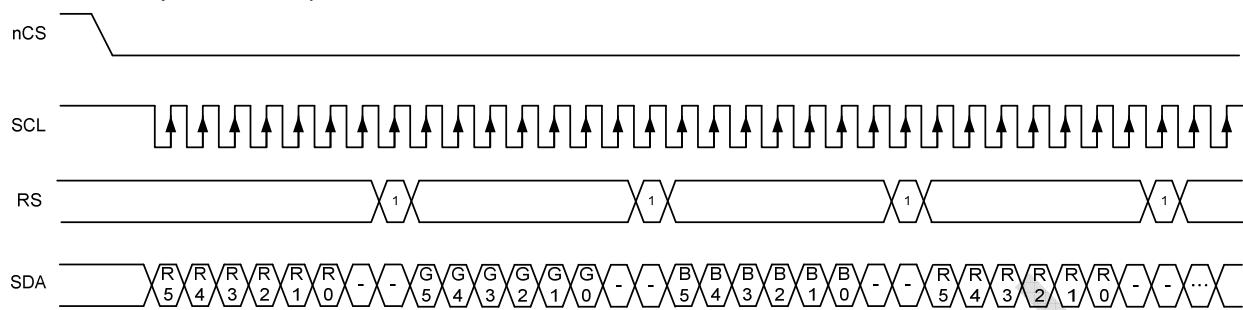
(b) Register Read Mode



(c) GRAM Write Mode (65K, MDT=2'h00)



(d) GRAM Write Mode (262K, MDT=2'h11)



(e) GRAM Read Mode (65K, MDT=2'h00)

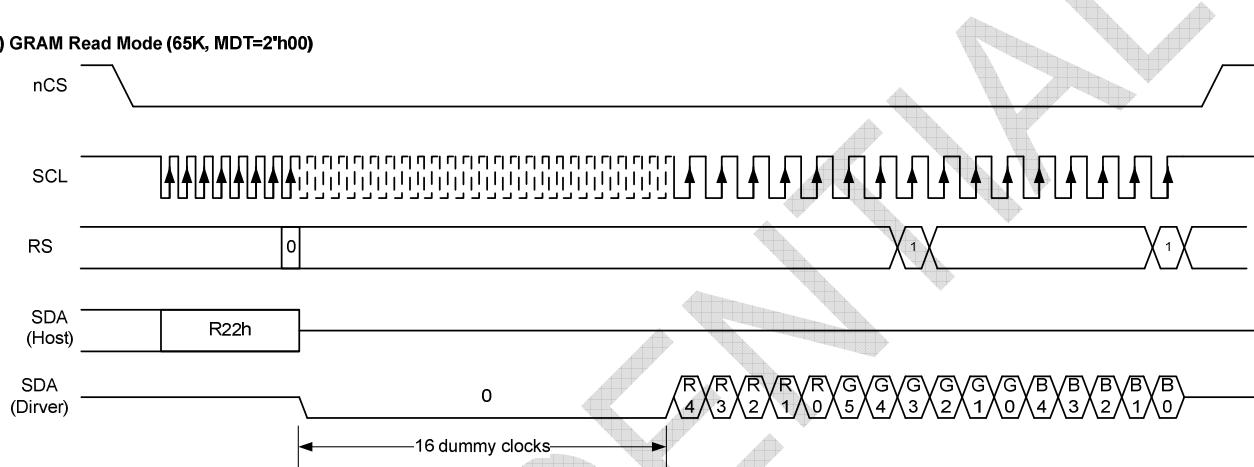


Figure 1813 Data Transfer in 4-wire Serial Interface

13. VSYNC Interface

RM68130 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

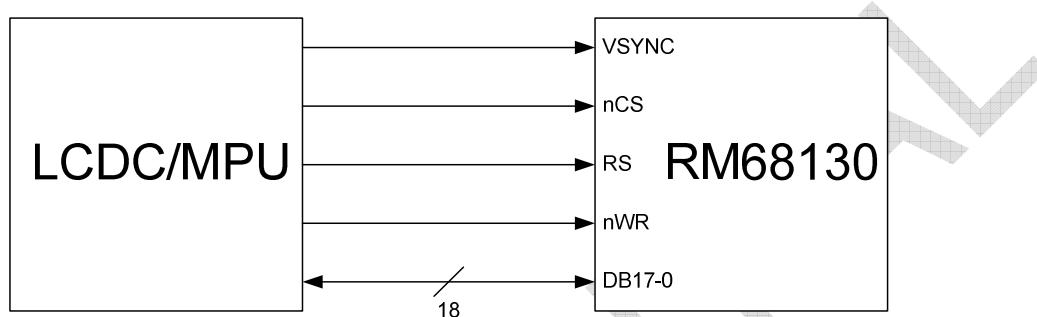


Figure 19 VSYNC Interface connection

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

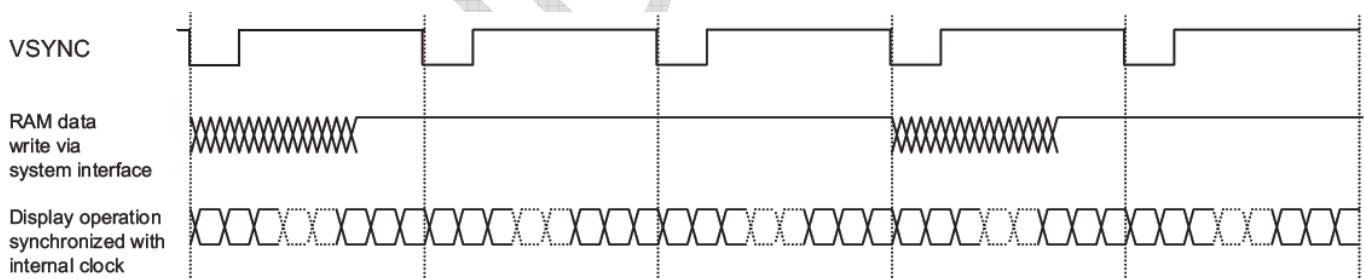


Figure 14 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

Internal clock frequency (fosc) [Hz]

$$= \text{FrameRate} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times \text{ClocksPerLine(RTN)} \times \text{variance}$$

$$\text{RAM Write Speed(min.)[Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{(\text{FrontPorch(FP)} + \text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16(\text{clocks}) \times \frac{1}{\text{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel Size 176 RGB x 220 lines (NL = 6'h1C: 220 lines)

Total number of lines (NL) 220 lines

Black/front porch 8/2 lines (BP = 8'h08, FP = 8'h02)

Frame frequency 60 Hz

Internal clock frequency (fosc) [Hz]

$$= 60 \text{ Hz} \times (220 + 2 + 8) \text{ lines} \times 16 \text{ clocks} \times 1.1 / 0.9 = 269.8 \text{ kHz}$$

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with $\pm 10\%$ margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz]

$$> 176 \times 220 / \{((8 + 220 - 2) \text{ lines} \times 16 \text{ clocks}) \times 1/269.8 \text{ kHz}\} = 3.87 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the RM68130 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 3.87MHz or more will guarantee the completion of GRAM write operation before the RM68130 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes:

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC

interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display and vertical scroll functions are not available in VSYNC interface mode and set the AM bit to "0" to transfer display data.

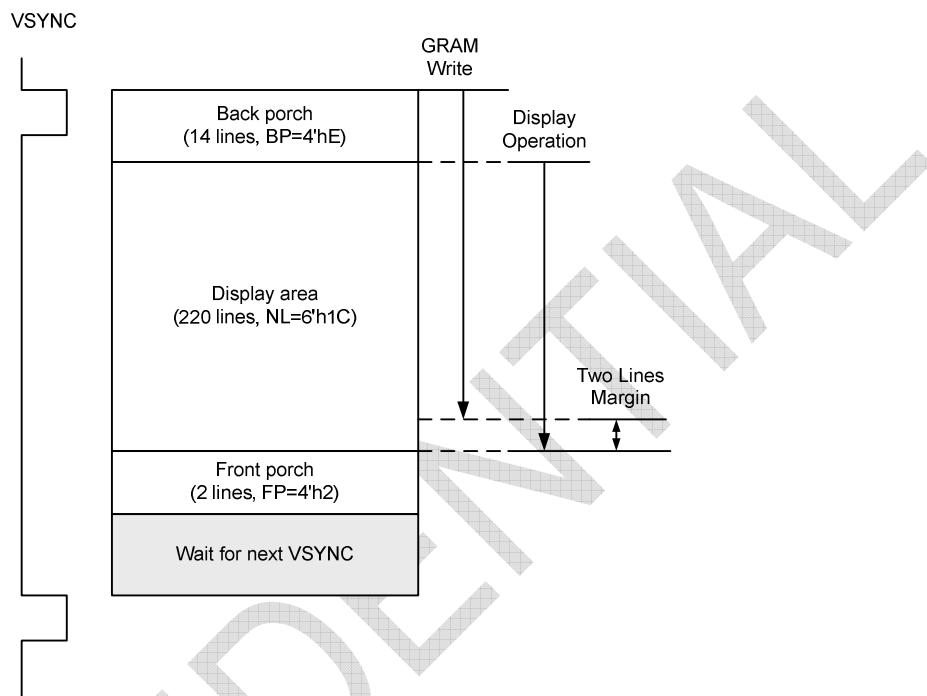
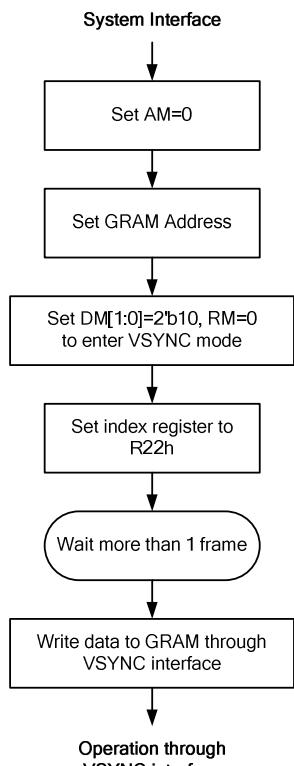


Figure 21 RAM Write Speed Margins

System Interface Mode à VSYNC Interface Mode

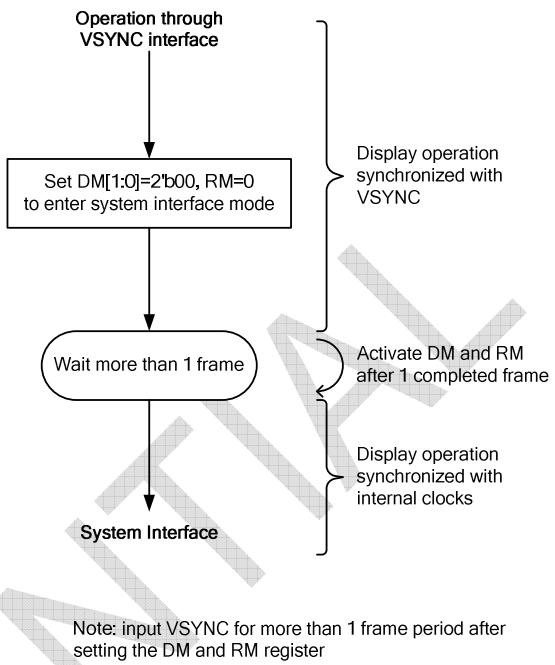


Display operation synchronized with internal clocks

Activate DM and RM after 1 completed frame

Display operation synchronized with VSYNC

VSYNC Interface Mode à System Interface Mode



Display operation synchronized with VSYNC

Activate DM and RM after 1 completed frame

Display operation synchronized with internal clocks

Note: input VSYNC for more than 1 frame period after
setting the DM and RM register

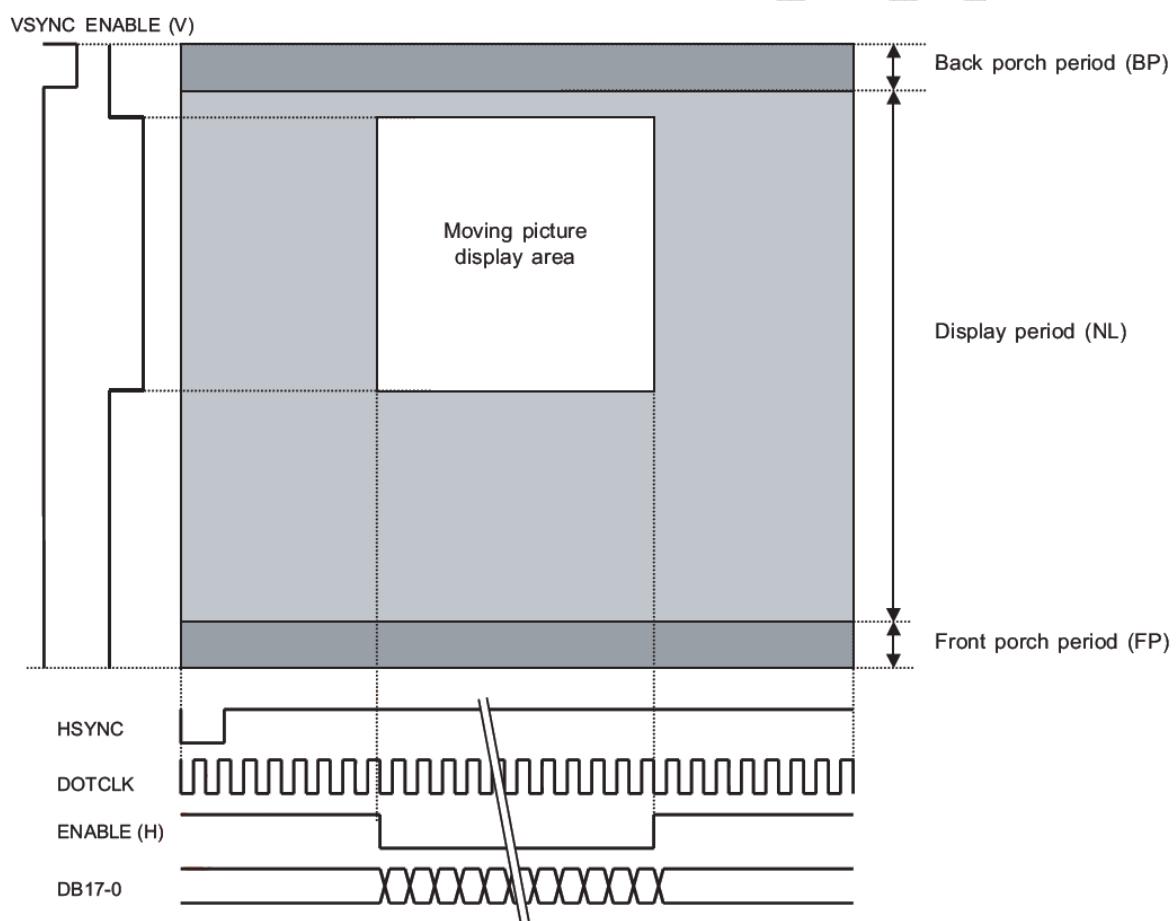
Figure 15 Sequences to Switch between VSYNC and Internal Clock Operation Modes

14. RGB Interface

The RM68130 supports the RGB interface. The interface format is set by RIM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 14 RGB interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting inhibited	-



- Notes:
1. The front porch period continues until next VSYNC input is detected.
 2. Make sure to match the VSYNC, HSYNC, and DOTCLK frequencies to the resolution of liquid crystal panel.

Figure 163 Display Operation via RGB Interface

14.1 RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

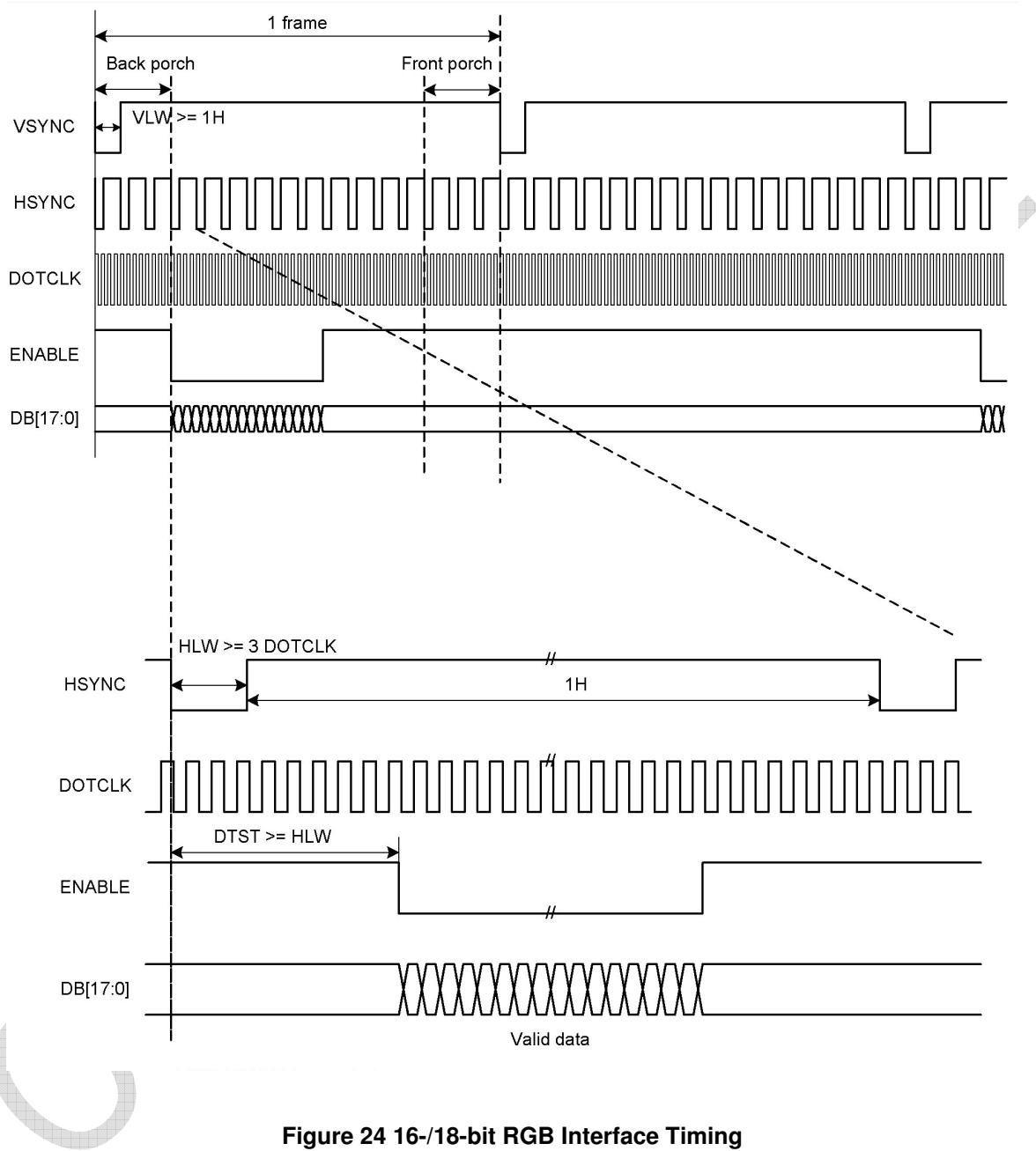


Figure 24 16-/18-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time

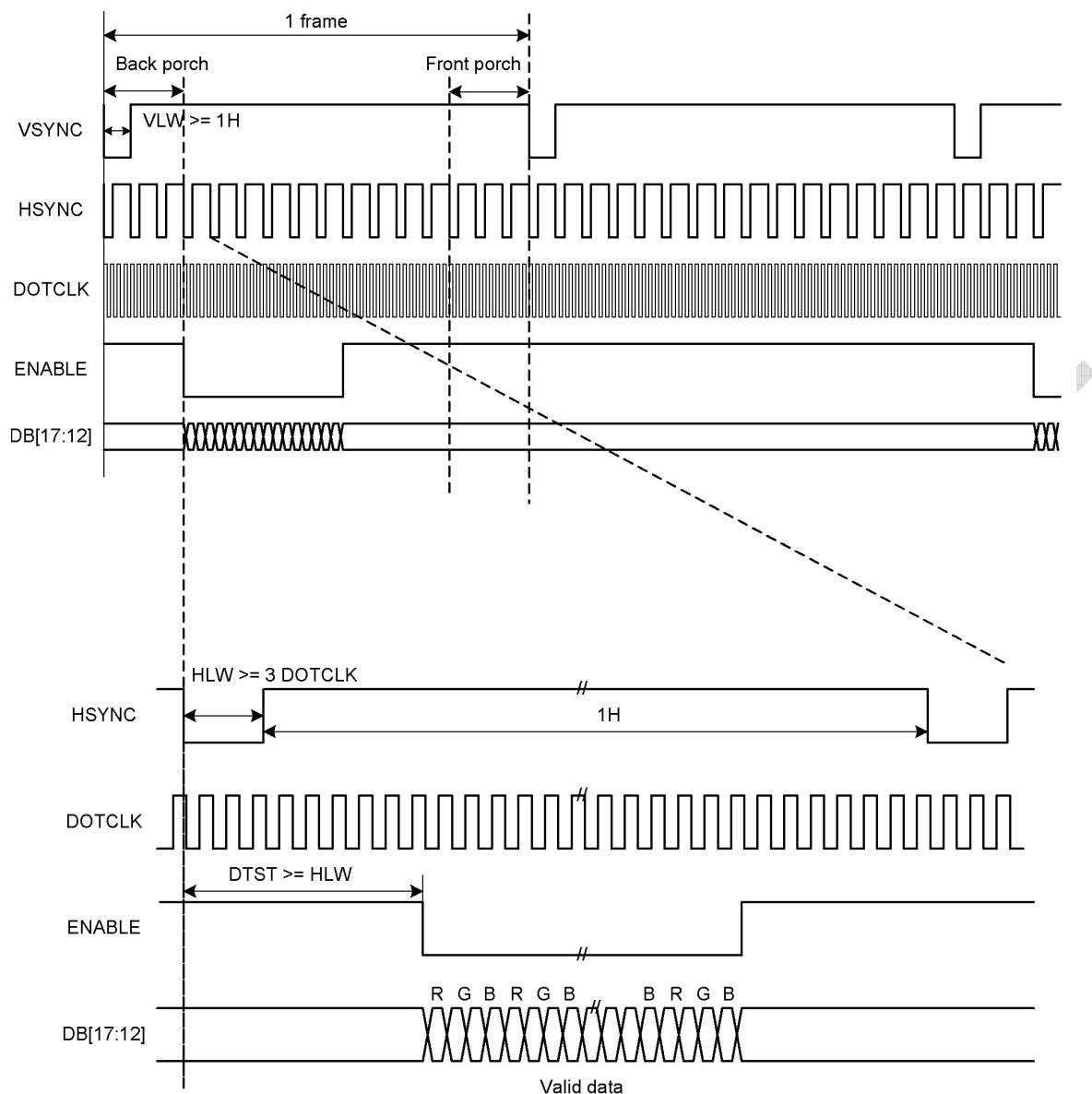


Figure 25 6-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time
4. In 6-bit RGB interface operation, set the VSYNC, HSYNC, ENABLE, DOTCLK cycles so that one pixel is transferred in units of three DOTCLKs via DB17-12.

14.2 Moving Pictures Mode

RM68130 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following advantages in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

14.3 RAM access via system interface in RGB interface operation

RM68130 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the RM68130 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

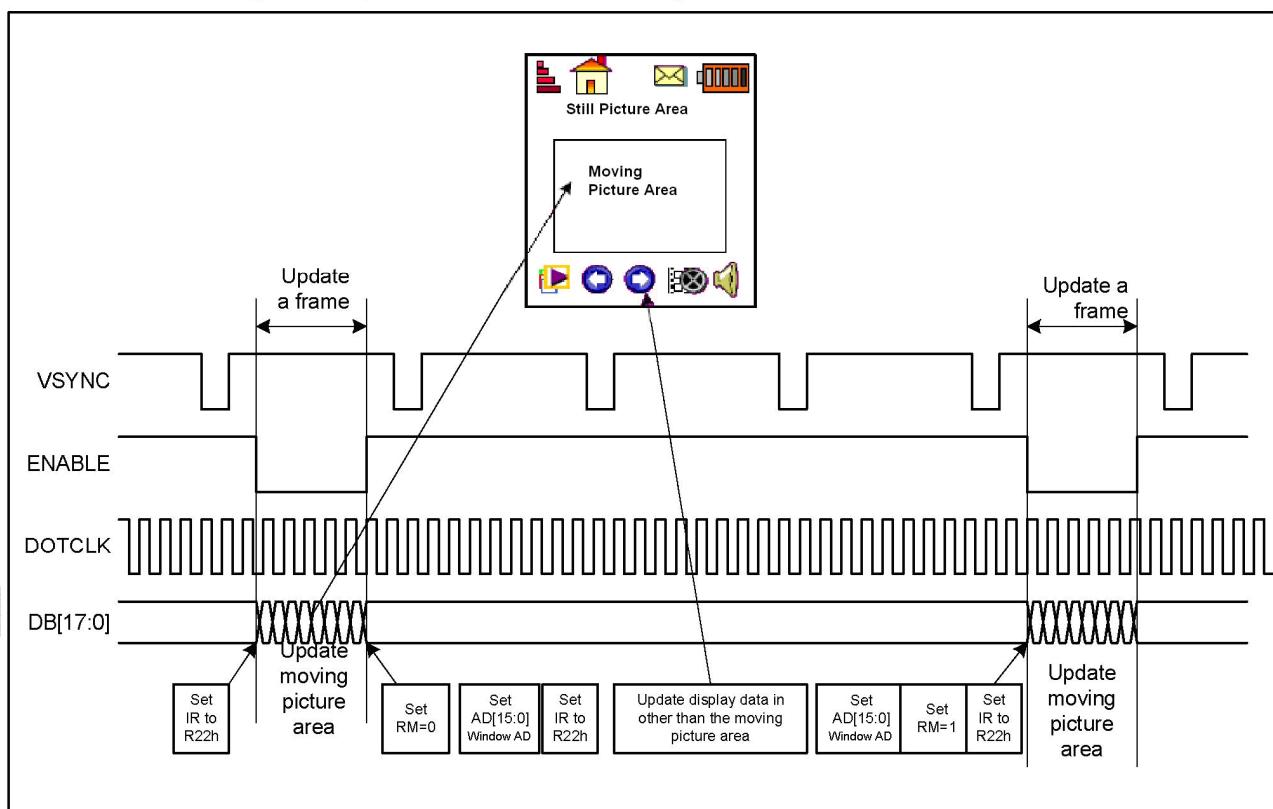


Figure 26 Updating the Still Picture Area while Displaying Moving Picture

14.4 6-bit RGB interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 2'b10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit port while data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins DB11-0 (DB17-6) must be fixed at either VDDI or GND level.

Instruction bits can be transferred only via system interface.

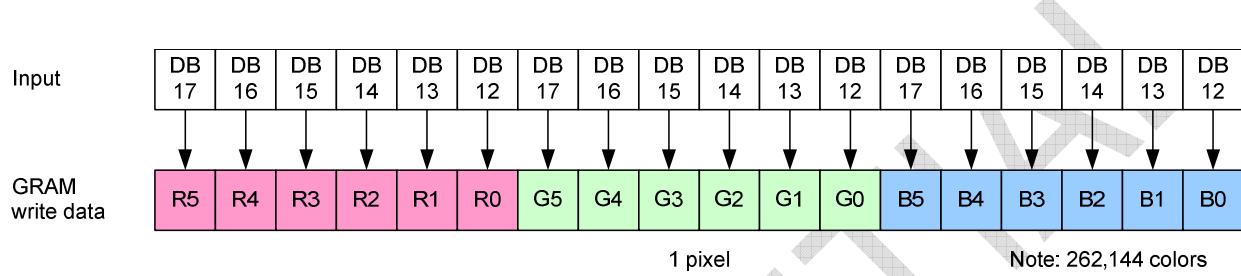


Figure 17 Example of 6-bit RGB Interface and Data Format

14.5 Data Transfer Synchronization in 6-bit Bus Interface Operation

The RM68130 has counters, which indicate the first, second, and third 6-bit transfer via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

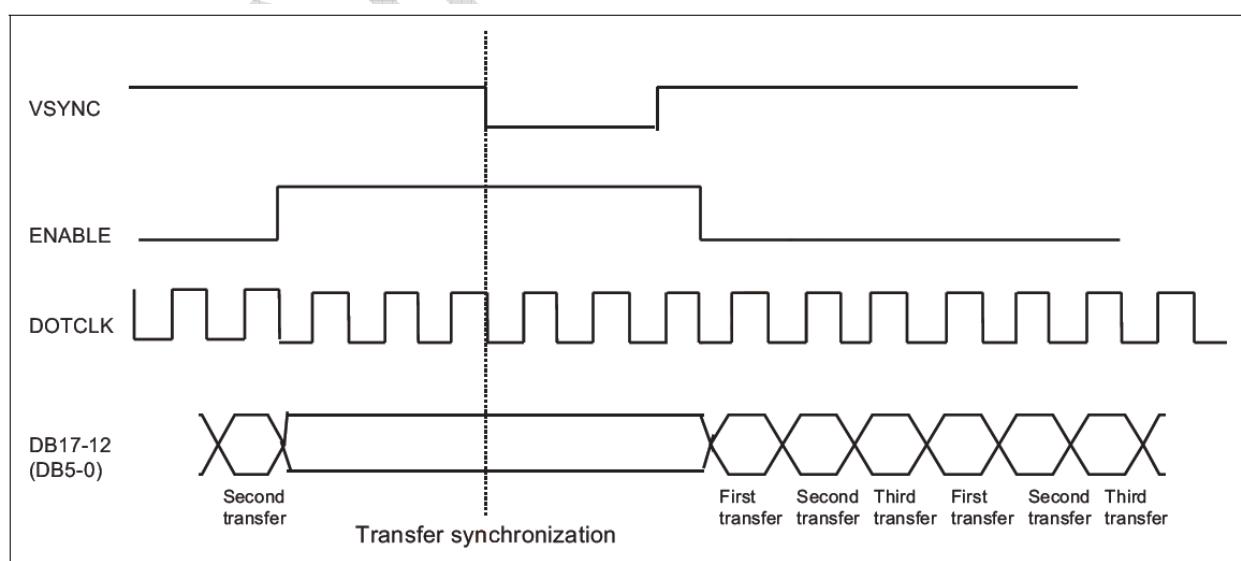


Figure 28 6-bit Transfer Synchronization

14.6 16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM[1:0] = 2'b01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

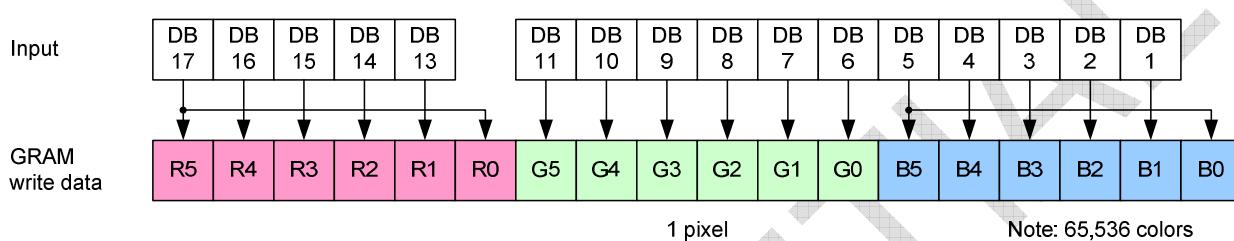


Figure 29 Example of 16-bit RGB Interface and Data Format

14.7 18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM[1:0] = 2'b00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

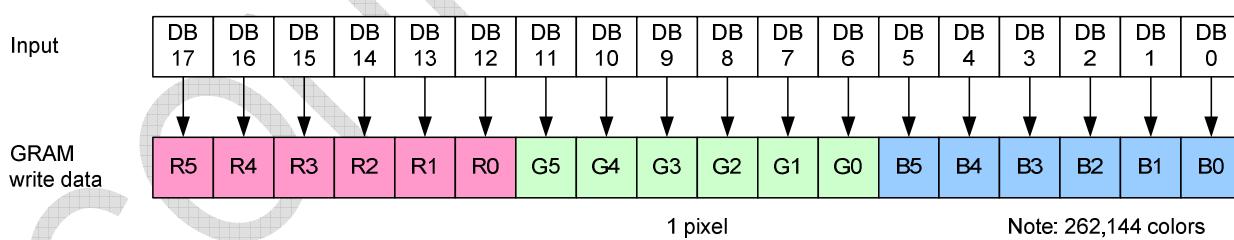


Figure 30 Example of 18-bit RGB Interface and Data Format

14.8 Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The period set with the NOWE[1:0] bits (gate output non-overlap period) is not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

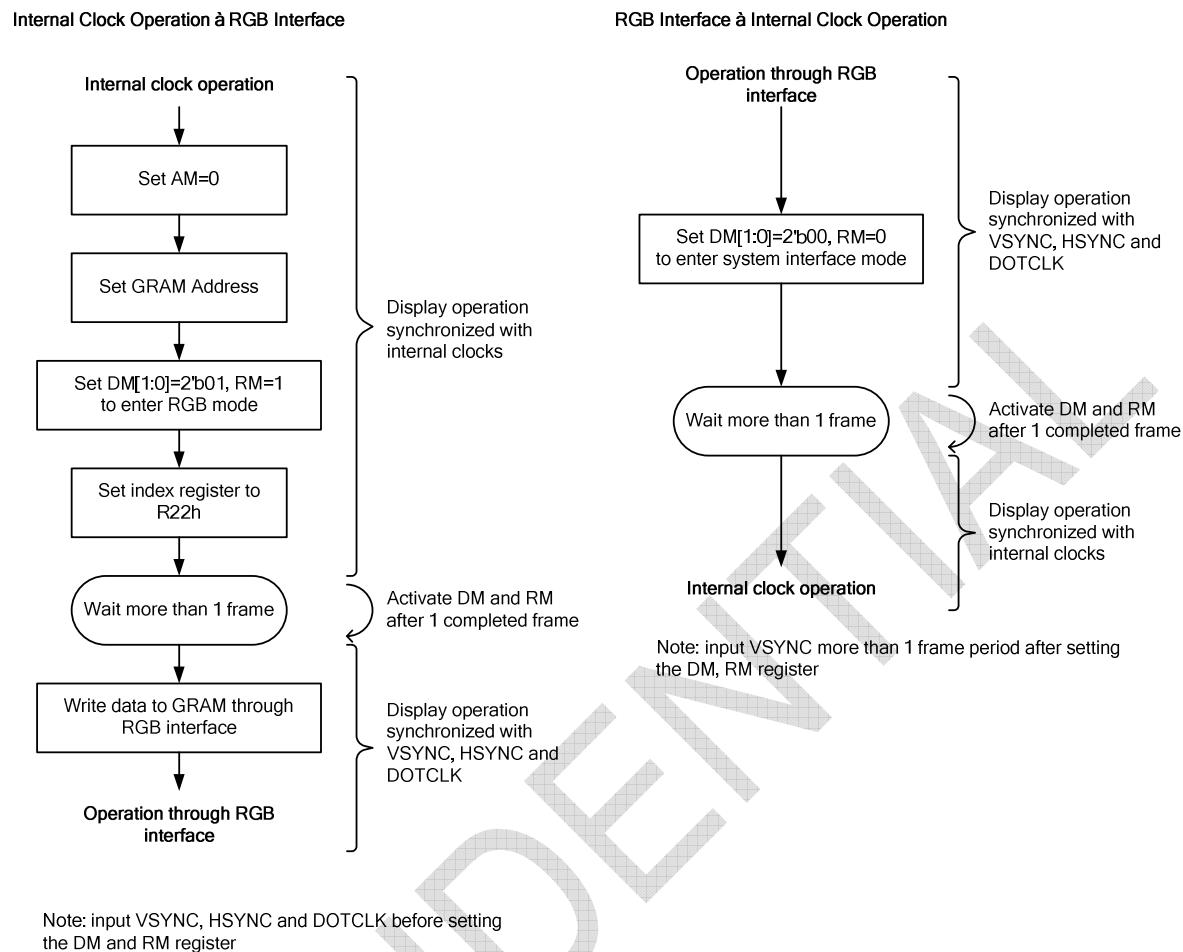


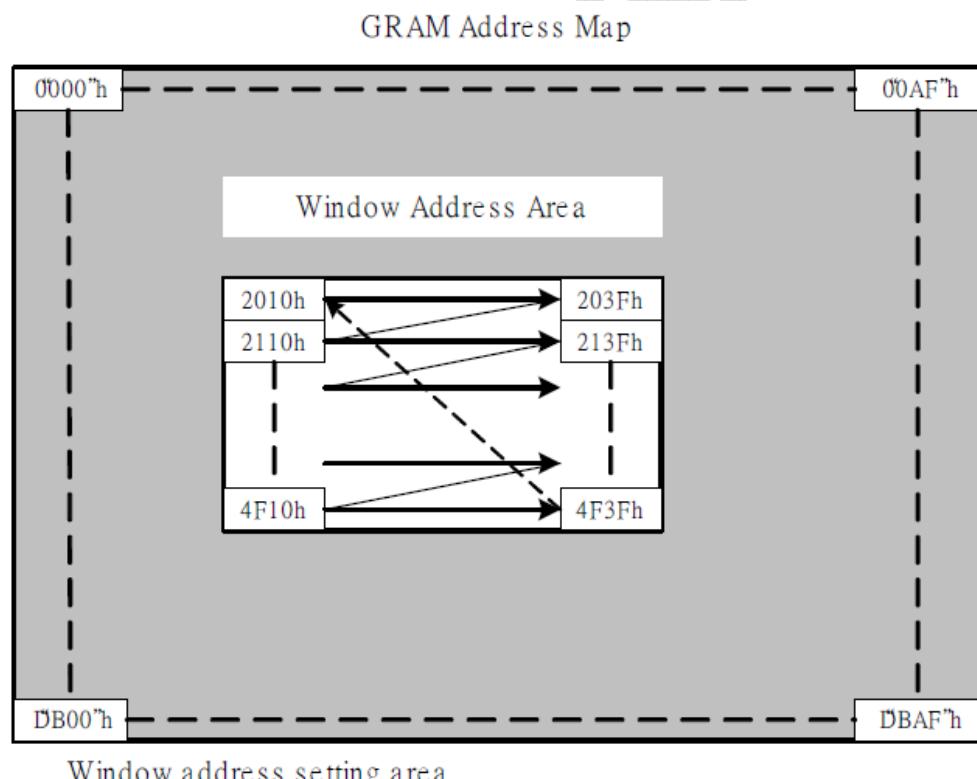
Figure 181 RGB and Internal Clock Operation Mode Switching Sequences

15. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA7-0, end: VEA7-0 bits). The AM and I/D bits set the transition direction of RAM address (increment or decrement, horizontal or vertical, respectively). Setting these bits enables the RM68130 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD15-0 bits (RAM address set register) must be set to an address within the window address area.

	Window address area setting range	RAM address area setting range
Horizontal direction	$8'h00 \leq HSA \leq HEA \leq 8'hAF$	$HSA \leq AD[7:0] \leq HEA$
Vertical direction	$8'h00 \leq VSA \leq VEA \leq 8'hDB$	$VSA \leq AD[15:8] \leq VEA$



Window address setting area

$$\begin{array}{ll} HSA[7:0] = 10h, HSA[7:0] = 3Fh, & I/D = 1 \text{ (increment)} \\ VSA[7:0] = 20h, VSA[7:0] = 4Fh, & AM = 0 \text{ (horizontal writing)} \end{array}$$

Figure 32 Automatic address update within a Window Address Area

16. γ Correction Function

The RM68130 supports γ -correction function to display in 262,144 colors simultaneously using gradient adjustment, amplitude-adjustment, and fine-adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative voltage setting.

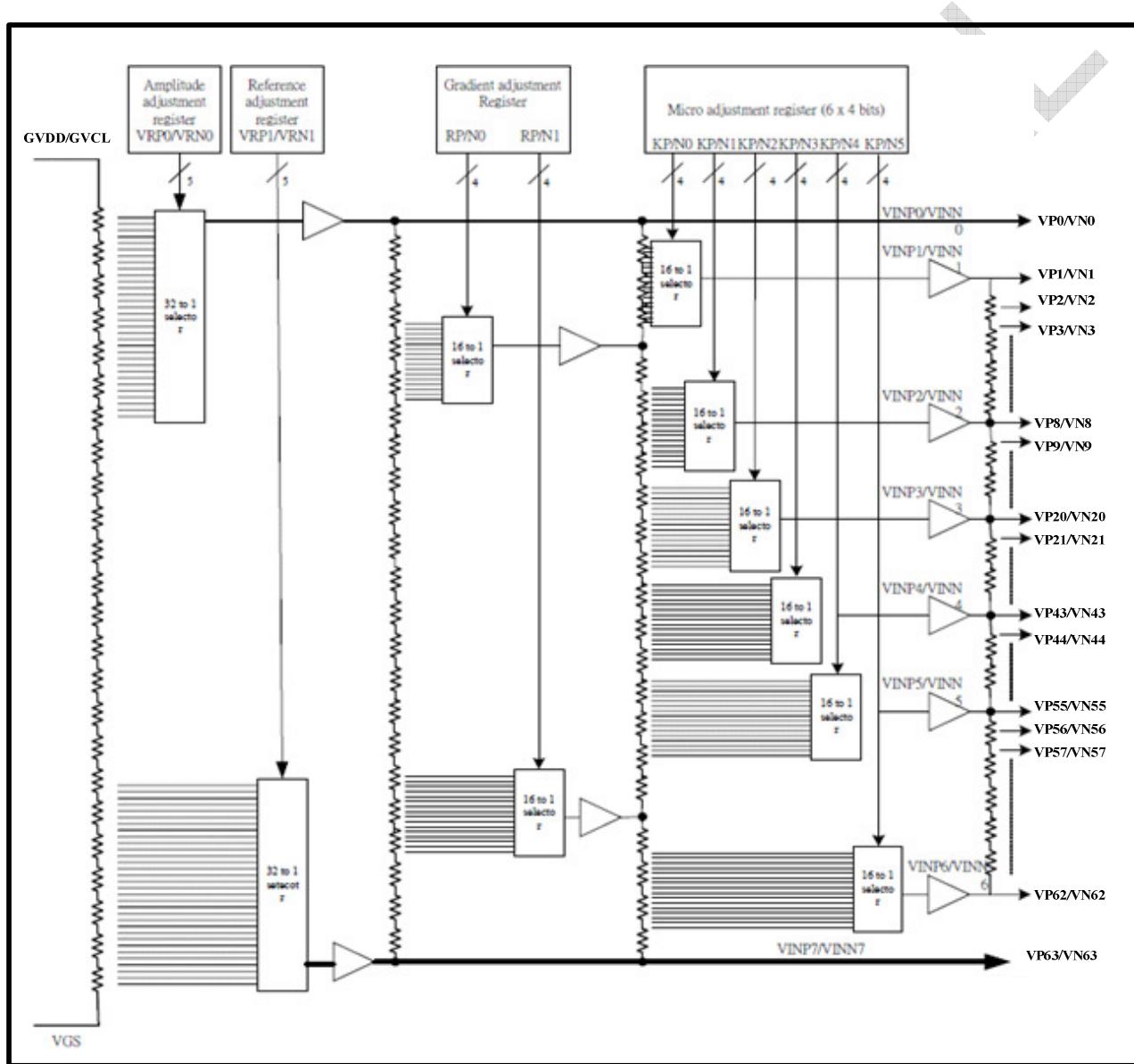


Figure 33 Structure of gamma correction function-positive/negative voltage setting

17. Power-Supply Generating Circuit

17.1 Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the RM68130 and the TFT display application voltage waveforms and electrical potential relationship.

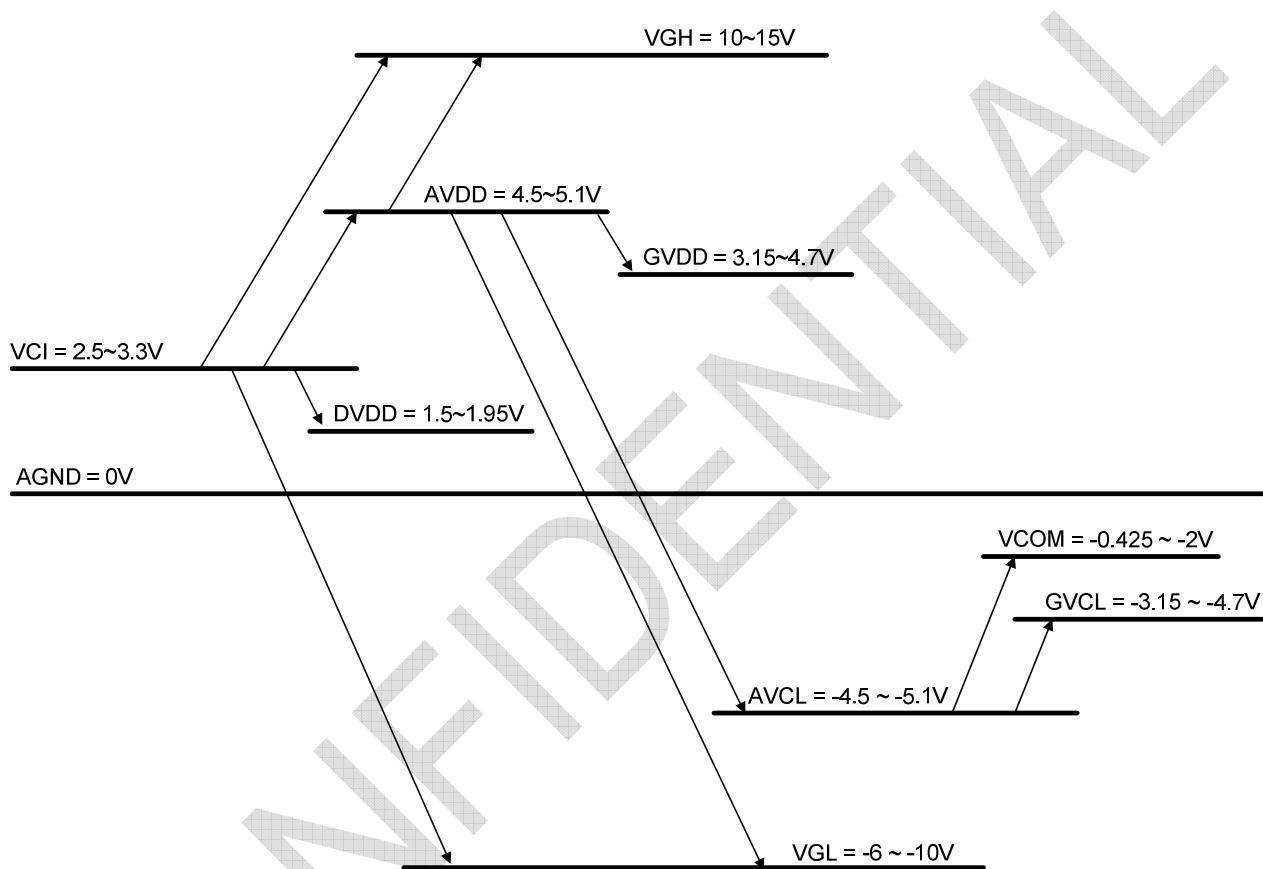


Figure 37 Diagram of voltage generation

Notes:

1. The AVDD, VGH, VGL, and AVCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationship: $(AVDD - GVDD) \geq 0.5V$, $(GVCL - AVCL) > 0.5V$. Also make sure $VGH - VGL \leq 28V$, $VCI - VCL \leq 6V$.
2. In operation, setting voltages within the respective voltage ranges are recommended.

18. NV Memory Programming Flow

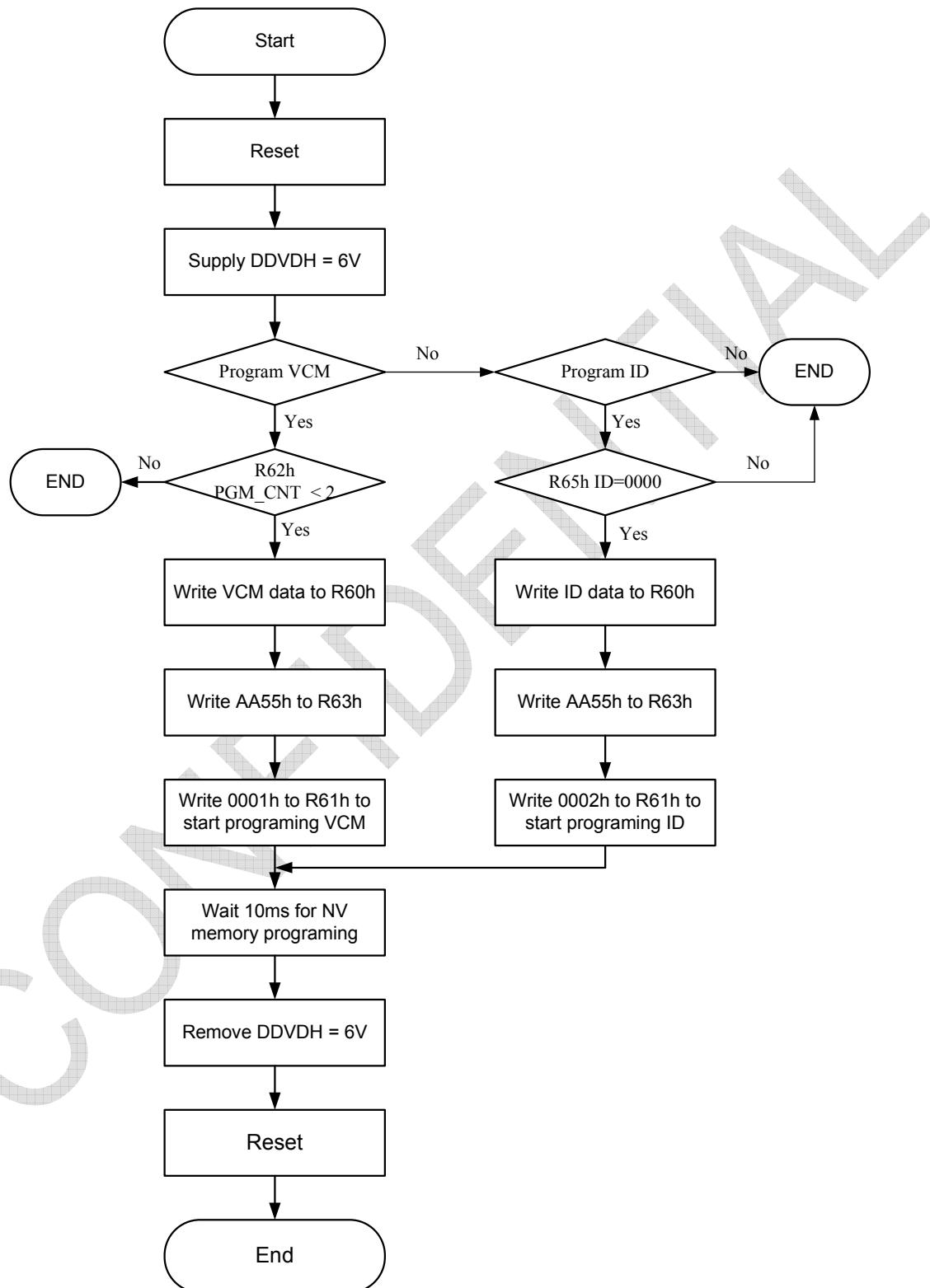


Figure 39 OTP control sequence diagram

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19. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

19.1 Power On Sequence

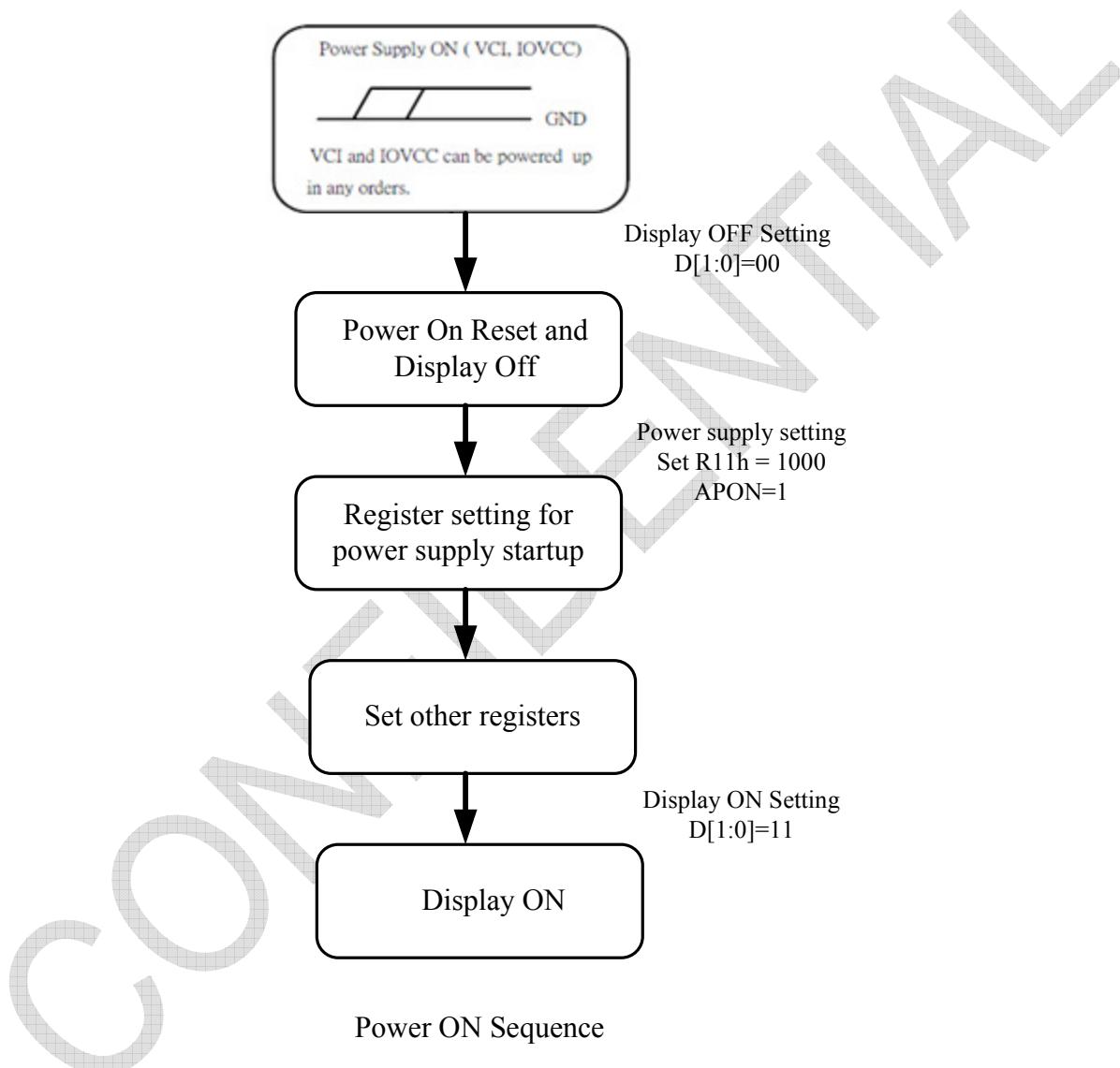
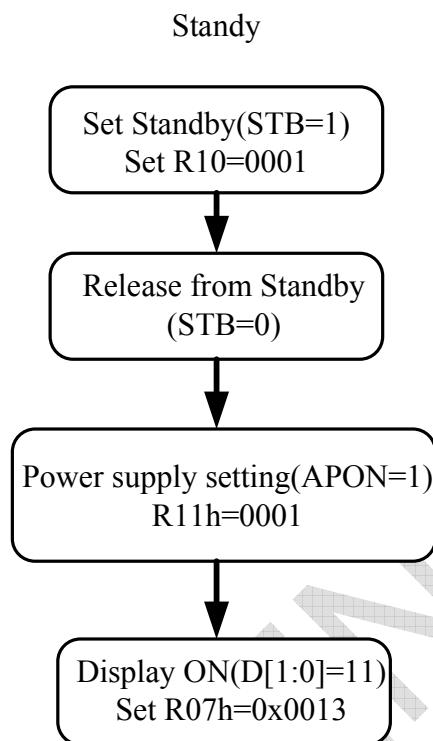
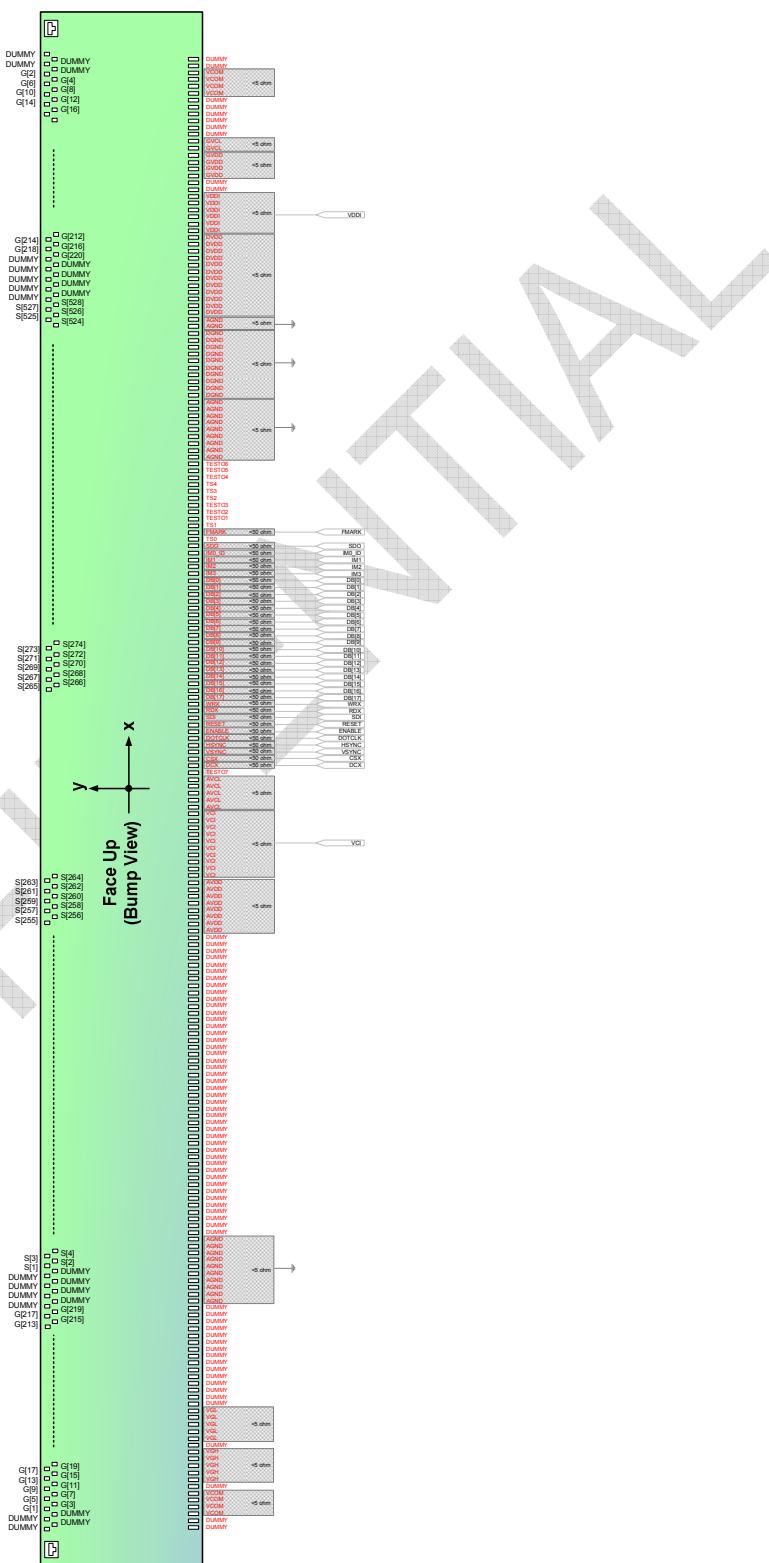


Figure 40 Power On Sequence

19.2 STB Mode Sequence**Figure 41 STB Mode Register Setting Sequence**

20. Application Circuit



21. ELECTRICAL SPECIFICATIONS

Absolute Operation Range

Item	Symbol	Rating	Unit
Supply voltage	VCI	-0.3 ~ +4.8	V
Supply Voltage (Logic)	VDDIO	-0.3 ~ +4.6	V
Supply Voltage (Digital)	DVDD	-0.3 ~ +1.95	V
Driver Supply Voltage	VGH-VGL	-0.3~+30.0	V
Logic input voltage range	VIN	-0.3~VDDIO+0.3	V
Logic output voltage range	VO	-0.3~VDDIO+0.3	V
Operating Temperature range	Topr	-30~+85	°C
Storage Temperature range	Tstg	-40~+125	°C

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

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22. Electrical Characteristics

DC Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	V _{C1}	Operating Voltage	2.5	2.8	3.3	V	
Interface Operating voltage	V _{DIO}	I/O supply voltage	1.65		3.3	V	
Input / Output							
Logic High level input voltage	V _{IH}		0.7V _{DIO}	-	V _{DIO}	V	Note 1
Logic Low level input voltage	V _{IL}	-	GND	-	0.3V _{DIO}	V	Note 1
Logic High level output voltage	V _{OH}	I _{OH} = -1.0mA	0.8V _{DIO}	-	V _{DIO}	V	Note 1
Logic Low level output voltage	V _{OL}	I _{OL} = +1.0mA	GND	-	0.2V _{DIO}	V	Note 1
Logic High level input current	I _{IH}	V _{IN} =V _{DIO}			1	µA	Note 1
Logic Low level input current	I _{IL}	V _{IN} =GND	-1			µA	Note 1
Logic Input leakage current	I _{IL}	I _{OH} = -1.0mA	-0.1	-	+0.1	µA	Note 1
VCOM Operation							
VCOM Amplitude voltage	V _{COM}		-2		-0.425	V	
Source Driver							
Source output range	V _{Sout}		G _{VCL}		G _{VDD}	V	Note 2
Gamma positive reference voltage	G _{VDD}		3.15		4.7	V	
Gamma negative reference voltage	G _{VCL}		-4.7		-3.15	V	
Output offset voltage	V _{OFSET}				35	mV	Note 3

Notes: 1. TA = -30 to 85 °C.

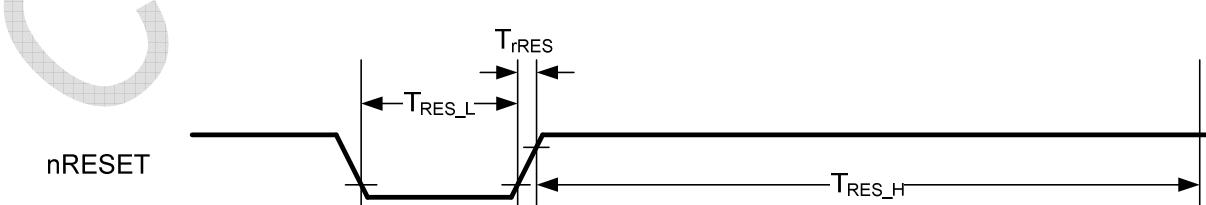
2. Source channel loading = $2K\Omega+12pF$ /channel, Gate channel loading= $5K\Omega+40pF$ /channel.

3. The maximum value is between measured point of source output and gamma setting value.

22.1 Reset Timing Characteristics

(V_{DDI} = 1.65V ~ 3.30V)

Item	Symbol	Unit	Min.	Max.
Reset low-level width	t _{RES_L}	ms	10	-
Reset back high-level width	t _{RES_H}	ms	50	-
Reset rise time	t _{rRES}	us		10



Note: After RESET releasing, the host processor have to wait 10 milliseconds before sending any command.

AC Timing Characteristics

22.1.1 i80-System Bus Interface

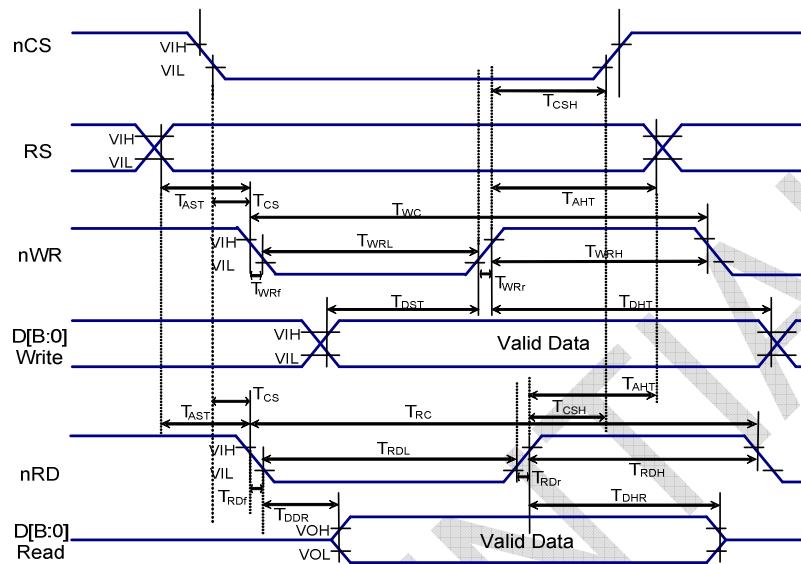


Figure 42 i80-system Bus Interface

Normal Write Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Parameter	Symbol	MIN	MAX	Unit	Description
RS	Address setup time	T _{AST}	10		ns	-
	Address hold time (Write/Read)	T _{AHT}	5		ns	-
CSX	Chip select setup time (Write)	T _{CS}	10		ns	-
	Chip select setup time (Read)	T _{CS}	10		ns	-
	Chip select hold time (Write)	T _{CSH}	5		ns	-
	Chip select hold time(Read)	T _{CSH}	5		ns	-
WRX	Write cycle	T _{WC}	70		ns	-
	Control pulse "H" duration	T _{WRH}	15		ns	-
	Control pulse "L" duration	T _{WRL}	15	500	ns	-
	Write rise time	T _{WRr}		15	ns	-
	Write fall time	T _{WFr}		15	ns	-
RDX (ID)	Read cycle	T _{RC}	300		ns	-
	Control pulse "H" duration	T _{RDH}	150		ns	-
	Control pulse "L" duration	T _{RDL}	150		ns	-
	Read rise time	T _{RDr}		15	ns	-
	Read fall time	T _{RDf}		15	ns	-
D[17:0]	Data setup time	T _{DST}	10		ns	-
	Data hold time	T _{DHT}	15		ns	-
	Read access time	T _{DDR}		100	ns	-
	Output disable time	T _{DHR}	5		ns	-

22.1.2 M68-System Bus Interface

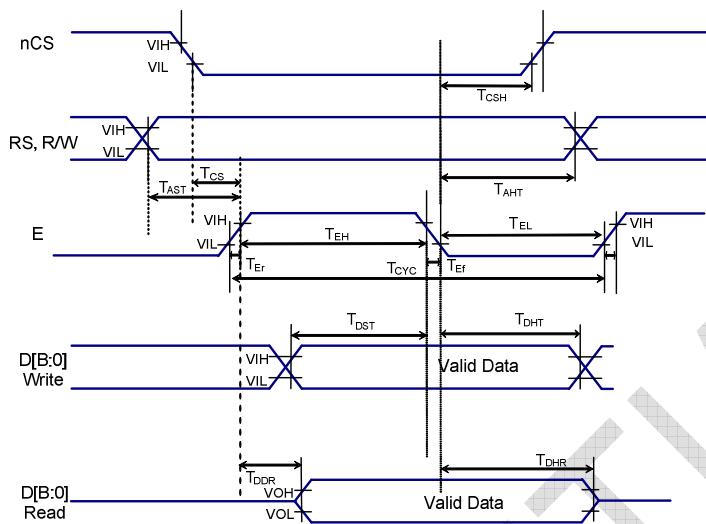


Figure 43 M68-system Bus Interface

Normal Write Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Parameter	Symbol	MIN	MAX	Unit	Description
RS,R/W	Address setup time	T_{AST}	10		ns	-
	Address hold time (Write/Read)	T_{AHT}	5		ns	
CSX	Chip select setup time (Write)	T_{CS}	10		ns	
	Chip select setup time (Read)	T_{CS}	10		ns	
	Chip select hold time (Write)	T_{CSH}	5		ns	
	Chip select hold time (Read)	T_{CSH}	5		ns	
E(wr)	Write cycle	T_{CYC}	70		ns	-
	Control pulse "H" duration	T_{EH}	50		ns	
	Control pulse "L" duration	T_{EL}	50	500	ns	
	Write rise time	T_{Er}		15	ns	
	Write fall time	T_{Ef}		15	ns	
E(rd)	Read cycle	T_{RC}	300		ns	-
	Control pulse "H" duration	T_{RDH}	150		ns	
	Control pulse "L" duration	T_{RDL}	150		ns	
	Read rise time	T_{Fr}		15	ns	
	Read fall time	T_{Ff}		15	ns	
D[17:0]	Data setup time	T_{DST}	10		ns	-
	Data hold time	T_{DHT}	15		ns	
	Read access time	T_{DDR}		100	ns	
	Output disable time	T_{DHR}	5		ns	

22.1.3 Clock Synchronous Serial Interface

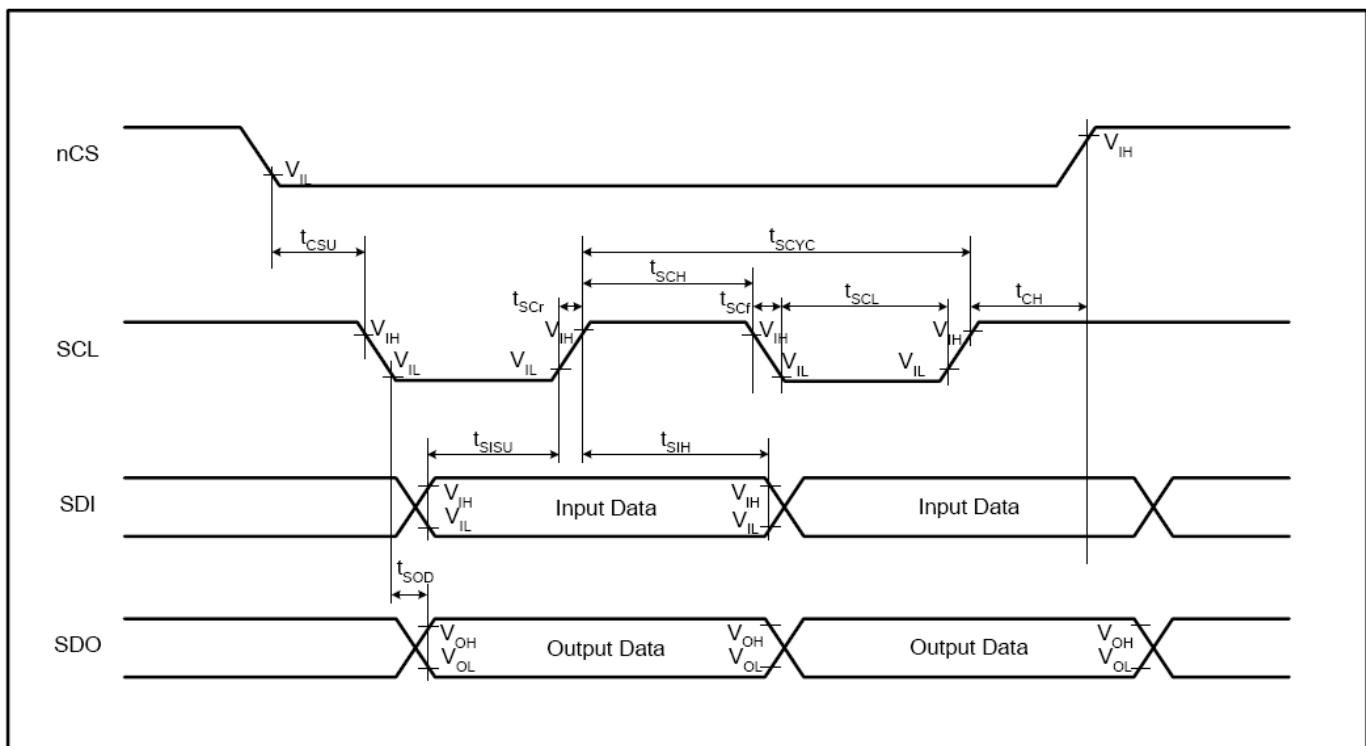


Figure 44 Clock Synchronous Serial Interface

VDDI = 1.65~3.3V, VCI=2.5~3.3V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T _{SCYC}	Clock cycle (Write)	80		ns	
	T _{SCYC}	Clock cycle (Read)	80		ns	
	T _{SCH}	Clock "H" pulse width (Write)	8		ns	
	T _{SCH}	Clock "H" pulse width (Read)	18		ns	
	T _{SCL}	Clock "L" pulse width (Write)	8		ns	
	T _{SCL}	Clock "L" pulse width (Read)	18		ns	
	T _{SCR}	Clock rise time		5	ns	
	T _{Scf}	Clock fall time		5	ns	
CSX	T _{CSU}	Chip select setup time	10		ns	
	T _{CH}	Chip select hold time	10		ns	
SDI	T _{SISU}	Data input setup time	5		ns	
	T _{SIH}	Data input hold time	5		ns	
SDO	T _{SOD}	Data output setup time		100	ns	
	T _{SOH}	Data output hold time	10		ns	

22.1.4 RGB Interface

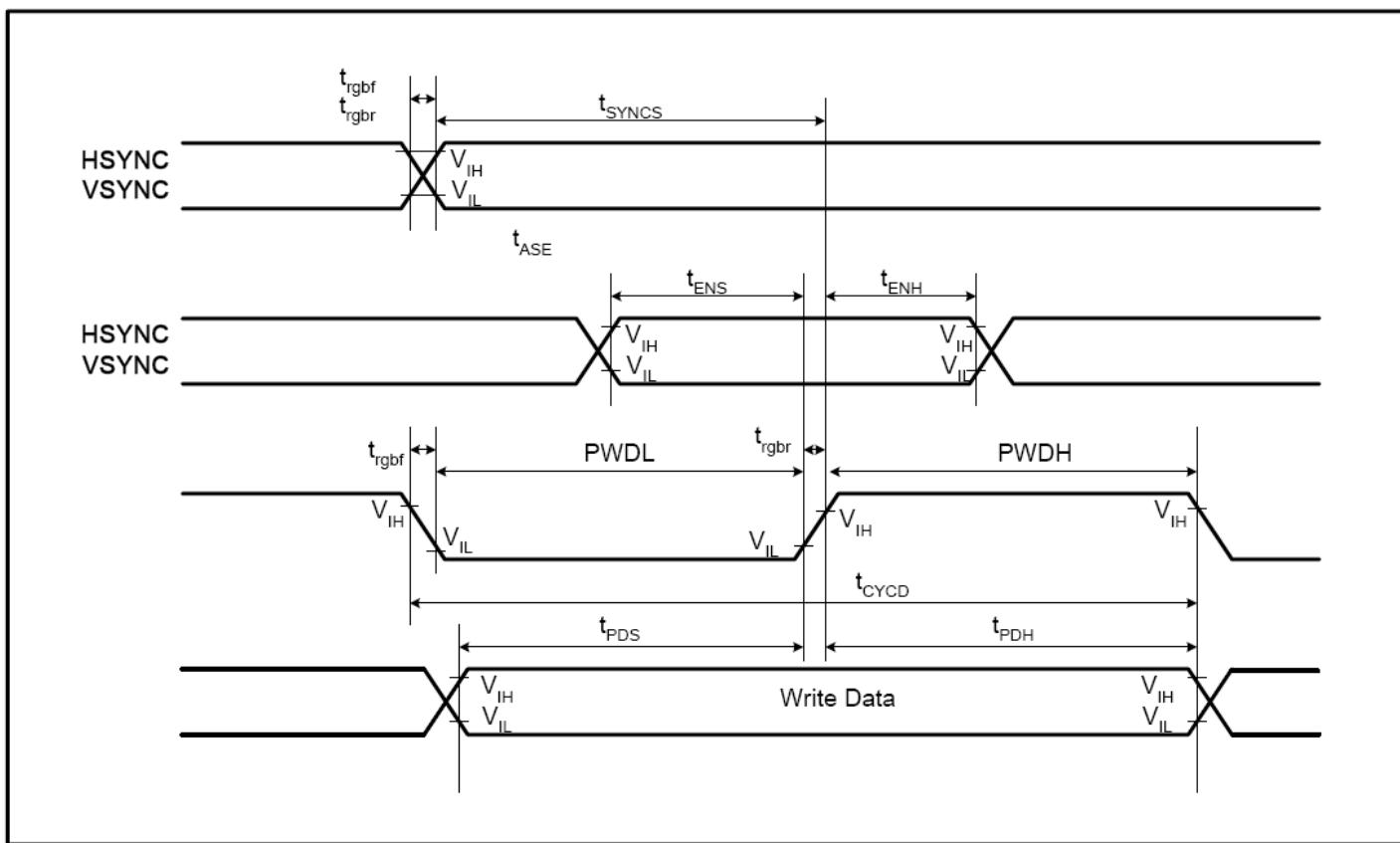


Figure 195 Timing chart for RGB Interface

18/16-bit Bus RGB Interface Mode (VDDI = 1.65~3.3V, VCI=2.5~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T _{SYCSX}	VSYNC setup time	0		ns	-
	T _{rghr}	VSYNC rise time		25	ns	-
	T _{rghf}	VSYNC fall time		25	ns	-
HSYNC	T _{SYCSX}	HSYNC setup time	0		ns	-
	T _{rghr}	HSYNC rise time		25	ns	-
	T _{rghf}	HSYNC fall time		25	ns	-
ENABLE	T _{EWS}	ENABLE setup time	10		ns	-
	T _{ENH}	ENABLE hold time	10		ns	-
DB[17:0]	T _{PDS}	Data input setup time	10		ns	-
	T _{PDH}	Data input hold time	40		ns	-
DOTCLK	PWDH	DOTCLK "H" pulse width	40		ns	-
	PWDL	DOTCLK "L" pulse width	40		ns	-
	T _{CYCD}	DOTCLK clock cycle	100			-
	T _{rghr}	DOTCLK rise time		25	ns	-
	T _{rghf}	DOTCLK fall time		25	ns	-

6-bit Bus RGB Interface Mode (VDDI = 1.65 ~ 3.3V, VCI=2.5~3.3V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T _{SYCSX}	VSYNC setup time	0		ns	-
	T _{rghr}	VSYNC rise time		25	ns	
	T _{rghf}	VSYNC fall time		25	ns	
HSYNC	T _{SYCSX}	HSYNC setup time	0		ns	-
	T _{rghr}	HSYNC rise time		25	ns	
	T _{rghf}	HSYNC fall time		25	ns	
ENABLE	T _{E_S}	ENABLE setup time	10		ns	-
	T _{E_H}	ENABLE hold time	10		ns	
DB[17:0]	T _{PDS}	Data input setup time	10		ns	-
	T _{PDH}	Data input hold time	30		ns	
DOTCLK	PWDH	DOTCLK "H" pulse width	30		ns	-
	PWDL	DOTCLK "L" pulse width	30		ns	
	T _{CYCD}	DOTCLK clock cycle	80		ns	
	T _{rghr}	DOTCLK rise time		25	ns	
	T _{rghf}	DOTCLK fall time		25	ns	