デジタルトレーニング

飯塚研究室　B4　福島幸弥

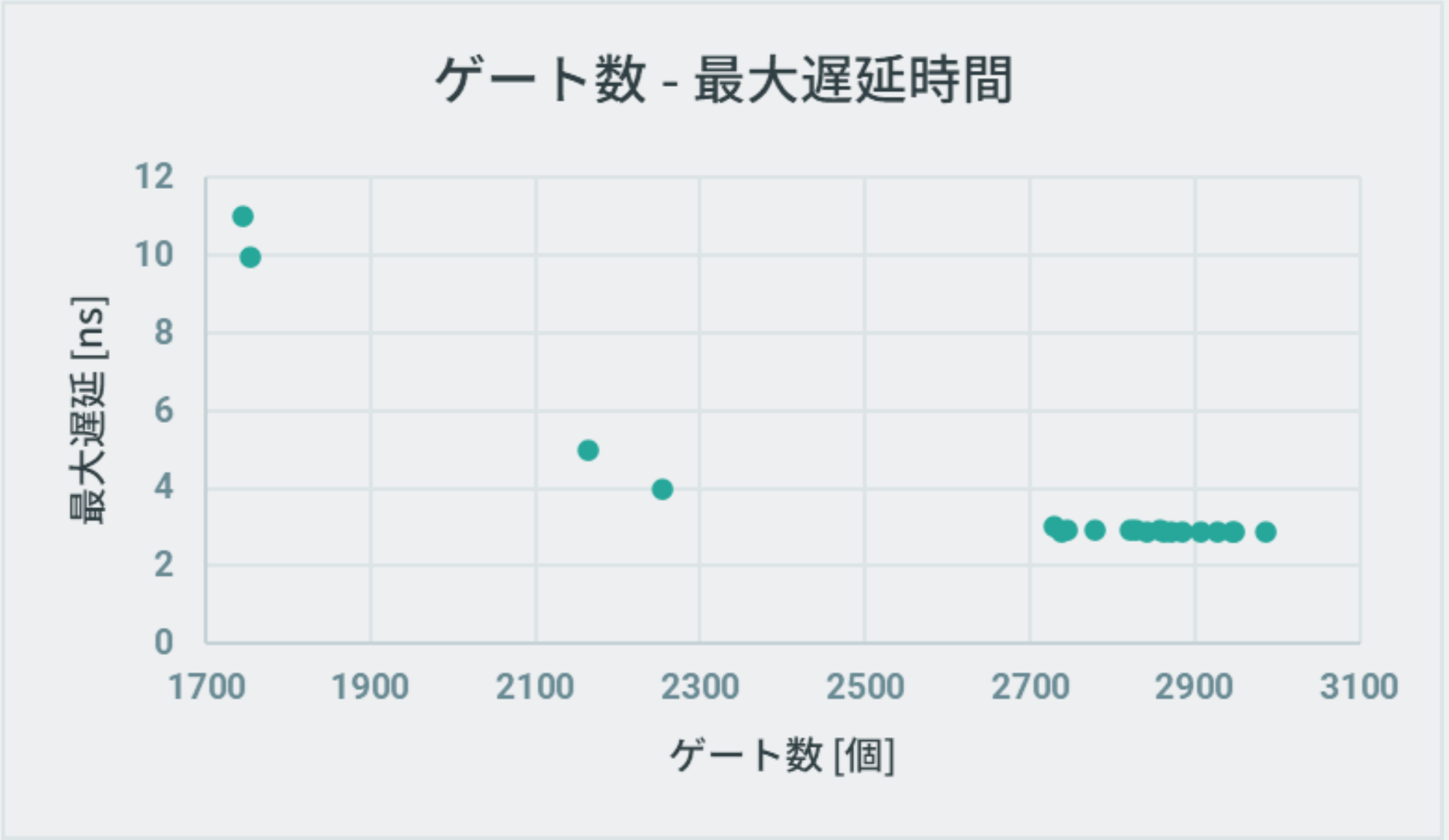
課題1　16bit

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	10.99	22514.69	1.94	24.25	35.85	21.32	1745.32
10	9.95	22637.26	2.16	24.84	35.37	21.49	1754.83
5	5.00	27907.89	4.80	29.18	36.78	23.98	2163.40
4	3.99	29075.56	6.32	31.86	35.91	25.21	2253.92
3	3.00	35217.10	9.44	40.84	50.56	28.32	2730.01
2.9	2.90	35317.09	9.80	41.32	62.97	28.43	2737.76
2.8	2.88	37210.52	10.19	43.79	56.31	29.35	2884.54
2.7	2.89	36920.22	10.07	43.34	64.50	29.11	2862.03
2.6	2.94	35404.19	9.63	41.55	58.63	28.30	2744.51
2.5	2.88	37487.92	10.19	44.12	54.60	29.34	2906.04
2.4	2.91	36868.61	10.13	43.55	58.14	29.47	2858.03
2.3	2.93	36478.31	9.95	43.05	58.01	29.16	2827.78
2.2	2.90	37020.21	10.19	43.73	58.95	29.54	2869.78
2.1	2.91	35839.64	10.00	42.02	53.04	29.09	2778.27
2	2.90	36662.17	10.13	43.12	60.01	29.39	2842.03
1.9	2.87	38016.92	10.44	45.14	64.87	29.96	2947.05
1.8	2.92	36407.35	10.07	42.98	59.39	29.40	2822.28
1.7	2.89	37758.87	10.24	44.70	56.27	29.61	2927.04
1.6	2.90	37981.44	10.26	45.01	62.48	29.75	2944.30
1.5	2.88	38516.89	10.47	45.38	63.20	30.15	2985.81

※このスライドを含め、Dynamic Powerはすべて換算値で表記

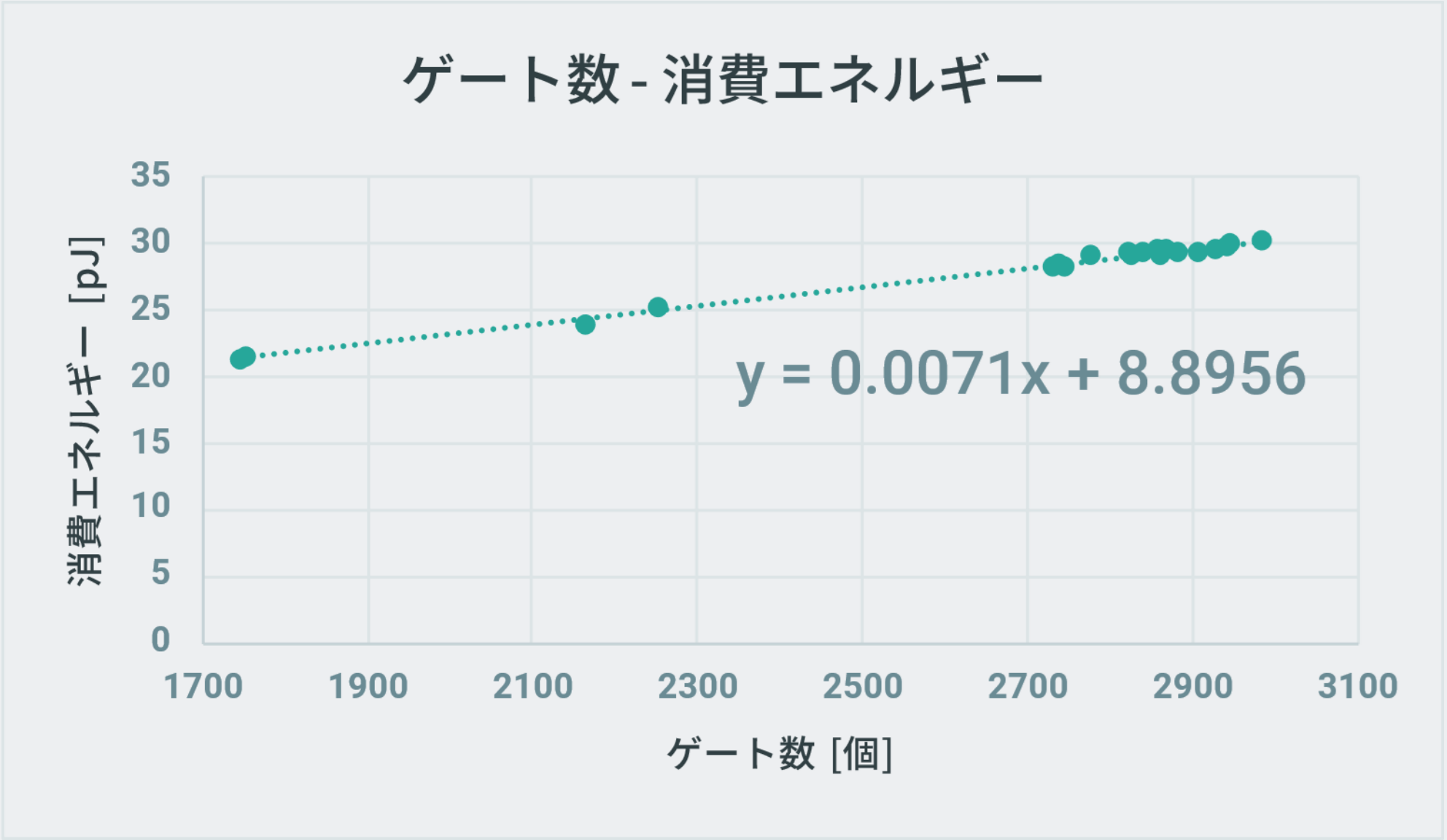
課題1　16bit

ゲート数が2000を超えたあたりからは
あまり遅延時間の減少に寄与していない



課題1　16bit

一次関数的特性が見られる
→比例ではないのはゲート以外の影響？



課題2　8bit

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	5.49	8680.09	1.40	8.76	35.24	7.68	672.88
10	5.49	8680.09	1.40	8.76	35.44	7.68	672.88
5	4.85	8689.77	1.58	8.80	34.44	7.66	673.63
4	3.90	8792.99	1.95	9.14	34.48	7.60	681.63
3	2.99	9483.26	2.68	9.58	34.66	8.02	735.14
2.9	2.90	9512.29	2.77	9.62	34.65	8.03	737.39
2.8	2.80	9638.09	2.89	9.82	35.04	8.10	747.14
2.7	2.70	9850.98	3.07	10.18	34.83	8.29	763.64
2.6	2.60	10021.94	3.27	10.43	35.11	8.49	776.89
2.5	2.50	10263.86	3.39	10.93	34.97	8.48	795.65
2.4	2.40	11396.04	3.80	12.81	35.52	9.12	883.41
2.3	2.39	12128.26	3.96	14.03	36.96	9.46	940.17
2.2	2.39	11721.83	3.95	13.48	36.13	9.45	908.67
2.1	2.39	11754.09	3.90	13.54	36.27	9.32	911.17
2	2.39	11921.82	3.94	13.83	36.33	9.41	924.17
1.9	2.78	12018.59	3.33	13.75	41.02	9.26	931.67
1.8	2.78	11708.93	3.30	13.31	41.52	9.17	907.67
1.7	2.78	11854.08	3.31	13.56	39.54	9.19	918.92
1.6	2.78	11857.31	3.31	13.57	40.74	9.19	919.17
1.5	2.78	11763.76	3.31	13.46	40.45	9.20	911.92

遅延が最小のもののうち、ゲート面積が最も小さいものを採用した

課題2　32bit

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.87	72198.60	3.27	78.86	38.19	64.92	5596.79
10	9.99	84901.02	7.06	89.49	40.31	70.55	6581.47
5	5.00	97477.63	15.31	107.78	39.60	76.57	7556.41
4	4.00	102096.69	20.05	112.81	42.06	80.20	7914.47
3	3.45	116857.04	26.02	137.30	135.49	89.77	9058.69
2.9	3.44	120531.00	26.78	142.25	126.09	92.11	9343.49
2.8	3.43	118653.70	26.58	140.71	121.18	91.15	9197.96
2.7	3.42	119653.63	26.74	142.00	126.37	91.45	9275.48
2.6	3.40	122253.47	27.29	144.72	160.11	92.78	9477.01
2.5	3.41	120447.13	27.05	142.67	151.67	92.23	9336.99
2.4	3.43	120811.62	26.72	143.37	122.73	91.66	9365.24
2.3	3.43	119908.46	26.62	141.31	141.31	91.32	9295.23
2.2	3.42	121259.98	26.91	143.45	122.75	92.03	9400.00
2.1	3.43	118702.08	26.45	140.11	128.68	90.72	9201.71
2	3.42	123137.28	27.11	145.92	156.66	92.71	9545.53
1.9	3.45	117505.38	26.21	138.77	102.20	90.43	9108.94
1.8	3.41	121776.08	27.18	144.50	129.04	92.68	9440.01
1.7	3.46	119002.06	26.32	140.32	113.92	91.05	9224.97
1.6	3.42	121772.85	27.21	144.40	141.29	93.07	9439.76
1.5	3.41	120872.91	27.06	142.79	141.89	92.26	9369.99

課題2　64bit

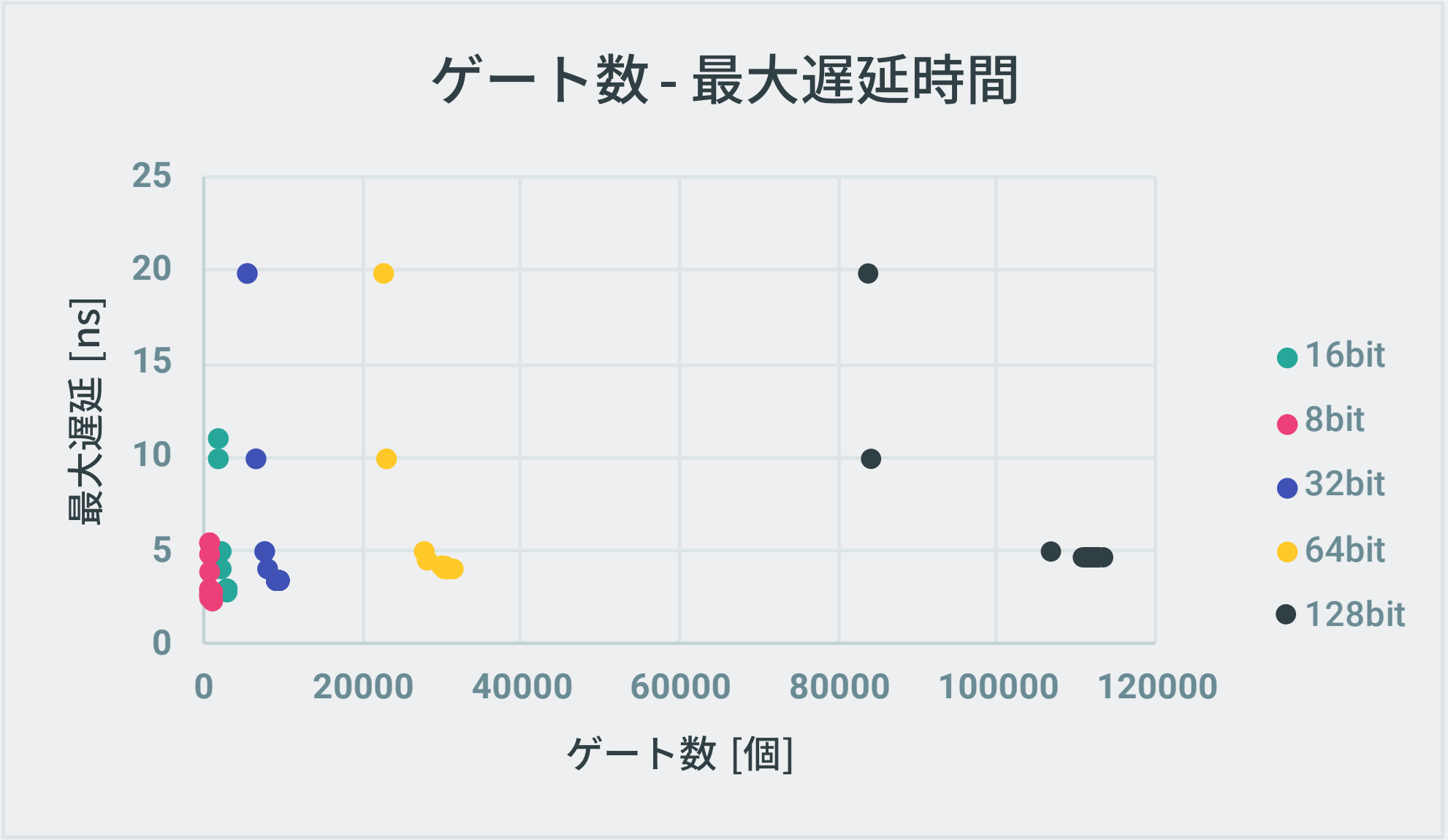
Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.99	293884.42	11.59	310.35	58.85	231.68	22781.74
10	10.00	296964.87	23.28	313.02	57.24	232.83	23020.53
5	5.00	356261.07	54.16	393.21	61.14	270.81	27617.14
4.5	4.50	364308.95	61.18	406.42	67.30	275.29	28241.00
4	4.10	398442.25	72.58	468.03	269.41	297.59	30887.00
3.8	4.10	397261.68	72.35	467.13	215.87	296.63	30795.48
3.6	4.13	393578.04	71.25	459.14	187.82	294.25	30509.93
3.4	4.11	396593.98	72.07	464.70	250.93	296.21	30743.72
3.2	4.12	392074.91	71.42	456.79	227.04	294.26	30393.40
3	4.12	395039.24	71.80	463.13	188.74	295.81	30623.20
2.8	4.10	395239.23	72.23	462.02	206.58	296.14	30638.70
2.6	4.09	395945.63	72.44	462.23	306.15	296.29	30693.46
2.4	4.11	394081.24	70.30	461.79	199.62	288.94	30548.93
2.2	4.11	396929.44	70.87	466.85	212.81	291.29	30769.72
2	4.06	404377.35	72.86	476.56	273.77	295.83	31347.08
1.8	4.13	387404.24	70.49	450.44	219.41	291.14	30031.34
1.6	4.08	402964.54	73.55	476.13	253.65	300.07	31237.56
1.4	4.14	387694.55	70.41	450.39	205.73	291.49	30053.84
1.2	4.10	399122.85	72.71	468.73	276.01	298.11	30939.76
1	4.10	394603.78	72.12	462.48	255.92	295.69	30589.44

課題2　128bit

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.99	1078240.67	41.24	1.14	147.43	824.47	83584.55
10	10.00	1083637.10	81.99	1.15	155.13	819.86	84002.88
5	5.00	1375053.95	196.67	1.55	447.93	983.34	106593.33
4.5	4.77	1450987.80	216.99	1.70	878.56	1035.03	112479.67
4	4.78	1442443.19	215.85	1.69	919.99	1031.76	111817.30
3.8	4.78	1437730.58	215.16	1.68	708.52	1028.48	111451.98
3.6	4.77	1447407.39	217.22	1.70	647.05	1036.12	112202.12
3.4	4.78	1430218.16	214.40	1.66	526.46	1024.84	110869.63
3.2	4.75	1450268.49	217.95	1.70	748.01	1035.27	112423.91
3	4.82	1440056.24	213.81	1.68	734.87	1030.58	111632.27
2.8	4.81	1438543.44	214.13	1.68	740.01	1029.95	111515.00
2.6	4.78	1460822.66	218.07	1.71	900.73	1042.37	113242.07
2.4	4.76	1451874.84	218.22	1.70	797.81	1038.71	112548.44
2.2	4.79	1450252.37	215.63	1.70	876.80	1032.89	112422.66
2	4.78	1441994.83	215.15	1.68	784.67	1028.40	111782.54
1.8	4.78	1439759.49	215.75	1.68	715.08	1031.28	111609.26
1.6	4.79	1439362.74	214.73	1.68	704.91	1028.57	111578.51
1.4	4.80	1435156.56	214.36	1.67	689.25	1028.94	111252.45
1.2	4.78	1430947.15	214.63	1.67	542.78	1025.91	110926.14
1	4.78	1437327.38	215.00	1.67	632.00	1027.70	111420.73

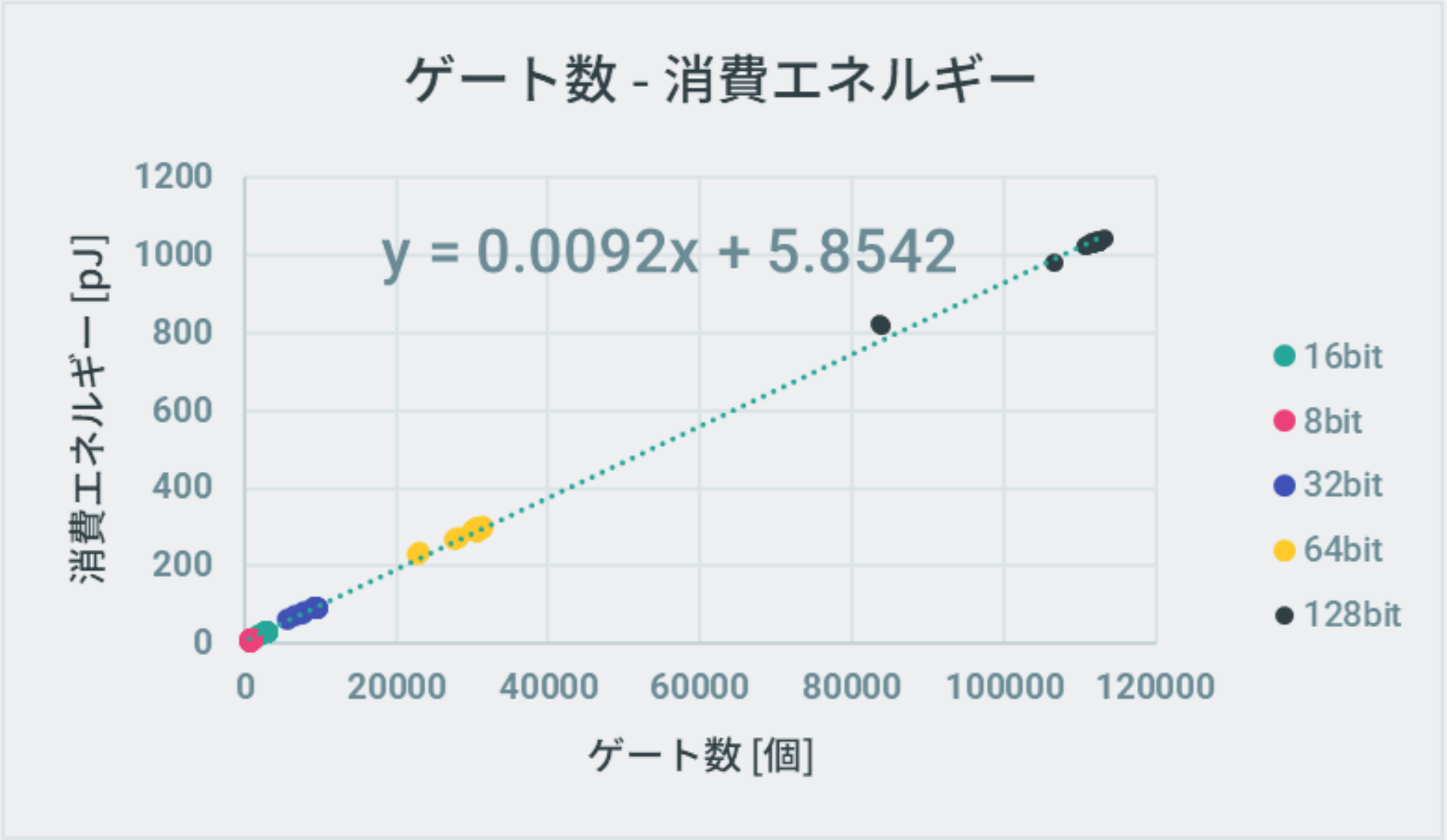
課題2　bitごとの比較

32bit以上は
最大遅延時間にあまり差がない

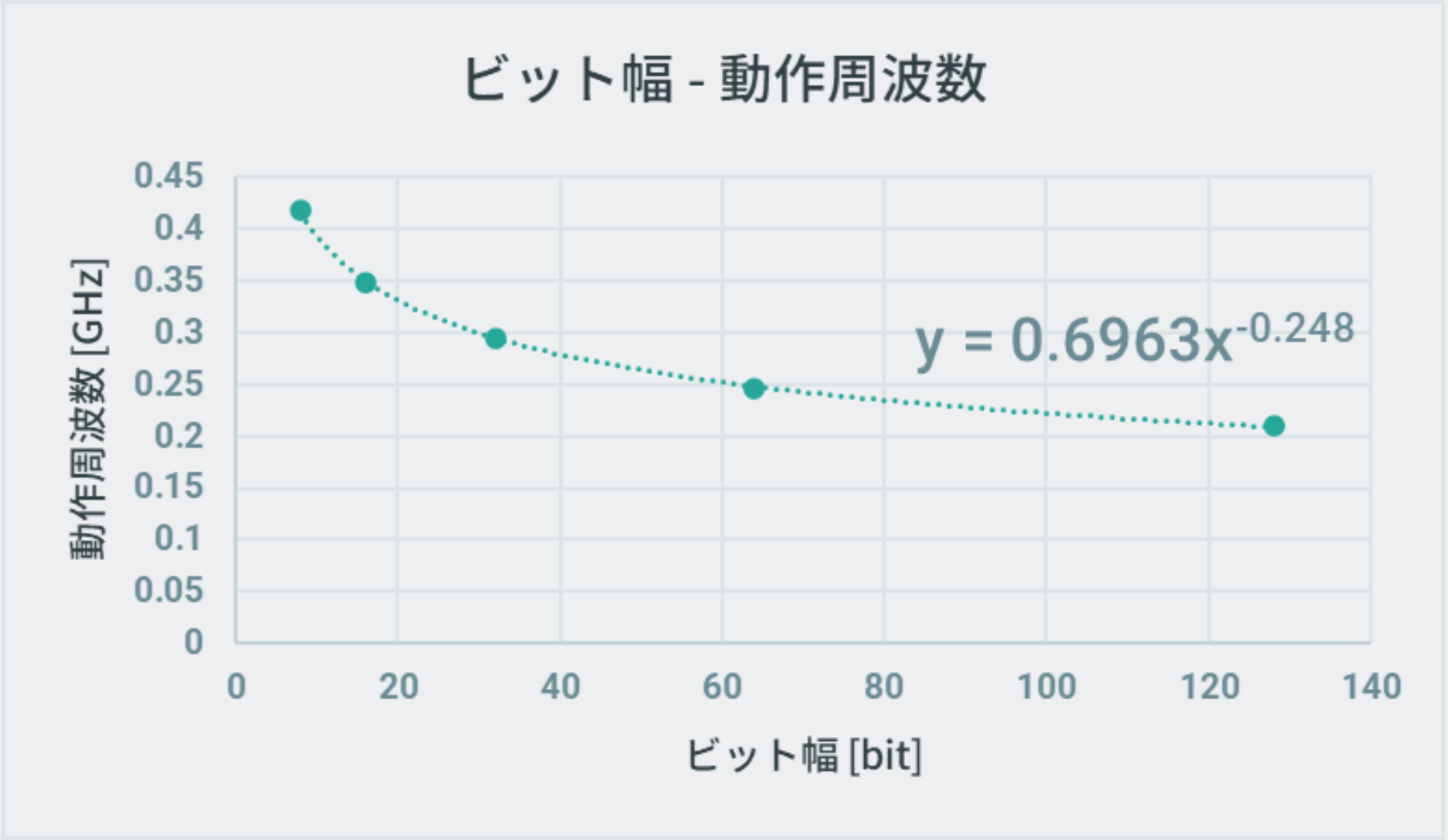


課題2　bitごとの比較

ほぼ比例のような特性がみられる
→ゲート以外(配線など)の影響は小さい

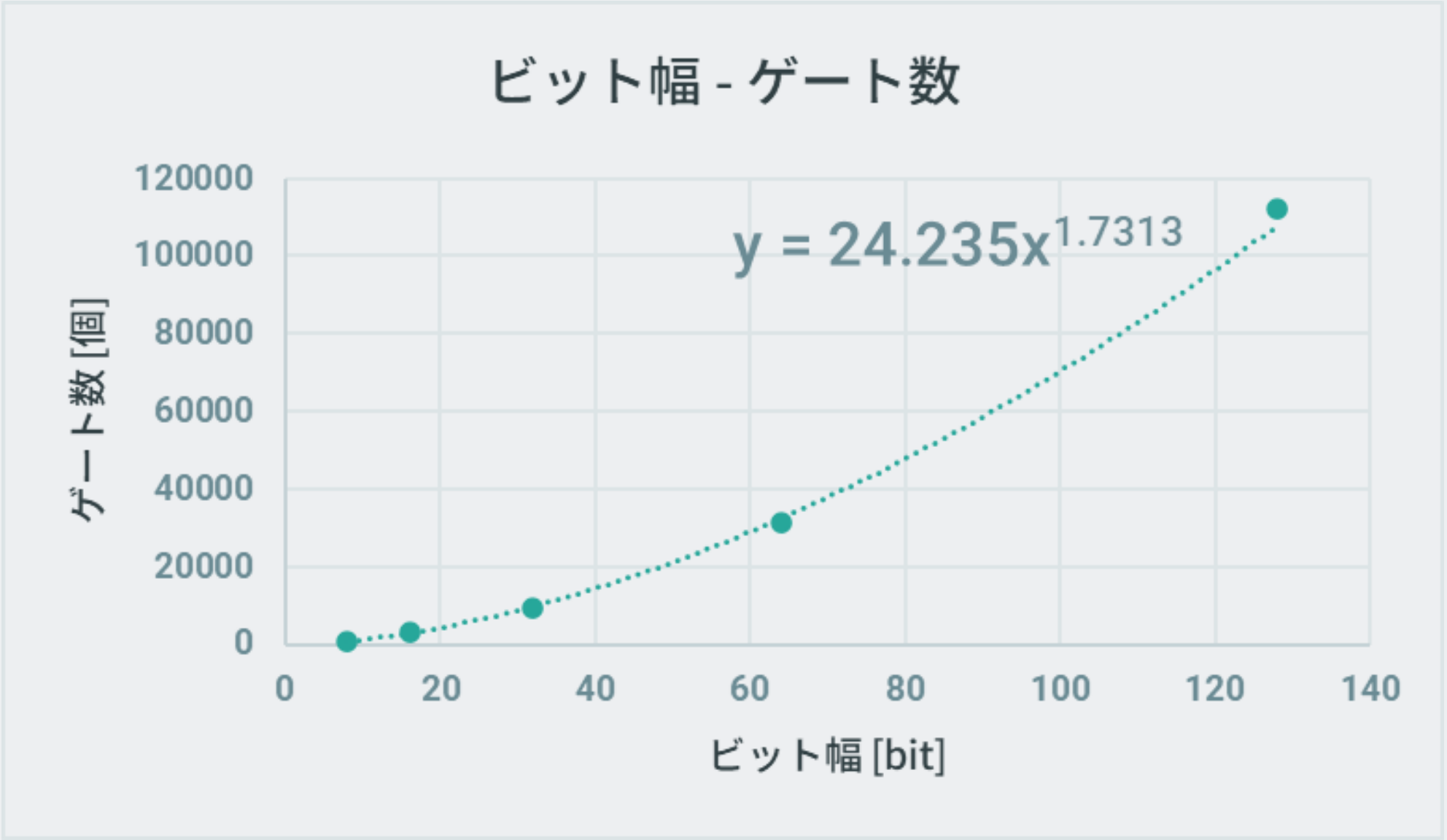


課題2　結果


ビット幅 - 動作周波数
動作周波数 [GHz]
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
0
20
40
60
80
100
120
140
ビット幅 [bit]
y = 0.6963x-0.248

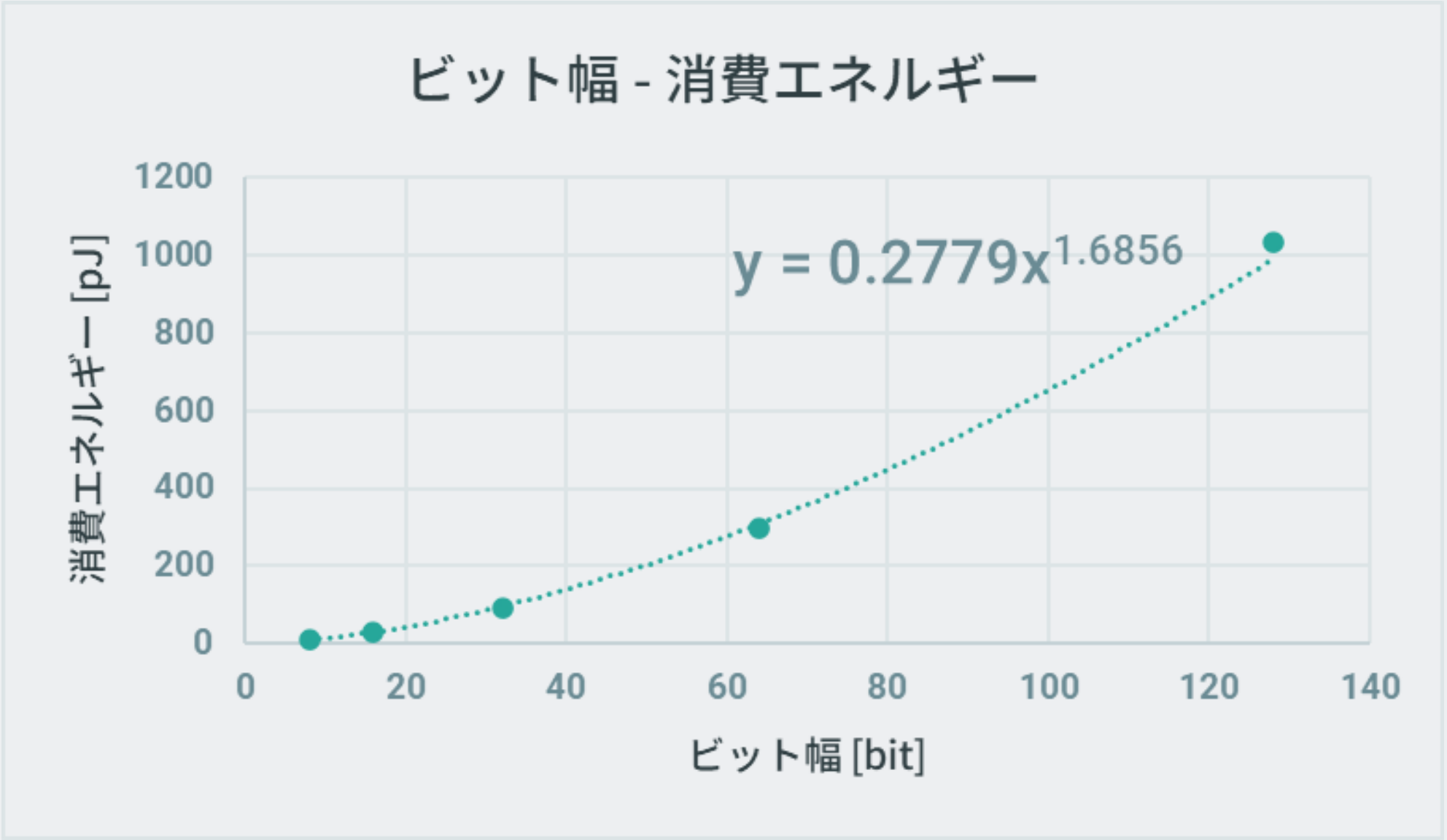
課題2　結果

Bit数が2倍になると
ゲート数は約3倍になった



課題2　結果

ゲート数と特性がほぼ同じ



課題3　2段

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.89	264299.21	11.92	291.85	60.38	237.15	20488.31
10	10.00	309522.13	24.84	331.63	74.39	248.42	23993.96
5	5.00	313338.01	51.09	335.52	72.52	255.46	24289.77
4.5	4.50	317702.25	58.16	341.77	72.83	261.74	24628.08
4	4.00	328969.27	70.82	357.38	78.02	283.28	25501.49
3.8	3.80	336942.95	79.11	367.51	69.77	300.61	26119.61
3.6	3.60	348448.67	89.36	382.94	68.98	321.70	27011.52
3.4	3.40	356712.65	98.09	391.90	74.65	333.52	27652.14
3.2	3.20	361302.68	104.89	399.23	75.69	335.66	28007.96
3	3.00	378862.85	106.49	426.51	71.59	319.46	29369.21
2.8	2.80	382962.59	115.24	432.84	69.68	322.66	29687.02
2.6	2.71	400384.06	128.35	456.83	215.86	347.83	31037.52
2.4	2.67	407812.61	130.13	472.30	183.38	347.44	31613.38
2.2	2.58	415663.73	135.38	489.16	182.89	349.27	32221.99
2	2.60	420340.85	136.66	497.05	178.01	355.31	32584.56
1.8	2.78	416389.49	124.68	493.10	178.57	346.60	32278.25
1.6	2.78	412638.11	124.72	485.48	284.13	346.73	31987.45
1.4	2.78	415625.02	124.92	492.43	223.97	347.29	32218.99
1.2	2.78	415747.59	127.90	488.05	197.06	355.56	32228.50
1	2.78	414908.93	125.05	489.84	176.66	347.65	32163.48

課題3　3段

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.98	271563.26	12.02	301.45	68.62	240.17	21051.42
10	10.00	283585.07	26.19	318.76	66.26	261.92	21983.34
5	5.00	320476.26	54.06	345.97	77.28	270.29	24843.12
4.5	4.50	324153.45	61.33	350.89	71.29	276.01	25128.17
4	4.00	335288.22	74.47	366.36	72.26	297.87	25991.33
3.8	3.80	343913.47	82.99	377.37	68.09	315.35	26659.96
3.6	3.60	343387.70	83.63	381.79	97.67	301.08	26619.20
3.4	3.40	343032.89	88.39	381.49	113.21	300.53	26591.70
3.2	3.20	346187.52	94.64	386.17	121.52	302.86	26836.24
3	3.00	407980.34	126.52	466.67	68.99	379.55	31626.38
2.8	2.80	413757.39	141.13	474.32	71.92	395.16	32074.22
2.6	2.60	433843.20	163.03	502.77	75.41	423.88	33631.26
2.4	2.41	445355.37	183.89	519.85	78.49	443.17	34523.67
2.2	2.41	445458.59	183.33	521.50	69.11	441.82	34531.67
2	2.41	478466.16	205.38	569.56	78.23	494.97	37090.40
1.8	2.78	492842.66	184.15	598.54	84.65	511.93	38204.86
1.6	2.78	503722.61	186.50	616.19	91.16	518.47	39048.26
1.4	2.78	487020.45	174.43	593.12	100.03	484.91	37753.52
1.2	2.78	476211.46	166.55	577.23	109.31	463.01	36915.62
1	2.78	478540.35	167.46	580.94	126.31	465.54	37096.15

遅延が最小のもののうち、ゲート面積が最も小さいものを採用した

課題3　4段

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.98	278169.29	12.68	310.54	74.19	253.38	21563.51
10	10.00	292155.49	27.96	329.92	60.98	279.57	22647.71
5	5.00	330930.43	55.68	361.78	74.57	278.41	25653.52
4.5	4.50	333094.81	61.51	364.57	74.89	276.78	25821.30
4	4.00	340552.40	72.74	375.82	87.85	290.97	26399.41
3.8	3.80	344684.39	79.15	381.37	93.27	300.79	26719.72
3.6	3.60	337268.74	81.67	370.81	100.00	294.01	26144.86
3.4	3.40	339158.94	85.93	374.06	98.42	292.15	26291.39
3.2	3.20	343642.52	93.81	380.77	102.10	300.20	26638.96
3	3.00	414115.43	130.76	475.42	63.53	392.27	32101.97
2.8	2.80	427546.83	147.14	494.96	67.23	412.01	33143.17
2.6	2.60	446929.46	172.04	521.48	67.15	447.32	34645.69
2.4	2.41	479014.51	207.67	567.96	68.52	500.48	37132.91
2.2	2.41	477243.65	206.02	568.37	70.27	496.51	36995.63
2	2.41	467873.29	193.47	566.44	75.04	466.27	36269.25
1.8	2.78	499409.98	168.63	620.78	176.21	468.78	38713.95
1.6	2.78	474411.58	148.35	586.78	164.99	412.41	36776.09
1.4	2.78	481088.57	153.95	601.16	131.90	427.98	37293.69
1.2	2.78	490355.72	155.94	609.26	174.78	433.51	38012.07
1	2.78	538801.01	190.93	678.91	132.78	530.78	41767.52

遅延が最小のもののうち、ゲート面積が最も小さいものを採用した

課題3　5段

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.98	284775.32	13.33	319.63	58.93	266.35	22075.61
10	9.99	298958.28	29.32	339.21	61.41	292.93	23175.06
5	5.00	336942.95	59.06	370.38	73.06	295.28	26119.61
4.5	4.50	342710.32	66.33	378.87	90.38	298.49	26566.69
4	4.00	347722.91	76.76	385.57	82.53	307.03	26955.26
3.8	3.80	351938.77	82.58	392.08	86.24	313.81	27282.07
3.6	3.60	357086.82	88.74	399.14	107.29	319.48	27681.15
3.4	3.40	347248.74	90.80	386.27	104.89	308.71	26918.51
3.2	3.20	352025.86	99.19	393.13	108.25	317.42	27288.83
3	3.00	395913.37	109.66	454.22	97.13	328.98	30690.96
2.8	2.80	404022.53	120.66	468.98	88.70	337.85	31319.58
2.6	2.60	410138.27	133.21	480.09	117.55	346.36	31793.66
2.4	2.41	477030.76	195.13	579.49	113.43	470.25	36979.13
2.2	2.41	434498.00	163.76	520.80	86.82	394.65	33682.02
2	2.41	424240.59	156.90	504.59	75.11	378.13	32886.87
1.8	2.78	471066.63	151.82	581.15	144.80	422.07	36516.79
1.6	2.78	486223.73	158.89	604.57	153.81	441.72	37691.76
1.4	2.78	490958.91	163.22	612.95	137.96	453.77	38058.83
1.2	2.78	471076.30	169.52	575.94	147.53	471.26	36517.54
1	2.78	515712.16	188.08	647.11	79.82	522.85	39977.69

遅延が最小のもののうち、ゲート面積が最も小さいものを採用した

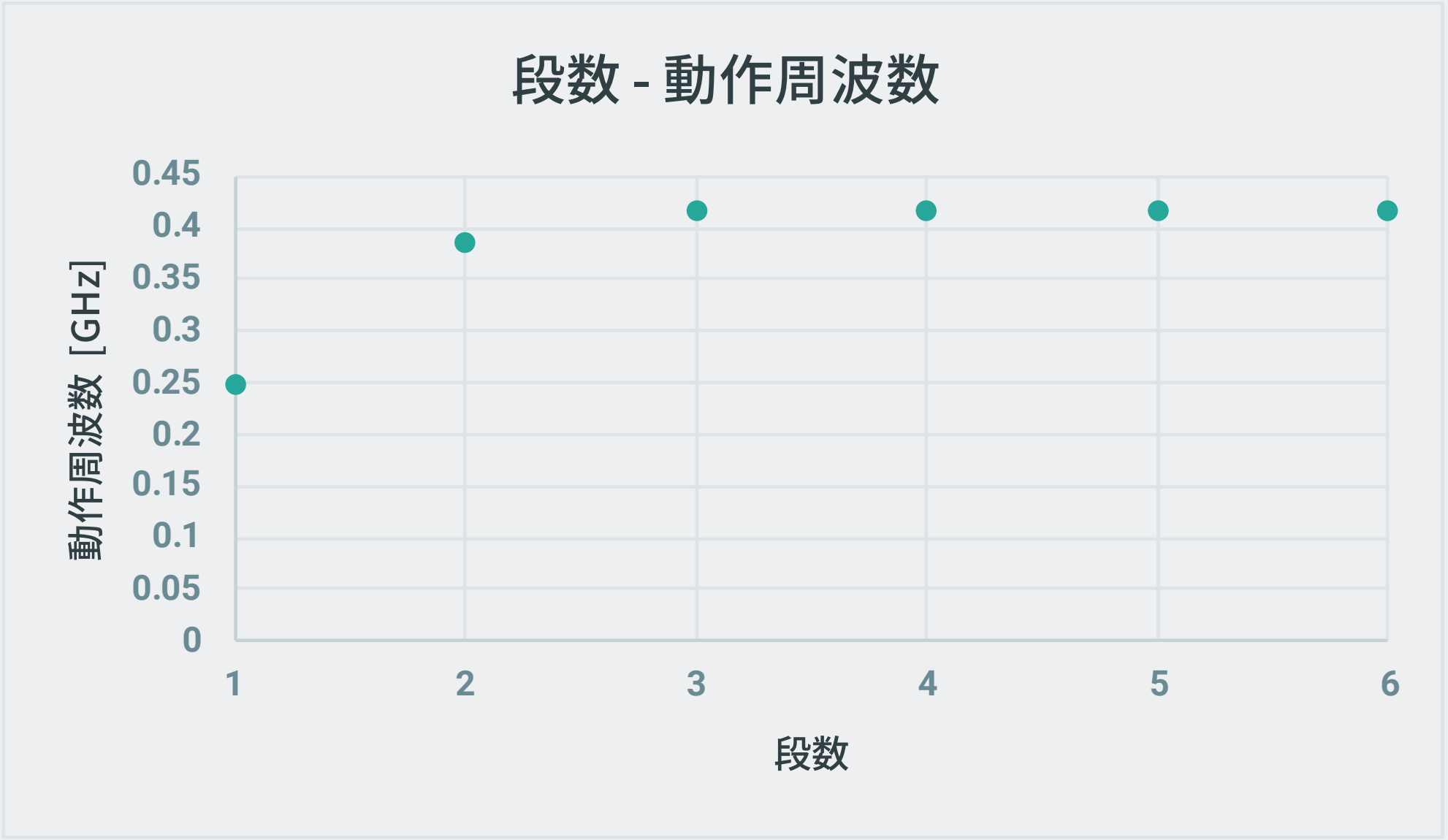
課題3　6段

Clock[ns]	MaxDelay[ns]	Area[um^2]	DynamicPower[mW]	LeakagePower[nW]	Cputime[s]	Energy[pJ]	Gates
20	19.98	291381.35	13.99	328.71	62.20	279.46	22587.70
10	10.00	305635.28	30.59	348.29	72.15	305.93	23692.66
5	5.00	343836.06	72.55	408.71	99.32	362.73	26653.96
4.5	4.50	350087.27	70.08	388.98	88.38	315.37	27138.55
4	4.00	356751.36	81.36	398.65	96.00	325.44	27655.14
3.8	3.80	360841.42	86.23	404.54	99.79	327.67	27972.20
3.6	3.60	365792.72	94.77	411.80	100.08	341.16	28356.02
3.4	3.40	356832.00	96.49	399.58	90.68	328.07	27661.40
3.2	3.20	360151.14	104.29	404.54	90.22	333.73	27918.69
3	3.00	402903.25	115.51	463.67	95.36	346.53	31232.81
2.8	2.80	408873.83	128.72	473.57	96.00	360.42	31695.65
2.6	2.60	414892.81	138.81	485.97	93.37	360.90	32162.23
2.4	2.41	422976.16	155.32	497.18	90.82	374.32	32788.85
2.2	2.41	464983.15	192.75	558.19	88.87	464.53	36045.21
2	2.41	430459.55	162.39	513.34	72.76	391.36	33368.96
1.8	2.78	474227.72	157.81	576.57	172.13	438.70	36761.84
1.6	2.78	490633.12	164.77	609.67	130.85	458.07	38033.58
1.4	2.78	493378.11	178.92	608.15	96.37	497.41	38246.36
1.2	2.78	503219.41	193.87	621.87	154.09	538.97	39009.26
1	2.78	555506.39	220.71	702.63	99.74	613.57	43062.51

遅延が最小のもののうち、ゲート面積が最も小さいものを採用した

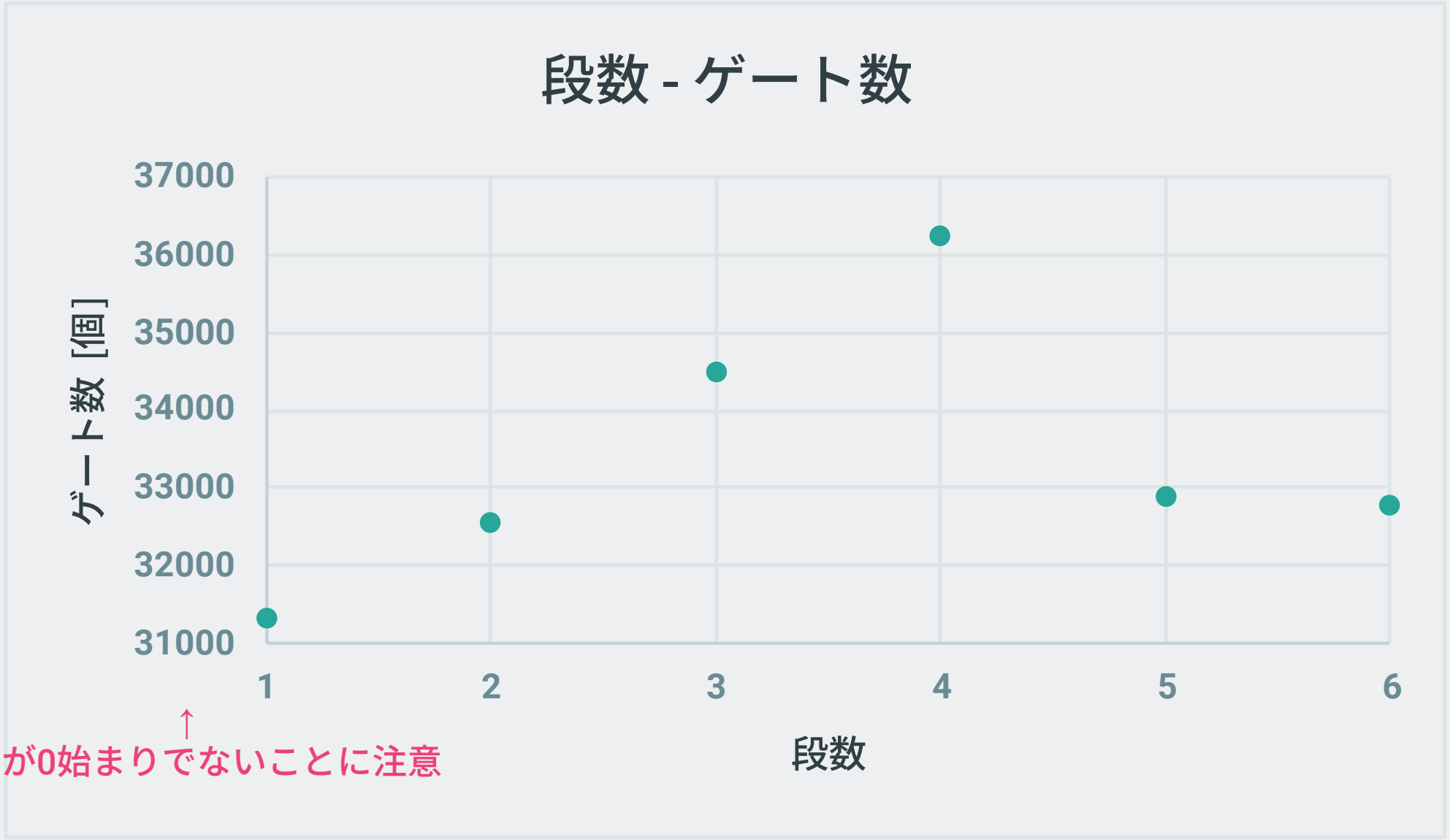
課題3　結果

2段、3段は動作周波数の向上が見られるが
4段以上の差はあまり見られない



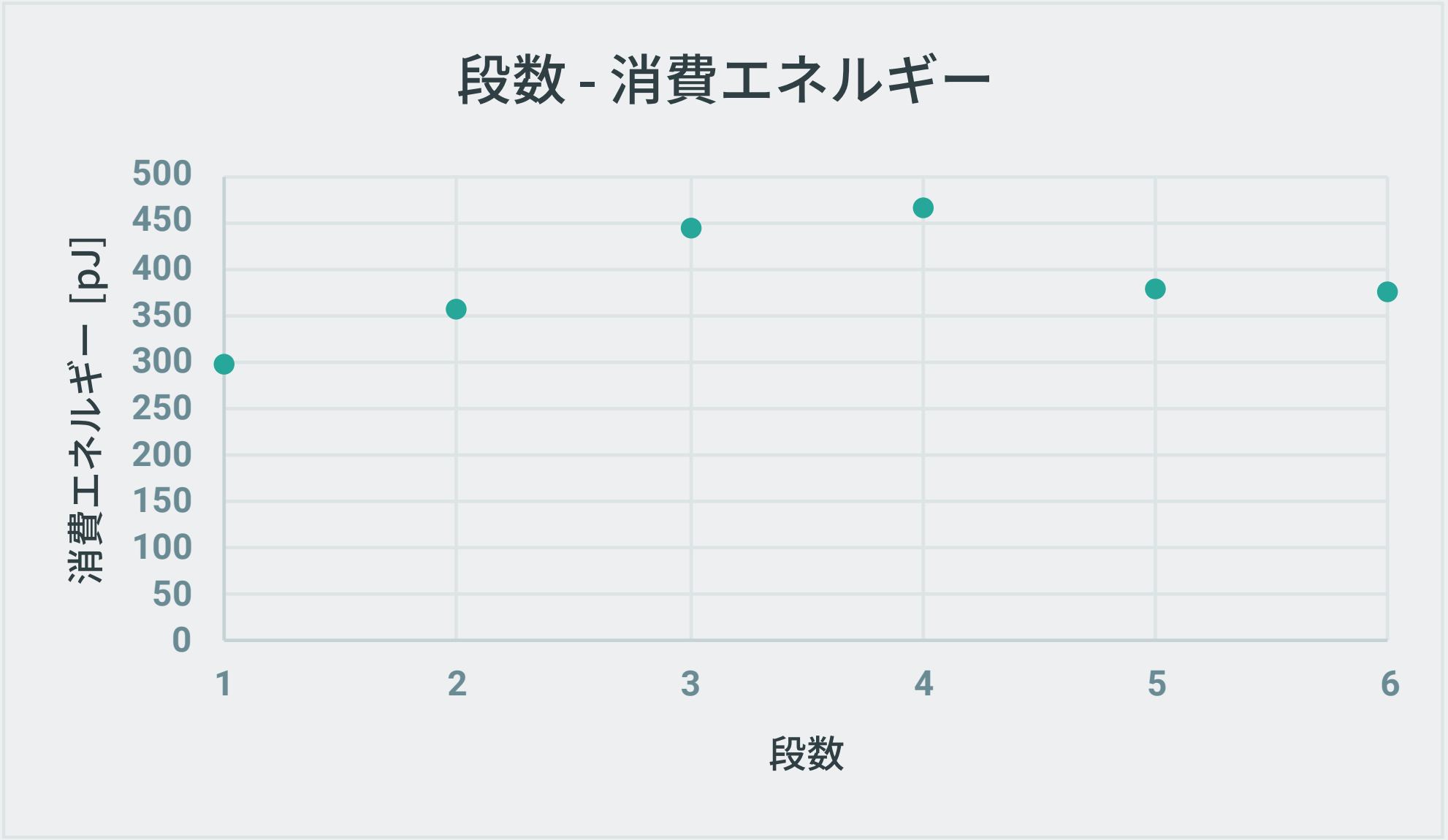
課題3　結果

5段以上になるとゲート数が減少した
→乗算には5サイクルがちょうどよい？



↑
縦軸が0始まりでないことに注意

課題3　結果


段数 - 消費エネルギー
消費エネルギー [pJ]
500
450
400
350
300
250
200
150
100
50
0
1
2
3
4
5
6
段数

課題4　32bit　Clock = 2.6ns

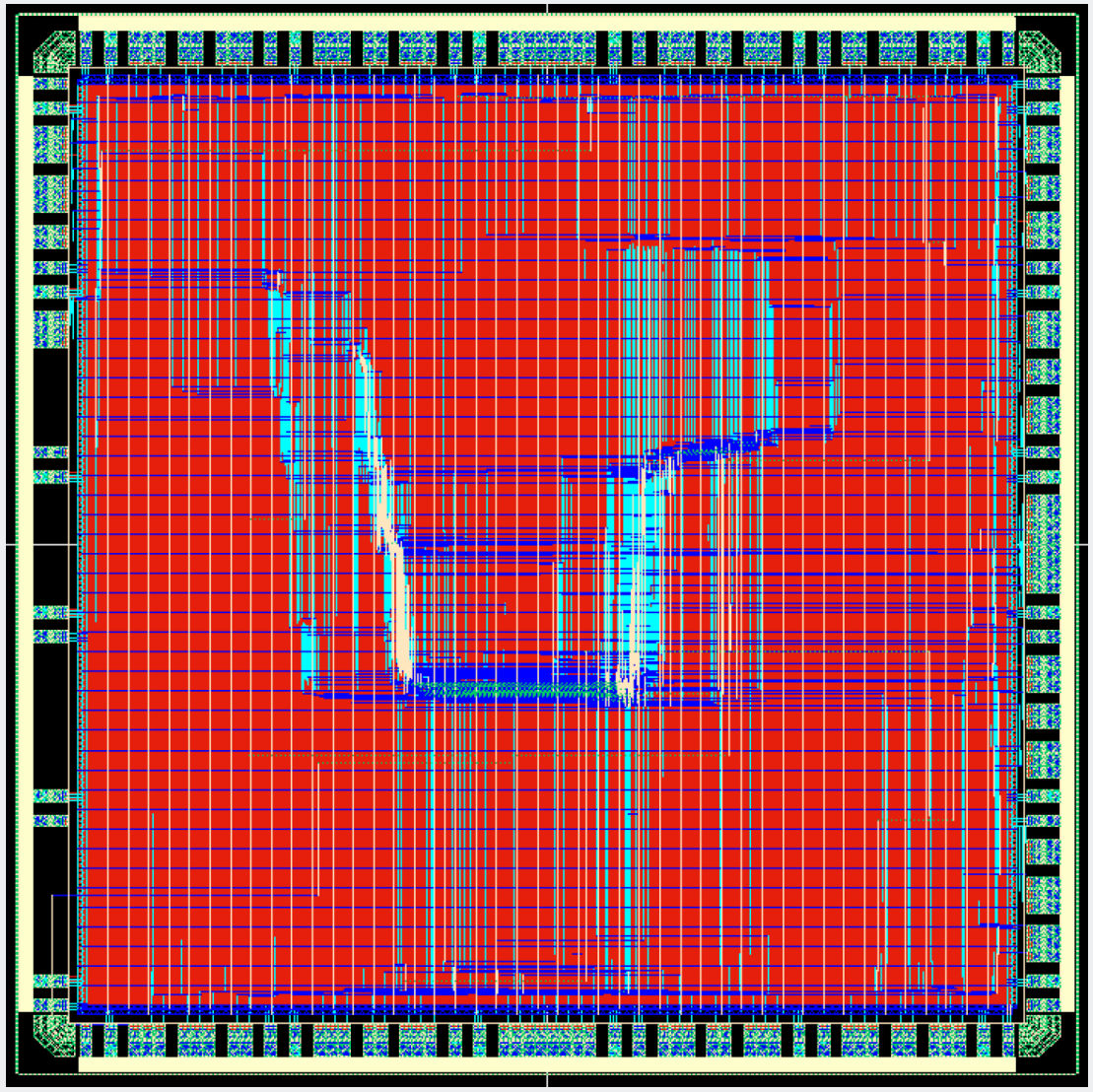
Core	Std Cell Utilization[%]	Total Violation(s)	Slack[ns]	Delay[ns]
0.5	55.56	2	-0.54	3.14
0.55	61.40	1	-0.55	3.15
0.6	68.15	5	-0.55	3.15
0.65	74.37	3	-0.53	3.13
0.7	79.57	4	-0.53	3.13
0.75	82.31	0	-0.54	3.14
0.8	87.31	1	-0.54	3.14
0.85	94.20	1	-0.51	3.11
0.9	96.93	2	-0.53	3.13
0.95	98.50	0	-0.59	3.19
1	98.57	2	-0.67	3.27

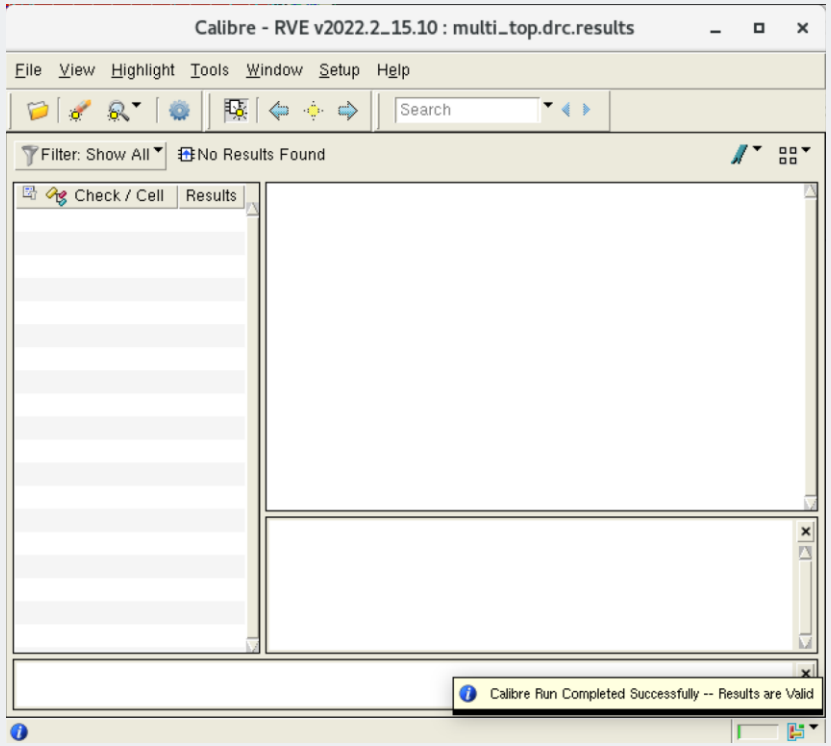
課題5　Core Utilization = 0.75

Clock[ns]	Std Cell Utilization[%]	Total Violation(s)	Slack[ns]	Delay[ns]
20	69.97	0	15.59	4.41
10	69.97	1	5.59	4.41
5	69.97	1	0.63	4.37
4.5	70.16	1	0.36	4.14
4	70.69	1	0.32	3.68
3.8	71.11	1	0.27	3.53
3.6	71.84	3	0.16	3.44
3.4	74.05	2	0.09	3.31
3.2	78.35	3	0.05	3.15
3	84.96	2	-0.10	3.10
2.8	83.43	4	-0.32	3.12
2.6	82.31	0	-0.54	3.14
2.4	83.81	4	-0.73	3.13
2.2	80.84	0	-0.95	3.15
2	84.73	5	-1.11	3.11
1.8	83.98	2	-1.34	3.14
1.6	84.58	2	-1.51	3.11
1.4	83.72	5	-1.70	3.10
1.2	83.58	3	-1.92	3.12
1	83.24	2	-2.13	3.13

最適なクロック制約は変わらなかったが、論理合成時(3.4ns)より遅延が減少

IOレイアウト





そのままではエラーが2つ存在したので
Virtuoso上で若干の修正を加えた