Zihao Yuan

Computer Engineer Ph.D. Candidate

27 August 1992

yuan1z@bu.edu

+1 9895135036

www.yuan-zihao.com,
www.linkedin.com/in/zihao-yuan-b4b718106/

Education

Boston University
Boston, MA
2017-present
Ph.D.: Computer Engineering
Research Advisor: Prof.Ayse K.Coskun

University of Southern California
Los Angeles, CA
2015-2017
Master of Science: Electrical Engineering
GPA: 4.0

Central Michigan University
Mount Pleasant, MI
2012-2015
Bachelor of Science: Electrical Engineering
GPA: 3.83

Skills

Programming Language: Python, Matlab, C++/C, Perl, Verilog, SPICE, HTML, CSS, Javascript

Design Tools: Vivado, Xilinx ISE, Cadence Virtuoso, Synopsis Design Compiler, Cadence Encounter, Synopsis Primetime, Eclipse, Pycharm, Jupyter Notebook, Minitab, PSpice, HSpice, NgSpice, Xyce

Hardware: Arduino, Raspberry-Pi, FPGA, Siemens PLC

Other: MS Office, Git, Latex

Certifications: refer to my Linkedin page

Work Experience

05/18-05/22 Research Assistant — Boston University, MA
Designing next-generation cooling systems and simulation infrastructures for high-performance processors.

01/16-06/16 Grader — University Of Southern California, CA
Graded homework and projects for computer organization class (EE457).

01/13-05/15 Research Assistant — Central Michigan University, MI
Designed a robot navigation and obstacle avoidance system as well as a gesture-controlled UAV system.

01/14-12/14 Teaching Assistant — Central Michigan University, MI
Worked as an undergraduate teaching assistant for Computer Circuit Simulation and Microprocessor Fundamentals classes.

Research and Projects

05/18-05/22 Modeling the Next-Generation Hybrid Cooling Systems for High-Performance Processors (Boston University)
Implemented and analyzed steady-state and transient compact thermal models for several emerging cooling methods, including two-phase vapor chambers (VCs) with micropillar wick evaporators, liquid cooling, two-phase cooling with microchannels, and various hybrid methods.

09/16-05/17 Hardware Stochastic Computing-Based Deep Convolutional Neural Network Design (University of Southern California)
Designed and optimized stochastic computing (SC)-based hardware function blocks for activation functions (hyperbolic tangent, logistic, and rectified linear units), softmax regression, and normalization. Demonstrated on LeNet and AlexNet with the ImageNet and MNIST dataset that the SC-based DCNN achieves low hardware footprints with negligible accuracy loss.

09/16-12/16 Design of a General Purpose Microprocessor Using Software and Hardware Components (University of Southern California)
Designed the schematic and full-custom layout of a MIPS five-stage pipeline CPU with 1KB on-chip memory using Cadence Virtuoso. Demonstrated that the implemented CPU is capable of doing 16 different operations and included additional hardware power gating and data gating methods.

01/17-05/17 Design of a DDR-III Memory controller for an SDRAM (University of Southern California)
Designed a DDR-III memory controller using Verilog and TSMC 45nm library. Synthesized the netlist using Synopsis Design Compiler and generated layouts using Cadence Encounter. Conducted additional static timing analysis (STA) using Synopsis PrimeTime.

01/16-05/16 On-Chip Random Pulse Generator(University of Southern California)
Designed an on-chip random pulse generator (RPG) using CMOS LED, waveguide, and single-photon avalanche diode (SPAD).

09/13-05/14 Semi-Autonomous Gesture Controlled UAV Transportation System(Central Michigan University)
Designed a gesture recognition system on the desktop/laptop computer with the ability to transmit appropriate commands to UAV for safe flight through wireless media. Implemented a wireless communication module to obtain real-time video from the UAV on an office computer.

Zihao Yuan

Computer Engineer Ph.D. Candidate

27 August 1992

yuan1z@bu.edu

+1 9895135036

www.yuan-zihao.com,
www.linkedin.com/in/zihao-yuan-b4b718106/

Education

Boston University
Boston, MA
2017-present
Ph.D.: Computer Engineering
Research Advisor: Prof.Ayse K.Coskun

University of Southern California
Los Angeles, CA
2015-2017
Master of Science: Electrical Engineering
GPA: 4.0

Central Michigan University
Mount Pleasant, MI
2012-2015
Bachelor of Science: Electrical Engineering
GPA: 3.83

Skills

Programming Language: Python, Matlab, C++/C, Perl, Verilog, SPICE, HTML, CSS, Javascript

Design Tools: Vivado, Xilinx ISE, Cadence Virtuoso, Synopsis Design Compiler, Cadence Encounter, Synopsis Primetime, Eclipse, Pycharm, Jupyter Notebook, Minitab, PSpice, HSpice, NgSpice, Xyce

Hardware: Arduino, Raspberry-Pi, FPGA, Siemens PLC

Other: MS Office, Git, Latex

Certifications: refer to my Linkedin page

Publications

1. Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Mostafa Said, Evelyn Wang, Sherief Reda, and Ayse K. Coskun, "A Learning-Based Thermal Simulation Framework for Emerging Two-Phase Cooling Technologies", in Proc. of Design, Automation and Test in Europe (DATE), 2020.
2. Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Mostafa Said, Sherief Reda, Evelyn Wang, and Ayse K. Coskun, "Two-Phase Vapor Chambers with Micropillar Evaporators: A New Approach to Remove Heat from Future High-Performance Chips", in Proc. of 19th IEEE Intersociety Conference on Thermal and Thermomechnanical Phenomena in Electronic Systems (ITHERM), 2019.
3. Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Sherief Reda, Evelyn Wang, and Ayse K. Coskun, "Modeling and Optimization of Chip Cooling with Two-Phase Vapor Chambers", in Proc. of ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2019.
4. Zihao Yuan, Geoffrey Vaartstra, Prachi Shukla, Sherief Reda, Evelyn Wang, and Ayse K. Coskun, "An EDA tool for co-designing high-performance processors and emerging cooling technologies", in Proc. of Workshop on Open-source EDA Technology (WOSET), 2019.
5. Zihao Yuan, Kevin Laubhan, Kumar Yelamarthi, "An Efficient and Dynamic Algorithm for Accurate Mobile Robot Navigation", in Proc. of IEEE International Conference on Electro/Information Technology, 2014.
6. Zihao Yuan, Ji Li, Zhe Li, Caiwen Ding, Ao Ren, Bo Yuan, Qinru Qiu, Jeffrey Draper and Yanzhi Wang, "Softmax Regression Design for Stochastic Computing Based Deep Convolutional Neural Networks", in Proc. of ACM Great Lakes Symposium on VLSI (GLSVLSI), 2017.
7. Ji Li, Zihao Yuan, Zhe Li, Ao Ren, Caiwen Ding, Jeffrey Draper, Shahin Nazarian, Qinru Qiu, Bo Yuan, and Yanzhi Wang, "Normalization and Dropout for Stochastic Computing-Based Deep Convolutional Neural Networks", in Elsevier's Integration, the VLSI Journal, 2018.
8. Ji Li, Zihao Yuan, Zhe Li, Caiwen Ding, Ao Ren, Qinru Qiu, Jeffrey Draper and Yanzhi Wang, "Hardware-Driven Nonlinear Activation for Stochastic Computing Based Deep Convolutional Neural Networks", in Proc. of International Joint Conference on Neural Networks (IJCNN), 2017.
9. Zihao Yuan, Kumar Yelamarthi, "A Dynamically Adapting Indoor Navigation Algorithm for Mobile Robots", in Proc. of American Society for Engineering Education North Central Section Conference, 2014.
10. Andrew Gigowski, Nicholas Martin, Timothy Root, Aaron Yoon, Zihao Yuan, Zhiyu Zhou, Kumar Yelamarthi, "Semi-Autonomous Gesture Controlled UAV Transportation System", in Proc. of American Society for Engineering Education North Central Section Conference, 2015. (All authors contributed equally to this paper.)

Rewards

06/14 Outstanding Paper Award, 2014 IEEE Region 4 Student Paper Contest
Milwaukee, WI

09/12-12/13 Academic Honor: Honor List consecutive semester
Central Michigan University

06/12 Third Prize, NCUT 9th PLC Innovation Design Competition
Beijing, China

06/12 Second Prize, China 6th "Challenge" Cup Science and Academic Competition
Beijing, China

06/19 Outstanding Poster Award, 19th IEEE Intersociety Conference on Thermal and Thermomechnanical Phenomena in Electronic Systems (ITHERM)
Las Vegas, NV

06/19 A. Richard Newton Young Fellowship to attend the 56th Design Automation Conference (DAC)
Las Vegas, NV