Yuanchao Xu

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Education

North Carolina State University *Raleigh, North Carolina, USA*
Ph.D. in Computer Science; Advisors: Prof. Xipeng Shen and Prof. Yan Solihin *Aug. 2018 - Present*

Tsinghua University *Beijing, China*
M.E. in Computer Science; Advisor: Prof. Wei Xue *Aug. 2015 - Jul. 2018*

Jilin University *Changchun, Jilin, China*
B.E. in Software Engineering; Ranking: 3/332 *Aug. 2011 - Jul. 2015*

Research Experience

Computer Science Department, North Carolina State University *Raleigh, NC, USA*

Research Assistant; Advisors: Prof. Xipeng Shen and Prof. Yan Solihin *Aug. 2018 - Present*

- ***Memory Exposure Reduction and Randomization for Persistent Memory Objects (ASPLOS'2020)***
  - Proposed a new approach to reduce memory disclosure/corruption vulnerabilities by reducing memory exposure time using attachment and detachment of a persistent memory object (PMO).
  - Designed a novel hardware support to make attachment/detachment fast by embedding a page table subtree into a PMO.
  - Designed an architecture support for providing process-specific PMO-wide permission.
- ***Hardware Domain Virtualization for Intra-process Isolation of Persistent Memory Objects (ISCA'2020)***
  - Proposed to improve security of PMOs from memory attacks by assigning each attached PMO to a protection domain, providing intra-process isolation of PMOs
  - Designed an architecture support for efficient memory protection key (MPK) virtualization, which supports a large number of domains sharing a limited number of protection keys.
  - Designed an architecture support for domain virtualization, which manages per-thread permission directly on domains, completely removing the mapping of domains to a limited number of keys.
  - Achieved 10X and 52X speedups over the state-of-art MPK virtualization.
- ***Temporal Exposure Reduction-Based Protection for Persistent Memory***
  - Explored and formalizing semantics of temporal exposure reduction protection (TERP).
  - Designed compiler and runtime system support to reduce TERP adoption difficulty
- ***Hardware-Based Address-Centric Acceleration of Key-Value Store (HPCA'2021)***
  - Designed an address-centric accelerator with hardware and software support to reduce address translation overhead in key-value store systems.
  - Leveraged the opportunities on the new tradeoffs between hashing complexities and overhead.

Future Technologies Group, Oak Ridge National Laboratory *Oak Ridge, TN, USA*

Research Assistant; Advisor: Prof. Mehmet E. Belviranli *May. 2019 - Aug. 2019*

- ***Hardware-Centric co-location Performance Modeling on Heterogeneous System-on-chip***
  - Designed a novel processor-centric performance modeling methodology and a new three region interference-conscious performance model
  - Provided memory-interference-aware hardware design insights by integrating our model with standalone bandwidth roofline model
  - Reduced average prediction errors of the state-of-art model from 24.8% to 8.7% on GPU, and from 13.0% to 3.3% on CPU, demonstrating much improved efficacy in guiding SoC designs.

Department of Computer Science, Tsinghua University *Beijing, China*

Research Assistant; Advisor: Prof. Wei Xue *Aug. 2015 - Jul. 2018*

- ***Performance Modeling and Optimization on the Heterogeneous Many-core Processor (IPDPS'2018, SC'16)***
  - Built a purely static performance model of SW26010, the heterogeneous many-core processor that powers Sunway TaihuLight. This model achieves an average accuracy as high as 95% on 17 benchmarks from Rodinia.
  - Designed a static compiler auto-tuning tool based on the performance model. This tool reduces 97% tuning time and achieves nearly optimal optimization (1.6X-3.7X speedup).
  - Designed a memory footprint analysis and code refactoring tool to fit the frequently-accessed variables into scratchpad memory.

Computer Science Department, ETH Zurich *Zurich, Switzerland*

Research Assistant; Advisors: Prof. Torsten Hoefler and Dr. Tobias Grosser *Apr. 2017 - Sep. 2017*

- ***Performance Model Generator***
  - Developed a Domain-specific Language (DSL) based on polyhedral model to generate performance models on different configurations.

Publication

HPCA'2021	ChenCheng Ye, **Yuanchao Xu**, Xipeng Shen, Xiaofei Liao, Hai Jin and Yan Solihin,"Hardware-Based Address-Centric Acceleration of Key-Value Store", 27th IEEE International Symposium on High-Performance Computer Architecture, Seoul, South Korea, February 2021, **Accepted, to appear**
ISCA'2020	**Yuanchao Xu**, ChenCheng Ye, Yan Solihin, Xipeng Shen,"Hardware-Based Domain Virtualization for Intra-Process Isolation of Persistent Memory Objects", 47th ACM/IEEE International Symposium on Computer Architecture, Valencia, Spain, June 2020, **[Paper][Slides]**
ASPLOS'2020	**Yuanchao Xu**, Yan Solihin, Xipeng Shen,"MERR: Improving Security of Persistent Memory Objects via Efficient Memory Exposure Reduction and Randomization", 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland, March 2020. **[Paper][Slides]**
IPDPS'2018	Shizhen Xu, **Yuanchao Xu**, Wei Xue, Xipeng Shen, Xiaomeng Huang, Guangwen Yang. "Taming the "Monster": Overcoming Program Optimization Challenges on SW26010 Through Precise Performance Modeling", 32nd IEEE International Parallel and Distributed Processing Symposium, Vancouver, Canada, May 2018. **[Paper]**

Honors & Awards

2013	**Silver Medal**, ACM-ICPC Asia Regional Programming Contest	*China*
2014	National Scholarships of China (highest scholarship for Chinese undergraduate)	*China*

Skills

Programming Languages:	C, C++, FORTRAN, JAVA, MATLAB
HPC Programming Models:	OpenMP, MPI, CUDA, OpenACC
Frameworks:	TensorRT, LLVM, Spark, Hadoop