# Yuanchao Xu

https://yuanchaoxu6.github.io/ | (+1) 919-884-0400 | yxu47@ncsu.edu

## Education

**North Carolina State University** — *Raleigh, North Carolina, USA*
*Ph.D. in Computer Science; Advisors: Dr. Xipeng Shen and Dr. Yan Solihin* — *Aug. 2018 - Present*

**Tsinghua University** — *Beijing, China*
*M.E. in Computer Science; Advisor: Dr. Wei Xue* — *Aug. 2015 - Jul. 2018*

**Jilin University** — *Changchun, Jilin, China*
*B.E. in Software Engineering; Ranking: 3/332* — *Aug. 2011 - Jul. 2015*

## Research Experience

**Computer Science Department, North Carolina State University** — *Raleigh, NC, USA*
*Research Assistant; Advisors: Dr. Xipeng Shen and Dr. Yan Solihin* — *Aug. 2018 - Present*

- ***Memory Exposure Reduction and Randomization for Persistent Memory Objects (ASPLOS 2020)***
  - Proposed a new approach to reduce memory disclosure/corruption vulnerabilities by reducing memory exposure time using attachment and detachment of a persistent memory object (PMO).
  - Designed a novel hardware support to efficiently attach/detach by embedding a page table subtree into a PMO.
- ***Hardware Domain Virtualization for Intra-process Isolation of Persistent Memory Objects (ISCA 2020)***
  - Proposed to use intra-process isolation to improve security of using PMOs.
  - Designed an architecture support for efficient memory protection key (MPK) virtualization and domain virtualization, achieving 10X and 52X speedups over the state-of-art MPK virtualization.
- ***Temporal Exposure Reduction-Based Protection for Persistent Memory (HPCA 2022)***
  - Explored and formalizing semantics of temporal exposure reduction protection (TERP).
  - Designed compiler and runtime system support to solve TERP adoption challenges
- ***User-transparent Legacy Code Support for Persistent Memory (ISCA 2021)***
  - Designed the sound persistent reference analysis, providing accurate analysis on various pointer manipulations.
  - Designed simple and efficient architecture support to assist pointer distinguishing and manipulation.
- ***Hardware-Based Address-Centric Acceleration of Key-Value Store (HPCA 2021)***
  - Designed an address-centric accelerator with hardware and software support to reduce address translation overhead in key-value store systems.
  - Leveraged the opportunities on the new tradeoffs between hashing complexities and overhead.

**Google** — *Sunnyvale, CA, USA*
*Research Intern & Student Researcher; Mentors: Dr. David E. Culler and Dr. Ravi Rajwar* — *May. 2021 - Present*

- ***Persistent Memory Enabling Transformative System Design Simplification***
  - Designed efficient execution environment to fully utilize low latency durability from persistent memory.
  - Abstracted interfaces from various application durable models to simply port applications by using our execution environment.

**Future Technologies Group, Oak Ridge National Laboratory** — *Oak Ridge, TN, USA*
*Research Intern; Mentor: Dr. Mehmet E. Belviranli* — *May. 2019 - Aug. 2019*

- ***Hardware-Centric co-location Performance Modeling on Heterogeneous System-on-chip (MICRO 2021)***
  - Built the fundamental understanding of memory contention on SoCs.
  - Designed a novel processor-centric performance modeling methodology and a new three region interference-conscious performance model to capture memory contention effects.
  - Predicted accurate memory contention effects, improving 70% accuracy over the state-of-the-art work.

**Computer Science Department, North Carolina State University** — *Raleigh, NC, USA*
*Research Assistant; Advisors: Dr. Xipeng Shen and Dr. Işil Dillig* — *April. 2020 - April. 2021*

- ***Translating UDFs to SQL through Lazy Inductive Synthesis (OOPSLA 2021)***
  - Achieved a good trade-off between expressiveness and scalability using a technique that we dub *lazy inductive synthesis*
  - Implemented our method in a tool and evaluated it on real-world SQL queries with UDFs targeting the Spark system, showing synthesised programs significantly improves performance.

**Department of Computer Science, Tsinghua University** *Beijing, China*

*Research Assistant; Dr. Wei Xue* *Aug. 2015 - Jul. 2018*

- ***Performance Modeling and Optimization on the Heterogeneous Many-core Processor (IPDPS 2018, SC 16)***
  - Built a purely static performance model of SW26010, the heterogeneous many-core processor in Sunway.
  - Designed a compiler auto-tuning tool from the model, reducing 97% tuning time with nearly optimal results.

**Computer Science Department, ETH Zurich** *Zurich, Switzerland*

*Research Assistant; Mentors: Prof. Torsten Hoefler and Dr. Tobias Grosser* *Apr. 2017 - Sep. 2017*

- ***Performance Model Generator***
  - Developed a Domain-specific Language based on polyhedral model to generate performance models

## Publication

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| **ISCA 2022** | **Yuanchao Xu**, Chencheng Ye, Yan Solihin, Xipeng Shen; "FFCCD: Fence-Free Crash-Consistent Concurrent Defragmentation for Persistent Memory"; The 49th ACM/IEEE International Symposium on Computer Architecture, New York City, USA, June 2022. **Accepted, to appear** |
| **HPCA 2022** | **Yuanchao Xu**, Chencheng Ye, Xipeng Shen, and Yan Solihin; "Temporal Exposure Reduction Protection for Persistent Memory"; The 28th IEEE International Symposium on High-Performance Computer Architecture, February 2022. **[Paper]** |
| **MICRO 2021** | **Yuanchao Xu**, Mehmet Esat Belviranili, Xipeng Shen and Jeffrey Vetter; "PCCS: Processor-Centric Contention Slowdown Model for Heterogeneous System-on-chips"; The 54th IEEE/ACM International Symposium on Microarchitecture, Online, October 2021. **[Paper][Slides]** |
| **ICDM 2021** | Hui Guan, Umang Chaudhary, **Yuanchao Xu**, Lin Ning, Lijun Zhang, and Xipeng Shen; "Recurrent Neural Networks Meet Context-Free Grammar: Two Birds with One Stone"; The IEEE International Conference on Data Mining, Online, December 2021. **[Paper]** |
| **OOPSLA 2021** | Guoqiang Zhang, **Yuanchao Xu**, Xipeng Shen, and Işil Dillig; "UDF to SQL Translation through Compositional Lazy Inductive Synthesis"; The ACM SIGPLAN Object Oriented Programming Languages, Systems and Applications, Chicago, Illinois, October 2021. **[Paper]** |
| **ISCA 2021** | Chencheng Ye, **Yuanchao Xu**, Xipeng Shen, Xiaofei Liao, Hai Jin and Yan Solihin; "Supporting Legacy Libraries on Non-Volatile Memory: A User-Transparent Approach"; The 48th ACM/IEEE International Symposium on Computer Architecture, Online, June 2021. **[Paper]** |
| **HPCA 2021** | Chencheng Ye, **Yuanchao Xu**, Xipeng Shen, Xiaofei Liao, Hai Jin and Yan Solihin; "Hardware-Based Address-Centric Acceleration of Key-Value Store"; The 27th IEEE International Symposium on High-Performance Computer Architecture, Seoul, South Korea, February 2021. **[Paper]** |
| **ISCA 2020** | **Yuanchao Xu**, Chencheng Ye, Yan Solihin, Xipeng Shen; "Hardware-Based Domain Virtualization for Intra-Process Isolation of Persistent Memory Objects"; The 47th ACM/IEEE International Symposium on Computer Architecture, Valencia, Spain, June 2020. **[Paper][Slides]** |
| **ASPLOS 2020** | **Yuanchao Xu**, Yan Solihin, Xipeng Shen; "MERR: Improving Security of Persistent Memory Objects via Efficient Memory Exposure Reduction and Randomization"; The 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland, March 2020. **[Paper][Slides]** |
| **IPDPS 2018** | Shizhen Xu, **Yuanchao Xu**, Wei Xue, Xipeng Shen, Xiaomeng Huang, Guangwen Yang; "Taming the "Monster": Overcoming Program Optimization Challenges on SW26010 Through Precise Performance Modeling"; The 32nd IEEE International Parallel and Distributed Processing Symposium, Vancouver, Canada, May 2018. **[Paper]** |

## Honors & Awards

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| 2021 | NCSU Computer Science Outstanding Research Award | *US* |
| 2014 | National Scholarships of China (highest scholarship for Chinese undergraduate) | *China* |
| 2013 | **Silver Medal**, ACM-ICPC Asia Regional Programming Contest | *China* |

## Skills

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| **Programming Languages:** | C, C++, Rust, FORTRAN, Python, JAVA, MATLAB |
| **HPC Programming Models:** | OpenMP, MPI, CUDA, OpenACC |
| **Frameworks:** | TensorRT, LLVM, Spark, Hadoop |
| **Simulator:** | Sniper, Gem5, Ramulator |