Yuanchao Xu

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Education

North Carolina State University — *Raleigh, North Carolina, USA*
Ph.D. in Computer Science; Advisors: Dr. Xipeng Shen and Dr. Yan Solihin — *Aug. 2018 - Present*

Tsinghua University — *Beijing, China*
M.E. in Computer Science; Advisor: Dr. Wei Xue — *Aug. 2015 - Jul. 2018*

Jilin University — *Changchun, Jilin, China*
B.E. in Software Engineering; Ranking: 3/332 — *Aug. 2011 - Jul. 2015*

Research Experience

Computer Science Department, North Carolina State University — *Raleigh, NC, USA*
Research Assistant; Advisors: Dr. Xipeng Shen and Dr. Yan Solihin — *Aug. 2018 - Present*

- ***Memory Exposure Reduction and Randomization for Persistent Memory Objects (ASPLOS 2020)***
  - Proposed a new approach to reduce memory disclosure/corruption vulnerabilities by reducing memory exposure time using attachment and detachment of a persistent memory object (PMO).
  - Designed a novel hardware support to efficiently attach/detach by embedding a page table subtree into a PMO.
  - Designed an architecture support for providing process-specific PMO-wide permission.
- ***Hardware Domain Virtualization for Intra-process Isolation of Persistent Memory Objects (ISCA 2020)***
  - Proposed to improve security of PMOs from memory attacks by assigning each attached PMO to a protection domain, providing intra-process isolation of PMOs
  - Designed an architecture support for efficient memory protection key (MPK) virtualization, which supports a large number of domains sharing a limited number of protection keys.
  - Designed an architecture support for domain virtualization, which manages per-thread permission directly on domains, completely removing the mapping of domains to a limited number of keys.
- ***Temporal Exposure Reduction-Based Protection for Persistent Memory (HPCA 2022)***
  - Explored and formalizing semantics of temporal exposure reduction protection (TERP).
  - Designed compiler and runtime system support to reduce TERP adoption difficulty
- ***User-transparent Legacy Code Support for Persistent Memory (ISCA 2021)***
  - Designed the sound persistent reference analysis, providing accurate analysis on various pointer manipulations.
  - Designed simple and efficient architecture support to assist pointer distinguishing and manipulation.
- ***Hardware-Based Address-Centric Acceleration of Key-Value Store (HPCA 2021)***
  - Designed an address-centric accelerator with hardware and software support to reduce address translation overhead in key-value store systems.
  - Leveraged the opportunities on the new tradeoffs between hashing complexities and overhead.

Google — *Sunnyvale, CA, USA*
Research Intern & Student Researcher; Mentors: Dr. David E. Culler and Dr. Ravi Rajwar — *May. 2021 - Present*

- ***Persistent Memory Enabling Transformative System Sesign Simplification***
  - Designed efficient execution environment to fully utilize low latency durability from persistent memory.
  - Abstracted interfaces from various application durable models to simply port applications by using our execution environment.

Future Technologies Group, Oak Ridge National Laboratory — *Oak Ridge, TN, USA*
Research Assistant; Mentor: Dr. Mehmet E. Belviranli — *May. 2019 - Aug. 2019*

- ***Hardware-Centric co-location Performance Modeling on Heterogeneous System-on-chip (MICRO 2021)***
  - Designed a novel processor-centric performance modeling methodology and a new three region interference-conscious performance model
  - Provided memory-interference-aware hardware design space exploration
  - Reduced average prediction errors of the state-of-art model from 24.8% to 8.7% on GPU, and from 13.0% to 3.3% on CPU, demonstrating much improved efficacy in guiding SoC designs.

Computer Science Department, North Carolina State University *Raleigh, NC, USA*

Research Assistant; Advisors: Dr. Xipeng Shen and Dr. Işil Dillig *April. 2020 - April. 2021*

- ***Translating UDFs to SQL through Lazy Inductive Synthesis (OOPSLA 2021)***
  - Achieved a good trade-off between expressiveness and scalability using a technique that we dub *lazy inductive synthesis*
  - Implemented our method in a tool and evaluated it on real-world SQL queries with UDFs targeting the Spark system. This tool is effective at translating UDFs to SQL expressions and significantly improves performance.

Department of Computer Science, Tsinghua University *Beijing, China*

Research Assistant; Dr. Wei Xue *Aug. 2015 - Jul. 2018*

- ***Performance Modeling and Optimization on the Heterogeneous Many-core Processor (IPDPS 2018, SC 16)***
  - Built a purely static performance model of SW26010, the heterogeneous many-core processor that powers Sunway TaihuLight. This model achieves an average accuracy as high as 95% on 17 benchmarks from Rodinia.
  - Designed a static compiler auto-tuning tool based on the performance model. This tool reduces 97% tuning time and achieves nearly optimal optimization (1.6X-3.7X speedup).

Computer Science Department, ETH Zurich *Zurich, Switzerland*

Research Assistant; Mentors: Prof. Torsten Hoefler and Dr. Tobias Grosser *Apr. 2017 - Sep. 2017*

- ***Performance Model Generator***
  - Developed a Domain-specific Language based on polyhedral model to generate performance models

Publication

HPCA 2022	**Yuanchao Xu**, Chencheng Ye, Xipeng Shen, and Yan Solihin; "Temporal Exposure Reduction Protection for Persistent Memory"; The 28th IEEE International Symposium on High-Performance Computer Architecture, February 2022. **Accepted, to appear**
MICRO 2021	**Yuanchao Xu**, Mehmet Esat Belviranili, Xipeng Shen and Jeffrey Vetter; "PCCS: Processor-Centric Contention Slowdown Model for Heterogeneous System-on-chips"; The 54th IEEE/ACM International Symposium on Microarchitecture, Online, October 2021. **[Paper][Slides]**
OOPSLA 2021	Guoqiang Zhang, **Yuanchao Xu**, Xipeng Shen, and Işil Dillig; "UDF to SQL Translation through Compositional Lazy Inductive Synthesis"; The ACM SIGPLAN Object Oriented Programming Languages, Systems and Applications, Chicago, Illinois, October 2021. **[Paper]**
ISCA 2021	ChenCheng Ye, **Yuanchao Xu**, Xipeng Shen, Xiaofei Liao, Hai Jin and Yan Solihin; "Supporting Legacy Libraries on Non-Volatile Memory: A User-Transparent Approach"; The 48th ACM/IEEE International Symposium on Computer Architecture, Online, June 2021. **[Paper]**
HPCA 2021	ChenCheng Ye, **Yuanchao Xu**, Xipeng Shen, Xiaofei Liao, Hai Jin and Yan Solihin; "Hardware-Based Address-Centric Acceleration of Key-Value Store"; The 27th IEEE International Symposium on High-Performance Computer Architecture, Seoul, South Korea, February 2021. **[Paper]**
ISCA 2020	**Yuanchao Xu**, ChenCheng Ye, Yan Solihin, Xipeng Shen; "Hardware-Based Domain Virtualization for Intra-Process Isolation of Persistent Memory Objects"; The 47th ACM/IEEE International Symposium on Computer Architecture, Valencia, Spain, June 2020. **[Paper][Slides]**
ASPLOS 2020	**Yuanchao Xu**, Yan Solihin, Xipeng Shen; "MERR: Improving Security of Persistent Memory Objects via Efficient Memory Exposure Reduction and Randomization"; The 25th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland, March 2020. **[Paper][Slides]**
IPDPS 2018	Shizhen Xu, **Yuanchao Xu**, Wei Xue, Xipeng Shen, Xiaomeng Huang, Guangwen Yang; "Taming the "Monster": Overcoming Program Optimization Challenges on SW26010 Through Precise Performance Modeling"; The 32nd IEEE International Parallel and Distributed Processing Symposium, Vancouver, Canada, May 2018. **[Paper]**

Honors & Awards

2021	NCSU Computer Science Outstanding Research Award	*US*
2014	National Scholarships of China (highest scholarship for Chinese undergraduate)	*China*
2013	**Silver Medal**, ACM-ICPC Asia Regional Programming Contest	*China*

Skills

Programming Languages:	C, C++, Rust, FORTRAN, JAVA, MATLAB
HPC Programming Models:	OpenMP, MPI, CUDA, OpenACC
Frameworks:	TensorRT, LLVM, Spark, Hadoop
Simulator:	Sniper, Gem5, Ramulator