YUAN-CHUN LUO

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RESEARCH INTEREST

Nanoelectronics

EDUCATION

National Tsing Hua University (NTHU), Hsinchu, Taiwan *Sep. 2014 - Jun. 2018*
B.S., Electrical Engineering (EE) Overall GPA: 4.07/4.3 (3.93/4)

EXPERIENCE

Purdue University - ALD Group West Lafayette, IN
Visiting Student *Oct. 2018 - present*

- Advisor: Professor Peide(Peter) Ye
- Apply germanium ferroelectric nanowire FETs as analog memories.

National Chiao Tung University (NCTU), DSML Group Hsinchu, Taiwan
Research Assistant *Dec. 2017 - Sep. 2018*

- Advisor: Professor Steve S. Chung
- Measured mobility and free energy in Ferroelectric FETs (FeFET) (submitted to VLSI-TSA'19)
- Extracted negative capacitance values, and minimize hysteresis in FeFETs (SSDM'18) (submitted to APL).
- Verified RF characteristics for FinFETs using the simulation tool, TCAD.

NTHU - THz Optoelectronic Devices Lab Hsinchu, Taiwan
Research Assistant *Jun. 2017 - Jun. 2018*

- Advisor: Professor Shang-Hua Yang
- Designed THz plasmonic photomixers and antenna arrays using COMSOL and MATLAB.

NTHU - SSD LAB Hsinchu, Taiwan
Research Assistant *Sep. 2016 - Aug. 2017*

- Advisor: Professor Ren-Shuo Liu.
- Achieved adaptive Convolutional Neural Networks using Python (VLSI-DAT'18).

PUBLICATION

An Experimental Method of Negative Capacitance(NC) Extraction in NC-gated-FinFET and Obtainment of near-free-Hysteresis Characteristics by Body Effects

- **Y. C. Luo**, E. R. Hsieh, C. J. Su, S. S. Chung, T. P. Chen, S. A. Huang, T. J. Chen, and O. Cheng; *Applied Physics Letter (Submitted)*

The Guideline on Designing a High-Performance NC MOSFET by Matching the Gate Capacitance and Mobility Enhancement

- **Y. C. Luo**, F. L. Li, E. R. Hsieh, C. H. Liu, S. S. Chung, T. P. Chen, S. A. Huang, T. J. Chen, and O. Cheng; *2019 VLSI-TSA (Submitted)*

New Experimental Approaches to Extracting Negative Capacitances of 14nm NC-FinFET in Exploration of Short-channel & Body Effect to Achieve Free Hysteresis.

- **Y.-C. Luo**, E. R. Hsieh, C. J. Su, S. S. Chung, T. P. Chen, S. A. Huang, T. J. Chen, and O. Cheng; *2018 SSDM Late News (Accepted, oral presentation)*

DrowsyNET: Convolutional Neural Networks with Runtime Power-Accuracy Tunability Using Inference-Stage Dropout.

· R. S. Liu, Y. C. Lo, **Y.-C. Luo**, C. Y. Shen, and C. J. Lee; *2018 VLSI-DAT (Accepted, oral presentation)*

SELECTED HONOR AND AWARD

Champion, Contest of implementation with more than 100 student competitors. *EE, NTHU, 2018*

Runner up, Contest of implementation with more than 250 student competitors. *EECS, NTHU, 2018*

Excellent-EECS student award for top 10% of all students. *EECS, NTHU, 2017*

Oversea exchange student scholarship with USD 3100. *EE, NTHU, 2016*

Outstanding academic achievement for top 5% of all students. *EE, NTHU, 2015*

LEADERSHIP & TEAMWORK

President, Student Association *Jun. 2016 - Jun. 2017*
EE, NTHU

· Built a 20-student team to receive students and an advisor from City University of Hong Kong.
· Organized Christmas party for more than 200 students from four different departments.

RELEVANT COURSES

Core Courses	**Other Courses**
ULSI Technology (A+, graduate level, nano-fabrication)	Data Structure (A+)
Semiconductor Microwave Devices (A+, graduate level)	Electromagnetic Waves (A+)
Introduction to Solid-State Physics (A+)	Feedback Control Systems (A+)
Introduction to Solid-State Electronic Devices (A+)	Computer Architecture (A+)
Introduction to Integrated Circuit Design (A+)	Modern Physics (A+)

SKILL

GRE score	331/340 (Q:170/170, V:161/170)
TOEFL score	105/120 (R:29/30, L:29/30, S:22/30, W:25/30)
Software Languages	C++, Matlab, and Python
Hardware Languages	Verilog, Hspice, and Laker
Simulation Tools	COMSOL Multiphysics, and TCAD

SELECTED COURSE PROJECT

VLSI, Memory System Circuit Design Project *Jun. 2016*
EE, NTHU

· Completed circuit design, pre-sim, layout, and post-sim of a memory system.

Semiconductor Microwave Electronic Devices, Term Paper *Jun. 2016*
EE, NTHU

· Investigated into silicon based RF semiconductor devices.