

# Yuanpeng Zhang

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## EDUCATION

### Carnegie Mellon University

Master of Science in Electrical and Computer Engineering

Dec 2024

**Graduate Level Coursework:** Analog Integrated Circuit Design, Board-Level RF Systems for IoT, Intro to Machine Learning, Advanced Analog Integrated Circuit Design, Advanced Digital Integrated Circuit Design, Digital Integrated Circuit Design, Design, Integration, and Tapeout of IoT Systems

### Binghamton University, State University of New York

Bachelor of Science in Computer Engineering

May 2023

**Graduate Level Coursework:** Digital Signal Processing, Embedded Systems Design, Systems on a Chip Design

## TECHNICAL SKILLS

### Advanced:

C, MATLAB, Python, Cadence Virtuoso, Microsoft Office Suite, LT-Spice, Oscilloscopes

### Intermediate:

Ansys HFSS, Linux, Bash, FPGA, UXM 5G Callbox, Soldering, SystemVerilog, GitHub

### Basic:

Assembly, Tcl, Q#, Arduino, VHDL, Solid Edge, Xilinx Vivado, Vitis, Verilog-A, CAD Modeling

## WORK EXPERIENCE

### Baseband/RF Cellular Hardware Intern, Apple

Jun 2024 – Aug 2024

- Performed hands-on hardware bring-up of baseband and RF boards in standalone and PCIe configurations
- Performed 5G phone call simulations using a UXM 5G callbox with patterns that reflect 5G communication protocols used in various worldwide regions
- Developed Python scripts to automate current and power measurements of 5G signal bands for a cellular chipset using an ADC and sampling resistors
- Investigated high-risk current draws and power nets using FFT analysis in MATLAB and provided results for cross-functional teams to drive improvements for future iterations

### Graduate Research Assistant, Analog Circuit Design, Carnegie Mellon University

Sep 2023 – May 2024

- Collaborated with a team of 6 in Prof. Rick Carley's FLOCI lab to design an improved FMR nano-particle interferometer in the TSMC 28nm process, spearheading research on future memory technologies
- Designed and laid out a low impedance pseudo-differential output driver using Cadence tools, reducing area by 60% and passing all post-layout specifications
- Designed and simulated Q factor optimized RF inductors using Ansys HFSS for further use in the development and testing of RF integrated systems

## ACADEMIC AND PERSONAL PROJECTS

### 5V to 3.3V LDO Project, Personal Project

Feb 2025 – Jun 2025

- Designed an LDO in the Cadence 45nm GPDK capable of providing low stable power for other electronic devices
- Created a bandgap reference to output a stable bias voltage independent of temperature with hand calculations and iteration and a high gain low power OTA using gm/ld design to pass PSRR and power specifications

### Mixed-Signal DAC-ADC Pixel Image Sensor Chip Project, Carnegie Mellon University

Aug 2024 – Dec 2024

- Taped out a 3x5 pixel image sensor chip for IoT systems applications in the TSMC 65nm process
- Designed a current steering DAC and a pulse-counting ADC to process incoming digital signals using gm/ld design and hand analysis, meeting all post-layout specifications
- Successfully completed layout of the chip with minimized parasitics and mismatch and conducted full-chip integration using the Cadence Innovus digital-on-top integration flow

### High Bandwidth Operational Amplifier Design Project, Carnegie Mellon University

Nov 2023 – Dec 2023

- Designed a 2-stage high bandwidth operational amplifier with compensation using the Cadence 45nm GPDK using gm/ld design, meeting all specifications
- Successfully completed layout of the circuit with no DRC and LVS errors and performed Monte Carlo Analysis to analyze chip failure rates in all process, voltage, and temperature corners, meeting 95% of sampling points