

Some Notes for simulation with Quartus 17.1 and DE1-SoC

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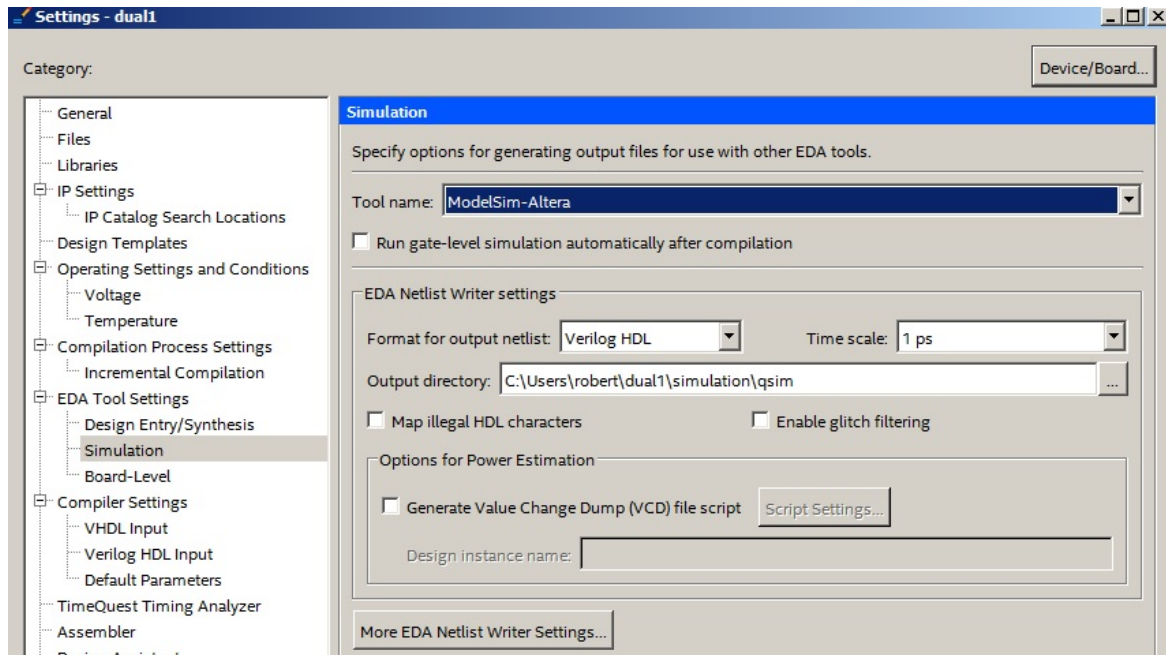
Requirements to simulate a Quartus project:

1. Before simulation, the Quartus project needs to be successfully compiled.
2. Make sure Quartus settings, especially the settings for EDA tools, are correct.
3. Create a new input waveform file, or open an existing input waveform file.
4. In the “Simulation Waveform Editor” window, make sure the settings are correct. Then click “Simulation | Run Functional Simulation”.

PLEASE NOTE: Timing simulations are not supported by Cyclone V for Quartus version 17.0 (and 17.1). For DE1-SoC boards, with Quartus 17.1, timing simulation will give the same simulation result as the functional simulation.

Quartus EDA tools settings for doing simulation using ModelSim_Altera :

1. In Quartus Prime, click “Assignment | Settings...”. From the “Category” window, select “Simulation” under the “EDA Tool Settings” category. In the right side panel, select and set the “Tool Name” to “ModelSim-Altera”. Set the “Format for output netlist” as “Verilog HDL”. For the “Output directory”, browse and set it to:
“YOUR PROJECT FOLDER/simulation/qsim/”. Then click “Apply” and “OK” to close the setting window.



2. In Quartus Prime, go to Tools | Options | ..., then select EDA Tools Options.

At the right side of the window, set the correct path for “ModelSim_Altera”.

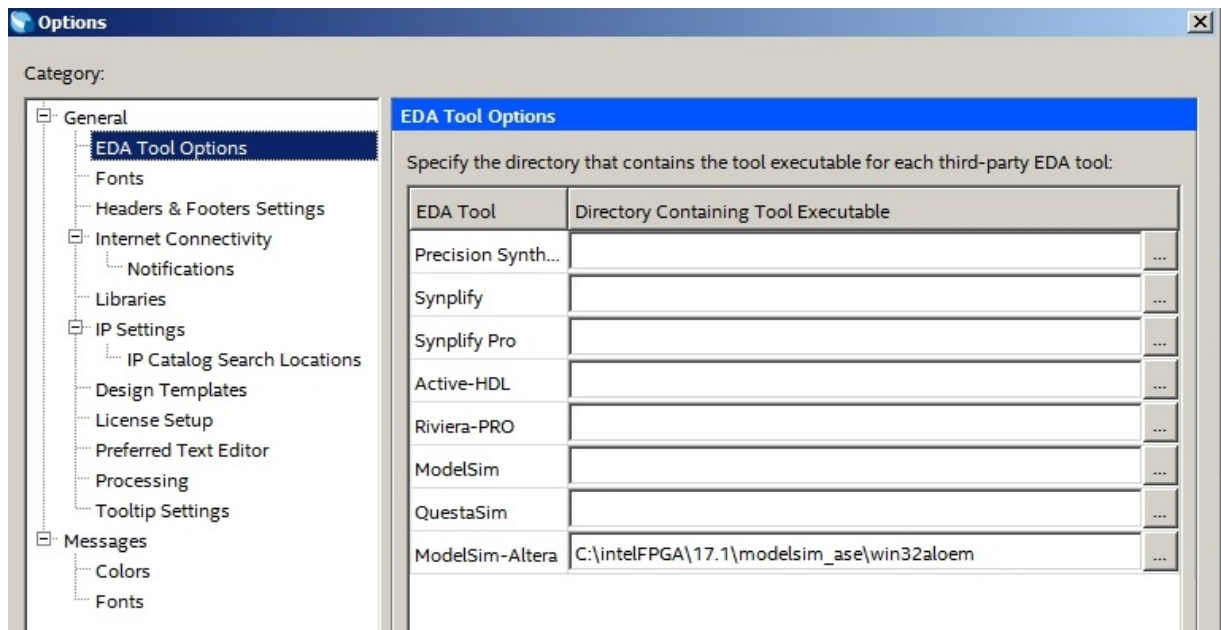
Depending on where the Quartus and Modelsim_Altera are installed, the path may look like: “C:\intelFPGA\17.1\modelsim_ase\win32aloem”

Or:

“C:\intelFPGA\17.1\modelsim_ae\win32aloem”

The folder “modelsim_ase” is for Modelsim ASE (Altera Starter Edition).
The folder “modelsim_ae” is for Modelsim AE (Altera Edition).

Modelsim ASE (Altera Starter Edition) does not require a license (It is FREE). Since our lab does not have a license for Modelsim Altera Edition, at this step, **please choose the folder “...\modelsim_ase\win32aloem”.**



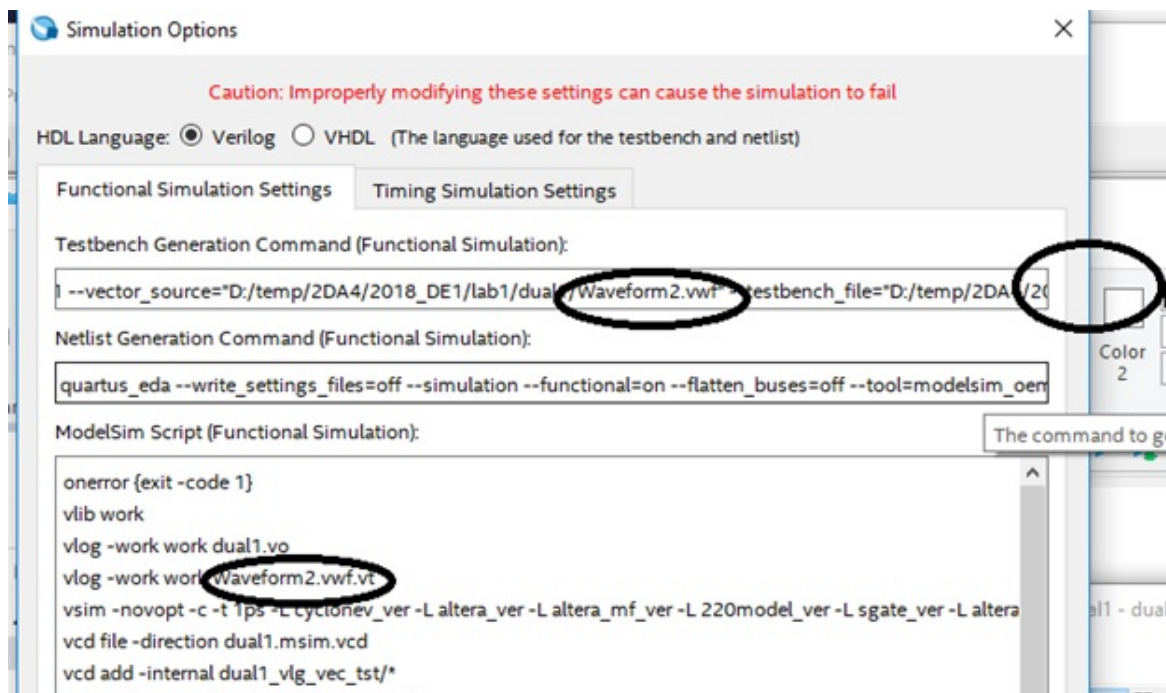
Create a new input waveform file:

1. In Quartus, click File | New..., then select file type "University Program VWF". This will open the "Simulation Waveform Editor".
2. In "Simulation Waveform Editor", click Edit | Insert | Insert Node or Bus
3. In the opened "Insert Node or Bus" window, click "Node Finder..."
4. In the "Node Finder" window, choose the appropriate Filter, then click "List".
5. Select the desired Nodes. Then click "OK". Then click "OK" again to insert the node or bus.
6. Save the input waveform file.

Simulation Waveform Editor settings for functional simulation:

1. If simulation failed, please go to "Simulation Waveform Editor" window, and click "Simulation | Simulation Settings".
2. Select tab "Functional Simulation Settings" (as we can only do functional simulation for DE1-SoC with Quartus 17.1).
3. Click button "Restore Defaults" at the bottom of the window. Typically this can fix the setting problems.

4. If the simulation still fails, please check the “Testbench Generation Command” box . At the end of the command, the path and the folder for the “—testbench_file=” should be “YOUR PROJECT FOLDER/simulation/qsim/”, which is set in Quartus for the simulation output directory. If not, manually change the path and folder for “—testbench_file=”.
5. Also, in the “Testbench Generation Command” box , check the “—vector-source-...” section and “—testbench-file=...” section to make sure the file names are the name of you current input waveform file’s name. Check the “Modelsim Script(Functional Simulation)” box, make sure on the “vlog —work work XXX.vwf.vt” line, that XXX is also your current input waveform file name. ModelSim tends to use “Waveform” as the default name for its input and output file names. If your input waveform file name is not “Waveform.vwf”, the simulation may fail.



6. Click “Save” to close the Simulation Settings window.