1. What is the **reg** data type and what is the **wire** data type in Verilog?

**reg** stands for registers datatype, it stores values from assignment to another. It is by default a 1-bit unsigned value.

**wire** stands for physical connections between structural identities. It doesn’t store values.

1. Can the **wire** data type be used on the left side of the assignment statement in a procedural block?

**wire** can be only used on the left-hand side of a continuous assignment and often declared as an input.

1. What are the rules for module port connection?

**Inputs:** internally must always be of type net, externally the inputs can be connected to a variable of type reg or net.

**Outputs:** internally can be of type net or reg. externally, can be of datatype or net type net.

**Inouts:** internally or externally must always be type net

1. What is continuous assignment, blocking assignment and nonblocking assignment?

**Continuous Assignment:** continuous assignment drives a value into a net. It is declared outside of procedural blocks.

**Blocking Assignment:** executed before the execution of the statements that follow it in a sequential block. The operator is “=”

**Nonblocking Assignment:** it allows us to assign values without blocking the procedural flow. The operator is “<=”.

1. What is the difference in procedural coding when implementing combinational logic and sequential logic?

**Combinational logic** is time independent, and logic does not depend on the previous inputs.

**Sequential logic** is dependent on the clock cycles and the output depends on present as well as past inputs.

1. How does one avoid inferred latches when using Verilog to describe circuits?
2. Include all the branches of an if or case statement
3. Assign a value to every output signal in every branch.
4. Use default assignment at the start of the procedure, so every signal will be assigned.
5. What is the difference between the operators “<<” and “<<<”?

<< is binary logical shift, and <<< is arithmetic left shift.

1. How to declare an array of 6 elements of a 7-bit wire?

reg[6:0] x[5:0]; //x is the array with 6 element of a 7-bit wire.