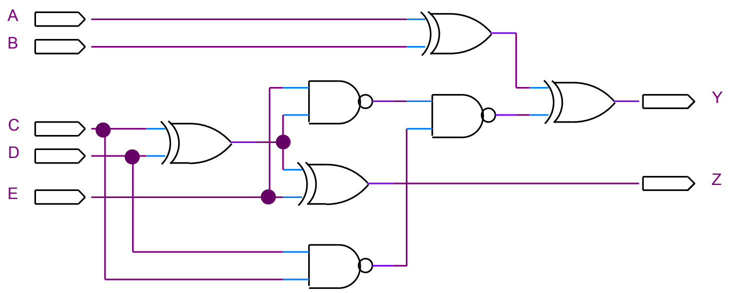
Final Exam 7.1.15

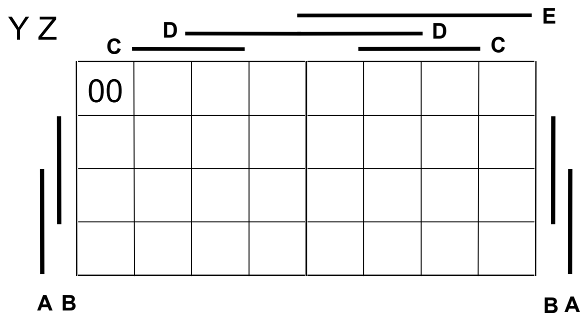
Logic Systems And Processors (České Vysoké Učení Technické v Praze)

Surname and Given name:...

7.1.2015-write here only your anwers

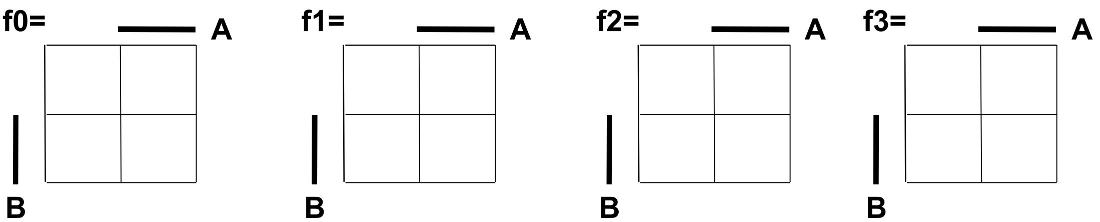
1. *You see this unnamed scheme.. Create its truth table. Write outputs Y Z into the one Karnaugh's map as two bit group in Y Z. order*





2. Decompose Q:=f(A,B,C,D) := (A or B) and (((A and not B) xor (D and not A)) or (C and not D));

function to the form Q=$\bar{C}$.$\bar{D}$.f0(A,B) + $\bar{C}$.D.f1(A,B) + C.$\bar{D}$.f2(A,B) + C.D.f3(A,B) with the aid of *Shannon's decomposition. Write f0, f1, f2 a f3 functions as Karnaugh's maps*:



3. Mark all function below that have another equal function here.

f1<=(A xor C) or (A and not C); f1 ☐
f2<=(B or C) and (not A or B or C); f2 ☐
f3<=((C and not B) or (B and A)); f3 ☐
f4<=(A or C) and (not A or not C); f4 ☐
f5<=(A and not B) xor (A and C); f5 ☐
f6<=(A and not C) or (C and not A); f6 ☐

4. Inputs A, B, C have values shown in the figure in times t_0, t_1, t_2, t_3 . Write values of X and Y outputs. Assume that the intervals between changes in the inputs are so long so we can neglect delays of gates.

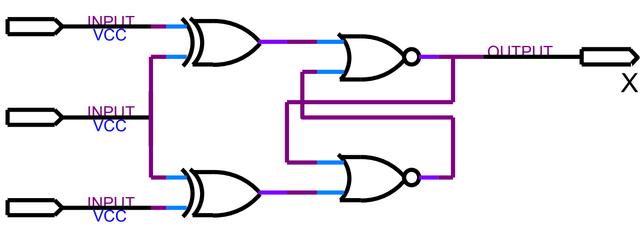
A = ..0..|..1..|..1..|..1..|

t_0..|..t_1..|.. t_2..|..t_3..|..

B = ..0..|..0..|..0..|..1..|

t_0..|..t_1..|.. t_2..|..t_3..|..

C = ..1..|..1..|..0..|..0..|

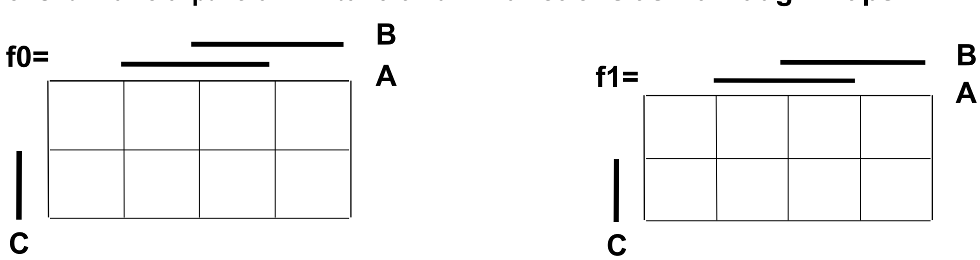


X = ...|.......|.......|.......|

t_0..|..t_1..|..t_2..|..t_3..|..

5

5. Function X=f(A,B,C, X) from question 4, decompose into X= (not X and f0(A, B,C)) or (X and f1(A,B,C)) with the aid of **Shannon's expansion. Write f0 and f1 functions as Karnaugh maps:**



f0/3

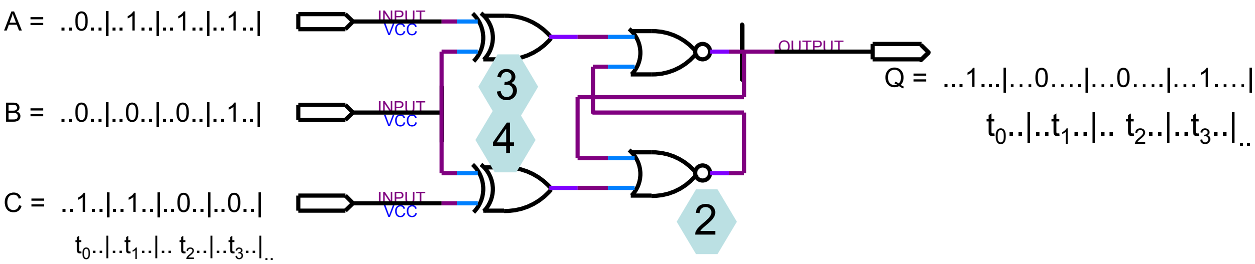
f1/3

Do not write here

6. *Add missing parts of VHDL program to create 100 bit shift register, i.e.,* ***q*** *output of the shift register is* ***d*** *input delayed by 100 clock pulses of* ***clk*** *signal. The register is cleared by synchronous signal* ***sclrn****='0'. Use shortest possible code. (Hint. The shortest code does not contain loops).*

library IEEE; use IEEE.STD_LOGIC_1164.all;

entity pos100 is port (**clock, d, sclrn** : in std_logic; **q**: out std_logic) end pos100;



f0 := f(A,B,C,'0') := (A ≡ B) . ('0' + (B ≠ C)) := (A ≡ B) . ('0' + (B ≠ C)):= **(A ≡ B)** . **(B ≠ C)**

f1 := f(A,B,C,'1') := (A ≡ B) . ('1' + (B ≠ C)) := (A ≡ B) . '1' := **(A ≡ B)**

*Obě nalezené funkce f0:=***(A ≡ B)** . **(B ≠ C)** a *f1:=***(A ≡ B)** *zapíšeme jako Karnoughovy mapy*

f0=

A
B

0	0	**1**	0
1	0	0	0

C

(B ≠ C)

(A ≡ B)

f1=

A
B

1	0	**1**	0
1	0	**1**	0

C

(A ≡ B)

5. Mark all logic functions that have another equivalent logic function here *:*

f1<=(A xor C) or (A and not C);
f2<=(B or C) and (not A or B or C);
f3<=((C and not B) or (B and A));
f4<=(A or C) and (not A or not C);
f5<=(A and not B) xor (A and C);
f6<=(A and not C) or (C and not A);

f1	■
f2	☐
f3	☐
f4	■
f5	☐
f6	■

S   x3=e

0	1
1	0
0	1
1	0

x1=a   x2=a   x1=a

Y Z

E=x3
D   D´=x2
C   C=x1

00	*01*	*10*	*01*	10	11	10	01
10	*11*	*00*	*11*	00	01	00	11
00	*01*	*10*	*01*	10	11	10	01
10	*11*	*00*	*11*	00	01	00	11

A=x1   B=x2   A=x1   B=x2

Do not write here

3

f0=

		A
	0	1
B	0	0

f1=

		A
	0	1
B	1	0

f2=

		A
	0	1
B	1	1

f3=

		A
	0	1
B	1	0

Do not write here