LSP Exam - January 21, 2015

> **CVUT FEL (ČVUT) - České vysoké učení technické v Praze | Czech Technical University in Prague**
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> **AI-Generated Solution** - Reference analysis below

Question 2: RS Latch Circuit Simulation Frequently Tested

Problem: Given inputs A, B, C values at times t0, t1, t2, t3 as shown, write the Q output value.

```
A = ..0..|..1..|..1..|..1..|
B = ..0..|..0..|..0..|..1..|
C = ..1..|..1..|..0..|..0..|

t0   t1   t2   t3
```

Answer
```
Q = ...1...|…0….|…0….|…1.…|
```

Question 3: Shannon Expansion Frequently Tested

Problem: Decompose the function `Q=f(A,B,C,Q)` from question 2 into:

```
Q = (not Q and f0(A,B,C)) or (Q and f1(A,B,C))
```

Solution Method

```
f0 := f(A,B,C,'0') := (A  B) · ('0' + (B  C)) := (A  B) · (B  C)
f1 := f(A,B,C,'1') := (A  B) · ('1' + (B  C)) := (A  B) · '1' := (A  B)
```

f0 Karnaugh Map (A B) · (B C)

f0	C=0	C=1
AB=00	0	1
AB=01	0	0
AB=11	1	0
AB=10	0	0

f1 Karnaugh Map (A B)

f1	C=0	C=1
AB=00	1	1
AB=01	0	0
AB=11	1	1
AB=10	0	0

Question 4: Signed/Unsigned Bit Values Frequently Tested

Problem: What is the decimal value of the 10-bit binary number `10 0000 1111`?

a) **Unsigned**: _____

b) **Two's-complement (signed)**: _____

Answer

```
10 0000 1111 (binary)

a) Unsigned: 2^9 + 2^3 + 2^2 + 2^1 + 2^0 = 512 + 8 + 4 + 2 + 1 = 527

b) Two's-complement (signed):
   MSB is 1, indicating negative number
   = -2^9 + (0 0000 1111)
   = -512 + 15 = -497
```

Question 5: Equivalent Logic Functions Frequently Tested

Problem: Mark all logic functions that are equivalent to other functions:

```vhdl
f1 <= (A xor C) or (A and not C);
f2 <= (B or C) and (not A or B or C);
f3 <= ((C and not B) or (B and A));
f4 <= (A or C) and (not A or not C);
f5 <= (A and not B) xor (A and C);
f6 <= (A and not C) or (C and not A);
```

Solution Method
Draw Karnaugh maps for each function and compare to find equivalent ones!

Hint: f4 and f6 are both equivalent to A XOR C

Question 6: RS Latch Drawing Frequently Tested

Problem: Draw RS latch using only NOR gates, and draw RS latch using only NAND gates.

NOR Gate RS Latch
```
S    [NOR]    Q


R    [NOR]    Q


```

NAND Gate RS Latch
```
S    [NAND]    Q


R    [NAND]    Q


```

Note: NAND-type RS latch inputs are active-low!

Question 7: Asynchronous Divider Design

Problem: Add gates and connections to the incomplete diagram to create an asynchronous divide-by-18

Use 5 DFF flip-flops for implementation.

Design Approach
- 18 = 2 × 9 = 2 × 3 × 3
- Need to detect count value 17 (10001) and reset

Question 8: VHDL Code Analysis

Problem: Analyze the following poorly formatted VHDL code, draw the corresponding logic circuit dia

```vhdl
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity test20140214 is port (a, b, c, d : in std_logic; e : out std_logic); end;
architecture rtl of test20140214 is begin
process(a, b) variable z:std_logic_vector(0 to 3); begin
if b = '0' then z:=(others=>'0');
elsif rising_edge(a) then
  if c='1' then z:=d & z(0 to 2);
  else z:=z(3) & z(0 to 2);
```

```
  end if;
end if;
e<=z(3);
end process;
end rtl;
```

Code Analysis
- **Function**: 4-bit shift register
- **Inputs**: a (clock), b (async clear), c (mode select), d (data input)
- **Output**: e = z(3)
- When c='1': Serial input d, shift right
- When c='0': Circular right shift

Knowledge Summary

Question Type	Concept	SEL Reference
Shannon Expansion	Function decomposition	p.11-14
Signed/Unsigned	Bit value calculation	p.2-3
Equivalent Functions	Karnaugh map comparison	p.4-7
RS Latch	NOR/NAND implementation	p.11-14
Divider	Digital counter design	-
VHDL Analysis	Code understanding	-