



Exam 25 January 25.1.16, questions and answers

Logic Systems And Processors (České Vysoké Učení Technické v Praze)



Scan to open on Studocu

Zde
nepíše

3

F=

C

|| || || ||

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5

The diagram shows a logic circuit for a 3-input majority gate. It has three inputs, each labeled 'INPUT VCC', and one output labeled 'OUTPUT Q'. The circuit consists of two 2-input OR gates and two 2-input NAND gates. The first OR gate takes the top two inputs. The second OR gate takes the bottom two inputs. The output of the first OR gate is connected to the top input of the first NAND gate. The output of the second OR gate is connected to the top input of the second NAND gate. The output of the first NAND gate is connected to the top input of the second NAND gate. The output of the second NAND gate is connected to the output 'Q'.

$$\overline{Q} = \begin{array}{cccc} \dots\dots & | & \dots\dots & | & \dots\dots & | & \dots\dots & | \\ t_0.. & | & ..t_1.. & | & ..t_2.. & | & ..t_3.. & | \end{array}$$

0 1 1 1 2 1 3 1

f0/3

A diagram showing a 2x4 grid of squares. Above the grid, there are two horizontal bars: a shorter one above the first two columns and a longer one above the last two columns. To the left of the grid is a vertical bar. Labels are placed around the grid: 'f0=' to the left of the top bar, 'B' to the right of the top bar, 'A' to the right of the grid, and 'C' to the left of the bottom bar.

f1=

B
A
C

 $f_{1/3}$

2

4

f1	
f2	
f3	
f4	
f5	
f6	

3/Nand

$$S \rightarrow \quad \rightarrow Q$$
$$R \rightarrow \quad \rightarrow Q_{not}$$

3/nor

3/nor

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Part 1

Part 1

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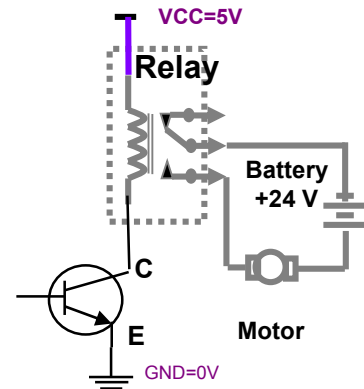
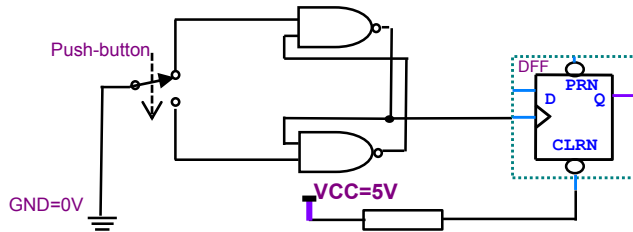
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7. One student came to an exam just to try it. Complete his non-functioning schematic - the motor is switched on by the push-button, and switched off by pressing it again. After powering up, the motor must be in stop mode. Help: You should add

7 additional elements to finish schematics.



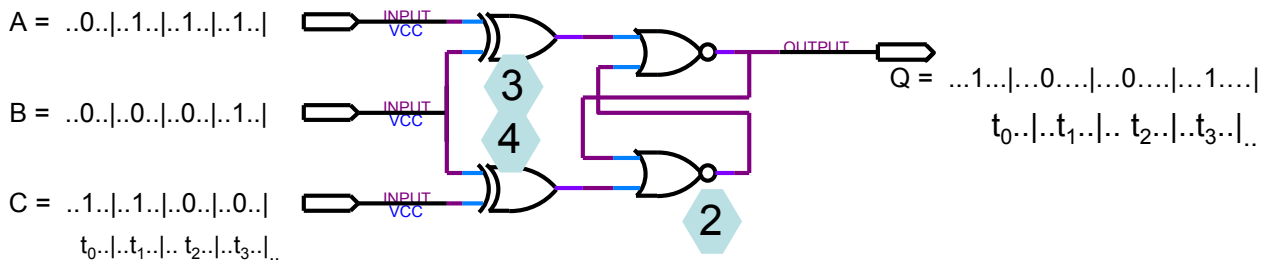
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8. An editor ask you if you could analyze wrong formatted VHDL code:

```
library IEEE; use IEEE.STD_LOGIC_1164.all;
entity test20140214 is port (a, b, c, d : in std_logic; e : out std_logic); end;
architecture rtl of test20140214 is begin
  process(a, b) variable z:std_logic_vector(0 to 3); begin
    if b = '0' then z:=(others=>'0'); elsif rising_edge(a) then
      if c='1' then z:=d & z(0 to 2); else z:=z(3) & z(0 to 2); end if; end if; e<=z(3); end process; end rtl;
```

Draw a logical circuit diagram corresponding to this VHDL code and give it appropriate title that describes its function. Guide: First, rewrite this program in the correct formatting.

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$$f_0 := f(A, B, C, '0') := (A \equiv B) \cdot ('0' + (B \neq C)) := (A \equiv B) \cdot ('0' + (B \neq C)) := (A \equiv B) \cdot (B \neq C)$$

$$f_1 := f(A, B, C, '1') := (A \equiv B) \cdot ('1' + (B \neq C)) := (A \equiv B) \cdot '1' := (A \equiv B)$$

Obě nalezené funkce $f_0 := (A \equiv B) \cdot (B \neq C)$ a $f_1 := (A \equiv B)$ zapíšeme jako Karnoughovy mapy

$f_0 =$

	A			
	B			
C	0	0	1	0
	1	0	0	0

$(A \equiv B)$ (blue dashed box)
 $(B \neq C)$ (red dashed box)

$f_1 =$

	A			
	B			
C	1	0	1	0
	1	0	1	0

$(A \equiv B)$ (red dashed box)

5. Mark all logic functions that have another equivalent logic function here :

- $f_1 \leq (A \text{ xor } C) \text{ or } (A \text{ and not } C);$
- $f_2 \leq (B \text{ or } C) \text{ and } (\text{not } A \text{ or } B \text{ or } C);$
- $f_3 \leq ((C \text{ and not } B) \text{ or } (B \text{ and } A));$
- $f_4 \leq (A \text{ or } C) \text{ and } (\text{not } A \text{ or not } C);$
- $f_5 \leq (A \text{ and not } B) \text{ xor } (A \text{ and } C);$
- $f_6 \leq (A \text{ and not } C) \text{ or } (C \text{ and not } A);$

f_1 ☒
 f_2 ☐
 f_3 ☐
 f_4 ☒
 f_5 ☐
 f_6 ☒