Exam 2019, questions and answers

Logic Systems And Processors (České Vysoké Učení Technické v Praze)

Sample of English Test - Version 1.1 – *corrected swapped result of Q3 – f1*

Zde nepište

1. Rewrite logic function in VHDL syntax by the way that final function will contain only operations "or", "and" and "not" and "not" operation will never be in front of any round bracket.

F1<= A xor (B or C);

F1<=.....

F2<= **not** (A and (B **xor** C));

F2<=.....

4

2. Inputs A, B, C have values shown in the figure in times t_0, t_1, t_2, t_3, t_4 . Write values of X and Y outputs. Assume that the intervals between changes in the inputs are so long so we can neglect delays of gates.

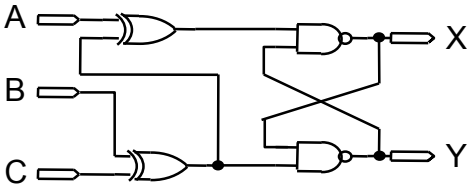
A = **..1..| 1..|..0..|..0.. |..1..|**

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

B = **..0..|..1..|..1..|..1.. |..1..|**

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

C = **..0..|..0..|..0..|..1.. |..1..|**



X = ...|... ....|... ....| .....|... ...|

t_0..|..t_1...|.. t_2..|..t_3..|..t_4..|..

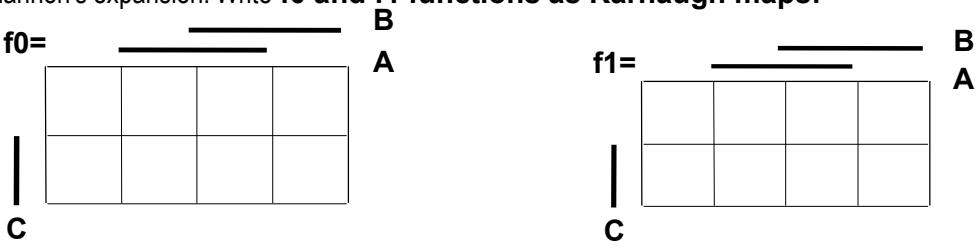
Y = ...|... ....|... ....| .....|... ...|

5

3. Function X=f(A,B,C, X) from question 2, decompose into X= (not X and f0(A, B,C)) or (X and f1(A,B,C)) with the aid of Shannon's expansion. Write **f0 and f1 functions as Karnaugh maps:**

f0/3

f1/3



2

4. What decimal value is 12-bit number 1000 0000 0111 if we interpret it as an integer

a) unsigned ..... b) signed in two's-complement..... ...

5. Mark all logic functions that have another equivalent logic function here *:*

f1<=((C and not B) or (C and B and A)); f1 ☐

f2<=(A xor C) or (A and not C); f2 ☐

f3<=(A or B) and (not A or B or C); f3 ☐

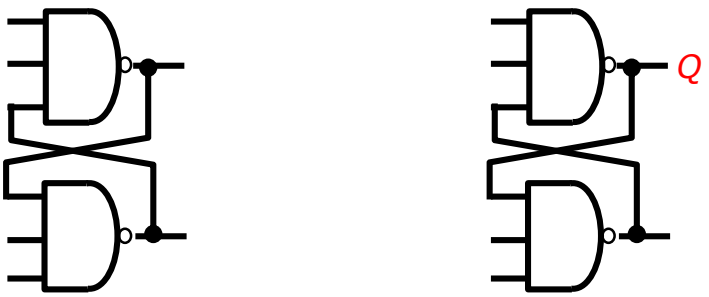
f4<=(not A or not C) and (C or A); f4 ☐

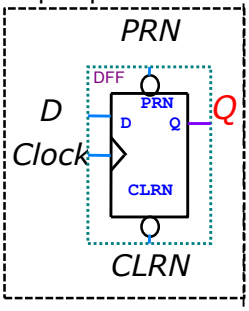
f5<=(not C and A) or (not A and C); f5 ☐

f6<=(A and not B) xor (A and and not B and C); f6 ☐

6

6. By adding gates (4 NAND and 3 NOT) and wires, create internal schematic of master-slave flip-flop DFF.



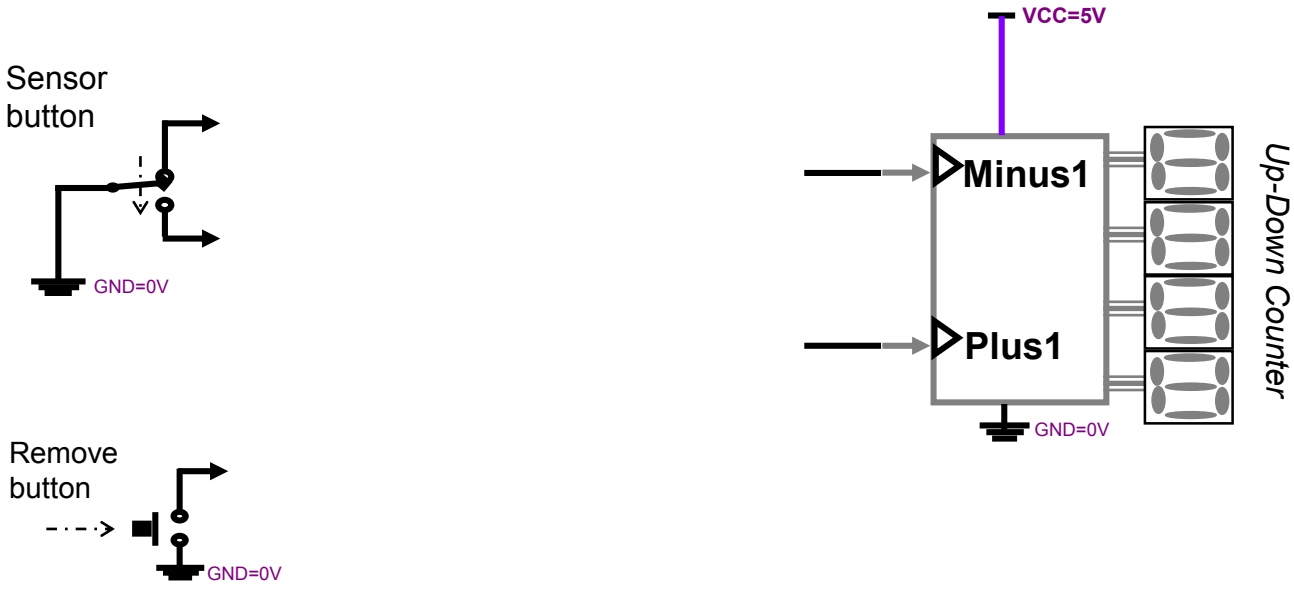


7

Part 1

30

7. On an assembly line, there is a mechanical sensor created as two pole button. The sensor detects passes of products. During a next manual check operation, any product can be removed, which is announced by one pole button Remove. The buttons activate clock inputs of Up-Down counter: Plus1 clock input is driven by the sensor, Minus1 clock input by the remove button.
Add 7 necessary elements and wires.



15

8. *An editor ask you if you could analyze wrong formatted VHDL code:*

```
library ieee; use ieee.std_logic_1164.all;
entity XXX is port(  A, B, C, D : in std_logic; Q : out std_logic ); end;
architecture rtl of XXX is  constant E:std_logic:='0'; begin  process (A, D)
variable qv:std_logic;  begin  if D='0' then qv:=E;  elsif rising_edge(A) then
if C='1' then qv:=B; else  qv:=not qv; end if;   end if;  Q<=qv;  end process; end rtl;
```

Draw a logical circuit diagram corresponding to this VHDL code and give it appropriate title that describes its function. Guide: First, rewrite this program in a better formatting.

15

2. part
30

B1.

F1<= A xor (B or C);

F1<=(A and not B and not C) or (not A and (B or C));.....

F2<= **not** (A and (B **xor** C));

F2<=not A or ((not B or C) and (B or not C));.....

SOLUTION

2. Inputs A, B, C have values shown in the figure in times t_0, t_1, t_2, t_3, t_4 . Write values of X and Y outputs. Assume that the intervals between changes in the inputs are so long so we can neglect delays of gates.

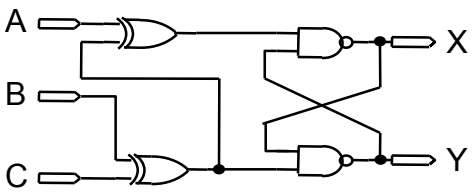
A = ..**1..**| **1..**|..**0..**|..**0..** |..**1..**|

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

B = ..**0..**|..**1..**|..**1..**|..**1..** |..**1..**|

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

C = ..**0..**|..**0..**|..**0..**|..**1..** |..**1..**|



X = ... 0..|…1...|…1..| ...1...|...0…|

t_0..|..t_1...|.. t_2..|..t_3..|..t_4..|..

Y = ...1...|…0….|…0….| ..1…|.. 1…|

3. Function X=f(A,B,C, X) from question 2, decompose into X= (not X and f0(A, B,C)) or (X and f1(A,B,C)) with the aid of Shannon's expansion. Write **f0 and f1 functions as Karnaugh maps:**

f0=

C \ B A	00	01	11	10
0	1	0	1	0
1	0	1	0	1

f1=

C \ B A	00	01	11	10
0	1	0	1	1
1	1	1	0	1

4. What decimal value is 12-bit number 1000 0000 0111 if we interpret it as an integer

a) As unsigned....2055..... *b)* signed in two's-complement*.....-2041.*

SOLUTION

5. Mark all logic functions that have another equivalent logic function here

f1<=((C and not B) or (C and B and A));

f2<=(A xor C) or (A and not C);

f3<=(A or B) and (not A or B or C);

f4<=(not A or not C) and (C or A);

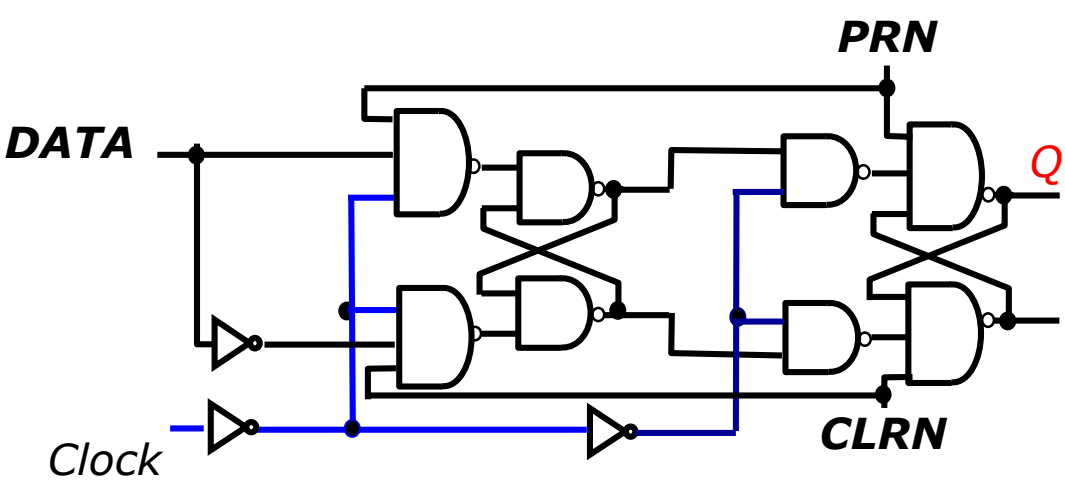
f5<=(not C and A) or (not A and C);

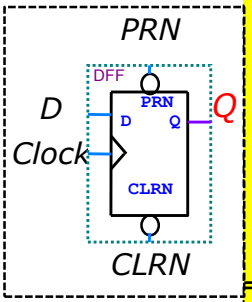
f6<=(A and not B) xor (A and and not B and C);

f1 ☐
f2 ■
f3 ☐
f4 ■
f5 ■
f6 ☐

SOLUTION

6. By adding gates (4 NAND and 3 NOT) and wires, create internal schematic of master-slave flip-flop DFF.





SOLUTION

7. On an assembly line, there is a mechanical sensor created as two pole button. The sensor detects passes of products. During a next manual check operation, any product can be removed, which is announced by one pole button Remove. The buttons activate clock inputs of Up-Down counter: Plus1 clock input is driven by the sensor, Minus1 clock input by the remove button.
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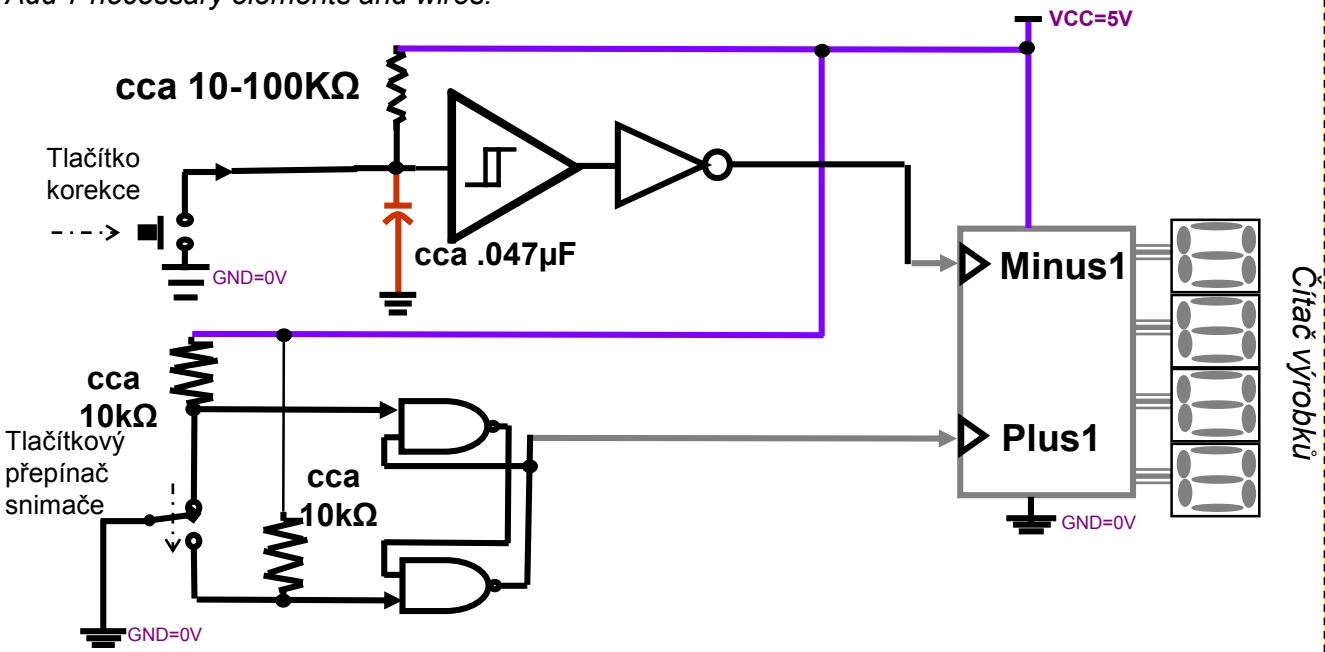

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