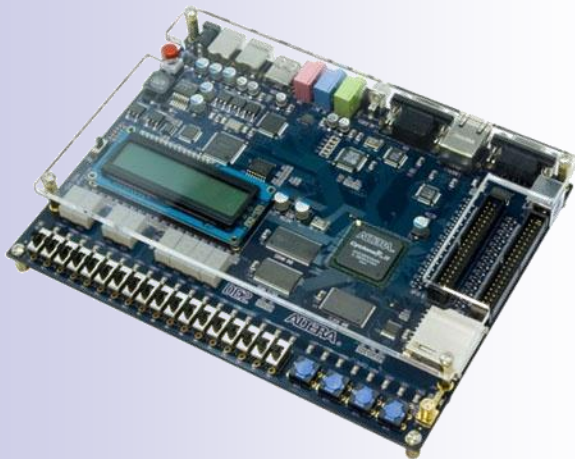


Logic Systems and Processors

cz: Logické systémy a procesory

Exercise 1: Introduction to Tasks



Teachers



Ing. Martin Hlinovský, Ph.D.

hlinovsm@fel.cvut.cz,

martin.hlinovsky@fel.cvut.cz

+420 2 2435 7477



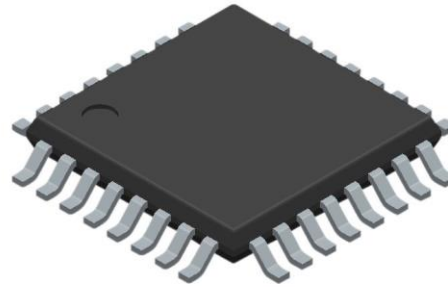
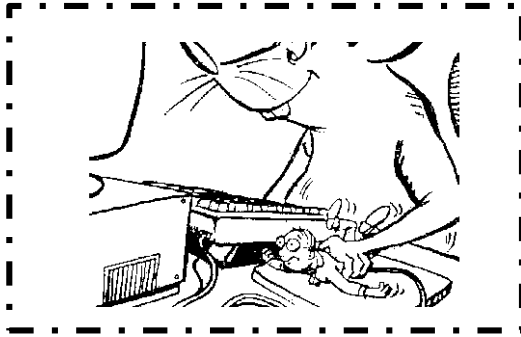
Ing. Richard Šusta, Ph.D.

susta@fel.cvut.cz

+420 2 2435 7359

<https://susta.cz>

Example: How to Build Small Systems



**Microcontroller
or microprocessor**



???? connection



Peripherals

*We write program
for ready-to-use processor board.*

But how do we connect our peripherals...

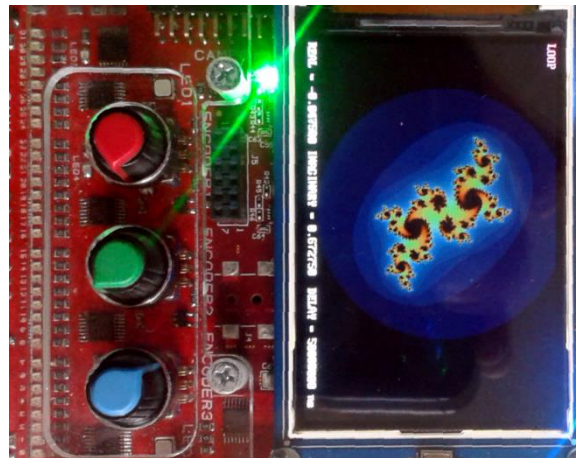
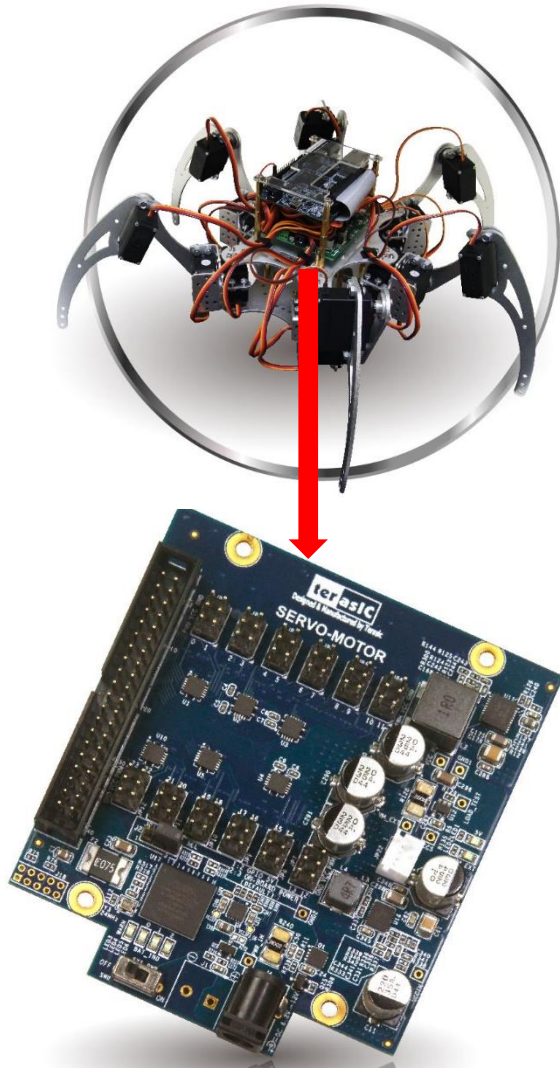


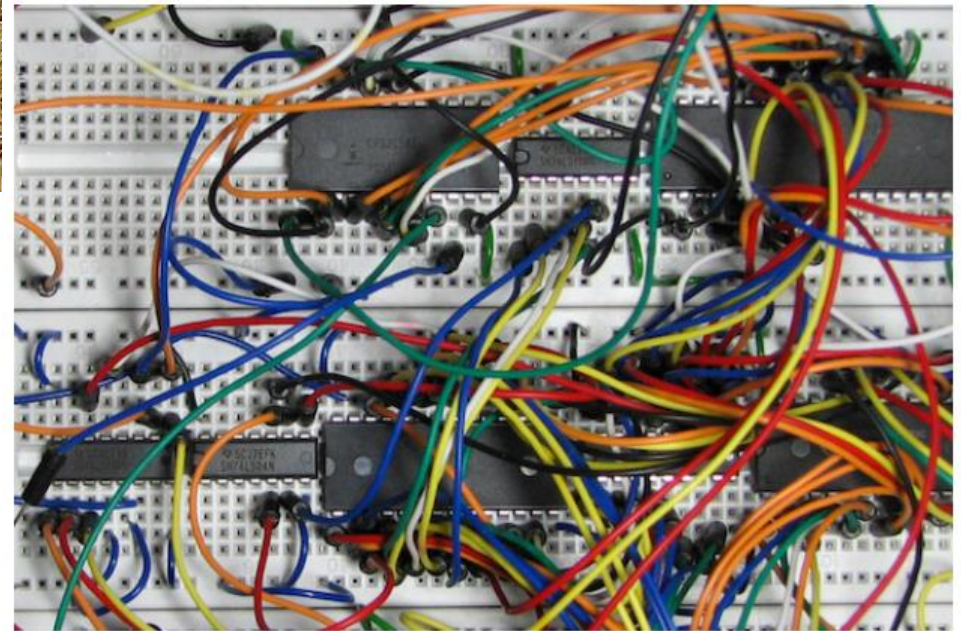
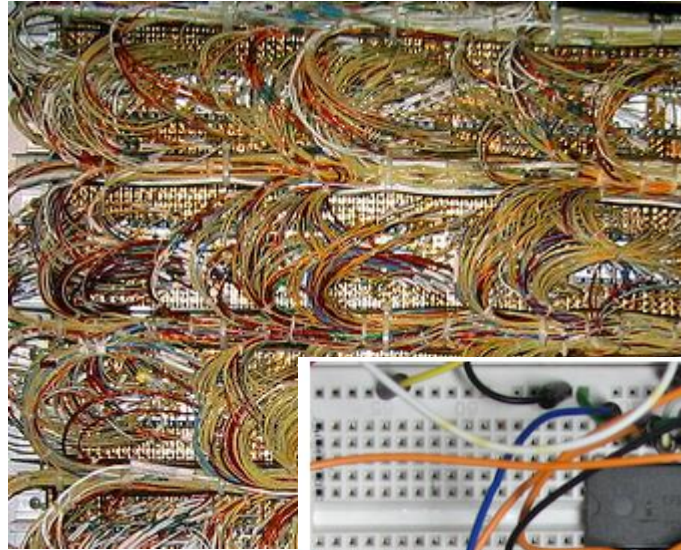
Image: AHajokes

How do we connect the peripherals?

Sometimes suitable modules are produced, but we must create the specialties ourselves...



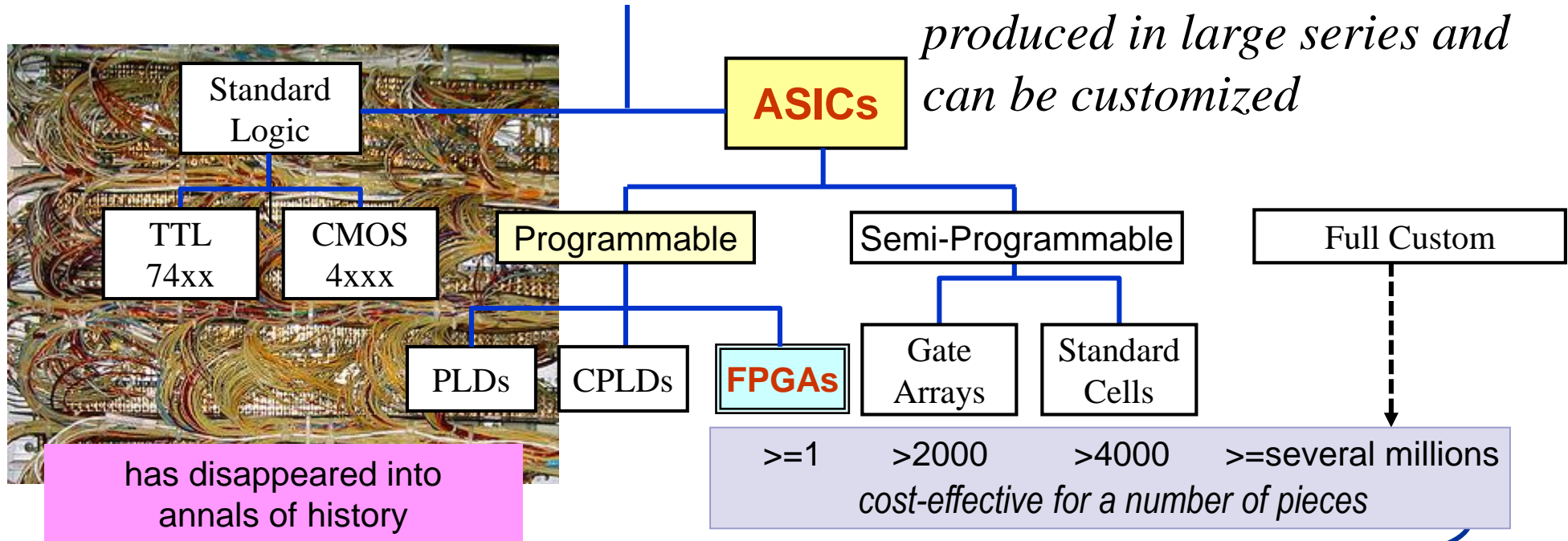
Terasic: [Server Motor Kit](#)



Interface wired on breadboard

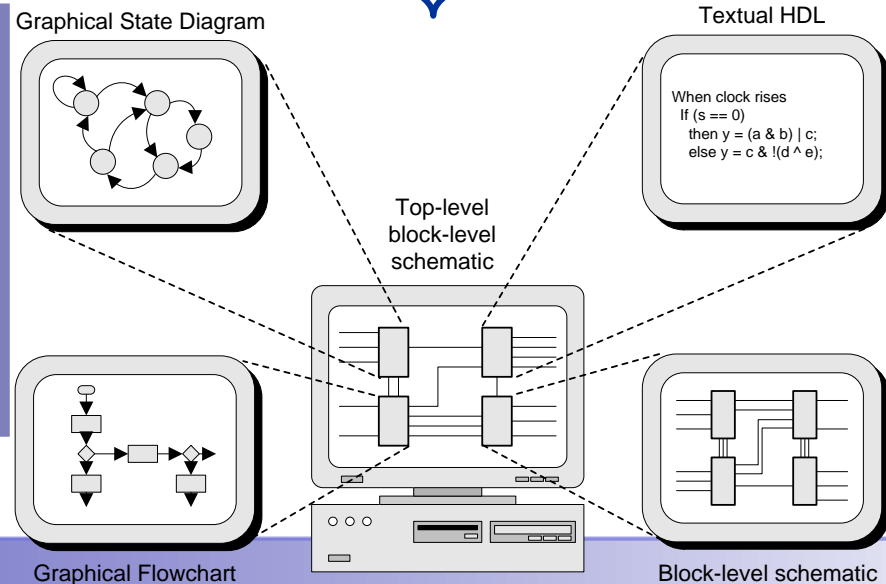
Source: [All About Circuits](#)

Individually Configurable IO Circuits



ASIC-Application Specific Integrated Circuits

- Programmable Logic Device (**PLD**)
- Complex PLD (**CPLD**)
- Field Programmable Gate Arrays (**FPGAs**)



FPGA

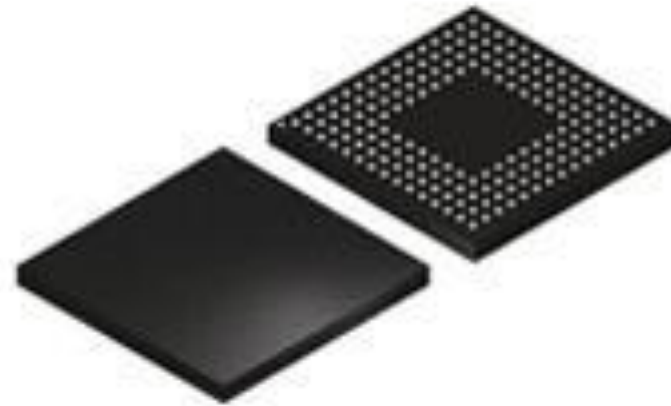
Field

Programmable

Gate

Array

*= programmable
(configurable) gate
array*



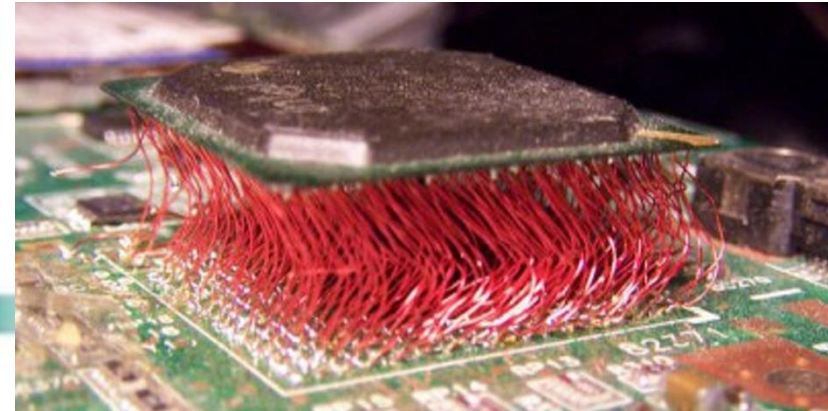
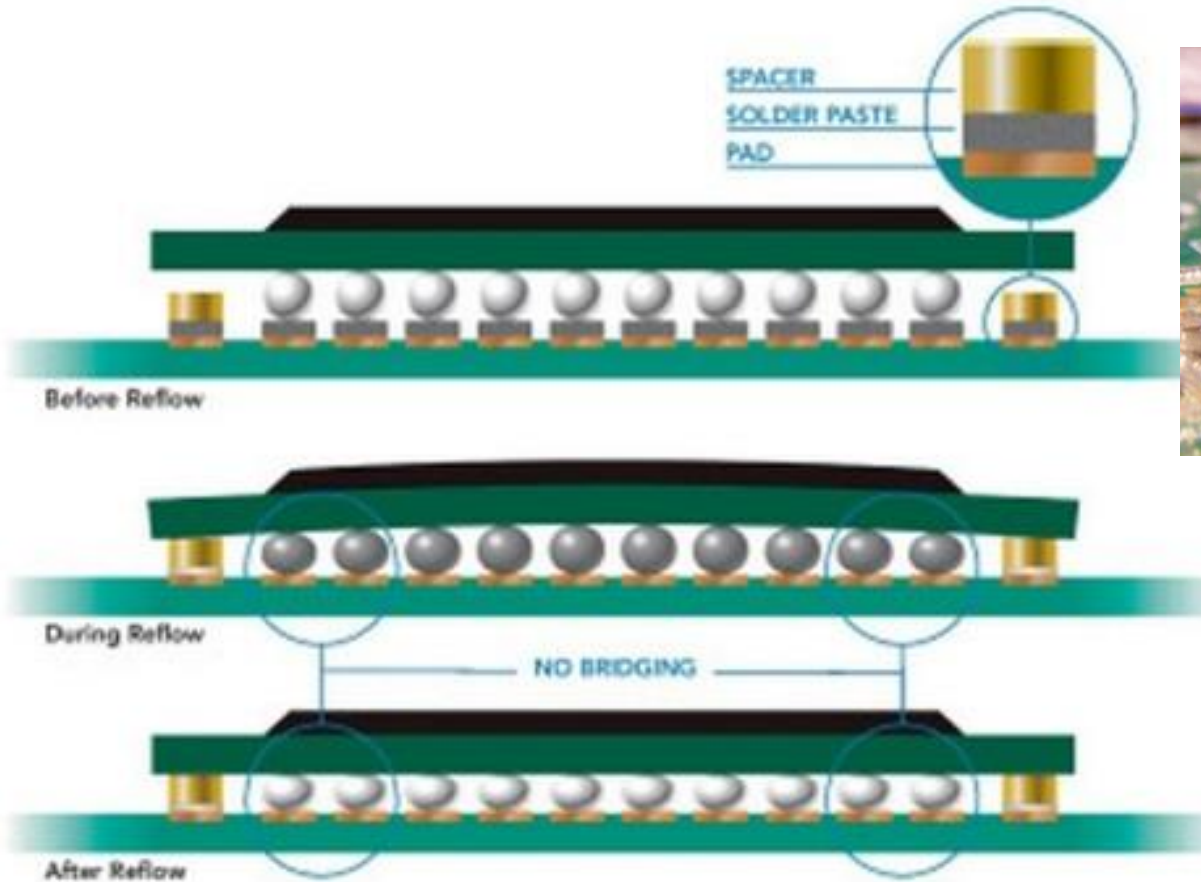
EP4CE115F29C7N

FBGA chip

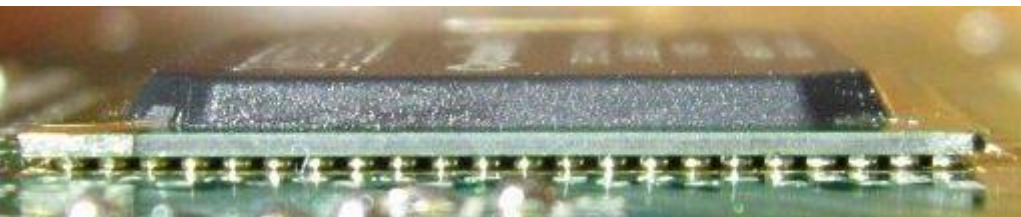
= Fine-Pitch Ball Grid Array

Detail of Real SMD Soldering FPGA

and his jokey non-SMD soldering



SMD
Surface Mount Device
on **PCB**
Printed Circuit Board



Source: Fairchild Semiconductors

FPGA circuits sometimes include processors

Xilinx Zynq™ 7000 Series

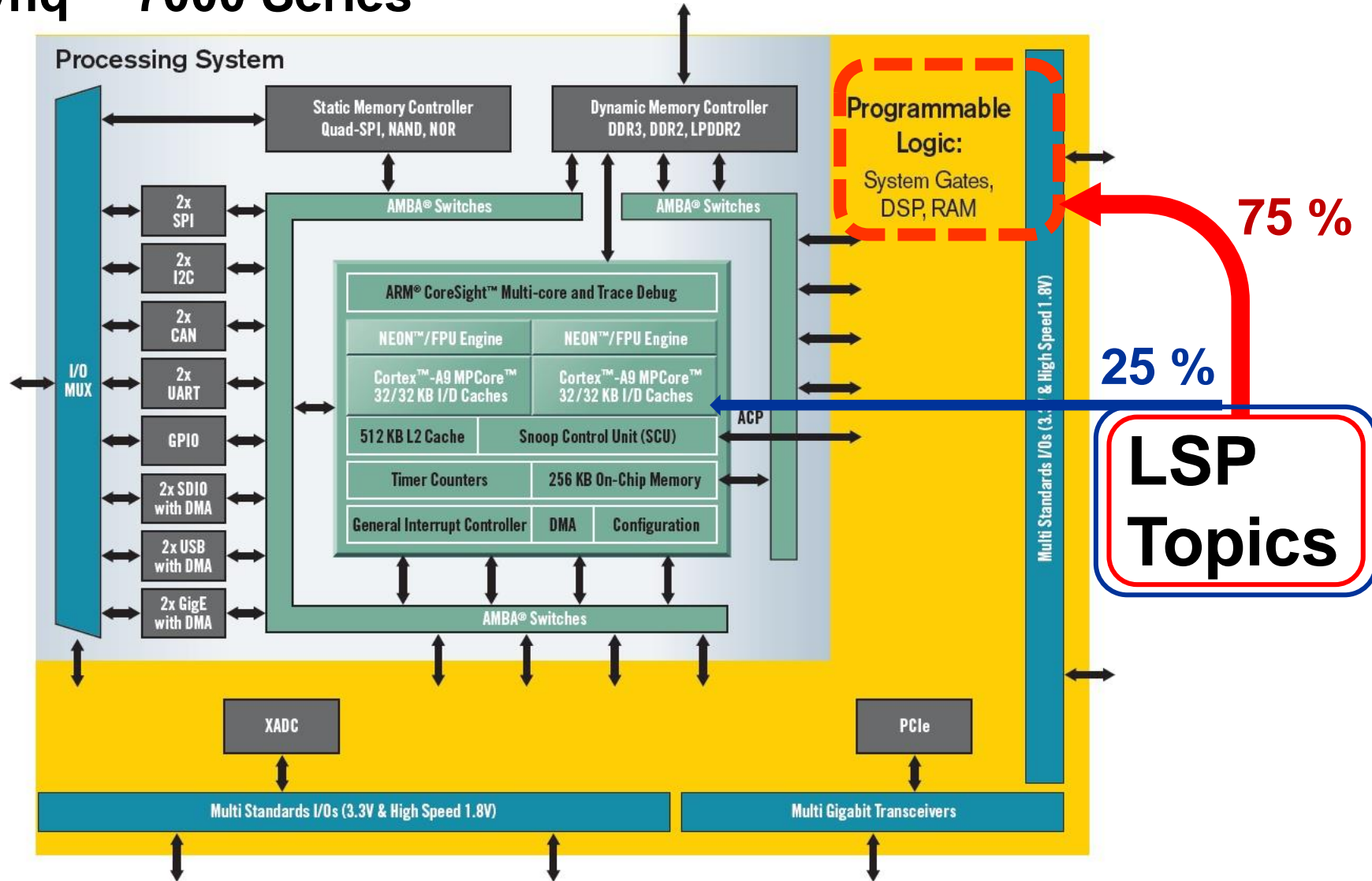
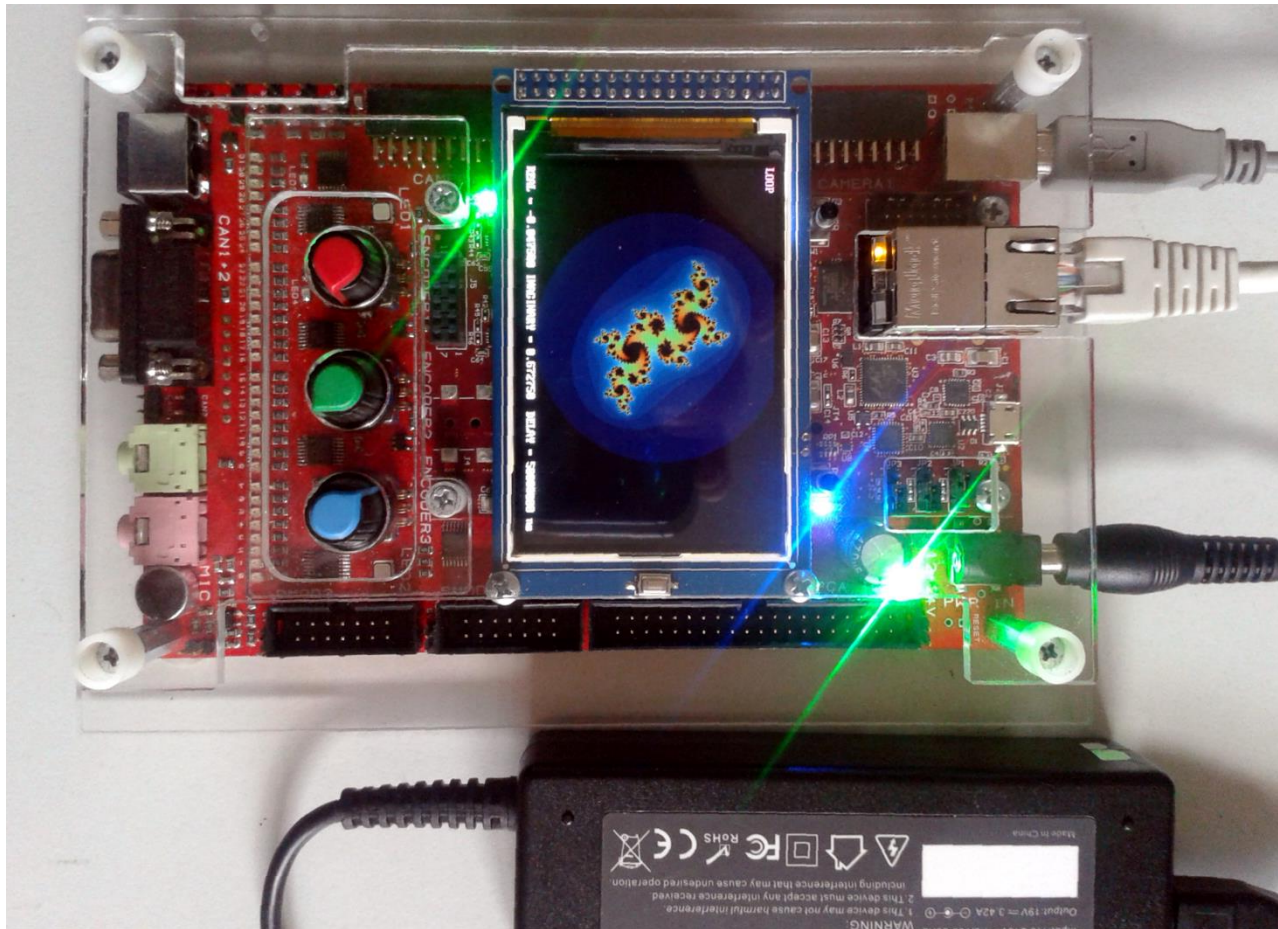


Image source: [Xilinx](https://www.xilinx.com)

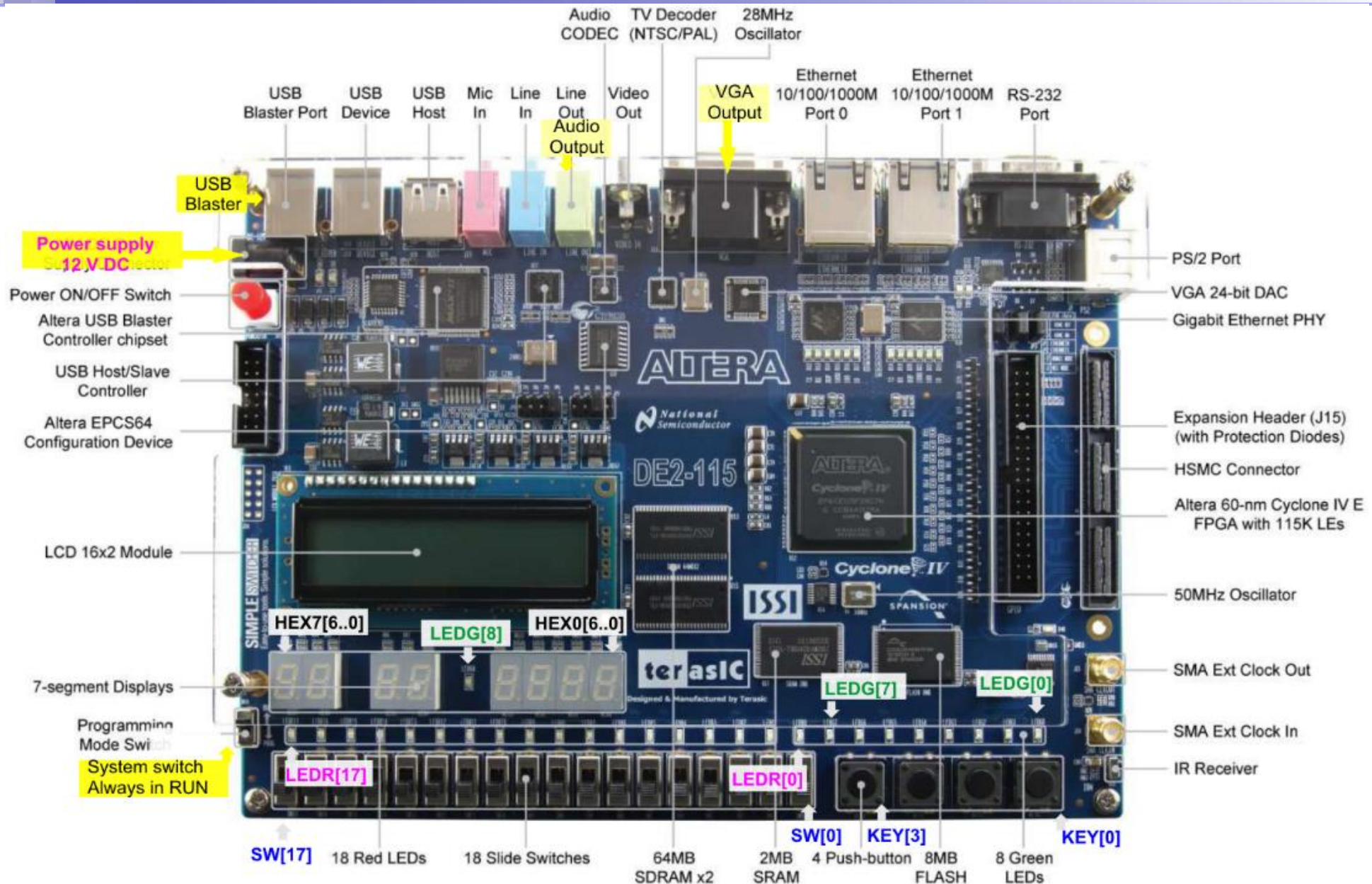
*Students in the APO Computer Architecture course will work with Zynq in the lab, but only at the program level.
In LSP we will be working on FPGA logic.*



Video and Embedded Evaluation Kit Multi-touch, Second Edition



VEEK-MT2 other side = DE2-115



LSP Website



DCENET = Department of **C**ontrol **E**ngineering **NET**work

<https://dcenet.fel.cvut.cz/>

They have a public section, FELid, and a link to Moodle

Our Site

DCENET

Department of Control Engineering .NET Website



&

[A0B36APO - Architektura počítačů](#) - stránky vznikly za podpory od projektu

[AE0B36APO - Computer Architectures](#) - the site was supported by the grant



&

[B0B35LSP - Logické systémy a procesory](#)

[BE5B35LSP - Logic Systems and Processors](#)



[Protokoly na bezpečnost práce](#)

Not recommended now - it became unstable in Windows 10 after their recent updates....

Installing Quartus 13.0sp1 web

<https://dcenet.fel.cvut.cz/edu/fpga/install.aspx>

Installing Quartus II Web Edition (Free) 13.0.1.232

Select Components

Select the components you want to install

- ☒ Quartus II Web Edition (Free)
 - ☒ Quartus II Software (includes Nios II EDS) (4440MB)
 - ☒ Quartus II Software 64-bit support (962MB)
 - ☒ Quartus II Help (631.2MB)
 - ☒ Devices
 - ☐ Arria II (482.8MB)
 - ☒ Cyclone II/III/IV (615.2MB)
 - ☐ Cyclone V (751.8MB)
 - ☐ MAX II/V, MAX 3000/7000 (9.1MB)
- ☒ ModelSim-Altera Starter Edition (Free) (3211.7MB)
- ☐ ModelSim-Altera Edition (3211.7MB)

- You can work with the older free version, the full version of which is installed in the lab, and we have extensive support for it.
- When installing, choose **only Cyclone II/III/IV**, then it only wants **10 GB**.

Windows 10

- ❖ **Quartus 20.1 Lite** version needs **14 GB** and is on our laboratory computers. It includes free modules of the Intel University program and ModelSim.

Note: Lite or web versions can be run without a license.

Windows 11

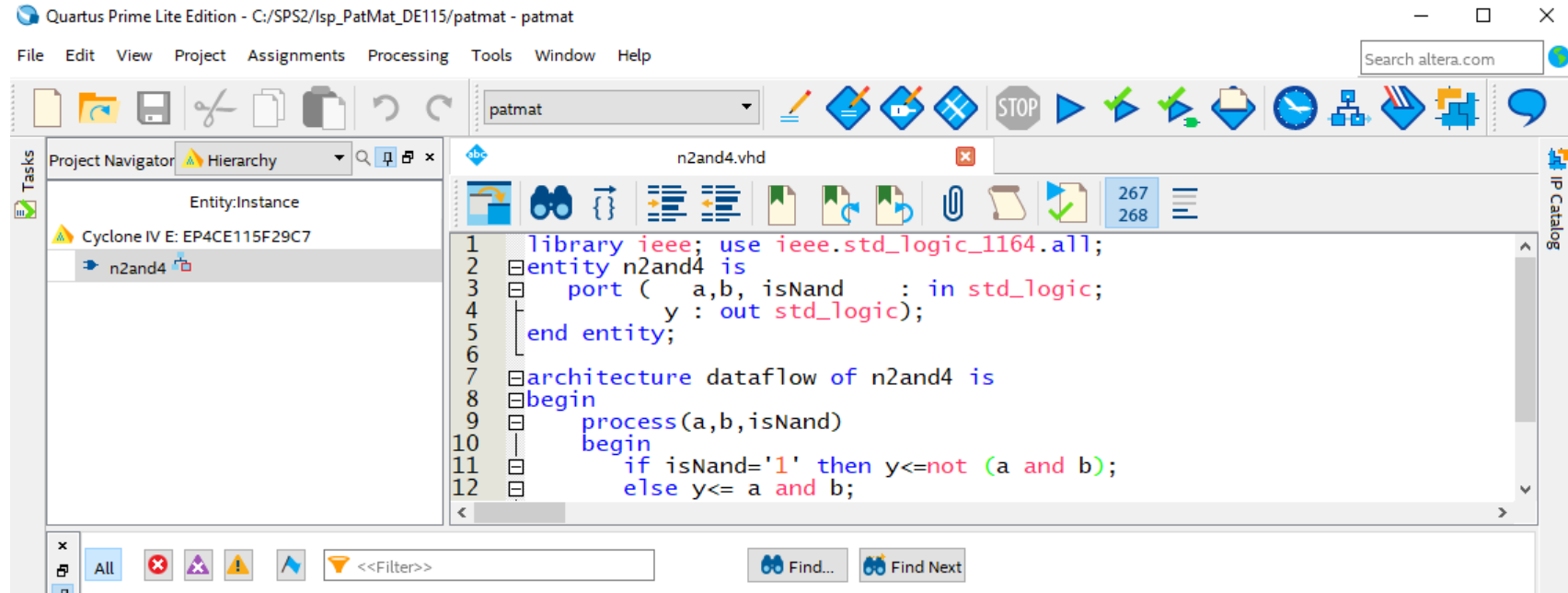
- ❖ You can install 20.1, but it can be a little troublemaker.
- ❖ **Quartus 23.1 Lite** is the first version that fully supports Win11 but no longer includes a free ModelSim simulation environment.
- ❖ *You need to register Questa simulator individually, which requires many steps, such as two registrations to Intel accounts, mobile and email validations, waiting for enrollment response, authentication via Microsoft Azure..., etc.*

In the case of Quartus 23.1, it is better to simulate by the free GHDL tool.

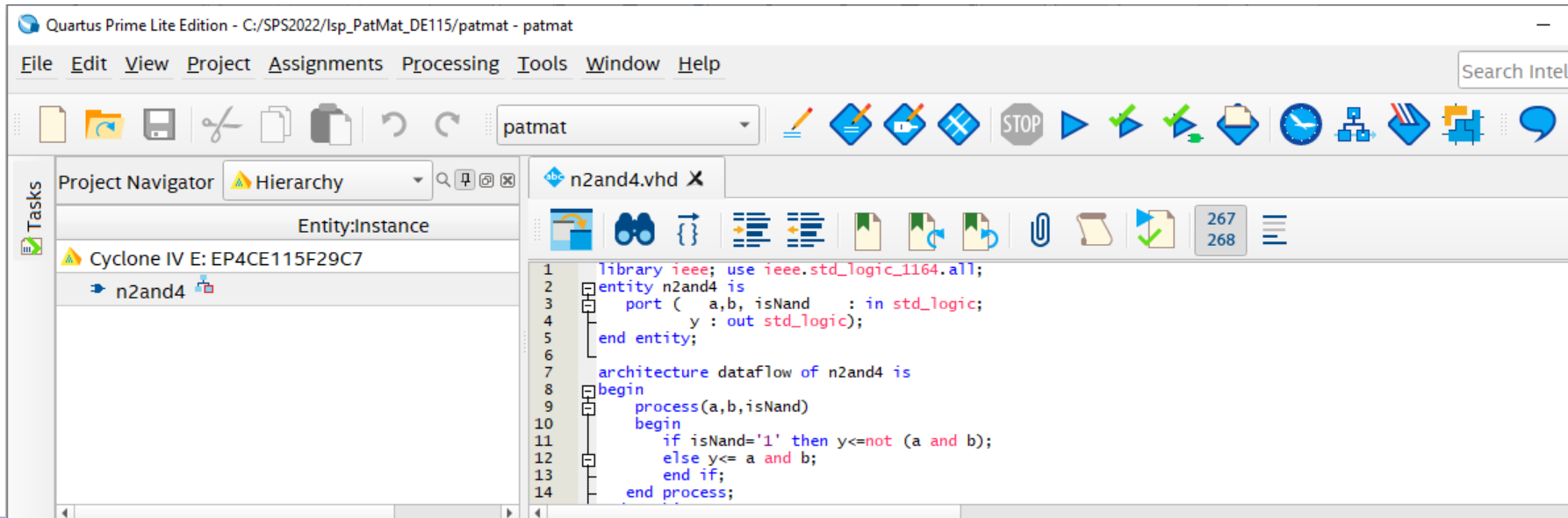
- ☐ You can install several different versions of Quartus on your computer. They will not argue with each other.
- ☐ Quartus is a Linux program running under Cygwin on Windows and does not write to the Windows registry. It is uninstalled cleanly when the semester is over.

Quartus 20.1 and 23.1 have the same skins

Quartus
20.1



Quartus
23.1



DE2_115_ControlPanel.exe	16 335 360	06.09.2010
DE2_115_ControlPanel.sof	3 541 384	06.09.2010
dinkum_alt.dll	694 272	06.09.2010
jtag_client.dll	110 592	06.09.2010
TERASIC_DOWNLOAD.dll	519 680	06.09.2010
TERASIC_JTAG.dll	52 736	06.09.2010
TERASIC_JTAG_DRIVE.dll	40 960	06.09.2010

Tools Window Help

Run Simulation Tool

Launch Simulation Library Compiler

It is necessary to upload *.sof first
via Quartus Programmer

Design Partition Planner

Netlist Viewers

SignalTap II Logic Analyzer

In-System Memory Content Editor

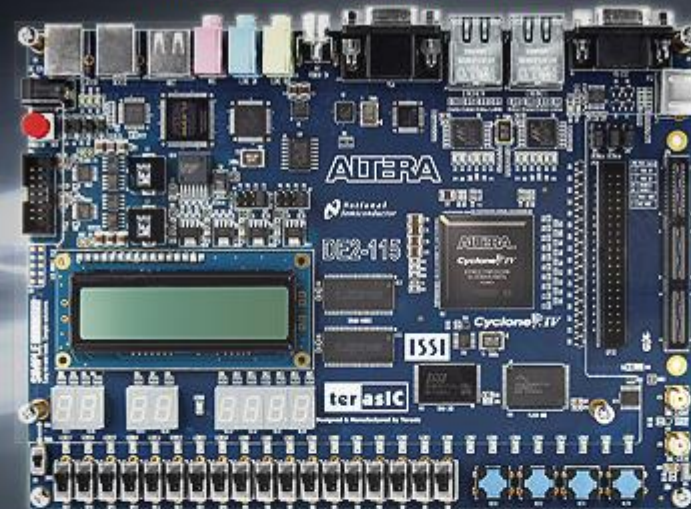
Logic Analyzer Interface Editor

In-System Sources and Probes Editor

SignalProbe Pins...

Programmer

Terasic-DE2-115 Control Panel V1.0.0



Today, we'll use a pre-made initial project

VeekMT2_Quartus20_defaultProject.zip

Page: https://dcenet.fel.cvut.cz/edu/fpga/veek-mt2_en.aspx

VEEK-MT2 BOARD

It consists of a DE2-115 board front panel and a rear 800x480 pixel colour LCD module.

Contain device: **EP4CE115F29C7**

Family Cyclone IV E Package FBGA Pin count 780 Speed grade 7

Parameters: 114480 logic elements, 3888 kbit embedded memory, 266 hardware multipliers 18x18 bits, 4 PLLs and 528 user pins

Picture overview of basic I/O of front DE2-115 board: [1500 x 1000](#) [750 x 500](#)

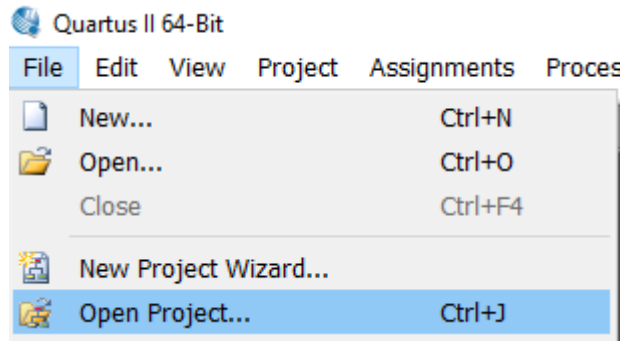
Important note: The board requires a power supply = 12 V. Always check that you are using the correct one !!!

Quartus projects require many complex settings. Beginners are advised to use a ready-made project for Quartus version V20.1 and higher: [VeekMT2_Quartus20_defaultProject.zip](#) And read our 1-page tutorial [OpenProject.pdf](#).

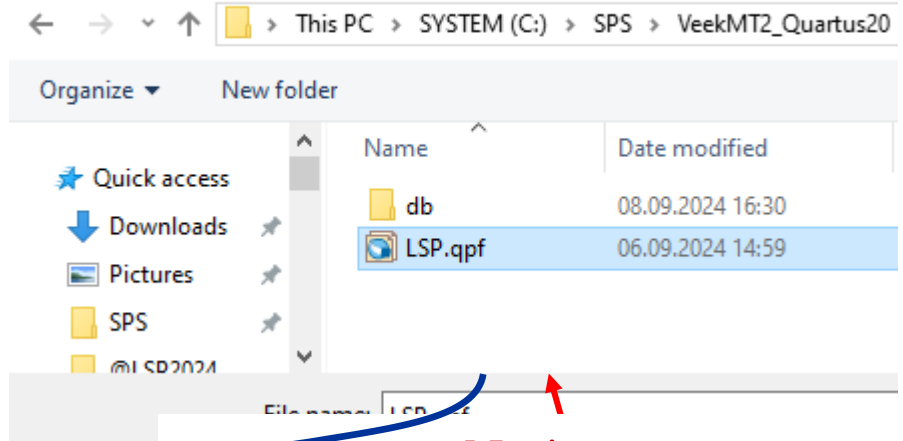


...in the presentation will be on the next slides

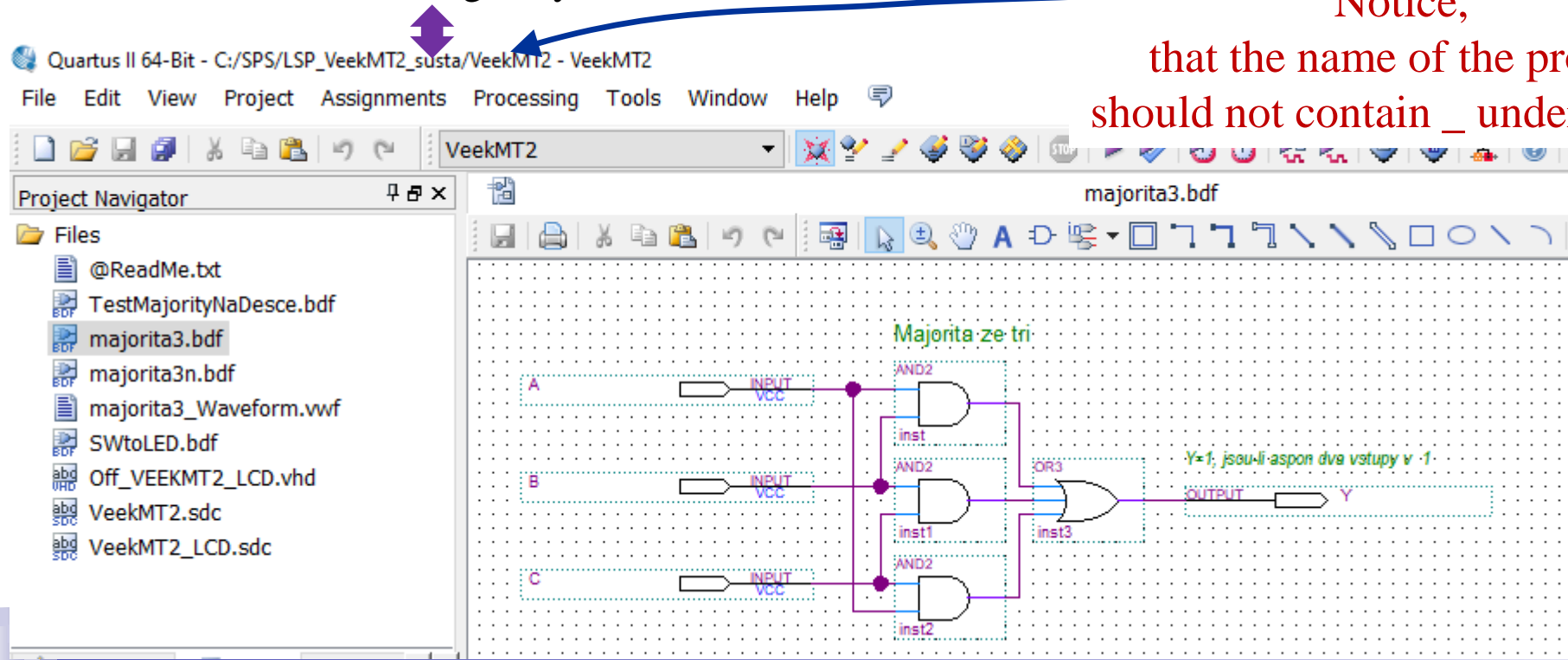
Opening of the project



Open Project



You should rename the created directory after closing Quartus and append your identification to it. Let others know it belongs to you.

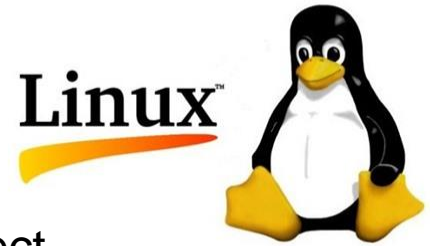


Notice,

that the name of the project should not contain _underscores!

Quartus is a Linux program running in CygWin

*Cygwin is a command-line Linux distribution,
which includes popular GNU and other open source tools.
It allows you to adapt Linux programs to Microsoft Windows.*



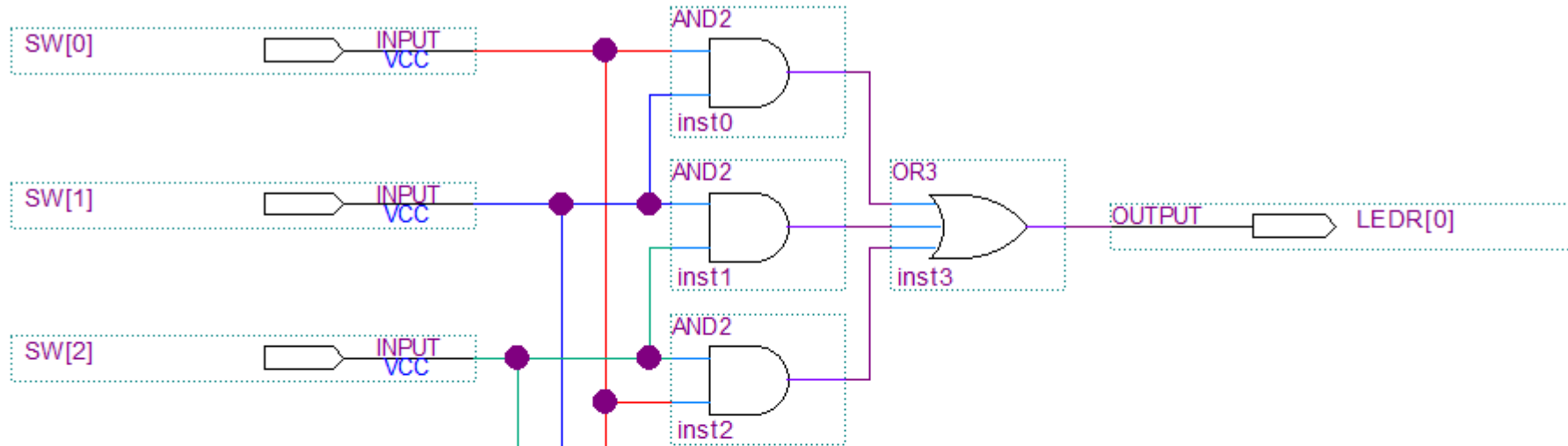
- **Quartus project its own folder** that is never shares with another project.
- All file names and paths must contain only letters (without diacritics), numbers or _ underscores, but not two connected, and not at the beginning and end.
- Do not store projects in Windows folders in our school laboratory, such as **Desktop**, **Downloads**, **Documents**, etc. They are redirected to Active-directory server and contain \$ in their paths, which you need not see. Windows shows you only links, not actual folder names.
- It is better to enter project names without _ underscores, the simulation may not work with them. (The reason is hidden somewhere in the window updates:-)
- You can rename the project's top folder or move the whole project to another folder.
- The file names entered in the paths have / slashes as a rule, not \ *backslashes*.
- !!! Spaces and other Windows specialties are strictly forbidden in paths, file names, and entity names (circuit descriptions).
- Do not use non-ASCII characters in comments inside Quartus. Sometimes even Chinese kanji is OK, as the foreign students tried, but sometimes not. :-)



Example from Default Project

Majority aka Median Operator

Majority of Three - $Y = '1'$ if we have at least two inputs in '1's



Majority of Three - $Y = '0'$ if we have at least two inputs in '0's

