# LSP Exam 2022–01–11

**Course**: B0B35LSP – Logické systémy a procesory | BE5B35LSP – Logic Systems and Processors **University**: CVUT FEL (ČVUT) – České vysoké učení technické v Praze | Czech Technical University in Prague **Keywords**: LSP, Exam, Zkouška, 2022–01–11, RS latch, Shannon expansion, VHDL

CN Version | EN Version | CZ Version

---

# LSP Exam 2022–01–11

**AI–derived version** – No official answers in the PDF; the following is an inferred walkthrough/notes.

## Exam Info

- Date: 2022–01–11
- Language: Czech
- Total: 50 points (Part 1: 25 pts ⩾ 9 + Part 2: 25 pts ⩾ 9)

---

## Q1 – Equivalent Logic Functions (8 pts)

**Task:** Check all logic functions that have an equivalent function:

```
y1 <= (A and not D) or (not A and not B and C) or (B and D);
y2 <= ((B or not C) and (not A or C)) xor ((A or not B or not D)
       and (not A or not B or not C) and (not A or B or not D));
y3 <= (A or not B or D) and (not A or B or not D) and (A or B or C);
y4 <= (B xor not D) or (A and B) or (not A and not B and C);
```

---

## Q2 – RS Latch Simulation (5 pts)

**Task:** Given inputs A, B, C values at times t0—t4, write the values of outputs Q and QN.

**Input sequence:**

```
A = 0 | 0 | 1 | 0 | 0
B = 0 | 1 | 1 | 0 | 1
C = 1 | 0 | 0 | 0 | 1
    t0  t1  t2  t3  t4
```

---

## Q3 – Shannon Expansion (8 pts)

**Task:** Decompose $Q = f(A, B, C, Q)$ into:

$$Q = (\overline{Q} \wedge f_0(A, B, C)) \vee (Q \wedge f_1(A, B, C))$$

---

## Q4 – 4–to–1 Multiplexer (4 pts)

**Task:** Add the minimum number of components to the circuit diagram to implement a 4–to–1 multiplexer with enable.

**Notation:**

```
y1y0 – select signals
a, b, c, d – data inputs
en – enable (active when en='1'; when en='0' output Z is '0')
Z – output
```

---

## Q5 – Moore/Mealy Automaton Definition (4 pts)

**Task:** Complete the definition: Moore (Mealy) automaton is a sextuple $M =< X, S, Z, \omega, \delta, s_0 \in S >$.

**Answer:** – **X**: Input alphabet (finite set of input symbols) – **S**: State set (finite set of states) – **Z**: Output alphabet (finite set of output symbols) – **δ**: State transition function – Moore: $\delta : S \times X \to S$ – Mealy: $\delta : S \times X \to S$ – **ω**: Output function – Moore: $\omega : S \to Z$ (output depends only on the state) – Mealy: $\omega : S \times X \to Z$ (output depends on the state and input) – **$s_0$**: Initial state

---

## Q6 – Product Counter (Debounce) Circuit (8 pts)

**Task:** On a production line there is a product sensor (single–pole button) and a manual correction button (double–pole button). The sensor triggers input **Plus1**, correction triggers input **Minus1**. Design a debounce circuit so the counter counts at the moment of pressing.

**Requirements:** – Add 8 necessary components – Rising–edge triggered – Immediate response

---

## Q7 – VHDL Code Analysis

**Task:** Analyze the given VHDL code and draw the RTL view.

---

## Q8 – Branch Prediction

**Not on Exam note:** According to the 2026 exam notes, branch–predictor calculation tasks are not tested; you can skip strategically.

**Task:** Calculate the number of branch mispredictions for the given program.