Exam 21 January 21.1.15, questions and answers

Logic Systems And Processors (České Vysoké Učení Technické v Praze)

Surname and first name:.....

Exam 21.1.2015 - write here only your answers

1. Rewrite the logical expression F so that not operators were only before variables - check your solution in K-map!

F = not ((not A and not C) **xor** (A and B and C))

F =.....

F= B A C

2. Inputs A, B, C have values shown in the figure in times t_0, t_1, t_2, t_3 . Write values of X and Y outputs. Assume that the intervals between changes in the inputs are so long so we can neglect delays of gates.

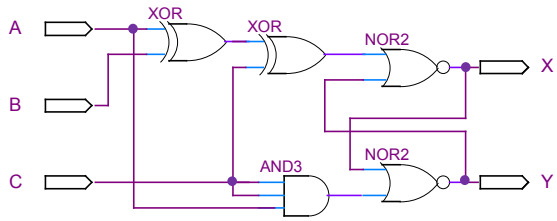
A = ..**1..**| **1..**|..**1..**|..**0..**|

t_0..|..t_1..|.. t_2..|..t_3..|..

B = ..**1..**|..**0..**|..**0..**|..**0..**|

t_0..|..t_1..|.. t_2..|..t_3..|..

C = ..**1..**|..**1..**|..**0..**|..**0..**|



X = ...|... ....|... ....| .....|

t_0..|..t_1...|.. t_2..|..t_3..|..

Y = ...|... ....|... ....| .....|

3. Function X=f(A,B,C, Q) from question 2, decompose into X= (not X and f0(A, B,C)) or (X and f1(A,B,C)) with the aid of **Shannon's expansion. Write f0 and f1 functions as Karnaugh maps:**

f0= **B** **A** **C**

f1= **B** **A** **C**

4. What decimal value is 12-bit number 1000 0000 0111 if we interpret it as an integer

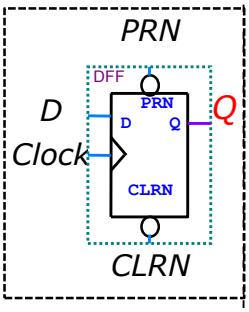
a) unsigned ..... b) signed in two's-complement..... ...

5. Mark all logic functions that have another equivalent logic function here *:*

y1 <= (A and D) or (B xor D);
y2 <= (A and B) or (B and not D) or (D and not B);
y3 <= (B or D) and (A or B or not D);
y4 <= A or (A and B and not D) or (A and C and D);
y5 <= (not B xor not D) or (A and B);
y6 <= (A and D) xor (C and D);

y1 ☐
y2 ☐
y3 ☐
y4 ☐
y5 ☐
y6 ☐

6. By adding gates (4 NAND and 3 NOT) and wires, create internal schematic of master-slave flip-flop DFF.



Zde nepište

3

5

f0/3

f1/3

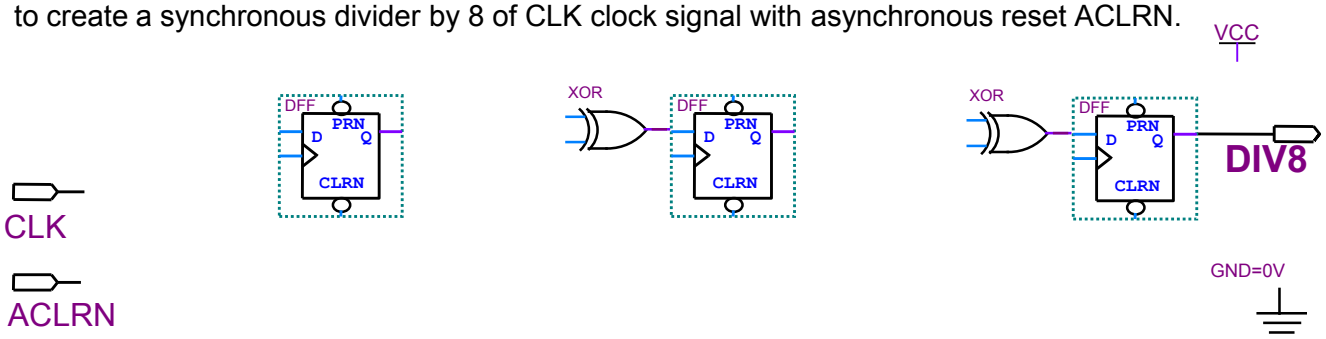
2

4

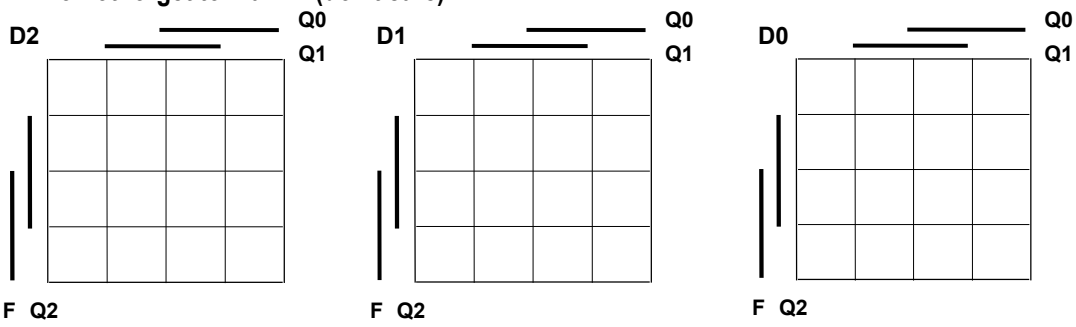
6

Part 1
26

7. Add gates and wires to the unfinished diagram below, you do not need to use everything in picture, to create a synchronous divider by 8 of CLK clock signal with asynchronous reset ACLRN.



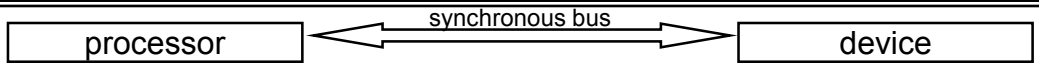
8. **Write Karnaugh maps of D0, D1, D2 inputs of DFF flip-flops to create 3-bit synchronous counter from 0 to 4, that counts up Q2, Q1, Q0 = 000,001, 010,011,100, *000, 001, 010*... atd.) if F=0. Otherwise, if F=1, that it counts down. Do not forget to mark X (don't care).**



9. *An editor **ask you if you could analyze wrong formatted VHDL code:***

```
library ieee; use ieee.std_logic_1164.all;
entity XXX is port(  A, B, C, D : in std_logic; Q : out std_logic ); end;
architecture rtl of XXX is  constant E:std_logic:='0'; begin  process (A, D)
variable qv:std_logic;  begin  if D='0' then qv:=E;  elsif rising_edge(A) then
if C='1' then qv:=B; else  qv:=not qv; end if;   end if;  Q<=qv;  end process; end rtl;
```

Draw a logical circuit diagram corresponding to this VHDL code and give it appropriate title that describes its function. Guide: First, rewrite this program in the correct formatting.



10. Add missing signals with their waveforms for synchronous bus. Signal WR = '1' denotes writing data into peripheral device and WR = '0' reading; Data is bi-directional signal. Data are first written to the device, then they are read from it. The dashed lines in the figure are auxiliary drawing grid.