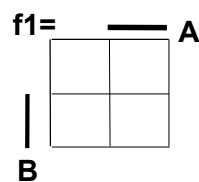
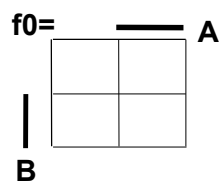
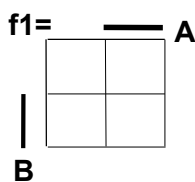
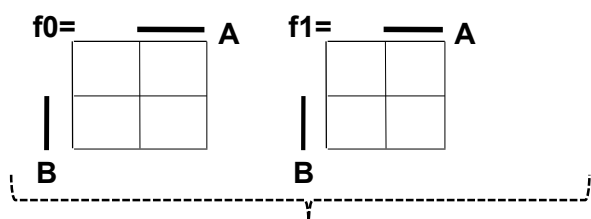


1. Funkce  $X, Y = f(A, B, C)$  obvodu, rozložte na tvar  $X, Y = (\text{not } C \text{ and } f_0(A, B)) \text{ or } (C \text{ and } f_1(A, B))$  pomocí Shannonovy expanze. Funkce  $f_0$  a  $f_1$  zapište jako Karnaughovy mapy:

X/3

$X, Y = f(A, B, C)$  function of the circuit, decompose into  $X, Y = (\text{not } C \text{ and } f_0(A, B)) \text{ or } (C \text{ and } f_1(A, B))$  using Shannon expansion. Functions  $f_0$  and  $f_1$  write down as Karnaugh maps:



Y/3

$$X = (\text{not } C \text{ and } f_0(A, B)) \text{ or } (C \text{ and } f_1(A, B))$$

$$Y = (\text{not } C \text{ and } f_0(A, B)) \text{ or } (C \text{ and } f_1(A, B))$$

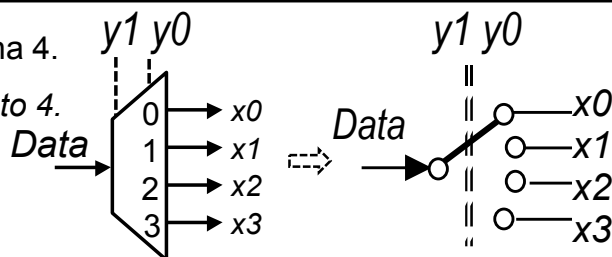
2. Provedeme-li operaci  $96+97+98+99$  na 8bitové sčítačce, jaký bude výsledek, budeme-li ho brát jako 8bitové číslo  
If we perform  $96+97+98+99$  by an 8-bit adder, what is its 8-bit result converted to a decimal number?

4

a) unsigned ..... b) signed in two's-complement.....

3. Nakreslete logické schéma demultiplexoru 1 na 4.


Draw the logical schema of a demultiplexer 1 to 4.



10

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A  X = ... ..  
t<sub>0</sub>..t<sub>1</sub>... t<sub>2</sub>..t<sub>3</sub>..t<sub>4</sub>..

$$t_{0..}|..t_{1...}|.. t_{2..}|..t_{3..}|..t_{4..}|..$$
[illegible]
$$Y = \dots \dots | \dots \dots | \dots \dots | \dots \dots | \dots \dots |$$
$$Y = \dots \dots | \dots \dots | \dots \dots | \dots \dots | \dots \dots |$$

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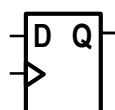
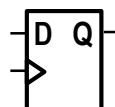
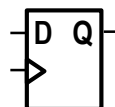
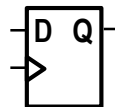
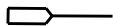
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7. Doplňte potřebné minimum součástek do nedokresleného schématu dole tak, aby vznikl **synchronní** dělič 16 hodinového signálu CLK. (Návod: použijte sčítačku +1)  
 Fill the required minimum components into the unfinished scheme below to create a **synchronous** divider by 16 of CLK signal. (Instructions: Use +1 Adder)

CLK

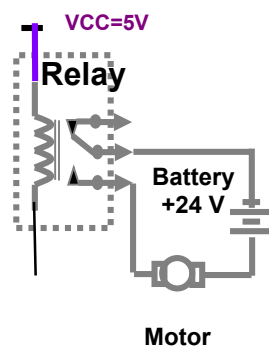


DIV16

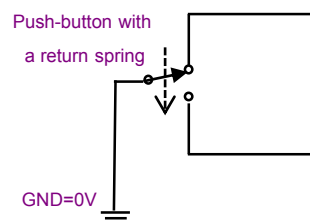
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8. Nakreslete obvod, který při jednom stisku dvoupólového tlačítka zapne motor a následujícím stiskem téhož tlačítka ho vypne. Totéž lze opakovat. Motor musí být vždy **po zapnutí napájení ve stavu vypnuto!**  
 Draw a circuit that turns on the motor after pushing the two-pole button. When we press the button again, the motor stops. The motor must always be off when we switch on the power supply!



Motor



5



**9. Prémiová otázka, u níž se uzná jen plně funkční řešení:**

Výstup Y jde do '1' na 1 cyklus hodin CLK jen tehdy, když D vstup změnil svou hodnotu.

RESET značí synchronní nulování, Y bude během něho '0'. Poté opět reaguje až na nové změny D.

**Premium question** for which only a fully functional solution is accepted:

Output Y goes to '1' for 1 CLK clock cycle only when D input has changed its value.

RESET indicates synchronous resetting, and Y will be '0' during it. Then, it reacts again to new changes of D.

library ieee; use ieee.std\_logic\_1164.all; use ieee.numeric\_std.all;

entity Edges is port (clk, Reset, D : in std\_logic; Y:out std\_logic);

end entity;

architecture rtl of Edges is

end architecture;