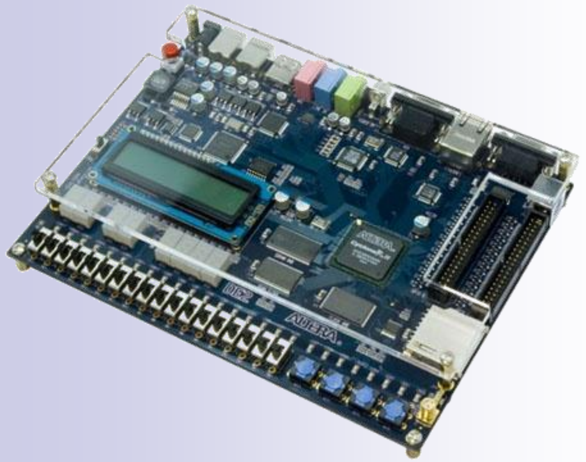
Logic Systems and Processors
cz:Logické systémy a procesory

Lecturer: Richard Šusta

richard@susta.cz, susta@fel.cvut.cz,
+420 2 2435 **7359**



Version V1.0

CTU-FEE in Prague, CR – subject BE5B35LSP

Stable Combinational Loops in

SRAM MEMORIES

Terminology

- Types: RWM (RAM), ROM, FLASH, SSD
- **RAM** = **R**andom **A**ccess **M**emory or **RWM** = **R**ead **W**rite **M**emory
- RAM memories:
  SRAM (Static), **DRAM** (Dynamic).

Type	CMOS	Area per cell	Access	First Reads/Writes Latency
SRAM	cca 6 to 8	**~140 F^2**	always	**< 1ns – 5ns**
DRAM	**1**	**6 to 10 F^2**	requires refresh	**25 ns – 40 ns**

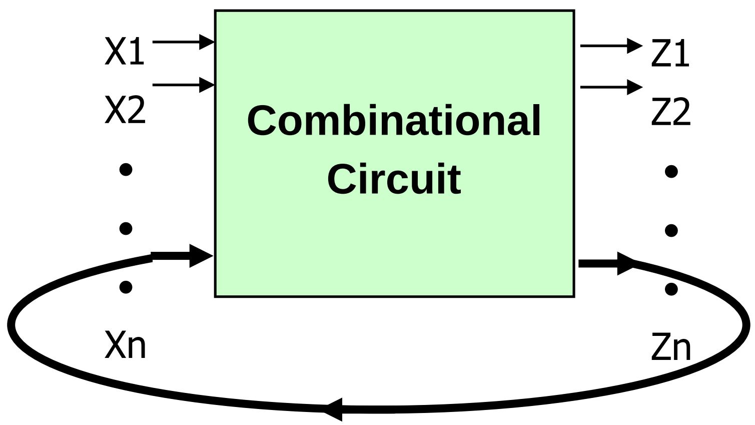
F^2 - 2D Feature - the smallest dimension realizable by a used technology

Notes:

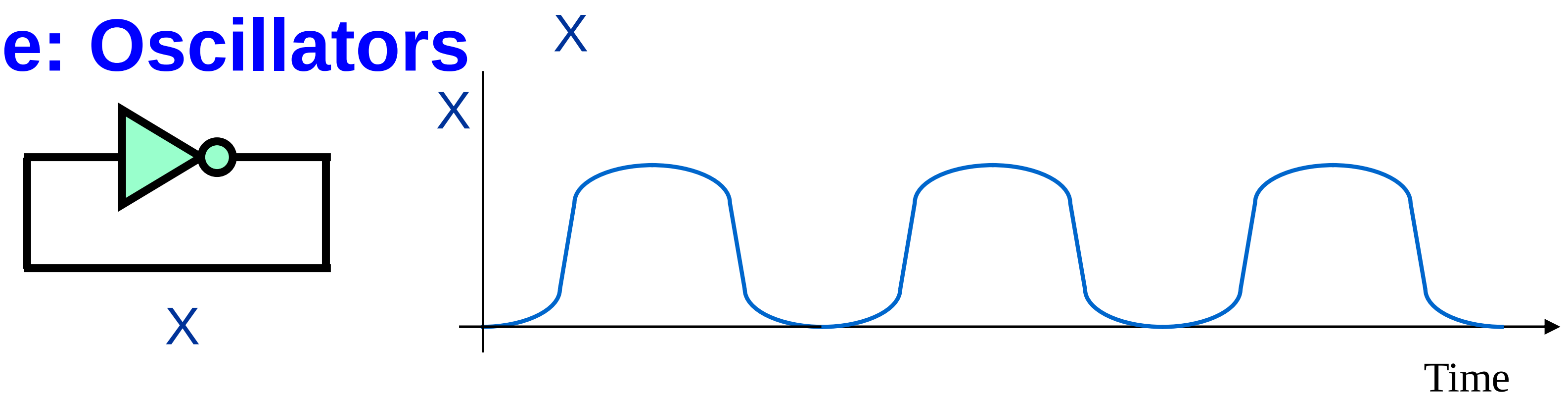
1) **SSDs or Flashes**, even the fastest ones, have their first read latencies in tens of microseconds and write times in the hundreds of microseconds.
   In FPGA, they are used to configure static interconnects between elements but are too slow as working memories.
2) **DRAM** productions need unique technology processes
   ⇒ It is difficult to integrating with technologies of logic circuits
3) **DDRx** memories accelerate only sequential readings/writings.
   Their first read/write latencies are slower.

We will deal with DRAMs and DDRx
in the lecture about processor memories.

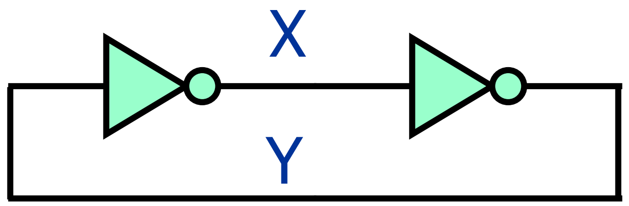
Combinational Loops



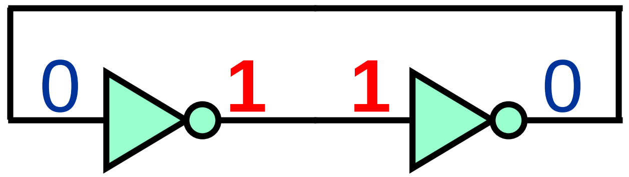
Unstable: Oscillators

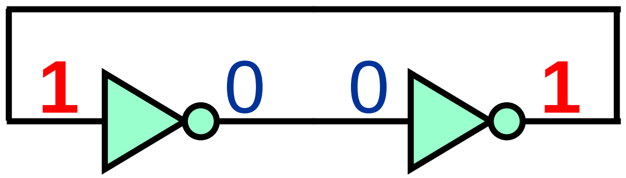


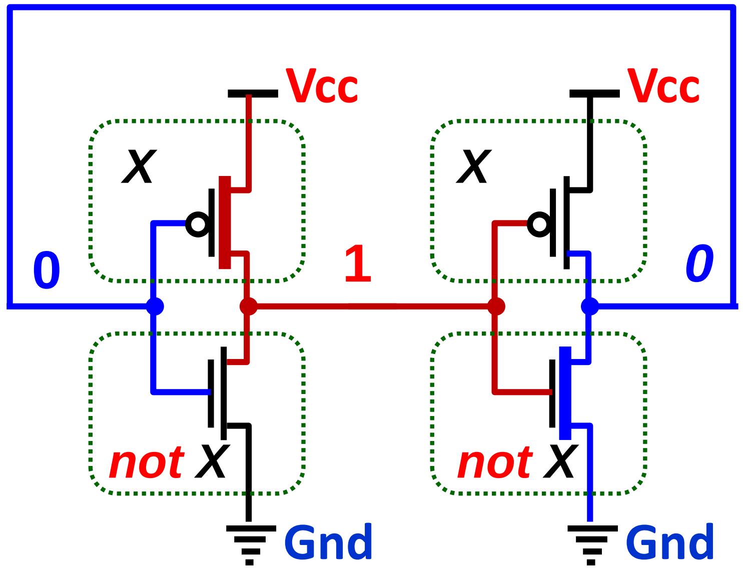
Stable: SRAMs

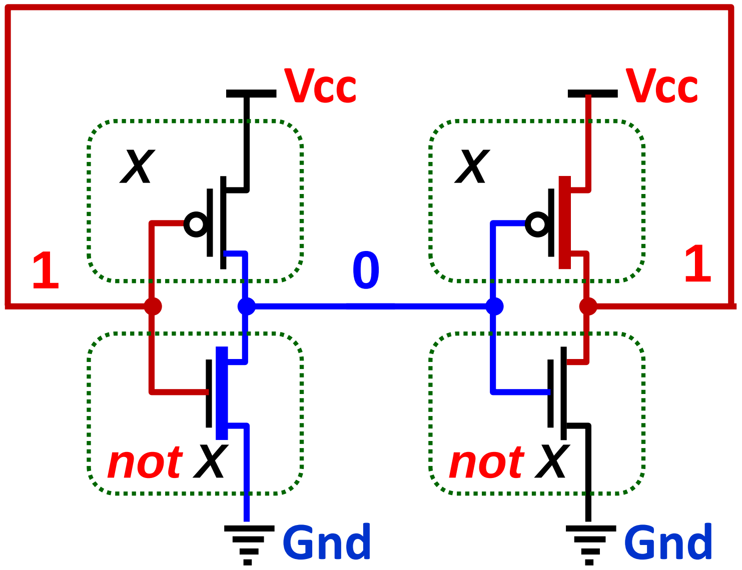


SRAM Stable Combinational Loop

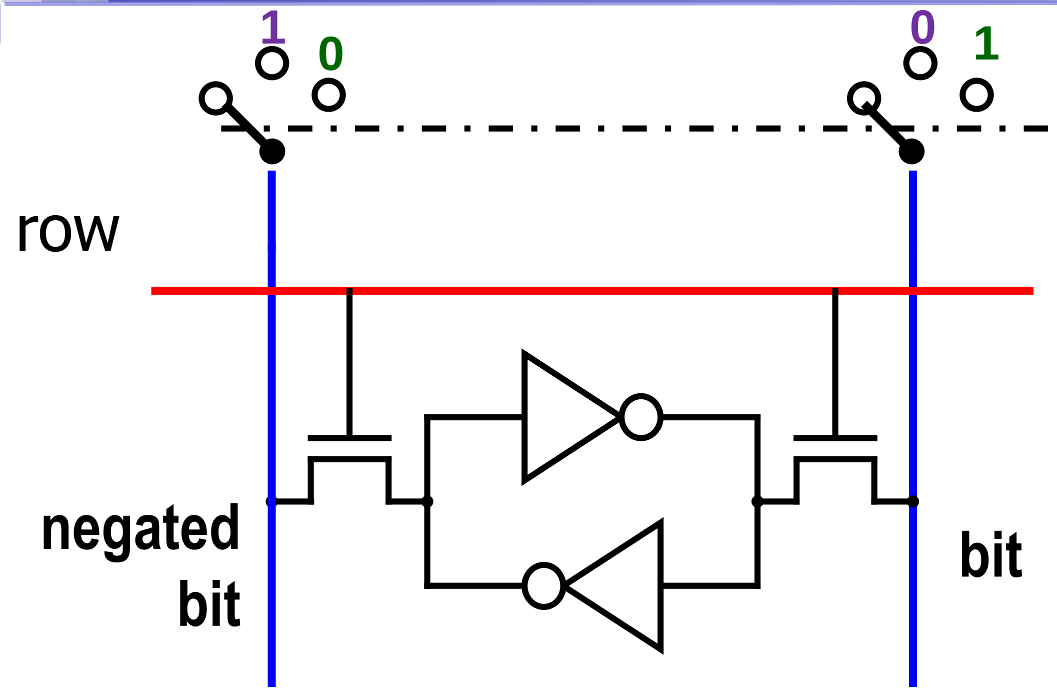






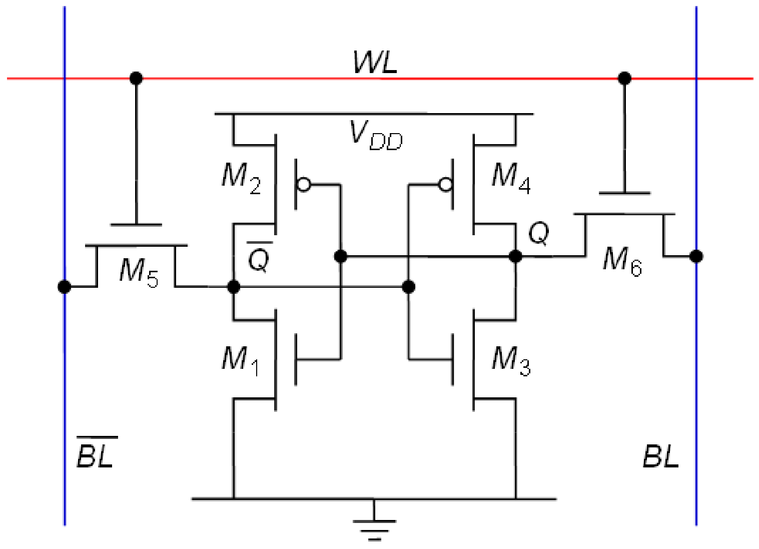


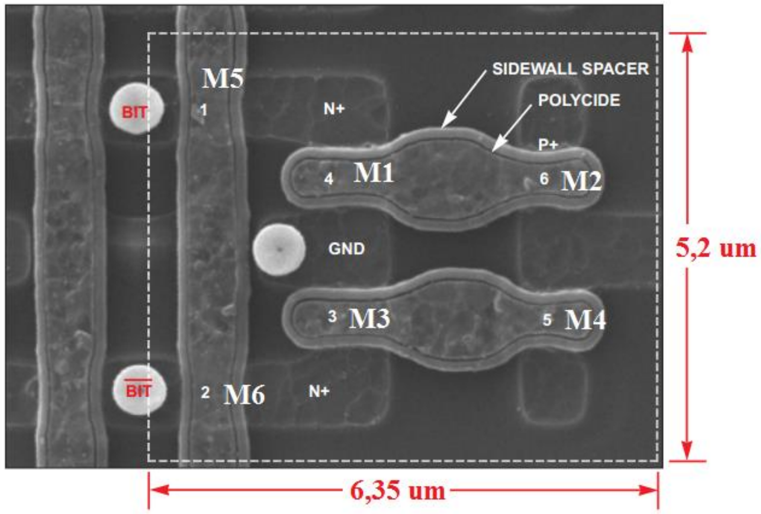
One SRAM Memory Cell



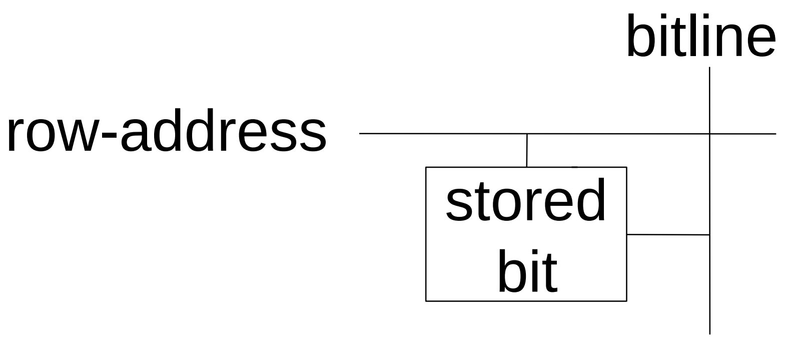
read | write 0 | write 1

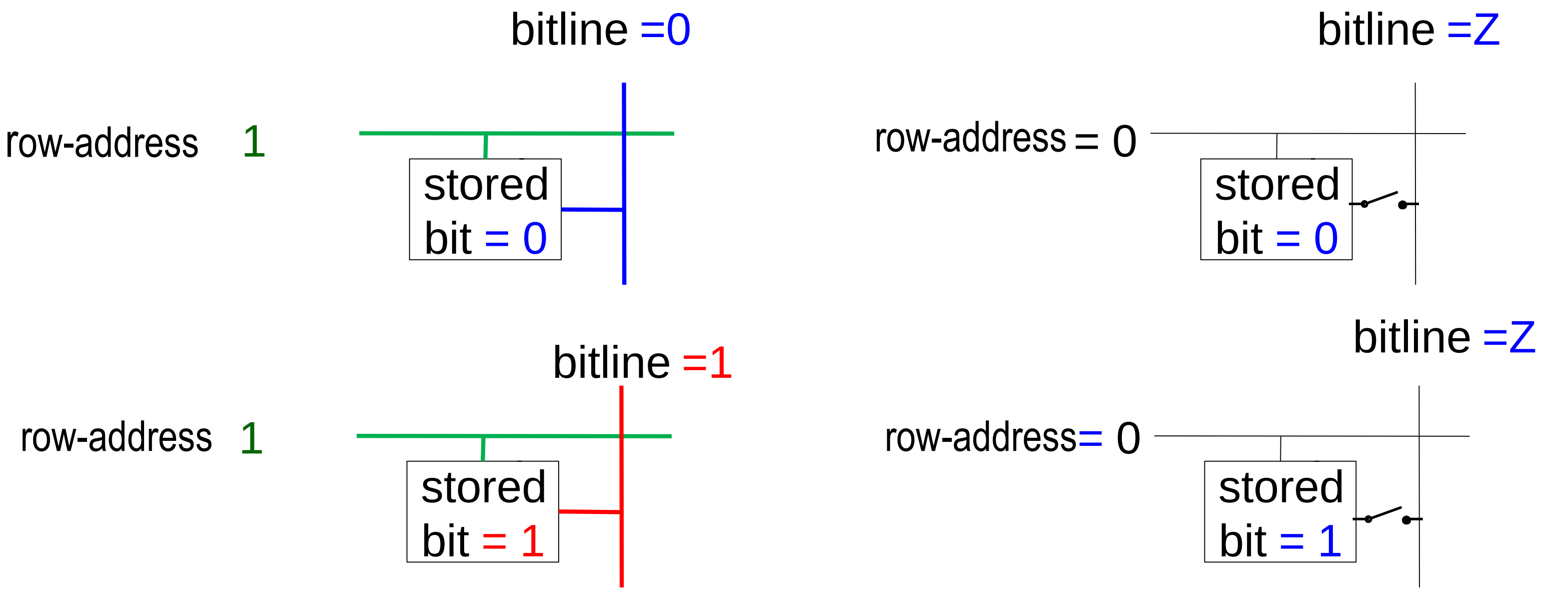
Two bit lines, positive and negated, ensure that at least one CMOS has good voltage conditions in each state of the invertor memory loop.





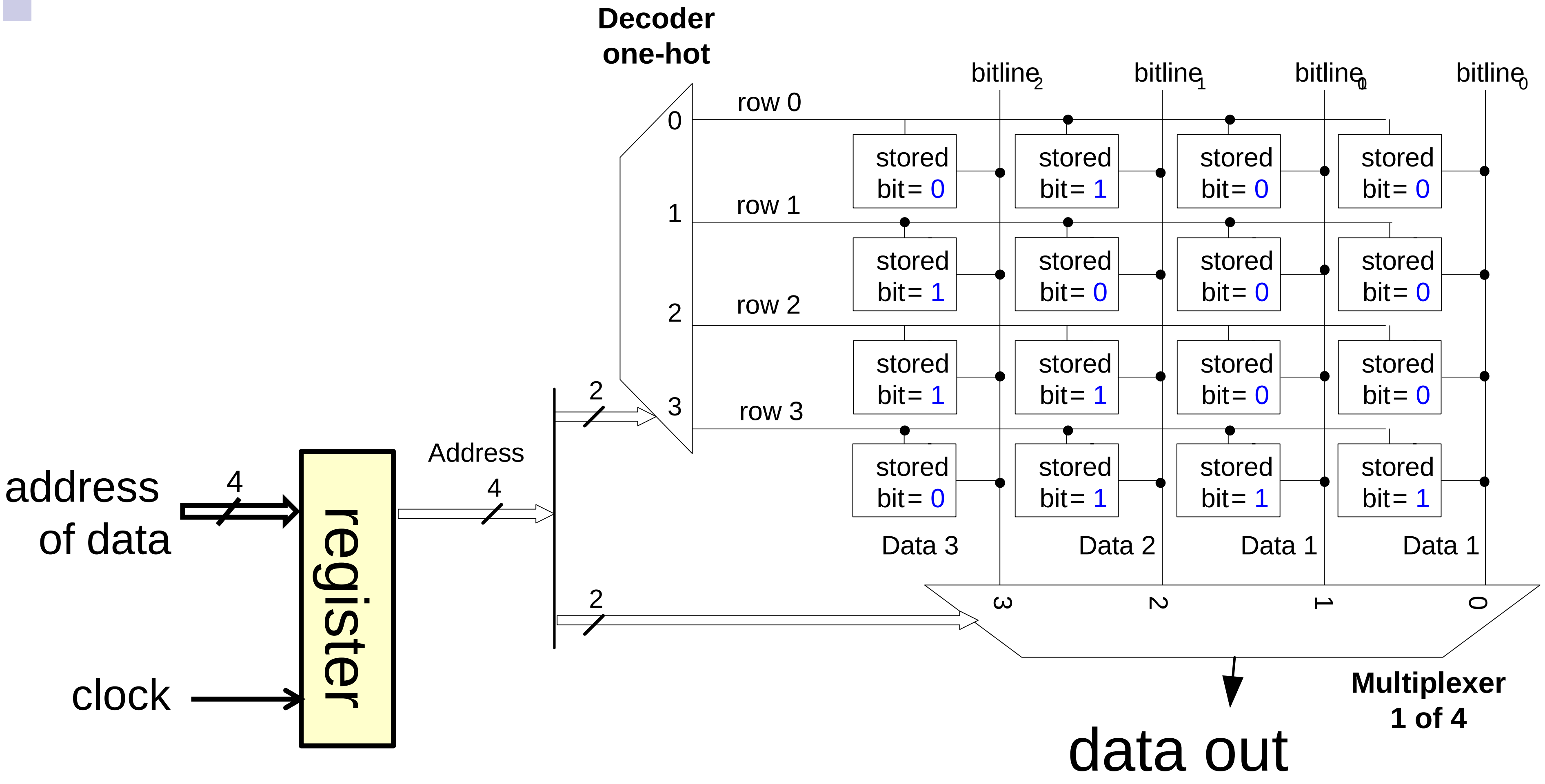
Simplified Memory Cell





MATRIX OF MEMORY CELLS

Memory Matrix



Register of address is a necessary condition for the implementation and to reduce power consumption

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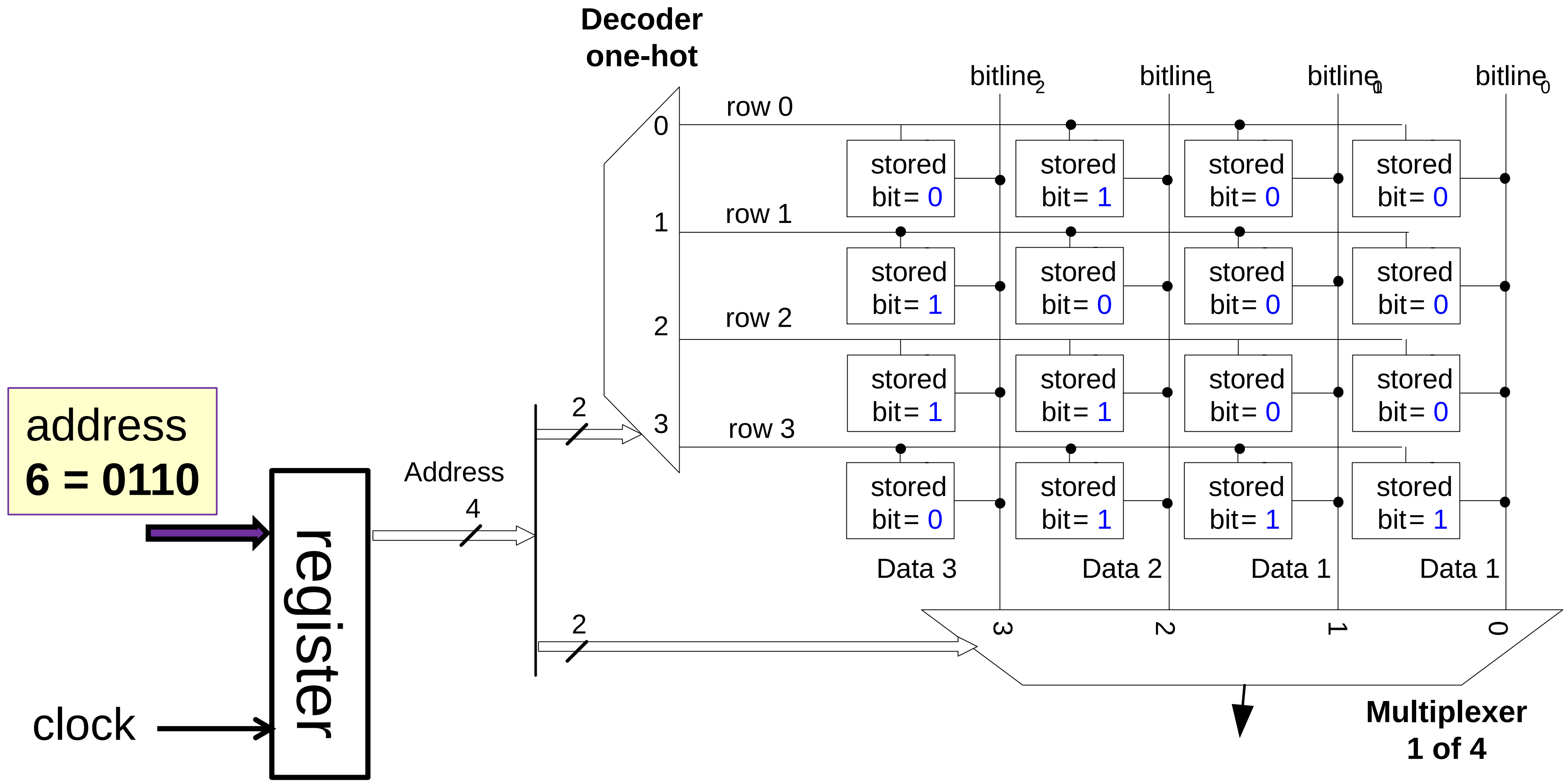
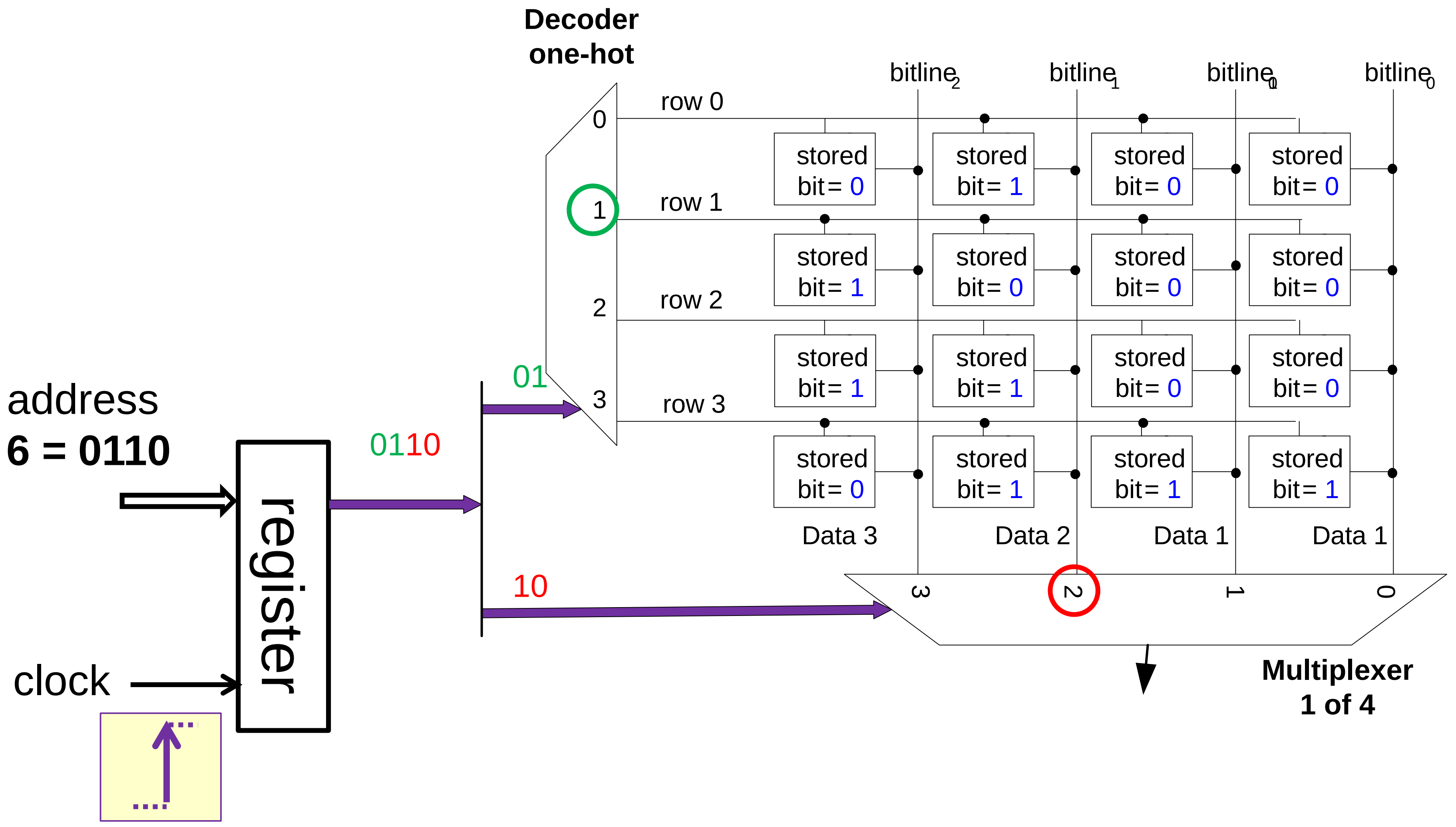
Memory Matrix - Example 1/4



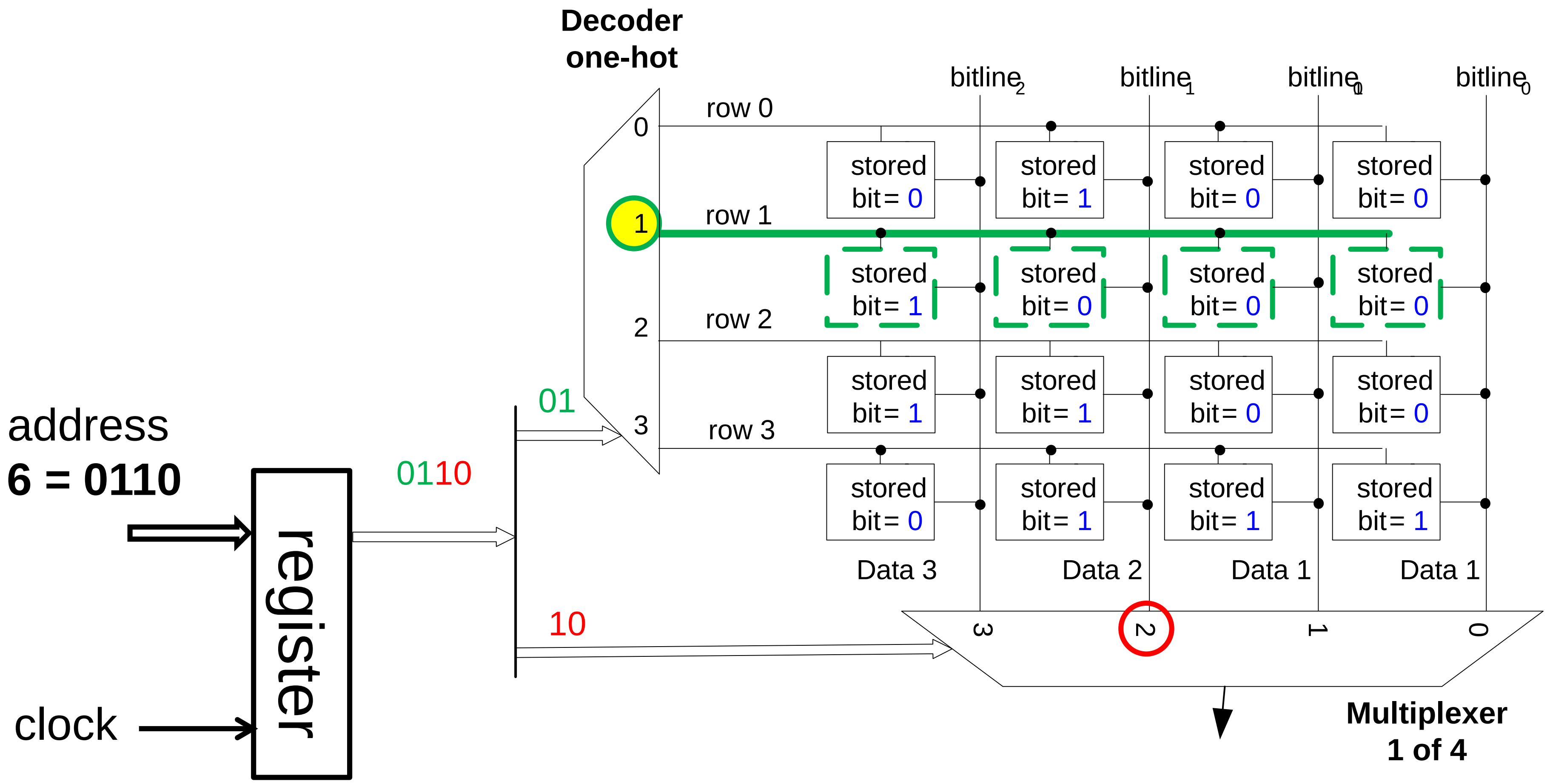
Address value is waiting for the rising edge of clocks

Memory Matrix - Example 2/4



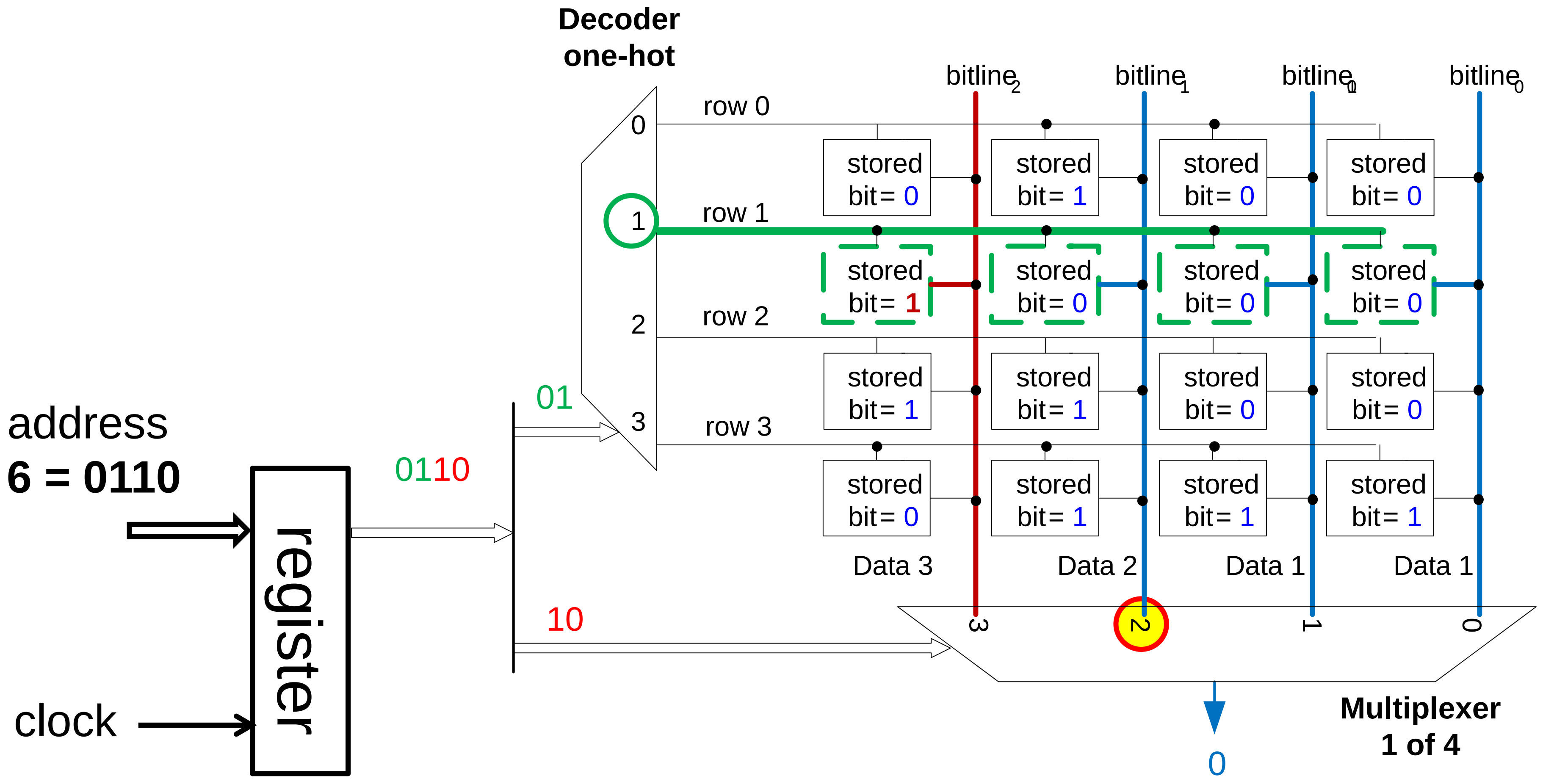
Address was loaded on the rising edge of clocks and divided to two parts, higher and lower bits

Memory Matrix - Example 3/4



Output of one-hot decoder 1 from N aktivate row and of cell in it.

Memory Matrix - Example 4/4



The cells are connected to bitlines, but the output multiplexer selects only one value - Data 2 = 0

ROM (read-only) memory by logic cells

On Cyclone II, it is mostly implemented by multiplexers 1 from 16, then 1bit memory type N x 1 requires>

- 16 x 1 : 1 row, 1 multiplexer
- 256 x 1 : 2 rows, 16+1=17 mux (multiplexers).
- 4 kbit =2^{12} x 1 : 3 rows, 256+16+1= 273 mux.
- 64 kbit = 2^{16} x 1 : 4 rows, 4096+256+16+1 = 4369 mux.
- 1 Mbit =2^{20} x 1 : 5 rows, 65536+4096+256+16+1 = 69905 mux.

cca 1/15 memory capacity must be added for selection logic.

For larger storage, it is too ineffective to use multiplexers that always select data even if they are not in use.

ROM (read-only) memory

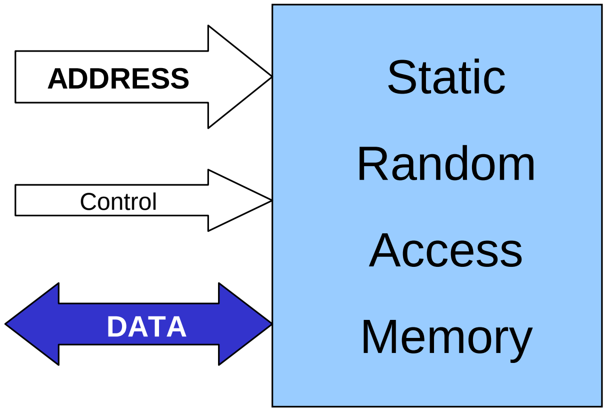
A memory matrix with 16 input multiplexers and decoders 1 from 16 requires for 1 bit memory N x 1

- 256 x 1 - 2 rows, 1 multiplexer + 1 decoder1 z N = 2 LE
- 64 kbit = 2^{16} x 1 - 4 rows, 17 mux + 17 dec. = 34 LE.
- 16 Mbit =2^{24} x 1 - 6 rows, 273 mux + 273 dec. = 546 LE.

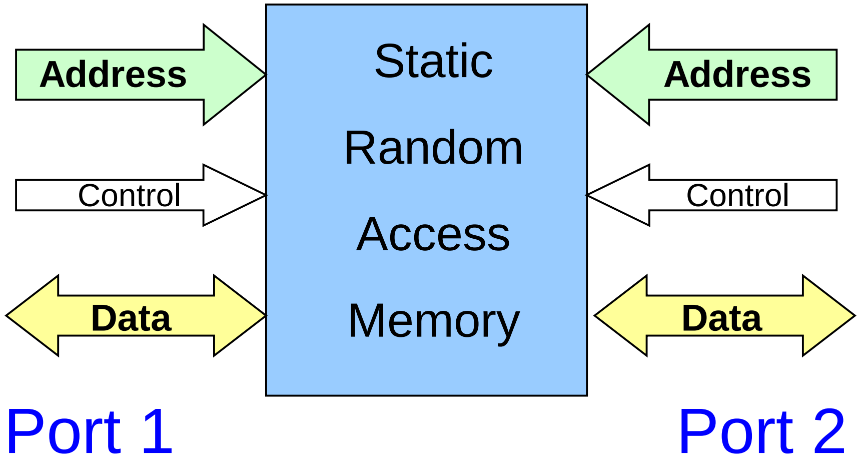
Selection logic was significantly reduced and requires less power, because we activate only one 16x16 matrix.

1 Port - 2 Port

1 port SRAM



2 port SRAM
- it doubles read/write logic



Memories always require address register

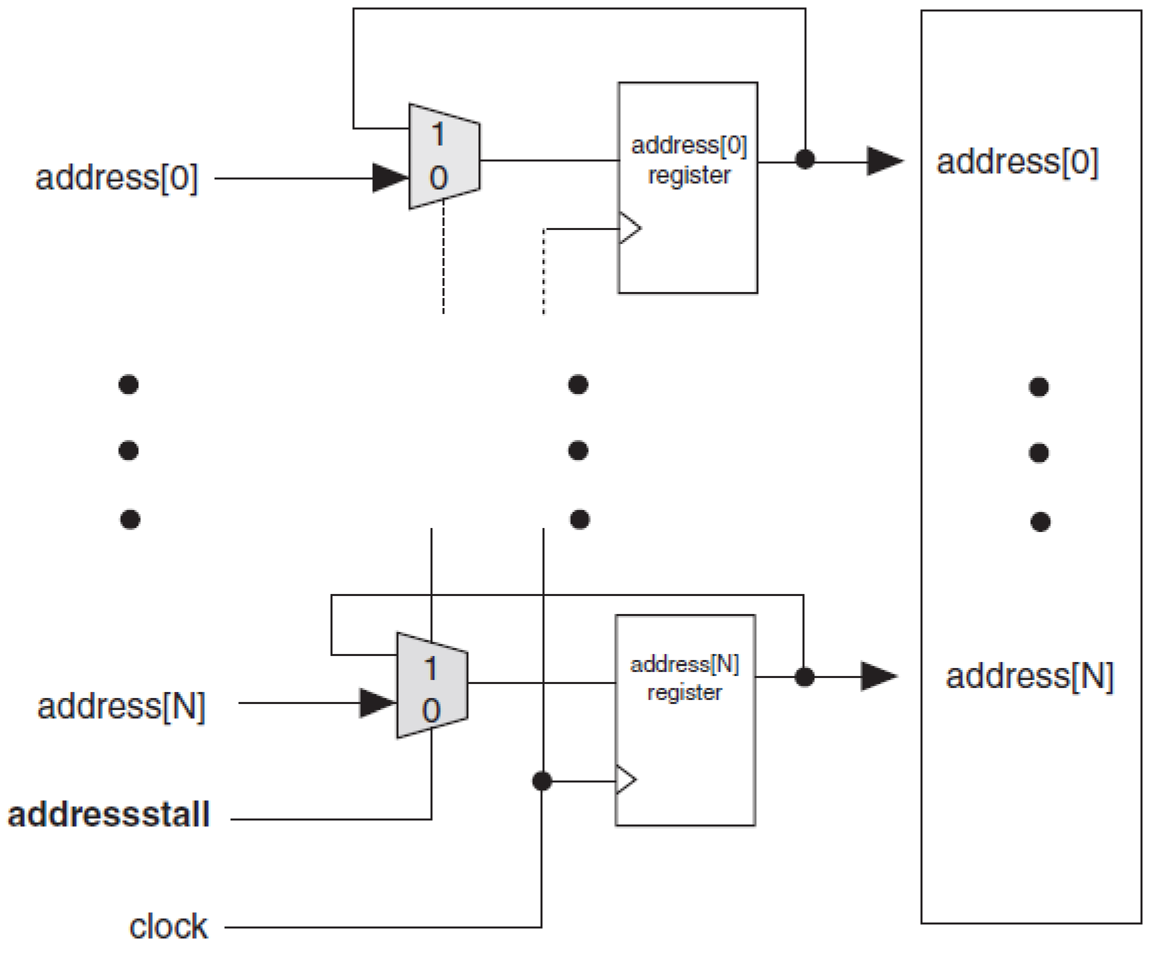
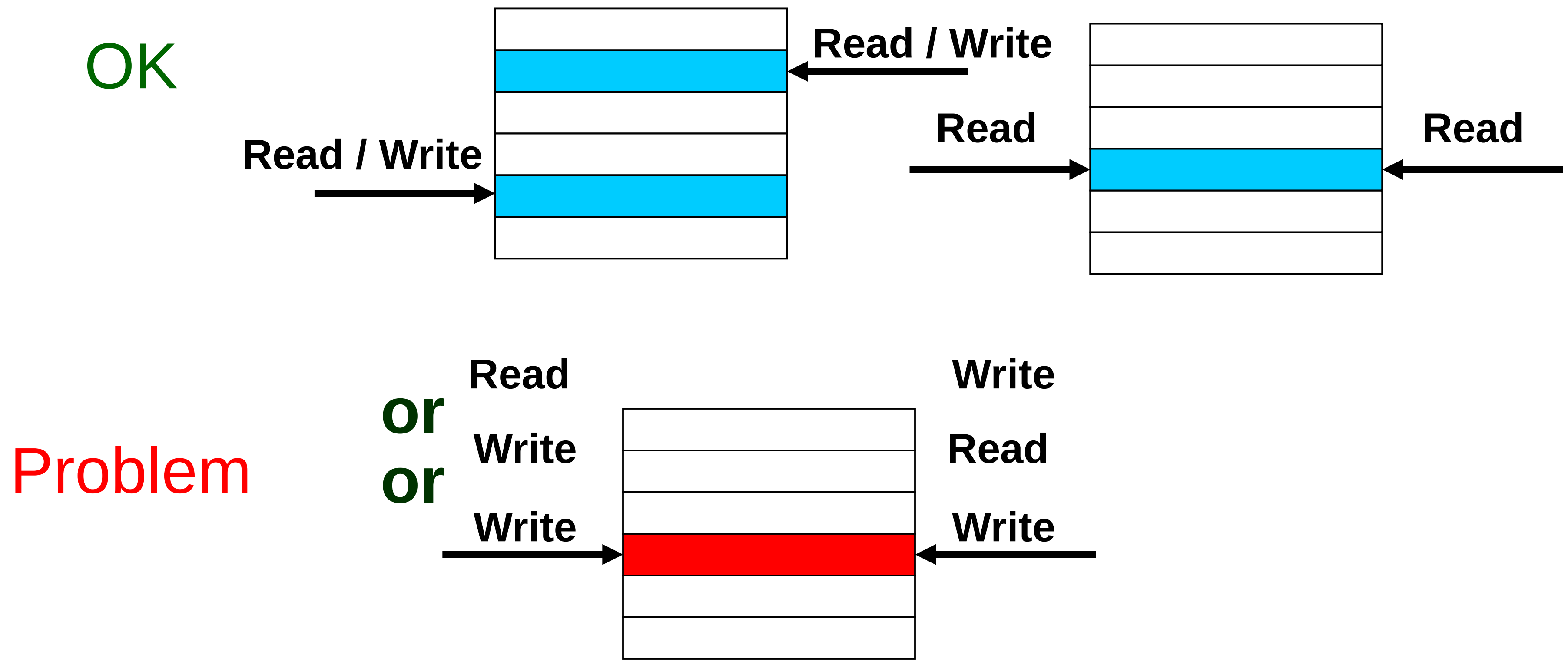


Image source: Intel

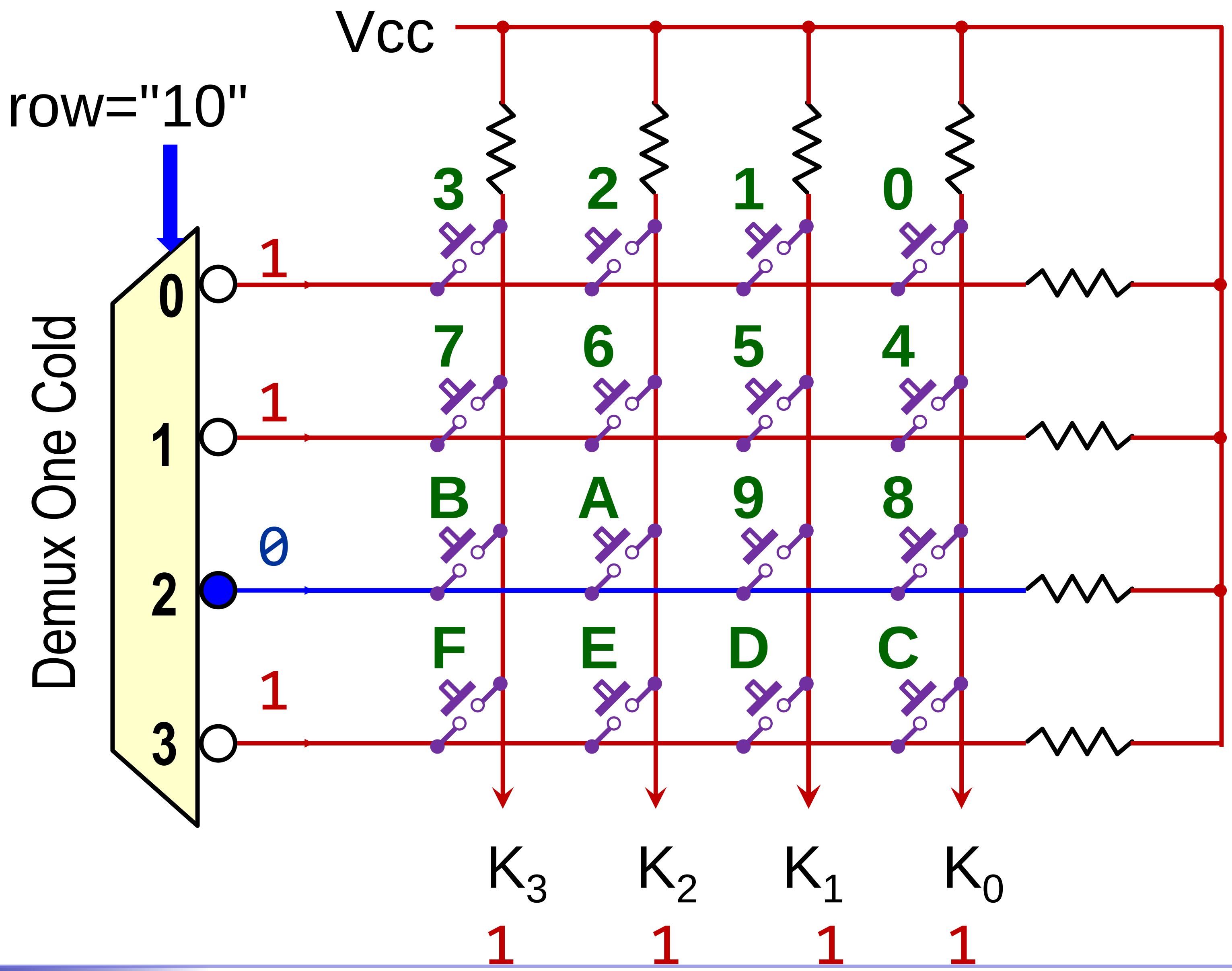
Simultaneous Access



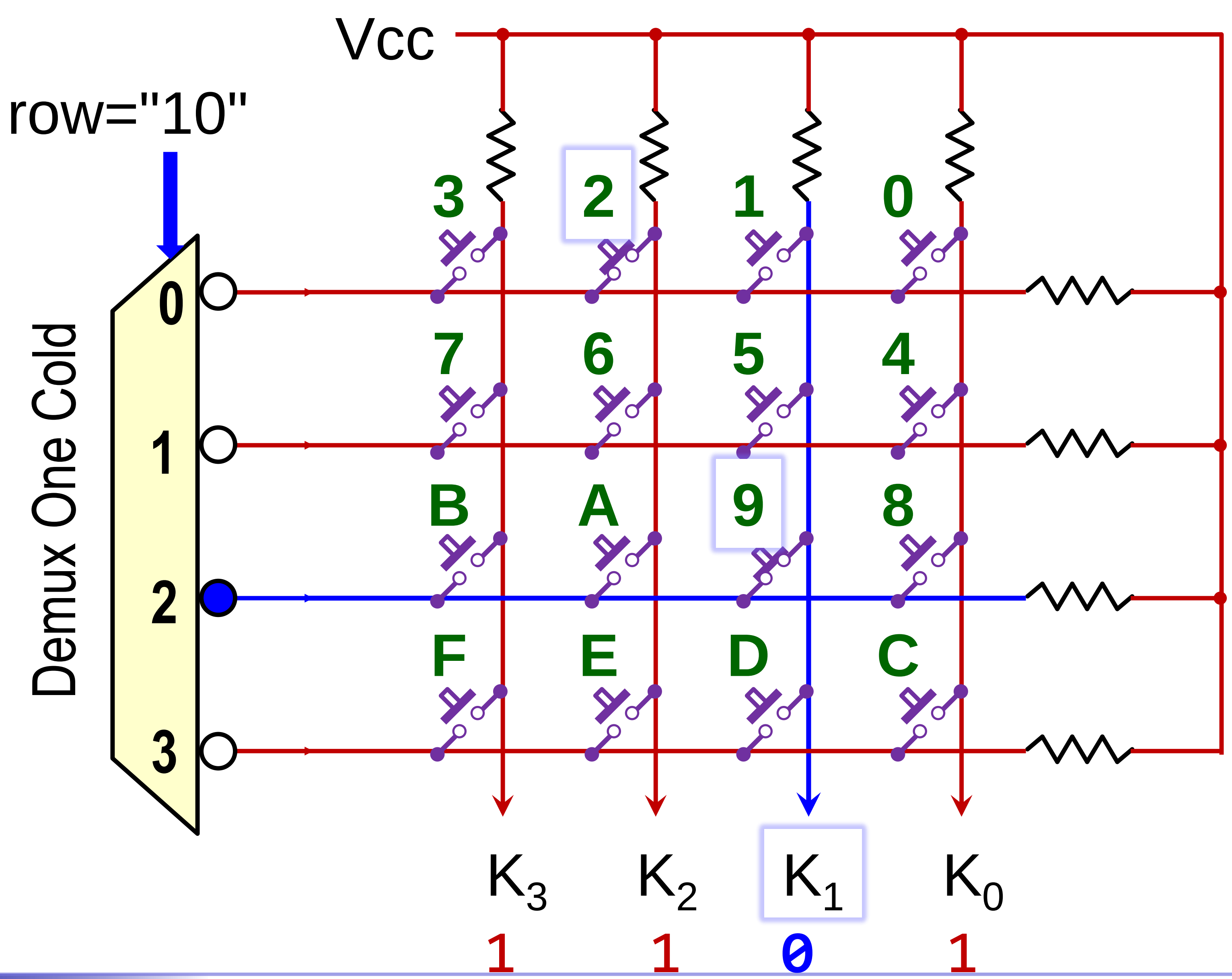
Cyclone family SRAM

Read & Write to the same address returns old data, but only if clocks are the same, otherwise the result is unknown

Reading Hex Keyboard by Matrix



Reading Hex Keyboard by Matrix



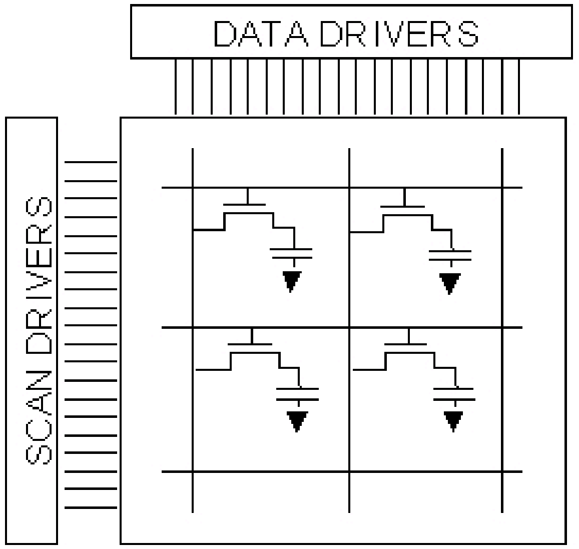
LCD - Liquid Crystal Display

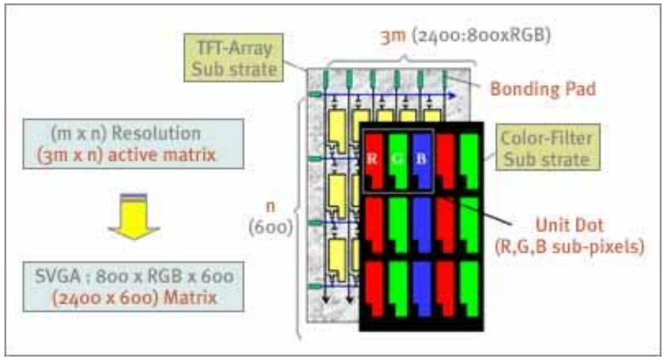
precisely TN LCD (Twist Nematic Liquid Crystal Display)
also uses a memory matrix

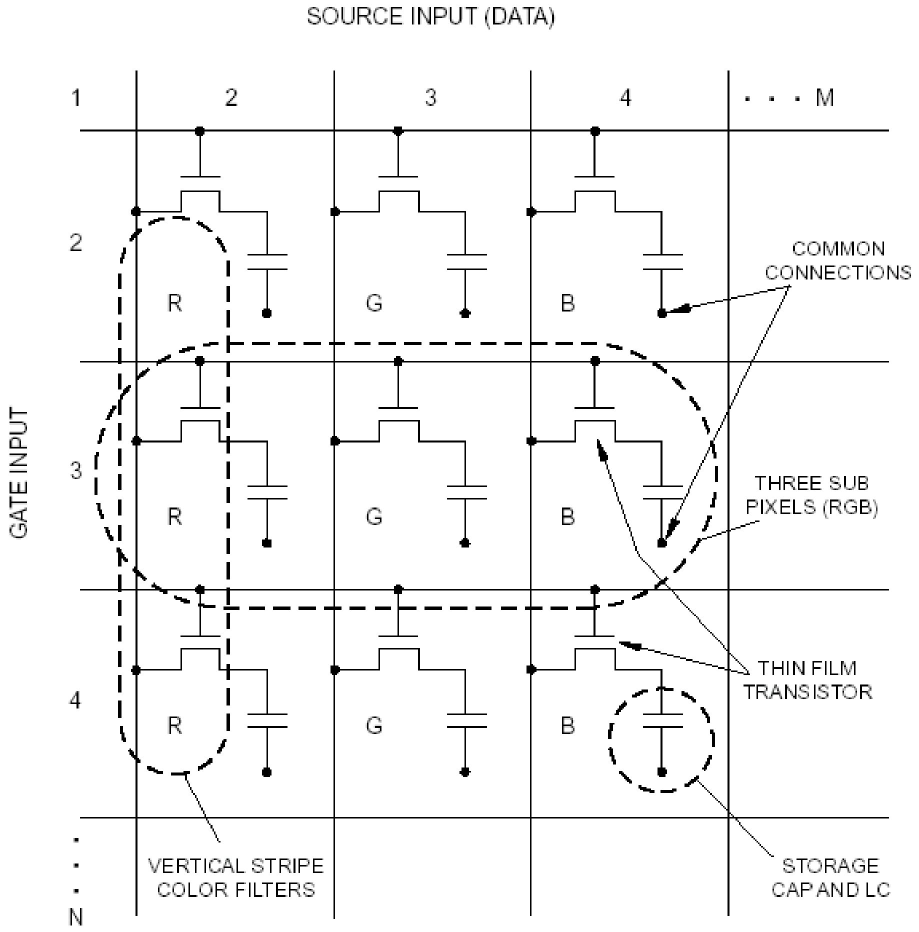
LSP course is also about the principles of modern digital systems, so we briefly look inside the topic of the third training task

Image: Terasic

TFT (Thin-Film Transistors) with active matrix



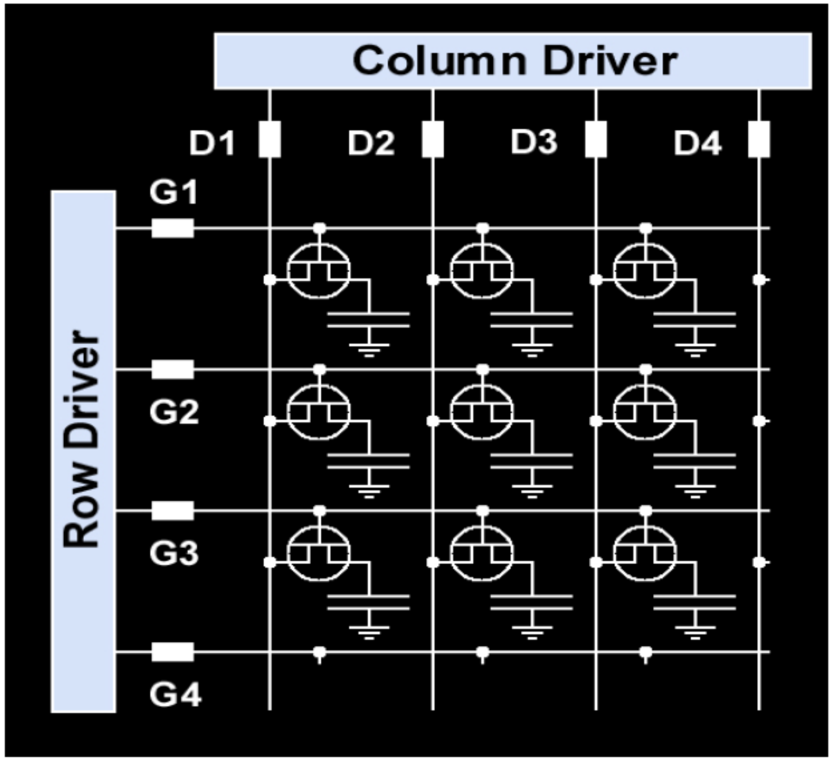




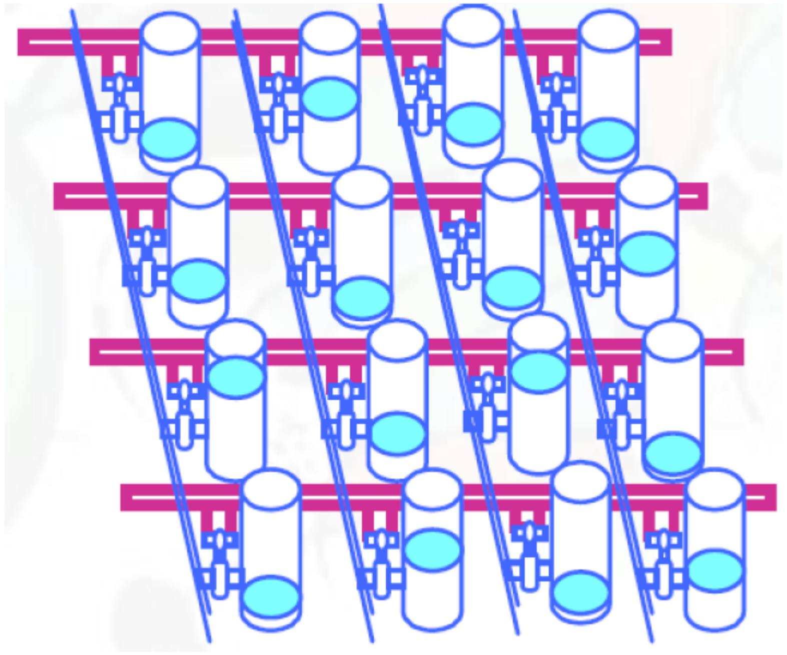
Source: Matrix

LCD capacitors distinguish multiple levels!

TFT (switch) + LC cell (capacity)

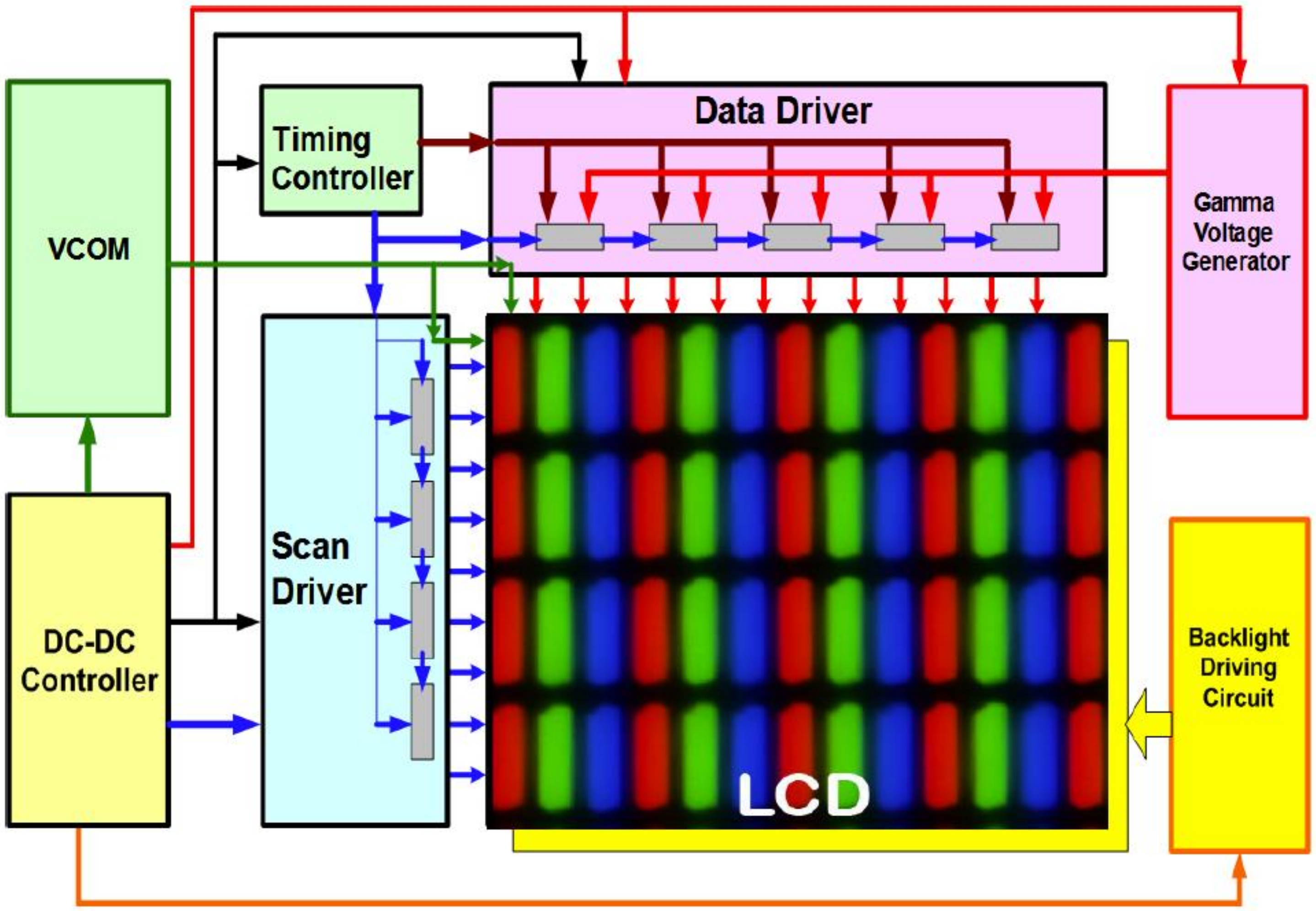


Hydrant (switch)+ Bucket (capacity)



Source: Dr. Zhibing Ge, College of Optics and Photonics

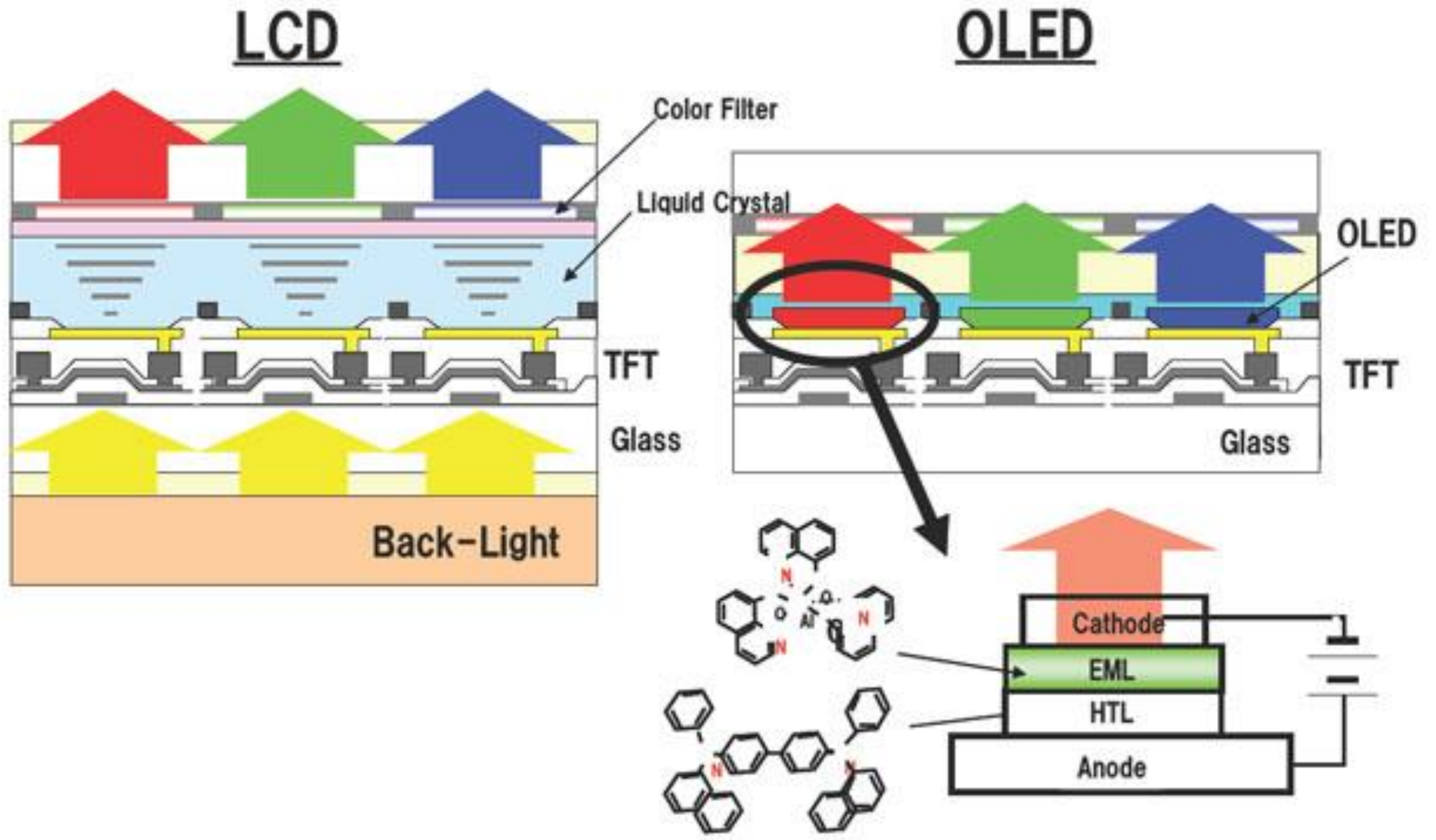
LCDs write whole lines



Source: Dr. Zhibing Ge, College of Optics and Photonics

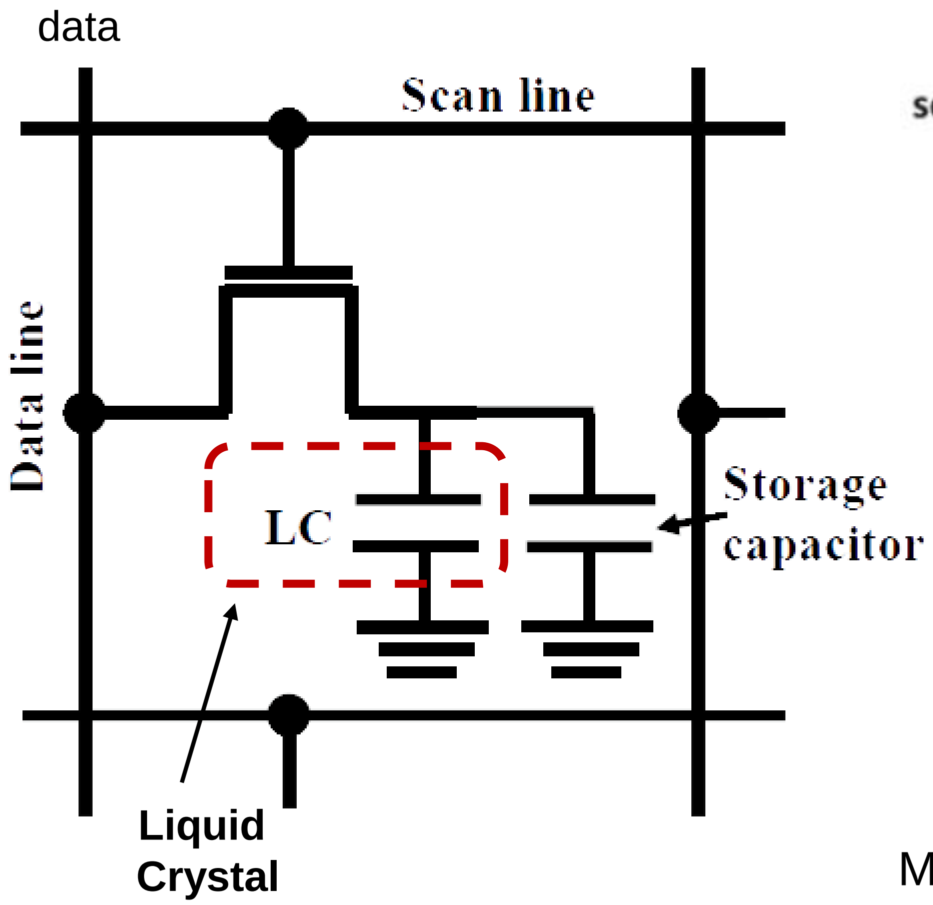
LCD versus OLED types

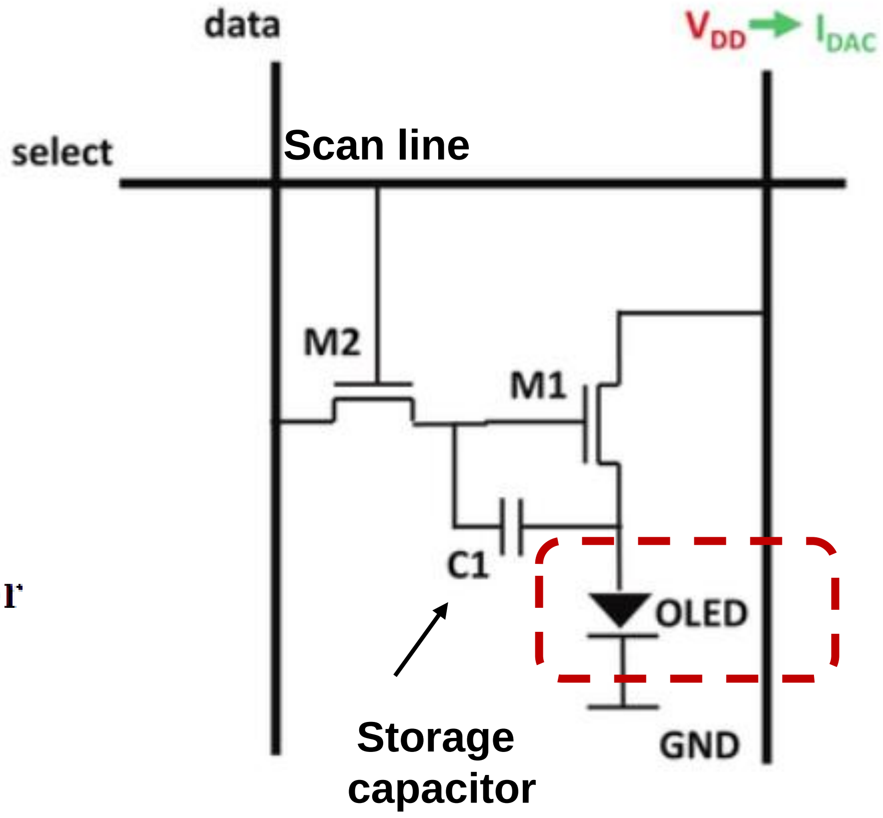
TN, IPS <-technologies-> AMOLED, PMOLED



Source: https://www.androidauthority.com/

LCD versus OLED



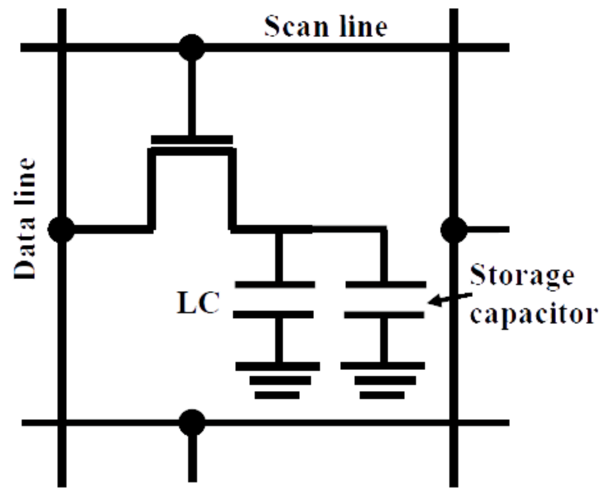


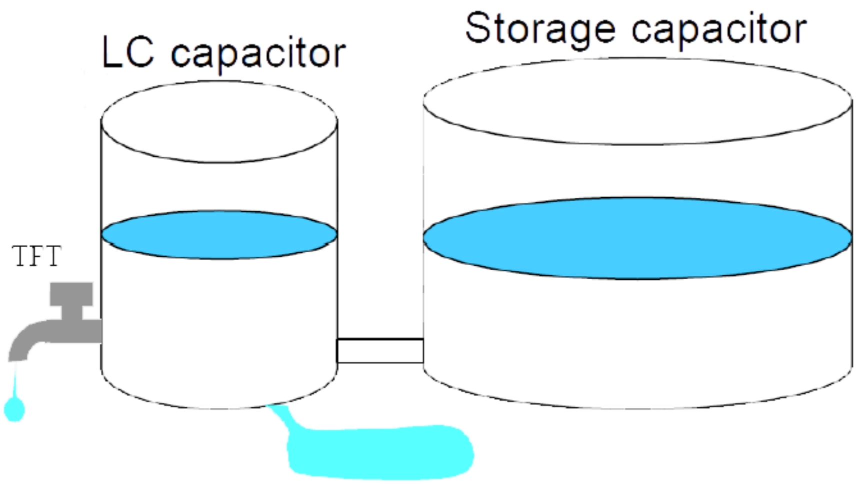
M1 NMOS powers the OLED according to the voltage of capacitor C1.

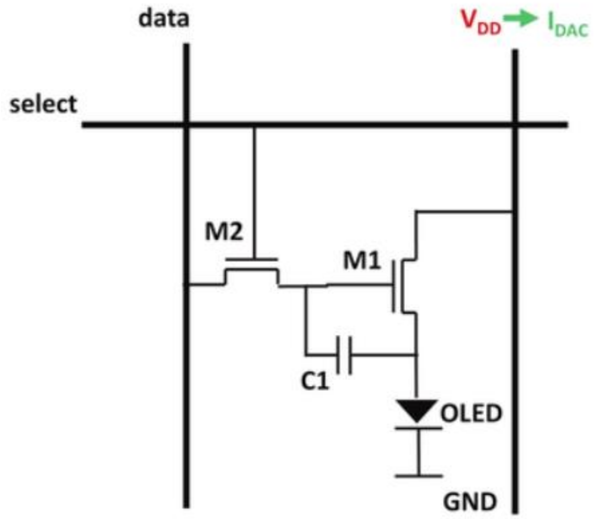
Source: Digital PWM-driven AMOLED display…, 2014 IEEE International Solid- State Circuits Conference (ISSCC)

LCD versus OLED - Refreshing

LCD TFT

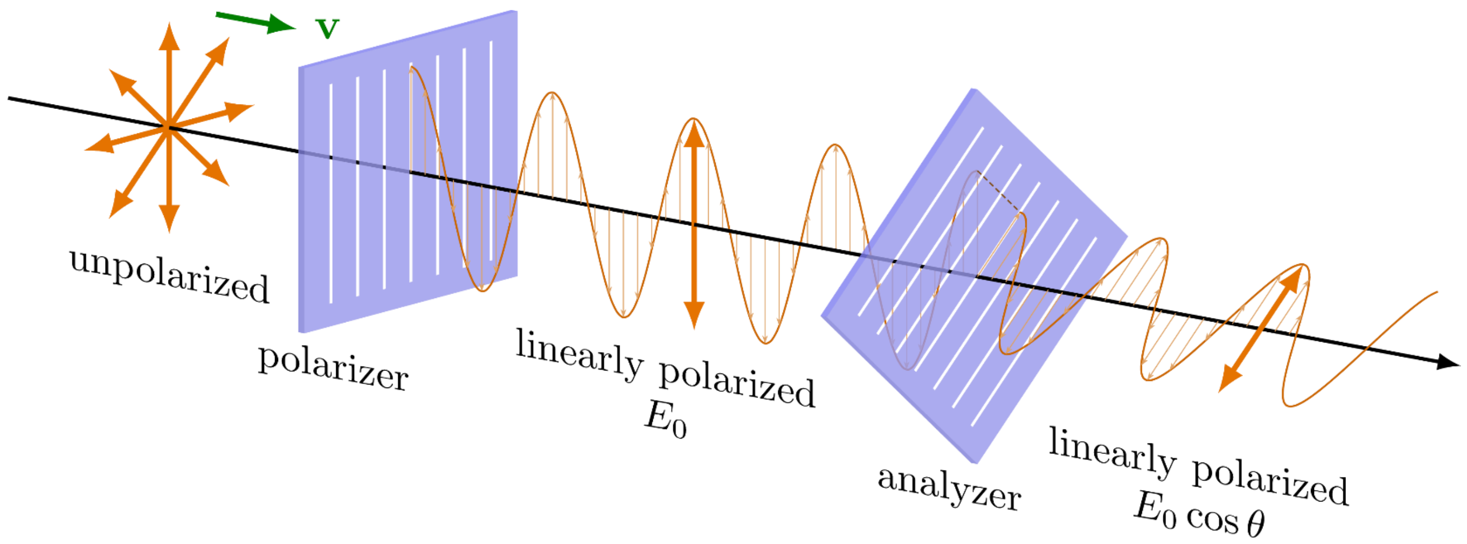


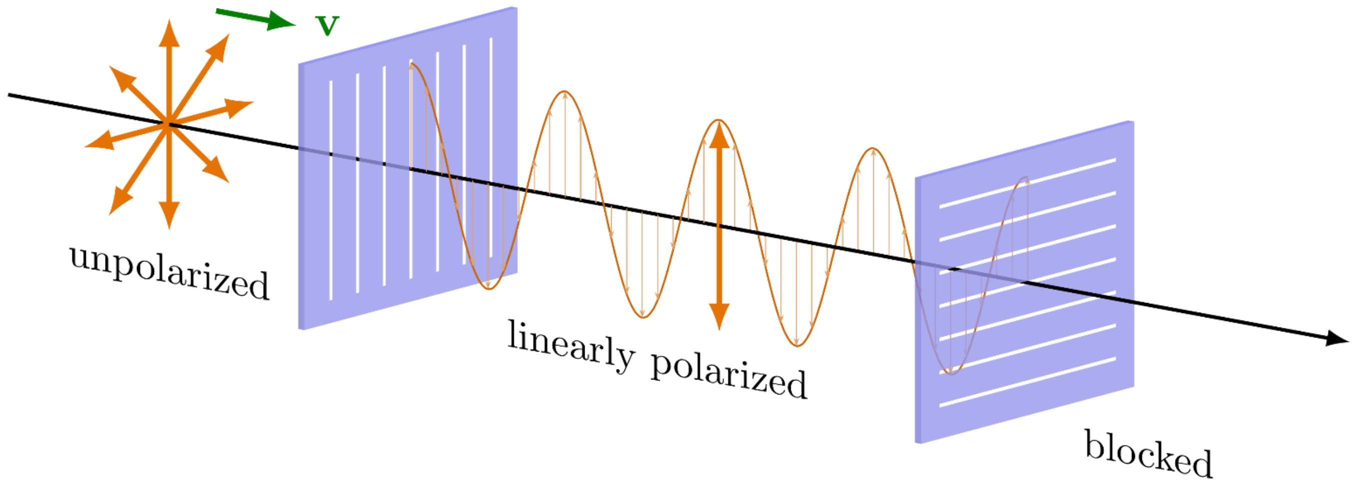




The capacitors need **regular refreshes**. Their typical values range from 100 fF (=0.1pF) to 2000 fF (=2pF).

Linear Polarization





Source: https://tikz.net/optics_polarization/

LCD Principle

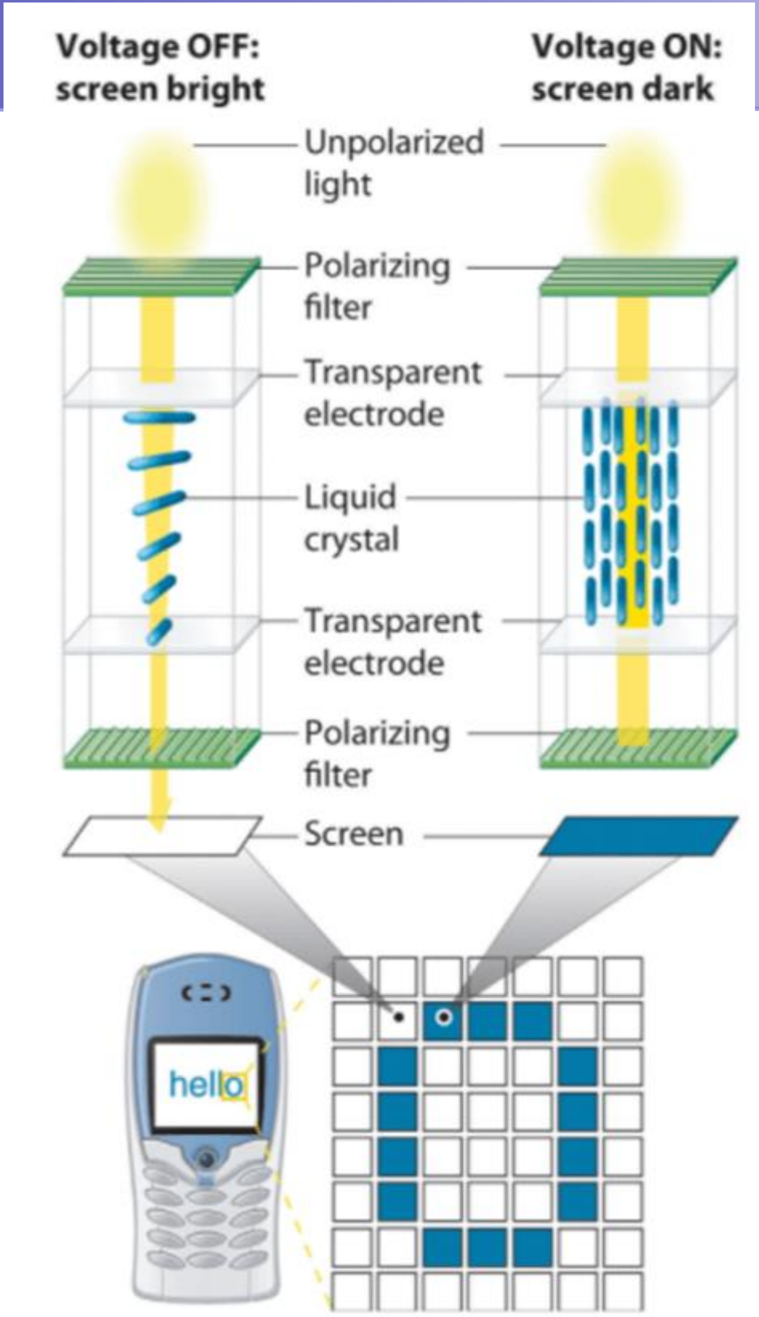


Image source:

ORIENT DISPLAY
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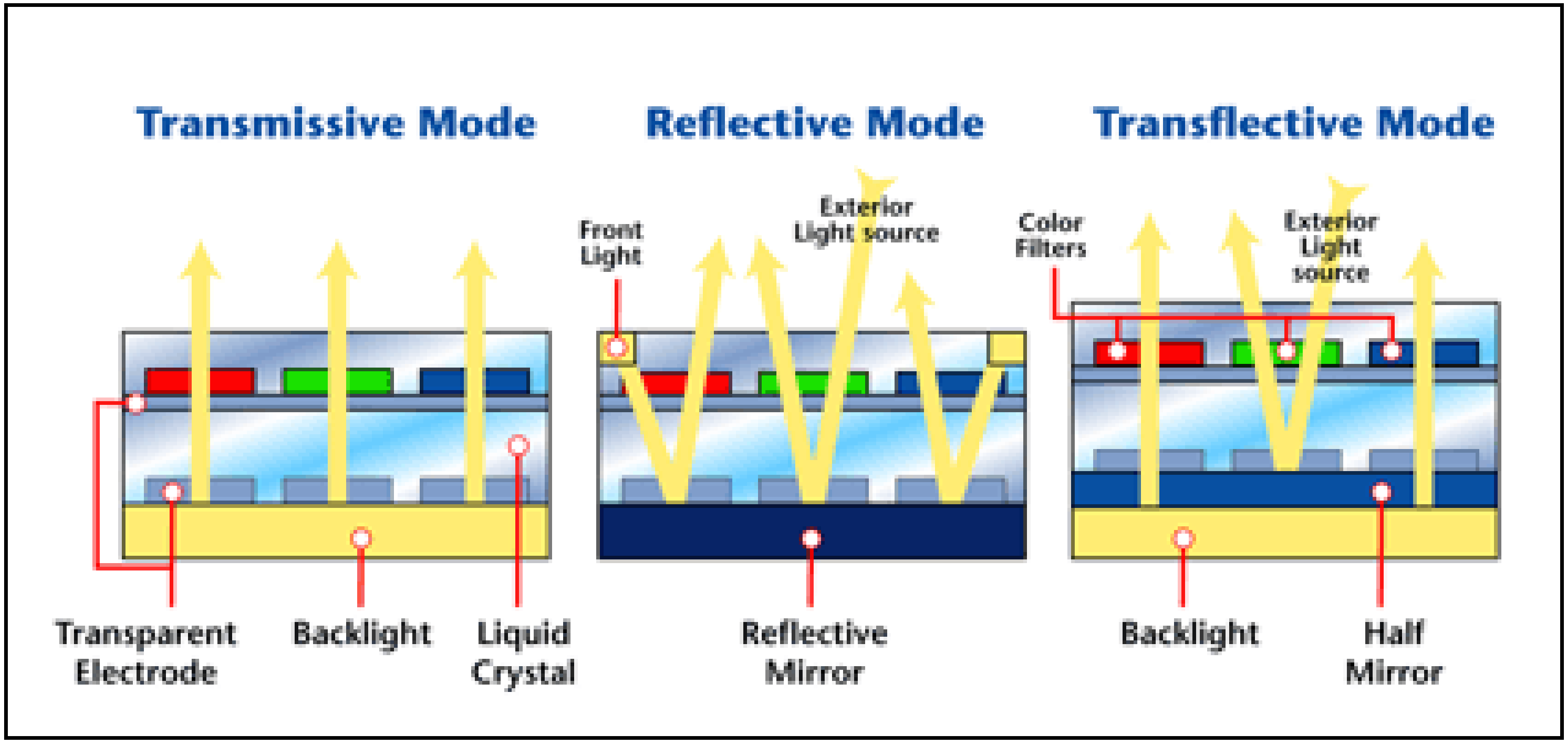
https://www.orientdisplay.com/

LCD Types



Source: Matrix