# LSP Exam - December 21, 2021

> **CVUT FEL (ČVUT) - České vysoké učení technické v Praze | Czech Technical University in Prague**
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> **AI-Generated Solution** - This exam PDF has no official answers, below is derived analysis
> Note: This exam uses a 4-input (A,B,C,D) RS latch variant

## Exam Information
- Date: December 21, 2021
- Language: Czech
- Total Points: 60 (Part 1: 30 points + Part 2: 30 points)

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## Question 1 - Equivalent Logic Functions (8 points)
**Question:** Check all logic functions that have an equivalent function:

```vhdl
y1 <= (D and not C) or (not C and A) or (D and B);
y2 <= (D and C) xor (B and A);
y3 <= (D or A) and (not C or B) and (D or not C);
y4 <= (D and B) or (D and not C and not B) or ((D xor A) and not C);
```

**Solution Method:** Use Karnaugh maps to verify if functions are equivalent

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## Question 2 - RS Latch Simulation (5 points)
**Question:** Given inputs A, B, C, D values at times t0-t4, write the values of X and Y outputs

**Input Sequence:**
```
A = 0 | 1 | 1 | 1 | 1
B = 0 | 0 | 1 | 0 | 0
C = 0 | 0 | 1 | 1 | 0
D = 1 | 1 | 0 | 0 | 1
    t0  t1  t2  t3  t4
```

**Solution Method:** Analyze the RS latch timing behavior

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## Question 3 - Shannon Expansion (8 points)
**Question:** Decompose the function X=f(A,B,C,D,X) from question 2 using Shannon expansion into:
$$X = (\overline{X} \land f_0(A,B,C,D)) \lor (X \land f_1(A,B,C,D))$$

Write f  and f  in Karnaugh map form

**Shannon Expansion Formula:**
- f  = f(A,B,C,D,0) - Function value when X=0

- f  = f(A,B,C,D,1) - Function value when X=1

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## Question 4 - Implement XOR with NAND Gates (3 points)
**Question:** Create an XOR gate using only 2-input NAND gates and wires

**Answer:**
```
Y = A xor B = (A NAND (A NAND B)) NAND (B NAND (A NAND B))
```
Requires 4 NAND gates

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## Question 5 - Full Adder Circuit (3 points)
**Question:** Complete the circuit diagram of a one-bit full adder

**Full Adder Formulas:**
- Sum = A   B   Cin
- Cout = (A   B)   (Cin   (A   B))

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## Question 6 - +1 Adder (3 points)
**Question:** Implement a 4-bit binary +1 adder using 6 logic gates

**Design Approach:**
```
Y0 = not A0
Y1 = A1 xor A0
Y2 = A2 xor (A1 and A0)
Y3 = A3 xor (A2 and A1 and A0)
```

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## Question 7 - VHDL Code Analysis
**Question:** Analyze the given VHDL code and draw the RTL view

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## Question 8 - State Machine Design
**Question:** Design a Moore/Mealy state machine with specified functionality