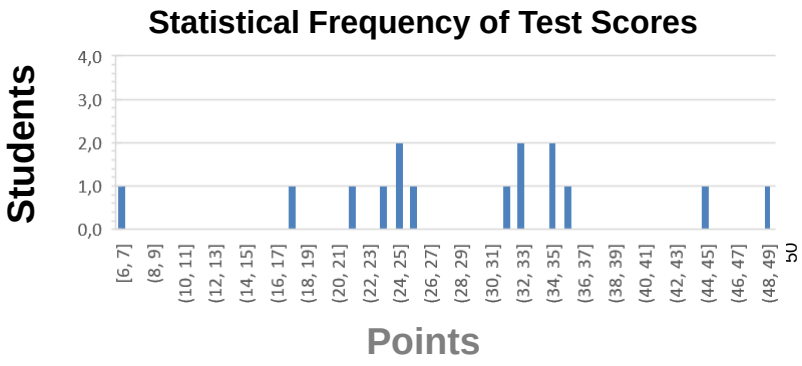
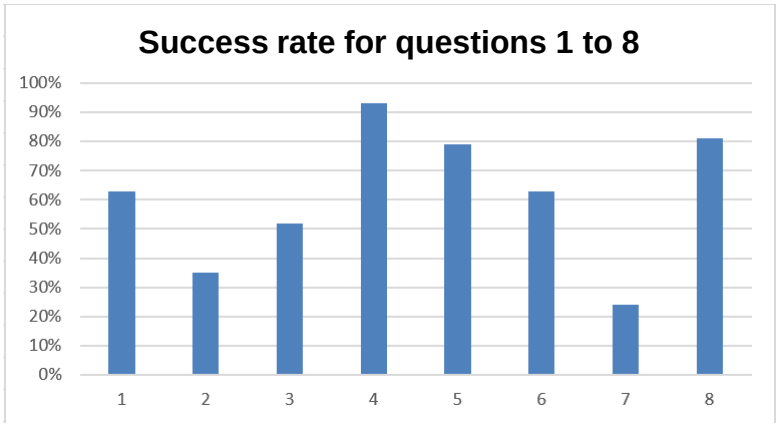
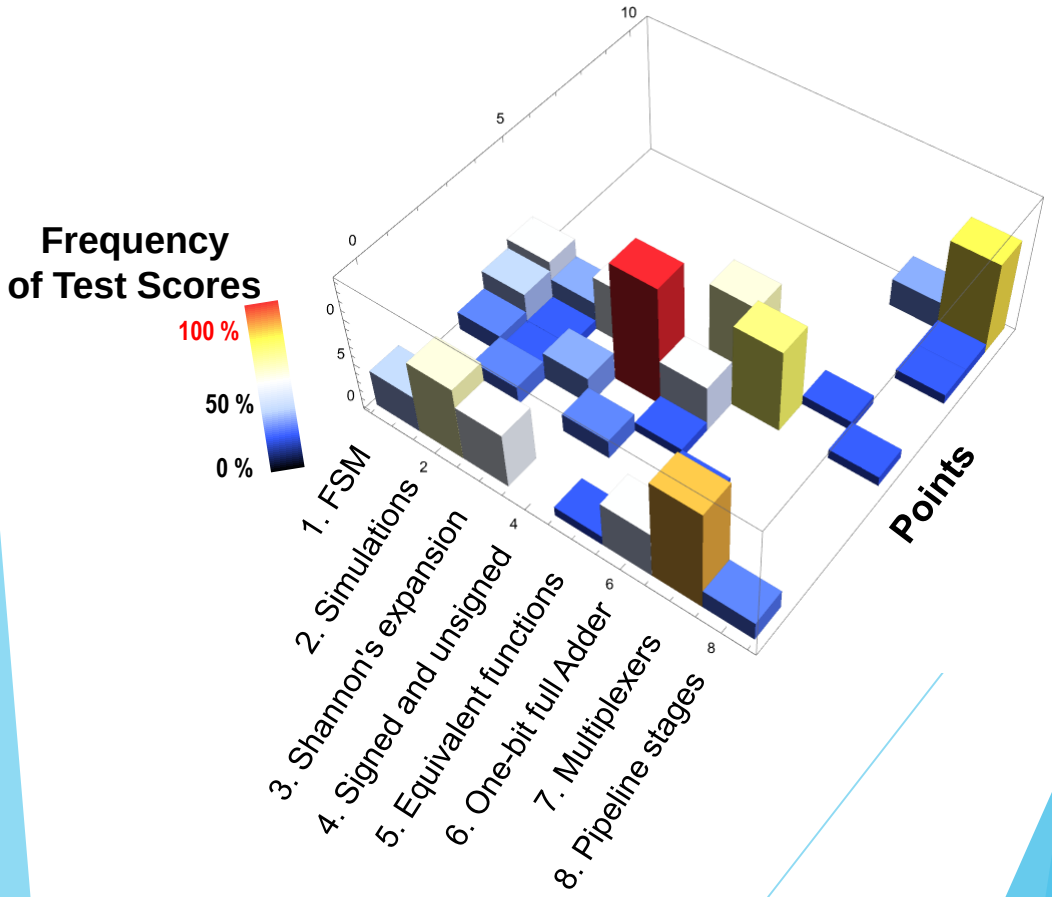
Statistical Results of LSP Written Exam January 13th, 2026







Surname and first name:.....

Exam Jan 13, 2026 - write here only your answers

Do not write here

1. Moore (Mealy) finite state machine is ordered tuple **M = < X, S, Z,** ω**,** δ**, $s_0 \in$ S >,**

where

X is..... .....

S is.....

Z is.....

δ is a mapping for Moore..... for Mealy.....

ω is a mapping for Moore.....for Mealy.....

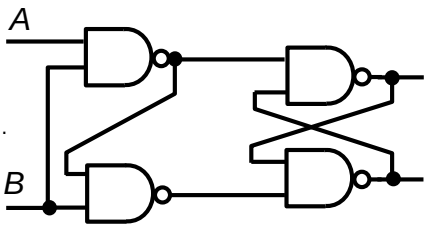
s0 is .....

5

2. Inputs A and B have values shown at the figure in times t_0, t_1, t_2, t_3 , t_4.
Write values of X and Y outputs. Assume that the intervals between changes of the inputs are so long so we can neglect propagation delays of gates.

A = .**0..| 1..|..1..|..0.. |..0..|**
t_0.. |..t_1..|.. t_2..|..t_3..|..t_4..|..

B = ..**1..|..1..|..0..|..0.. |..1..|**
t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

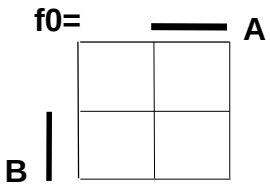


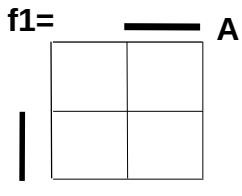
X = ...|… ….|… ….| ..…..|... …|

Y = ...|… ….|… ….| ..…..|.. ….|

5

3. Decompose X=f(A,B,X) function of the circuit from the question 2 into
X= (not X and **f0(**A, B**)**) or (X and **f1(**A,B**)**)
using Shannon expansion. Write down f0 a f1 as Karnaugh maps:





5

4. What decimal value is 12-bit number 1000 0001 1111 if we interpret it as an integer

a) unsigned .....

b) signed in two's-complement.....

4

5. Mark all logic functions that have another equivalent logic function here *:*

y1 <= (not A and not B) or (not C and not B) or (not A and C); **y1** ☐

y2 <= (not A or not C) and (not B or C) and (not A or not B); **y2** ☐

y3 <= (A and B) xor (A or C); **y3** ☐

y4 <= ((B xor not C) or (not A and not B)) and (not A or not B); **y4** ☐

6

Surname and first name:.....

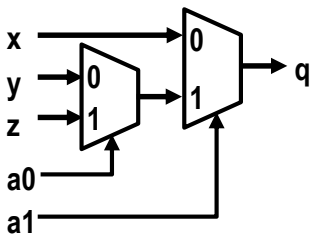
Exam Jan 13, 2026 - write here only your answers

Do not write here

6. Complete the schema of the one-bit full adder.

5

7. Use only AND, NAND, OR, NOR gates, and NOT inverters to connect the circuit on the left.



10

8. Write down the names of the **five basic phases of pipeline instruction processing** and explain what operations are performed during them.

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Results

Exam Jan 13, 2026 - write here only your answers

Do not write here

1. Moore (Mealy) finite state machine is ordered tuple **M = < X, S, Z, ω, δ, s_0 >,** where

X is *finite set of all* input vectors
S is *finite set of all* output vectors
Z is *finite set of all* internal states
δ is a mapping for Moore **δ: X x S -> S** for Mealy **δ: X x S -> S**
ω is a mapping for Moore **ω: S -> Z** .for Mealy **ω: X x S -> Z**
s0 is - initial state $S_0 \in S$.

5

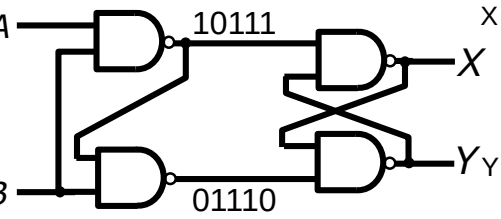
2. Inputs A and B have values shown in the figure in times t_0, t_1, t_2, t_3 , t_4. Write values of X and Y outputs. Assume that the intervals between changes in the inputs are so long so we can neglect delays of gates.

A = .**0..| 1..|..1..|..0.. |..0..|**

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..

B = ..**1..|..1..|..0..|..0.. |..1..|**

t_0..|..t_1..|.. t_2..|..t_3..|..t_4..|..



X = ... 0...|... 1....|...1 ....| ...1...|... 0...|

t_0..|..t_1...|.. t_2..|..t_3..|..t_4..|..

Y = ...1 ...|... 0....|...0 ....| ...0...|.. 1....|

5

3. Decompose X=f(A,B,X) function of the circuit from the question 2 into X= (not X and **f0**(A, B)) or (X and **f1**(A,B)) using Shannon expansion. Write the functions f0 a f1 as Karnaugh maps:

f0=

B \ A	0	1
0	0	0
1	0	1

f1=

B \ A	0	1
0	1	1
1	0	1

X=(A and B) or (X and (not B or (A and B)))

f0=**A and B**
f1=(A and B) or (not B or (A and B))
=(A and B) or not B = **A or not B**

5

4. What decimal value is 12-bit number 1000 0001 1111 if we interpret it as an integer
a) unsigned....***2079***..... *b)* signed in two's-complement.....***-2017***.

4

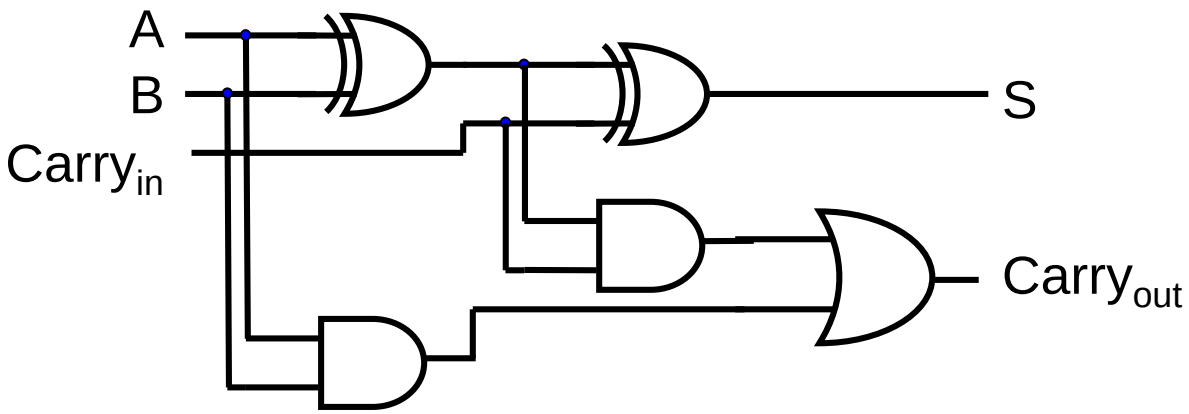
5. Mark all logic functions that have another equivalent logic function here *:*

y1 <= (not A and not B) or (not C and not B) or (not A and C);
y2 <= (not A or not C) and (not B or C) and (not A or not B);
y3 <= (A and B) xor (A or C);
y4 <= ((B xor not C) or (not A and not B)) and (not A or not B);

y1 ■
y2 ■
y3 □
y4 ■

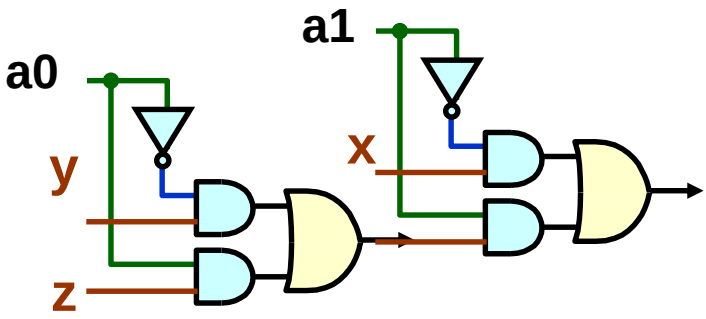
6

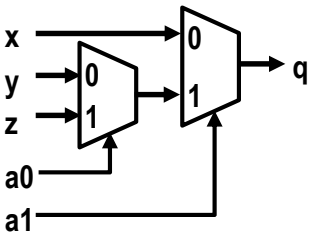
6. Complete the schema of the one-bit full adder.



5

7. Use only AND, NAND, OR, NOR gates, and NOT inverters to connect the circuit on the left.





10

8. Write down the names of the **five basic phases of pipeline instruction processing** and explain what operations are performed during them.

- **FETCH** - fetches an instruction from memory.
- **DECODE** - the instruction is decoded and the operand values are added to it from registers.
- **EXECUTE** - ALU (Arithmetic Logic Unit) performs an operation with the values prepared in the DECODE phase.
- **MEMORY** - possible work with memory, writing or reading the address calculated by ALU, if there is a branch then writing the new address to PC (Program Counter).
- **WRITE-BACK** - results are saved in registers

10