LSP Exam 2022-01-24

Course: B0B35LSP – Logické systémy a procesory | BE5B35LSP – Logic Systems and Processors **University**: CVUT FEL (ČVUT) – České vysoké učení technické v Praze | Czech Technical University in Prague **Keywords**: LSP, Exam, Zkouška, 2022-01-24, Shannon expansion, RS latch, VHDL

CN Version | EN Version | CZ Version

LSP Exam 2022-01-24 (English edition)

AI-derived version – No official answers in the PDF; the following is an inferred walkthrough/notes.

Exam Info

- Date: 2022-01-24
- Language: Czech / English
- Total: 50 points (Part 1: 25 pts > 8 + Part 2: 25 pts > 8)

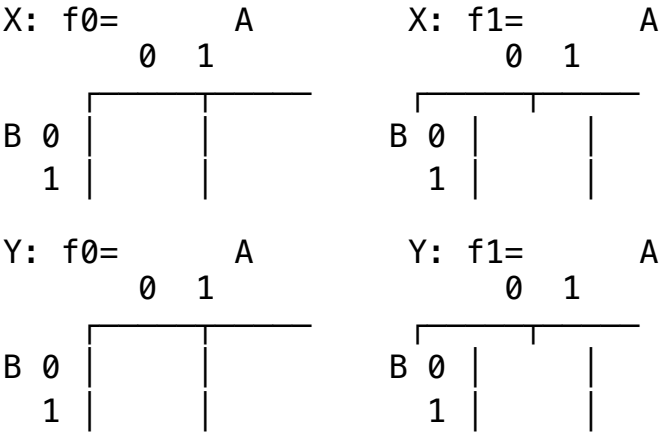
Q1 – Shannon Expansion (6 pts)

Task: Decompose the circuit functions $X, Y = f(A, B, C)$ using Shannon expansion into:

$$X, Y = (\overline{C} \wedge f_0(A, B)) \vee (C \wedge f_1(A, B))$$

Write f_0 and f_1 as Karnaugh maps.

For both X and Y draw two K-maps:



Q2 – Signed/Unsigned Arithmetic (4 pts)

Task: Perform 96+97+98+99 on an 8–bit adder. What is the decimal value of the result as an 8–bit number?

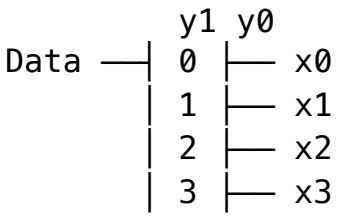
Computation: – 96+97+98+99 = 390 – 390 mod 256 = 134

Answer: – a) **unsigned**: 134 – b) **signed (two's complement)**: 134 – 256 = **–122**

Q3 – 1:4 Demultiplexer Design (10 pts)

Task: Draw the logic circuit diagram of a 1:4 demultiplexer.

Symbol:



Logic equations:

```
x0 = Data and (not y1) and (not y0)
x1 = Data and (not y1) and y0
x2 = Data and y1 and (not y0)
x3 = Data and y1 and y0
```

Q4 – RS Latch Simulation (5 pts)

Task: Given inputs A, B, C values at times t0—t4, write the values of outputs X and Y.

Input sequence:

```
A = 1 | 0 | 1 | 0 | 1
B = 0 | 0 | 1 | 0 | 0
C = 0 | 1 | 0 | 0 | 0
    t0  t1  t2  t3  t4
```

Q5 – VHDL RTL Analysis (10 pts)

Task: Draw the RTL view of the following VHDL code and correctly name the circuit.

```vhdl
library ieee; use ieee.std_logic_1164.all; use ieee.numeric_std.all;
entity XXX is port(a, b : in std_logic; c : out std_logic); end entity;
architecture beh of XXX is
```

```vhdl
begin
  process (a,b)
    variable d:std_logic:='0';
    variable e:integer range 0 to 25:=0;
  begin
    if b='0' then
      e:=0; d:='0';
    elsif rising_edge(a) then
      if e<25 then
        e:=e+1;
      else
        e:=0; d:=not d;
      end if;
    end if;
    c<=d;
  end process;
end architecture;
```

Functional analysis: – `b='0'` is an asynchronous reset – Triggered on rising edge of `a` – After counting up to 25, the output toggles – **Name: divide–by–26 frequency divider**

RTL view contains: – 5–bit counter (0—25) – comparator(s) (`e < 25`, `e = 25`) – D flip–flop to store `d` – async reset logic

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Q6 – Demultiplexer VHDL Description (5 pts)

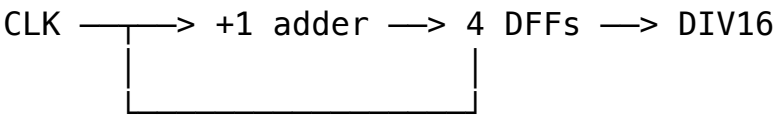
Task: Describe the demultiplexer from Q3 in the simplest way.

```vhdl
library ieee; use ieee.std_logic_1164.all; use ieee.numeric_std.all;
entity yyy is
  port(Data: in std_logic;
       y: in std_logic_vector(1 downto 0);
       x: out std_logic_vector(3 downto 0));
end entity;
architecture dataflow of yyy is
begin
  x <= (others => '0');
  x(to_integer(unsigned(y))) <= Data;
end architecture;
```

Q7 – Divide–by–16 Counter Design (5 pts)

Task: Add the minimum number of components to an incomplete circuit to create a synchronous divide–by–16 of CLK (using a +1 adder).

Idea:



- 4–bit counter (0—15 loop)
- DIV16 = Q3 (MSB)
- Toggles every 16 clock cycles

Q8 – Motor Control Circuit (5 pts)

Task: Design a circuit: press a double–pole button once to start the motor, press again to stop it. After power–up the motor must be OFF.

Key components: – D flip–flop – asynchronous clear (power–up reset) – relay driver – de–bounce circuit

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Q9 – Bonus: Edge Detector (10 pts)

Task: When input D changes value, output Y shall be '1'for one clock cycle. RESET is synchronous.

```vhdl
library ieee; use ieee.std_logic_1164.all; use ieee.numeric_std.all;
entity Edges is
  port (clk, Reset, D : in std_logic; Y: out std_logic);
end entity;
architecture rtl of Edges is
  signal D_prev : std_logic := '0';
begin
  process(clk)
  begin
    if rising_edge(clk) then
      if Reset = '1' then
        D_prev <= '0';
        Y <= '0';
      else
        if D /= D_prev then
          Y <= '1';
        else
          Y <= '0';
        end if;
        D_prev <= D;
      end if;
    end if;
```

```
  end process;
end architecture;
```

Key Topics Summary

Focus points in this exam

1. Shannon expansion (two outputs)
2. **8–bit signed/unsigned arithmetic** (important: 390 mod 256)
3. **1:4 demultiplexer design**
4. RS latch simulation
5. **VHDL RTL analysis** (divider recognition)
6. Demultiplexer VHDL description
7. Divide–by–16 design
8. Motor control circuit
9. Edge detector design

Important formulas

- 8–bit unsigned range: 0—255
- 8–bit signed range: –128 to 127
- overflow handling: `result mod 2^n`