



Display Logic Curve VHDL Code

Logic Systems And Processors (České Vysoké Učení Technické v Praze)



Scan to open on Studocu

```

1
2
3  library ieee;
4  use ieee.std_logic_1164.all;
5  use ieee.numeric_std.all;          -- type integer and unsigned
6
7  entity DisplayLogicCurve is
8  port (
9      yrow, xcolumn : in unsigned(9 downto 0); -- row and column number of VGA video
10     VGA_CLK : in std_logic;
11     VGA_R, VGA_G, VGA_B: out std_logic_vector(9 downto 0) -- color information
12 );
13 end;
14
15 architecture behavioral of DisplayLogicCurve is
16 -- Intensity of 10bit color in percent
17 constant C100 : std_logic_vector(9 downto 0) := (others=>'1');
18 constant C75  : std_logic_vector(9 downto 0) := (9=>'1', 8=>'0', others=>'1');
19 constant C50  : std_logic_vector(9 downto 0) := (9=>'0', others=>'1');
20 constant C25  : std_logic_vector(9 downto 0) := (9=>'0', 8=>'0', others=>'1');
21 constant C0   : std_logic_vector(9 downto 0) := (others=>'0');
22 constant G588 : std_logic_vector(9 downto 0) := "1001001100"; --G 147
23 constant B884 : std_logic_vector(9 downto 0) := "1101110100"; -- B 221
24 constant R40  : std_logic_vector(9 downto 0) := "0010100000"; --R 40
25 constant B22  : std_logic_vector(9 downto 0) := "0001011000"; -- B 22
26 constant G111 : std_logic_vector(9 downto 0) := "0110111100"; --G 111
27
28 -- records are VHDL equivalents of structures
29 type RGB_type is
30     record
31         R : std_logic_vector(9 downto 0);
32         G : std_logic_vector(9 downto 0);
33         B : std_logic_vector(9 downto 0);
34     end record;
35 -- Used colors - we defined them by the way allowing good overlapping
36 constant BLUE : RGB_type := (C0,C0,C50);
37 constant GREEN : RGB_type := (C0,C50,C0);
38 constant RED : RGB_type := (C50,C0,C0);
39 constant YELLOW : RGB_type := (C75,C75,C0);
40 constant BLACK : RGB_type := (C0,C0,C0);
41 constant SKY_BLUE: RGB_type := (C0,G588,B884);
42 constant NAVY_BLUE: RGB_type := (R40,B22,G111);
43 constant WHITE: RGB_type := (C100,C100,C100);
44
45 constant YSIZE : integer := 240;
46 constant XSIZE : integer := 320;
47 constant EMBORGX : integer := 220;
48 constant EMBORGY : integer := 32;
49 constant MEMROWSIZE : integer := 64;
50 constant MEMROWCOUNT : integer := 64;
51 constant MEM_END_ADDRESS : integer := 4095;
52
53 constant SORGX : integer := 16; -- positions for picture in the flag
54 constant SORGY : integer := 15;
55 constant SROW : integer := 128; -- memory organization
56 constant SROWCOUNT : integer := 56;
57
58
59 component Shark
60     PORT
61     (
62         address      : IN STD_LOGIC_VECTOR (12 DOWNT0 0);
63         clock        : IN STD_LOGIC := '1';
64         q            : OUT STD_LOGIC_VECTOR (1 DOWNT0 0)
65     );
66 end component;

```

```

67
68 COMPONENT BlackCurve is
69 PORT (
70     xcolumn : in unsigned(9 downto 0);
71     q       : out unsigned(6 downto 0)
72 );
73 END COMPONENT;
74
75
76
77 signal shark_address_s : STD_LOGIC_VECTOR(12 DOWNTO 0);
78 signal shark_q_s       : STD_LOGIC_VECTOR (1 DOWNTO 0);
79
80 signal blackCurve_q_s : unsigned(6 downto 0);
81
82 begin
83
84
85
86 shark_inst : Shark
87     port map (
88         address => shark_address_s,
89         clock    => VGA_CLK,
90         q        => shark_q_s
91     );
92
93
94 blackC_inst : BlackCurve
95 PORT MAP(xcolumn => xcolumn,
96         q => blackCurve_q_s);
97
98 LSPflag : process(xcolumn, yrow, blackCurve_q_s) -- output of process depends on
xcolumn and yrow
99     variable RGB : RGB_type; -- output colors
100     variable x, y : integer; -- renamed xcolumn and yrow
101     variable isPicture, isShark01, isShark02, isShark03 : boolean;
102     constant GREEN_LINE_ORG : integer := 100; -- TODO
103     begin
104         x := to_integer(xcolumn); y := to_integer(yrow); -- convert to integer
105
106         isShark01 := x >= SORGX and x < SORGX + SROW
107             and y >= SORGX and y < SORGX + SROWCOUNT;
108
109         isShark02 := x >= (SORGX + 150) and x < (SORGX + 150) + SROW
110             and y >= (SORGY) and y < (SORGY + SROWCOUNT);
111
112         isShark03 := x >= (SORGX + 90) and x < (SORGX + 90) + SROW -- 3rd Inverted Shark
113             and y >= (SORGY + 160) and y < (SORGY + 160) + SROWCOUNT;
114
115         if (x < 0) or (x >= XSIZE) or (y < 0) or (y >= YSIZE) then
116             RGB := BLACK; -- black if there is no flag
117
118         elsif (isShark01 or isShark02 or isShark03) and shark_q_s /= "01" then
119             case shark_q_s is
120                 when "10" => RGB := YELLOW;
121                 when "00" => RGB := BLACK;
122                 when "11" => RGB := BLUE;
123                 when others => RGB := BLACK;
124             end case;
125
126         elsif (y > to_integer(blackCurve_q_s) + 86) and (y < to_integer(blackCurve_q_s) +
104) then
127             RGB := BLACK;
128         elsif (y > to_integer(blackCurve_q_s) + 117) and (y < to_integer(blackCurve_q_s) +
135) then
129             RGB := BLACK;

```

```
130         elsif (y >= 81) and (y <= 161) then
131             RGB:=WHITE;
132
133         else
134             RGB:=SKY_BLUE;
135         end if;
136
137
138         if isShark01 then shark_address_s <= std_logic_vector(to_unsigned((y-SORGY)*SROW +
(SORGX+SROW-x),
139                                                                 shark_address_s '
LENGTH));
140         elsif isShark02 then shark_address_s <= std_logic_vector(to_unsigned((y-SORGY)*SROW
+ (SORGX+SROW + 150 - x),
141                                                                 shark_address_s '
LENGTH));
142         elsif isShark03 then shark_address_s <= std_logic_vector(to_unsigned((y-(SORGY+160
))*SROW + (x-(SORGX+90)),
143                                                                 shark_address_s '
LENGTH));
144
145         else shark_address_s <=(others=>'0');
146         end if;
147
148
149
150         -- Copy results in RGB to outputs of entity
151         VGA_R<=RGB.R; VGA_G<=RGB.G; VGA_B<=RGB.B;
152         -----
153     end process;
154
155
156 end architecture behavioral;
```