UNIVERSITY OF MIAMI
Department of Electrical and Computer Engineering
EEN 311

Name: _____
Section: _____
Date: _____

EXPERIMENT 7

COMMON EMITTER AND

COMMON COLLECTOR AMPLIFIERS

PURPOSE: The purpose of this experiment is to demonstrate the operation and characteristics of a common-emitter and a common-collector amplifier. The common-emitter amplifier is operated by applying the input signal to the base terminal of the transistor, while its output is taken from the collector with an 180^o phase-shift. In the common-collector amplifier the input is connected to the base terminal of the transistor and the output is taken from the emitter, without any phase shift

Preliminary Work

1. For the common-emitter amplifier stage of Fig. 4.1, design R_C, R_E, R_1 and R_2 to operate at $V_{CEQ} = 10$ V, $I_{CQ} = 1$ mA.
   Use $V_{CC} = 20$ V, $V_{BE} = 0.7$ V, $\beta = 100$ and assume that $V_{RE} = 0.1V_{CC}$ and $I_{CQ} = I_{EQ}$ since $\beta \gg 1$. Also, choose $R_{Th} = 10R_E$ for good bias stability.

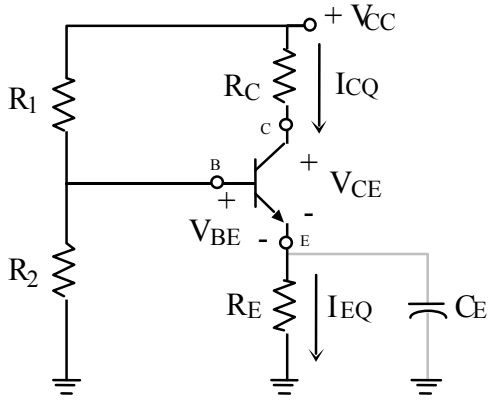


Figure 4.1 Common-emitter Amplifier Stage.

The use of $R_{Th} = 10R_E$ is a rule of thumb. With this, the collector current can be expressed as

$$ICQ = \frac{V_{TH} - V_{BE}}{R_E + \frac{R_{TH}}{\beta + 1}} = \frac{V_{TH} - V_{BE}}{R_E\left(1 + \frac{10}{\beta + 1}\right)}$$

where V_{Th} was defined in experiment 6. Hence, for this circuit it can be assumed that the Q-point will remain constant and independent of any changes that β might have. Therefore, as far as the biasing circuit is concerned, the value of β is immaterial as long as it is much greater than one.

2. A simplified small-signal (AC) model for a BJT common-emitter amplifier is given in Fig. 4.2.

   a) Derive the expressions for the voltage gain of the amplifier stage (i.e., $A_V = V_{out1} / v_{in}$) with and without the bypass capacitor C_E as shown in Fig. 4.1.
   Notice that $r_\Pi = h_{ie} = (0.025/I_{CQ})\beta_{DC}$ depends on the quiescent collector current and on the dc beta. In this case, it is important to use the correct β for the calculation of $r_\Pi = h_{ie}$ if we wish to have an accurate estimate of the small signal voltage gain. Also $\beta_{ac} = h_{fe}$ (the small signal forward current gain) which is calculated from $\Delta I_C/\Delta I_B$ must be estimated properly. For this purpose, both $\beta_{ac} = h_{fe}$ and β_{DC} will be estimated with the aid of the Tektronics 575 Curve Tracer in Experimental Procedure part (a).

   b) Derive the expression for the voltage gain if the output signal is taken across the emitter resistor R_E, without the capacitor C_E ($A_V = v_{out2} / v_{in}$).

   c) Can you tell if there exists a phase shift between the input and the output signals (v_{in} and V_{out}) in either case? If so, how much?

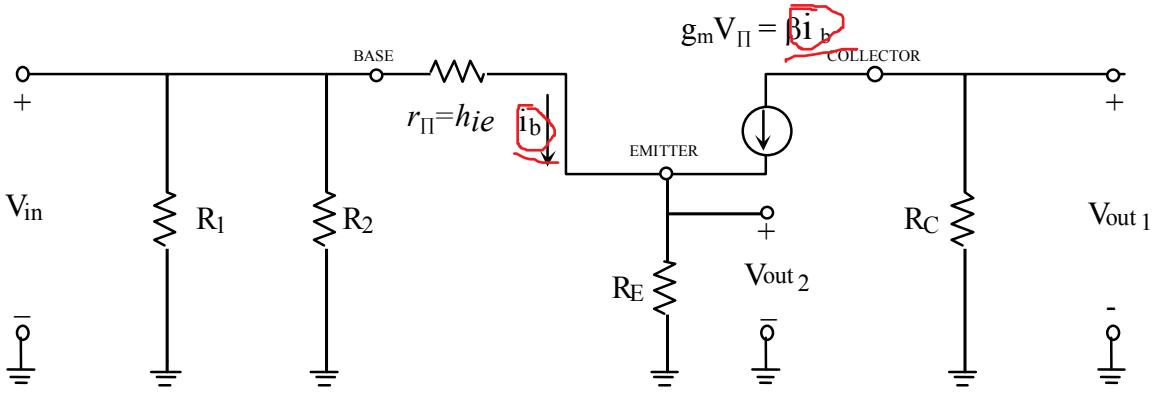


Figure 4.2 AC Small Signal Model for Common-emitter Amplifier Stage of Fig. 4.1.

I. DC Biasing:

a) This part can be left for last as the measurements here will be utilized in the discussion of the results. To estimate the small signal forward current gain $\beta_{ac}=h_{fe}$, use the curve tracer as done in experiment 3 and obtain the required values around a quiescent point given by V_{CEQ} = 10V and I_{CQ} = 1mA. List the values obtained from Experiment 3 below.

$\beta_{ac}=h_{fe}$ = 179 β_{DC} = 180=(beta+1)

b) Set up the circuit in Fig. 4.3 using the resistor values from your Preliminary Work.

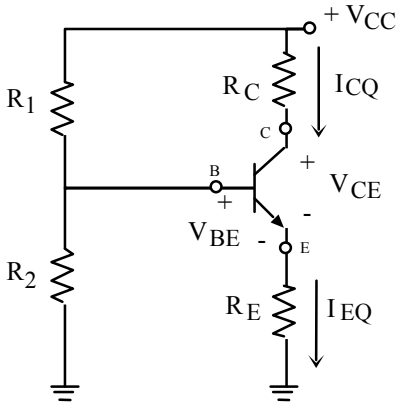


Figure 4.3 Common-emitter Amplifier for DC Biasing.

Measured values: R_C = 8K R_E = 1.99K R_1 = 249.7K R_2 = 42K

c) Set V_{CC} to 20 V and measure the following:

V_{CEQ} = ____ V_{RC} = _____ V_{RE} = _____ V_{BE} = 0.6V

Calculate the following:

$$I_{CQ} = \frac{V_{RC}}{R_C} = \_\_\_\_\_ \qquad I_{EQ} = \frac{V_{RE}}{R_E} = \_\_\_\_\_$$

NOTE: V_{CEQ} and I_{CQ} should be reasonably close to the desired Q-point values.

II. AC Characteristics:

Connect the signal generator to the input of the amplifier, in series with a coupling capacitor C_C, as shown in Fig. 4.4. Select C_C to be between 1μF and 10 μF.

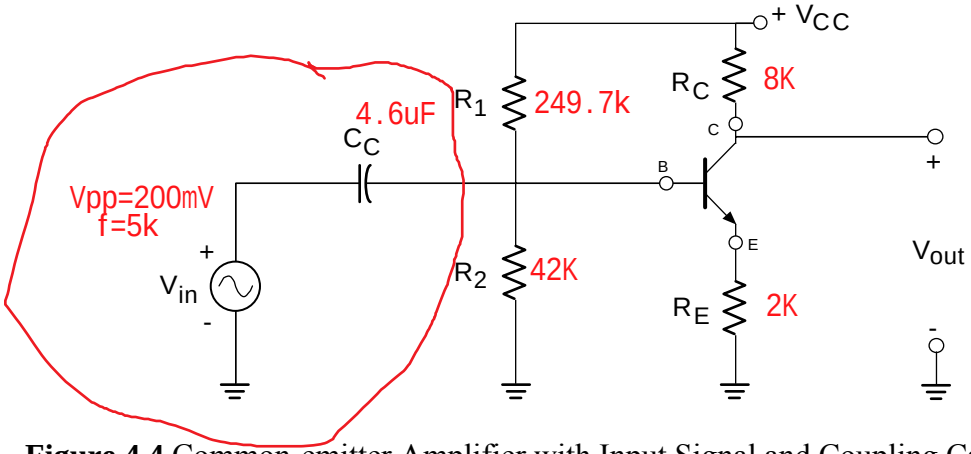
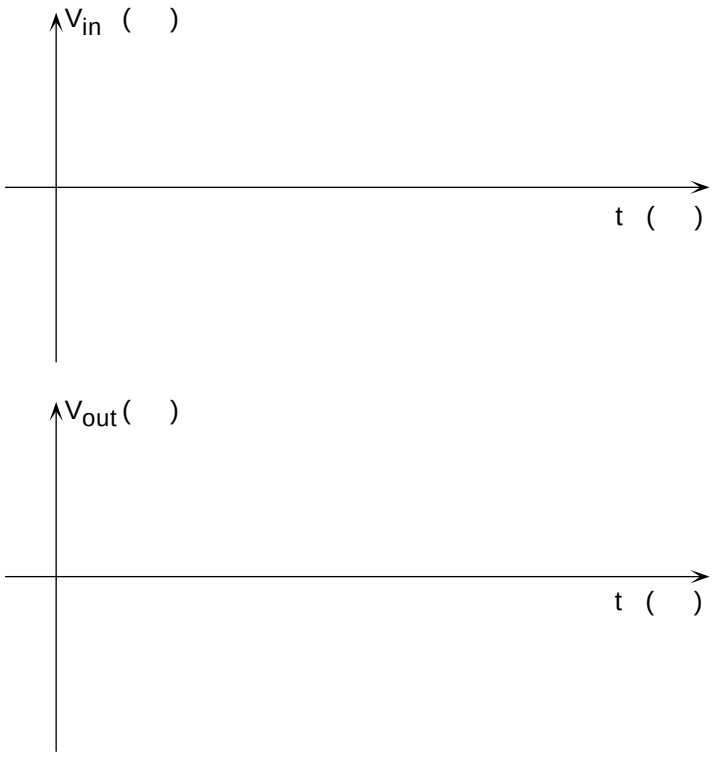


Figure 4.4 Common-emitter Amplifier with Input Signal and Coupling Capacitor.

a) Apply a sinusoidal input signal of frequency f = 5 kHz. Adjust its amplitude so that the output signal v_{out} is not distorted. Displaying v_{out} and v_{in} on the oscilloscope simultaneously, sketch the waveforms with their phase relation shown **clearly**.



$V_{out_{pp}}$ = _____ $V_{in_{pp}}$ = _____ $A_V = \frac{V_{out}}{V_{in}}$ = _____

Phase-shift at f = _____ is _____ also, the ratio of R_C/R_E = _____

b) Add a load resistor R_L = 1kΩ to the output of the amplifier via a second coupling capacitor C_C' (in the range 1μF to 10μF) as shown in Fig. 4.5 below. Adjust v_{in} so that v_{out} is not distorted. Measure $V_{out_{pp}}$, $V_{in_{pp}}$, and calculate the voltage gain A_V. Note that the load resistor will reduce the voltage gain. Explain.

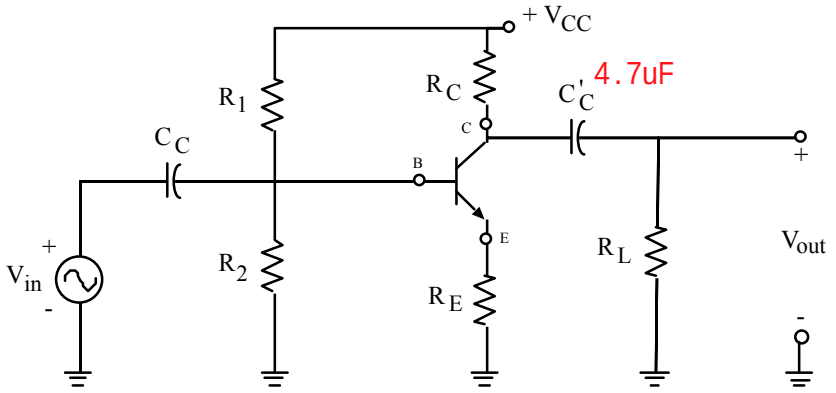
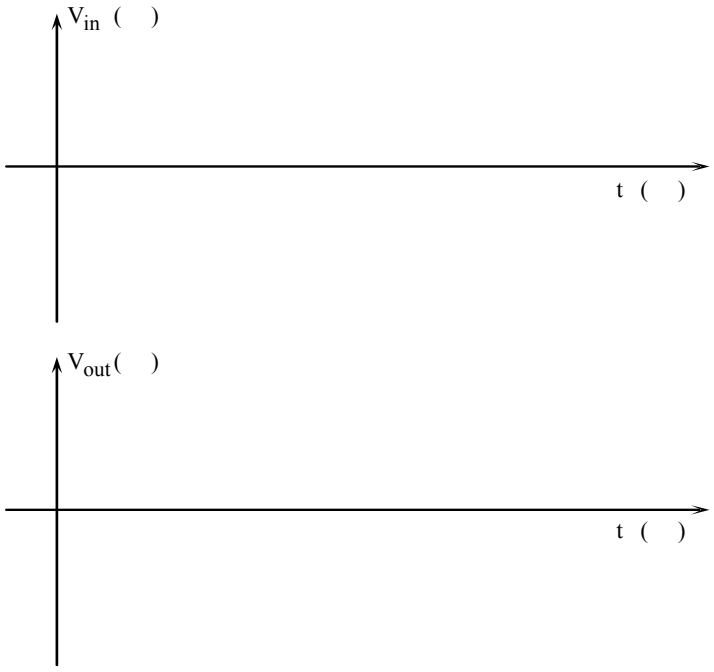


Figure 4.5 Common-emitter Amplifier with Loaded Output.

R_L = _____ $V_{out_{pp}}$ = _____ $V_{in_{pp}}$ = _____ $A_V = \frac{V_{out}}{V_{in}}$ = -0.5

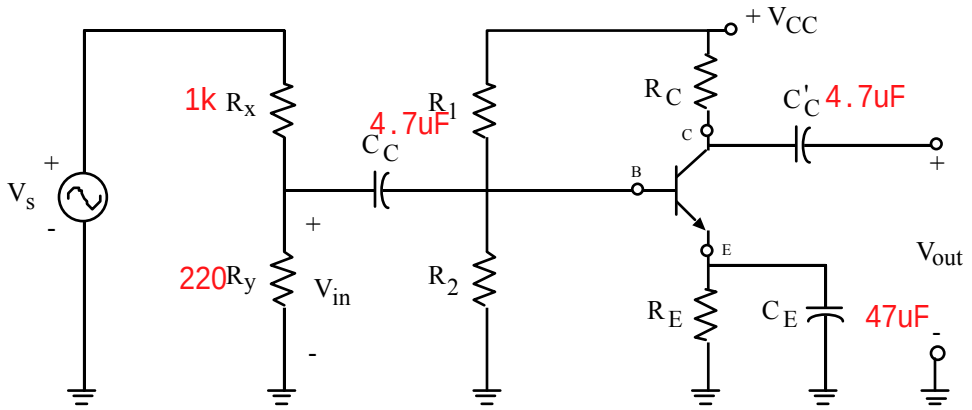
c) Disconnect C_C' and R_L. This time, take the output from the emitter instead of the collector (i.e., across R_E). In this case the amplifier is in the ***common-collector configuration***. Adjust V_{in} so that v_{out} is not distorted. Displaying v_{out} and v_{in} on the oscilloscope simultaneously, sketch the waveforms with their phase relationship shown **clearly**.



$V_{out_{pp}}$ = _____ $V_{in_{pp}}$ = _____ $A_V = \frac{v_{out}}{v_{in}}$ = -0.5

Phase-shift at f = _____ is _____ . Also, the ratio of $\frac{R_L'}{R_E}$ = _____ where R_L' is the parallel combination of R_C and R_L

d) Add an emitter by-pass capacitor C_E across R_E, and form a voltage-divider circuit at the input of the amplifier as shown in Fig. 4.6. Choose R_X = 1kΩ, R_Y = 220Ω, and C_E = 47μF-100μF. Adjust v_S so that v_{out} is not distorted. Measure $V_{out_{pp}}$, $V_{in_{pp}}$ and calculate the voltage gain A_V.



$V_{out_{pp}}$ = _____ $V_{in_{pp}}$ = _____ $A_V = \frac{v_{out}}{v_{in}}$ = 1

Figure 4.6 Common-emitter Amplifier with Voltage Divider at the Input and Emitter By-pass Capacitor.

III. Frequency Response:

Using the final form of the amplifier shown in Fig. 4.6, obtain its frequency response by measuring v_{in} and v_{out} at the frequencies specified in Table 4.1 below. **Make sure that v_{out} is not distorted before obtaining each reading.** Note that A_v in dB is $20.\log|A_v|$.

Freq. (Hz)	50	100	500	1k	5k	10k	50k	100k	500k	900k
$V_{out(p-p)}$										
$V_{in(p-p)}$										
A_v										
A_v (dB)										

Table 4.1 Frequency Response Data for Common-emitter Circuit of Fig. 4.6.

SPICE

Write a *SPICE* program to plot the AC response of the amplifier circuit of Fig. 4.6. Replace the voltage divider circuit to the left of C_C by a sine source of amplitude 10 mV_{p-p}. For the simulation, use the same component values you used to build the circuit in the lab. Use the transistor model provided by your instructor. The frequency range for the plot should include 50 Hz and 900 kHz as Table 4.1. Comment on the similarities or differences of this data from that in the spice simulation.

Discussion of the Results

1. Explain the reasons for using the coupling capacitors C_C and C_C' in the circuit.

2. Using the component values used in the lab, calculate the expected voltage gains vs. the experimental results for parts:
   a) II. a
   a) II. b
   c) II. c.
   d) II. d
   and find the percentage error in each part. Where needed, use $r_{\Pi}=h_{ie} = (0.025/I_{CQ})\beta_{DC}$ where β_{DC} is from Experimental Procedure part I.a.

3. Comment on the effects of adding a resistive load R_L in part II. b.

4. a) What are the advantages and disadvantages of using an emitter resistor R_E?
   b) Comment on the results of Experimental Procedure part II.d.

5. a) Plot $(A_V)_{db}$ vs *f* on **semi-log** paper using the data obtained in Experimental Procedure part III. (Optional: Use MATLAB for the plot)
   b) Find the bandwidth of the amplifier and explain the reasons for low and high frequency roll-offs. Notice that plotting the response in semi-log paper helps you to immediately identify the low and high break frequencies, f_l *and* f_h, respectively (the frequencies at which the gain is 3_{db} below the maximum midband gain).

6. Write a conclusion.