UNIVERSITY OF MIAMI
Department of Electrical and Computer Engineering
EEN 311

Name: _____
Section: _____
Date: _____

EXPERIMENT 9

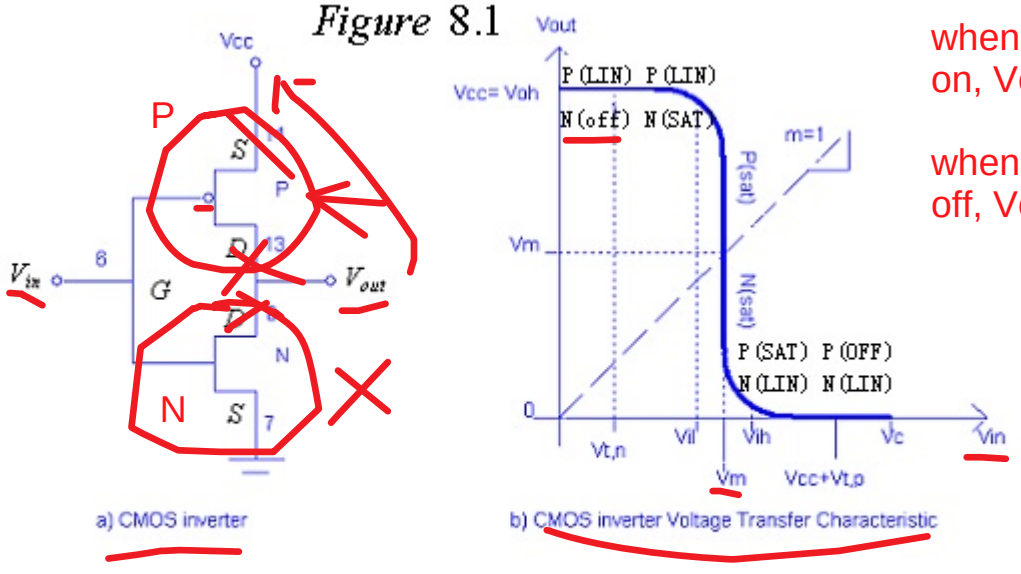
CMOS Inverter

PURPOSE: The purpose of this lab is to introduce the student to a basic building block in the design of digital integrated circuits: the *CMOS inverter*.

INTRODUCTION: CMOS stands for Complementary Metal Oxide Semiconductors. CMOS processes have both P-channel and N-channel type transistors (the enhancement type). This combination is advantageous because NMOS devices can act as a pull down load for a PMOS transistor and vice versa. Since CMOS has low power dissipation and high packing densities, it is a very common choice for digital logic circuits.

A CMOS inverter is shown in Figure 8.1a. The voltage Transfer Characteristic (VTC) of this circuit is shown in Figure 8.1b (the VTC here is drawn for a symmetric inverter). For low V_{in}, the NMOS is off and the PMOS is on. As V_{in} increases the NMOS turns on, operating in the saturation mode, and consequently forcing V_{out} to start decreasing. Around V_m, both devices are saturated and there is a sharp transition in V_{out}. As V_{in} increases further the PMOS changes to the saturation mode before eventually going into cutoff as V_{in} reaches V_{cc}.

Figure 8.1



a) CMOS inverter

b) CMOS inverter Voltage Transfer Characteristic

when Vi<Vm; N off, P on, Vout High,

when Vi > Vm, N on, P off, Vout=0

Equipment

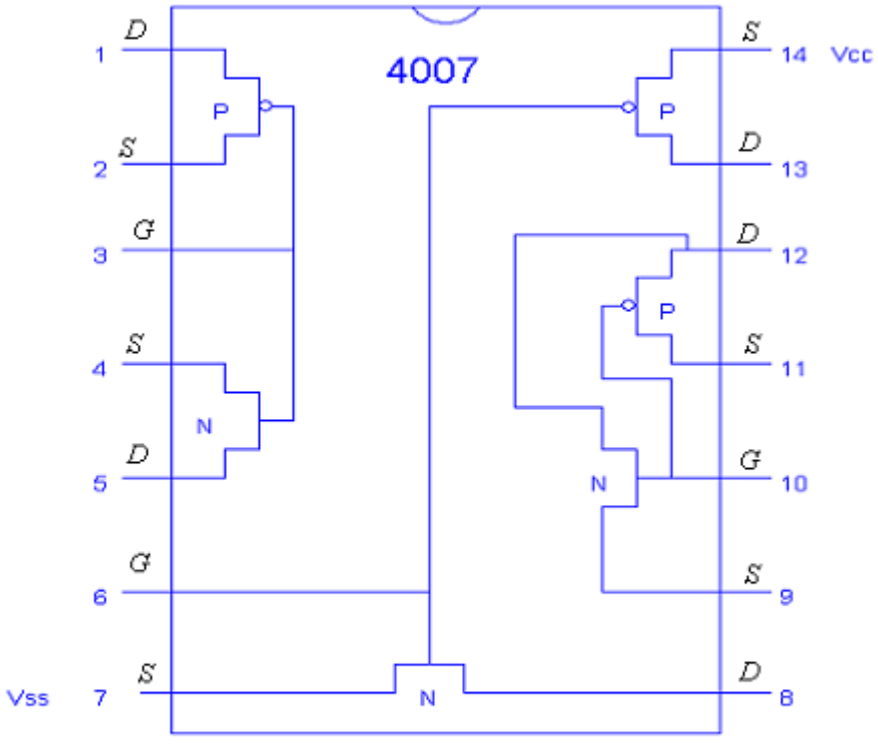
1 Frequency Generator
1 DVM (Multimeter)
Resistors
1 Power supply
1 4007 IC
1 Oscilloscope

Preliminary Work

1. For the following points on the CMOS inverter VTC shown in Figure 8.1b, justify why each transistor is in the mode of operation that it is in.

	NMOS	**PMOS**
$V_{t,n}$	cutoff	linear
V_{il}	saturation	linear
V_m	saturation	saturation
V_{ih}	linear	saturation
$V_{cc}+V_{t,p}$	linear	cutoff

Figure 8.2



Note: All P – channel substrates are connected to V_{cc} (pin 14)
All N – channel substrates are connected to V_{ss} (pin 7)

Experimental Procedure

I. Determining k_n, k_p, $V_{t,n}$ and $V_{t,p}$:

a) The circuits shown in Figure 8.3 will be used to estimate the threshold voltages and conductivity parameters of the NMOS and PMOS. Set V_{cc} to $10V_{DC}$. For the values of R_1 in Table 8.1a, measure V_{R1} and V_{DS}. Repeat for the circuit in Figure 8.3b. Plot $(2I_D)^{1/2}$ versus V_{DS} in Figure 8.4 for both N and P transistors.

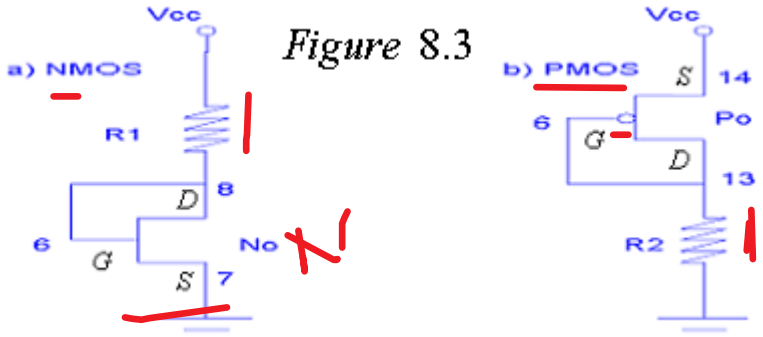


Figure 8.3

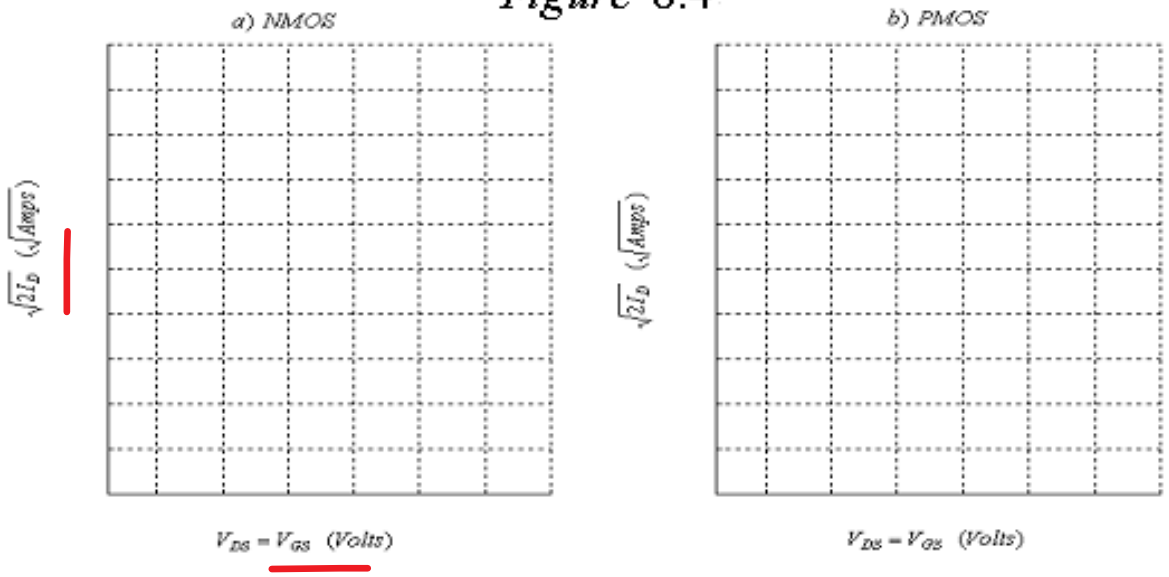
R_1	V_{DS} (Volts)	V_{R1} (Volts)	$I_D = V_{R1} / R_1$ (μA)	$\sqrt{2I_D}$ $\sqrt{Amps}$
5.1kΩ				
10kΩ				
22kΩ				
51kΩ				
100kΩ				

Table 8.1a Data to find k_n and $V_{t,n}$

R_2	V_{DS} (Volts)	V_{R2} (Volts)	$I_D = V_{R2} / R_2$ (μA)	$\sqrt{2I_D}$ $\sqrt{Amps}$
5.1kΩ				
10kΩ				
22kΩ				
51kΩ				
100kΩ				

Table 8.1b Data to find k_p and $V_{t,p}$

Figure 8.4



II. VTC and Transition time of a CMOS inverter:

a) Set up the circuit in Figure 8.5. Set V_{cc} to $10V_{DC}$. V_{in} is a 0 to 10 V sinusoid with a frequency of 100 Hz. Measure V_{in} with channel 2 of the oscilloscope and V_{out} with channel 1. Put the oscilloscope in XY-mode. Draw the VTC characteristic of the CMOS inverter. Find the slope of the region of sharp transition from high to low. (R is included to provide protection for diodes on the chip)

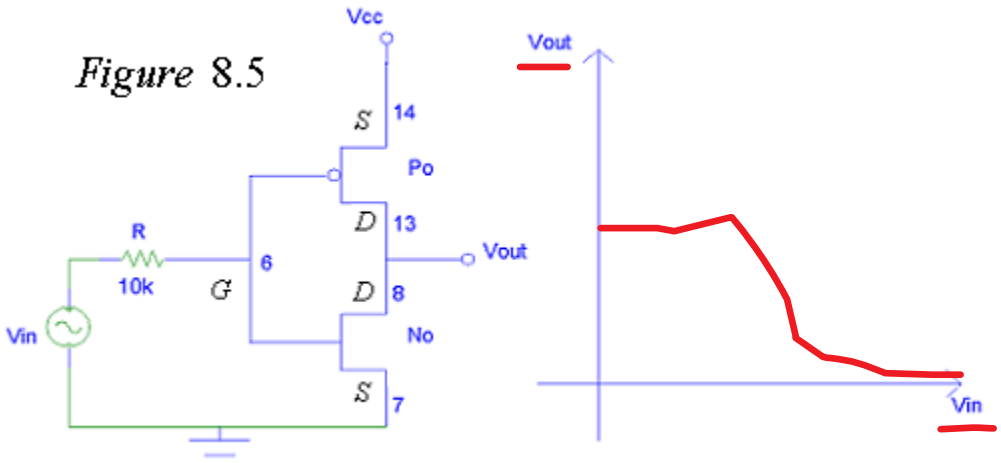
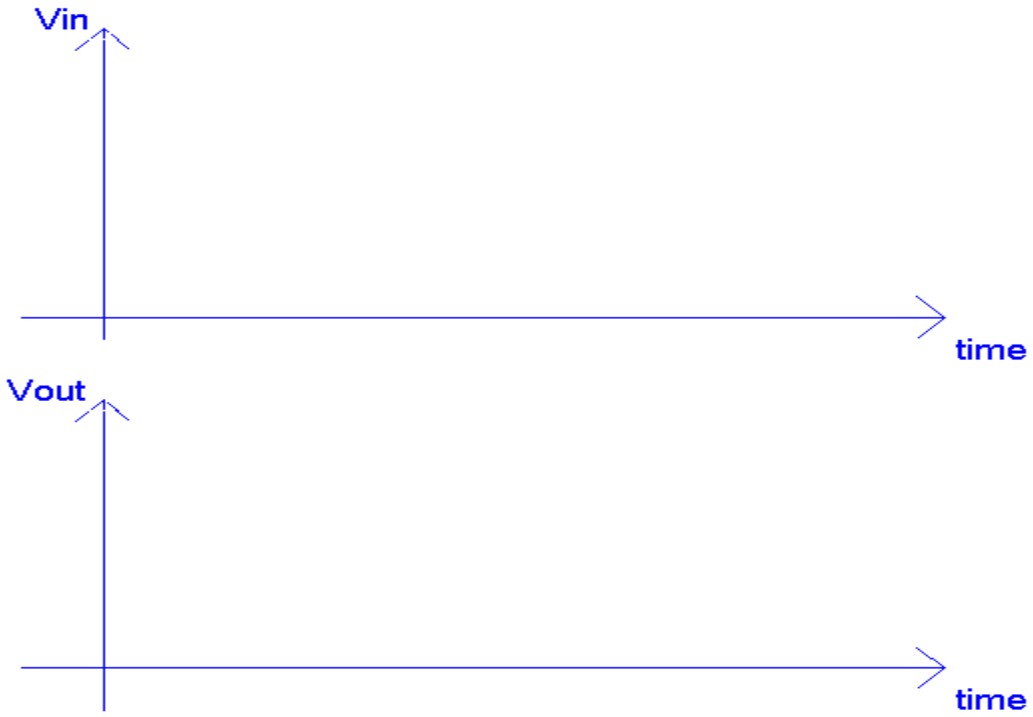


Figure 8.5

b) Change Vin to a square wave. Draw V_{in} and V_{out} on the axes below. Be careful to accurately draw the signals relative to each other. Measure and clearly label the transition times (10% to 90%) on the plots.



c) Add a load capacitor, C_L, of 10nF to the output of the inverter as shown in Figure 8.6. Measure the transition times and mark them on the plot of V_{out}.

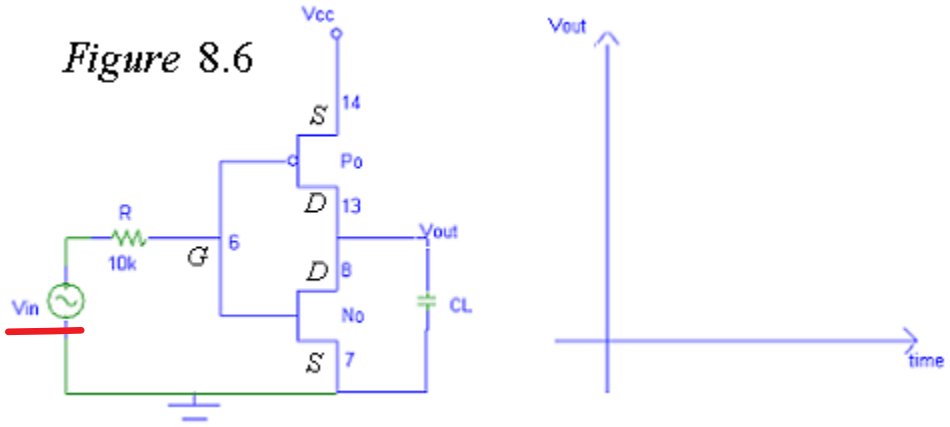
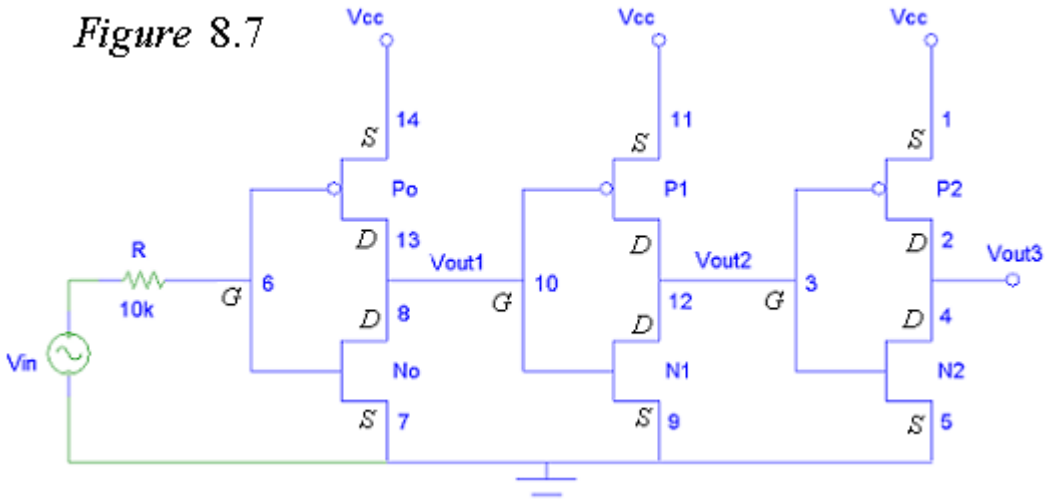


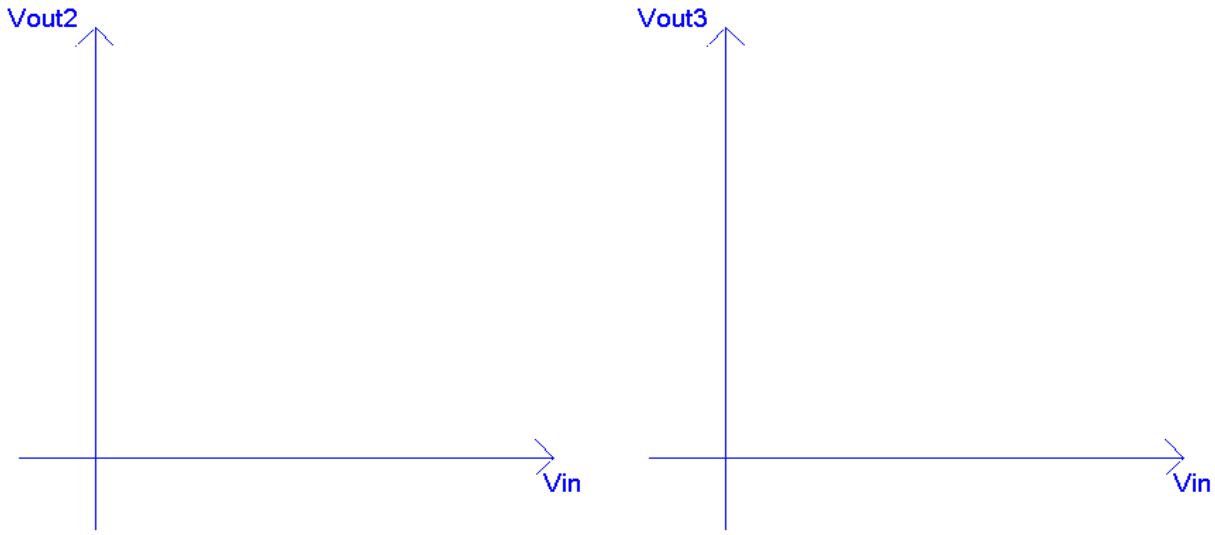
Figure 8.6

III. Cascaded Inverters:

a) Build the circuit in Figure 8.7 one inverter stage at a time. Test each stage for functionality before building the next one. Draw the VTC curves for V_{out2} and V_{out3} versus V_{in}. V_{out1} versus V_{in} was found in IIc. V_{in} is a 0 to 10V sinusoidal source with a frequency of 100Hz. (V_{in} must be on channel 2 with the oscilloscope in XY-mode to view the VTC curves)

Figure 8.7





Be sure to find and label the slope of the transition region for each VTC.

Discussion of Results

1. a) Using the data in Tables 8.1a & b, find k_n, k_p, $V_{t,n}$ and $V_{t,p}$. (Hint: the transistors are diode connected and are in saturation. V_t is the x-intercept of Figure 8.4a &b. $k^{1/2}$ is the slope.)
   $I_{d,sat}=0.5k(V_{DS}-V_t)^2$ (where k=k'(W/L))

   b) Will the current flowing through the DVM make a significant difference in finding the current flowing through the transistors in I? Explain.

   c) At $V_{in}=V_m\approx 0.5V_{cc}$, find $I_{d,n}=I_{d,p}$.

2. a) Explain why adding a load capacitance increased the transition times (10 to 90%) in IIc from those in IIb.

   b) What effect will this have on a CMOS inverter's ability to drive other digital circuits?

3. a) The VTC of V_{out2} has a sharper transition than that of V_{out1}. Similarly, V_{out3}'s transition is even steeper. Explain why this happens.

   b) What are the drawbacks of cascading inverters to improve the overall VTC characteristics?

4. Write a conclusion.