UNIVERSITY OF MIAMI
Department of Electrical and Computer Engineering
EEN 311

Name: _____
Section: _____
Date: _____

EXPERIMENT 8

JFET AMPLIFIER

PURPOSE: In the first part of this experiment, various JFET parameters will be obtained. These are:

I_{DSS} = The drain current with gate shorted to source or Vgs =0.
Vp = The pinch-off voltage
g_m = The transconductance (g_m) will be investigated

In the second part of the experiment, the student will design, construct and test the biasing network for a simple JFET Common Source amplifier while in the third part of the experiment; the student will investigate the operation of the JFET as an amplifier.

I. JFET Transfer Characteristics Curve:

Set up the circuit shown in Fig. 5.1. Make sure that the DC offset of the signal generator is set to zero. Apply a 1kHz sinusoidal waveform of about 12 $V_{p\text{-}p}$ amplitude.

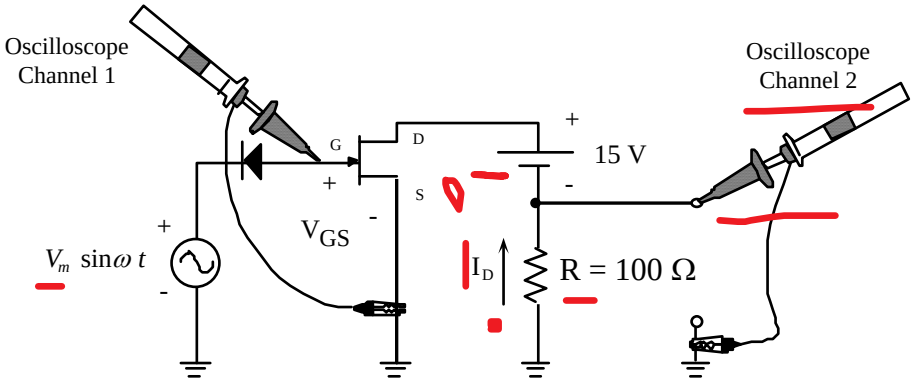


Figure 5.1 Simple JFET circuit to calculate transfer characteristics

Set the oscilloscope to the "X vs Y" mode. In this mode, the horizontal axis will correspond to V_{GS} and the vertical axis will correspond to V_R, which is equal to $V_R = -I_D R$

Set "INV CH 2" function so it will display positive drain currents. Then, the values of the drain current I_D can be read from the vertical axis as $I_D = V_R / R$.

The resulting curve will show the relation between V_{GS} and I_D. Note that for:

$I_D = 0$, $V_{GS} = -V_p$, or the pinch-off voltage, and for
$V_{GS} = 0$, $I_D = I_{DSS}$, the maximum drain current.

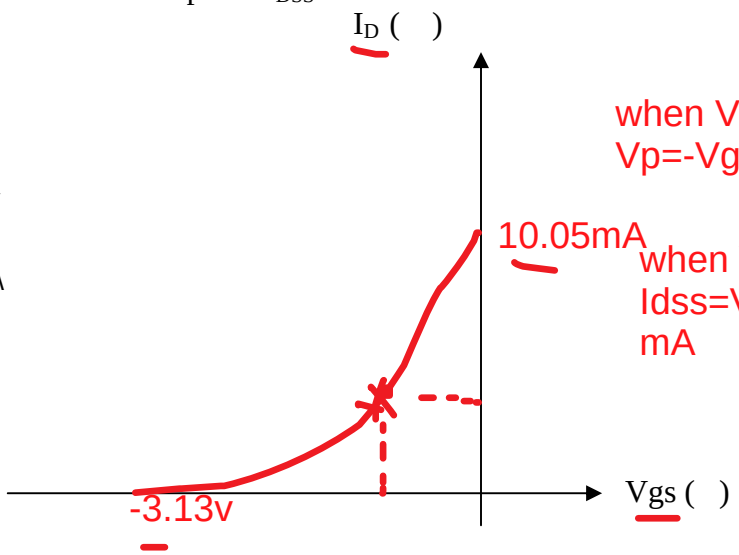
Id=0, Vgs=-Vp
Vp=-Vgs, when Id=0, VR=0

a) Plot I_D vs. V_{GS} and determine V_p and I_{DSS}.

R = 100

Vp = 3.131v

I_{DSS} = 10.18mA



when VR=0, Vgs=-3.13v
Vp=-Vgs=3.13v

when Vgs=0, VR=1.05v
Idss=VR/R=1.05/100=10.05 mA

b) Choose a point at approximately the mid-point of the active region and determine the corresponding V_{GSQ} and I_{DQ}, to be used in the part II.

V_{GSQ} = 3.131/2=1.57v I_{DQ} = -5.1mA

II. JFET Self-Biased Common Source Amplifier:

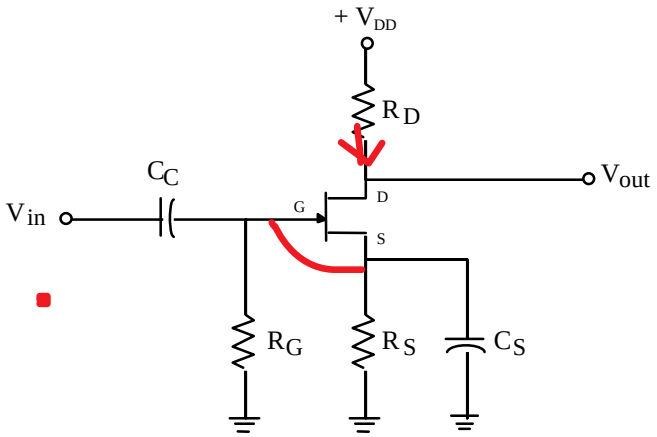


Figure 5.2 Common Source JFET amplifier circuit.

a) Design the bias circuit of Fig. 5.2 for V_{GSQ} and I_{DQ} from part Ib. Assume V_{DD} = 15 V.

i) Select R_G to be any large resistance. For example select R_G = 1 MΩ. (See note #1 at the end of this experiment)

ii) Since $I_G \cong 0$ and $V_G \cong 0$, then,

$$V_{GS} = V_G - V_S = -V_S;$$

therefore,

$$V_S = I_D R_S = -V_{GS}$$

$$R_S = \frac{-V_{GS}}{I_D} =$$ 1.57/5.1mA=307.8431

iii) From $V_{DD} = V_{DSQ} + I_{DQ} (R_S + R_D)$

Select V_{DS_Q} to be at the mid-point of the active region (See note #2 at the end of this experiment)

$$V_{DSQ} = \frac{V_{DD} - V_p}{2} = \text{(15-3.13)/2= 5.935v}$$

Then,

$$R_D = \frac{V_{DD} - V_{DS_Q}}{I_{D_Q}} - R_S = \text{(15-5.935)/5.1mA-307.8=1469.651}$$

b) Set up the circuit without the capacitors. Measure V_{R_D}, V_{DS_Q}, V_{GS_Q}, and calculate I_{D_Q}.

R_G = 1M R_S = 308 R_D = 1.47k

V_{GS_Q} = 3.0 V_{DS_Q} = 9.83 V_{R_D} = 6.75 $I_{D_Q} = \frac{V_{R_D}}{R_D}$ = 4.59mA

Make sure that the operating point is close enough to the designed one!

c) Add the capacitors C_C = 1 µF ~10 µF and C_S = 100 µF to the circuit. Apply a sinusoidal input signal and measure V_{out} and V_{in} at the frequencies shown in Table 5.1.

4.7uF

Vin(pp)=200mV
Vin_p=100mv

Freq (Hz)	**10**	**50**	**100**	**500**	**1k**	**5k**	**10k**	**50k**	**100k**	**500k**
$V_{in(p-p)}$	200mv									
$V_{out(p-p)}$										
(Av) dB										

Table 5.1 Frequency response of common source JFET amplifier.

Discussion of the Results

1. Calculate the voltage gain of the amplifier at 5KHz and compare it to the obtained value in the experiment

   Note that $$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{gs}}{V_P}\right)$$

2. Plot the frequency response of the amplifier based on the laboratory's results.

3. How could the voltage gain of the amplifier be increased?

NOTES

Note # 1

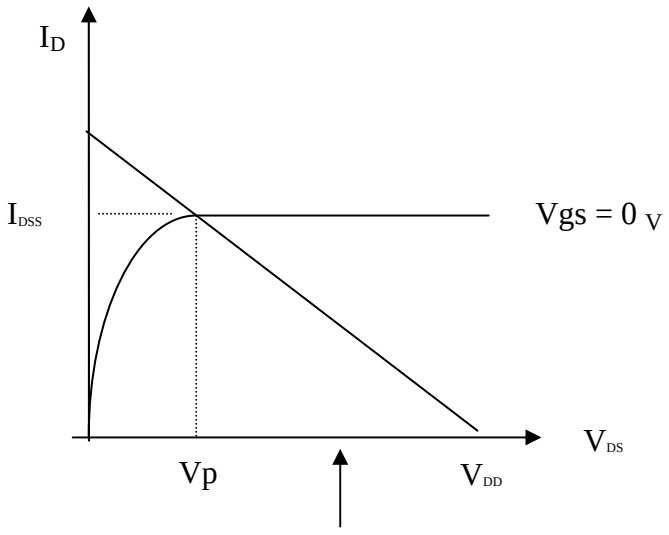
R_G

Since no current flows into the gate of the JFET, the voltage drop on R_G is zero. The only reason that it is selected to be a large resistor is to keep the input resistance of the amplifier large. Note that even a short between the gate and ground will be fine with the biasing of the device, however a short is not a possibility since it will short the input signal to ground.

Note # 2

Placement of V_{DS_Q} at the mid-point of the active region

From the shown I-V curve of the JFET and the load line, note that the operating point for a maximum swing in VDS is given by $V_{DSQ} = \frac{V_{DD} - V_p}{2}$:



For max swing in V_{DS} place the Q-point at ½(V_{DD} + V_P)