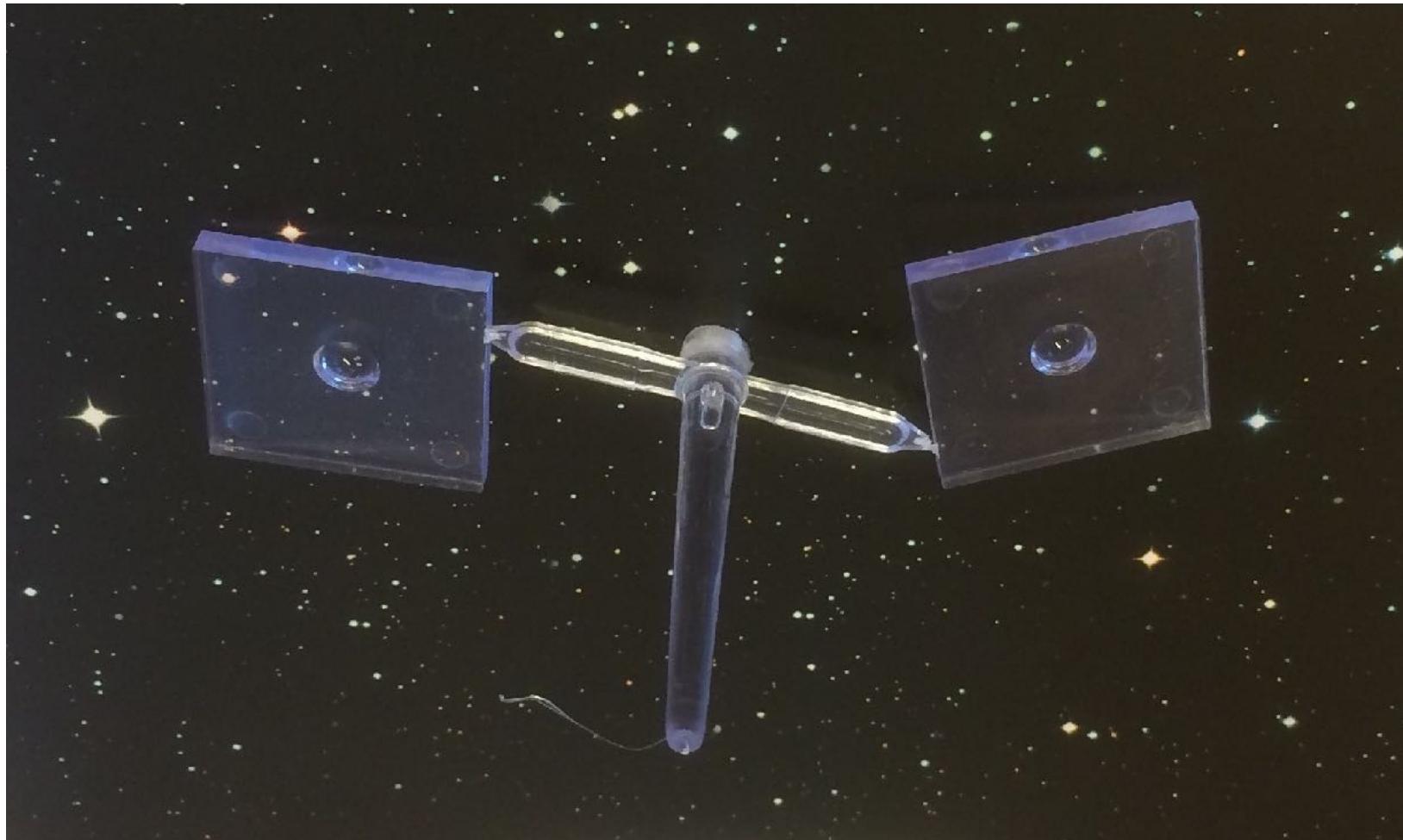


The new AH CAL prototype

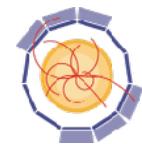


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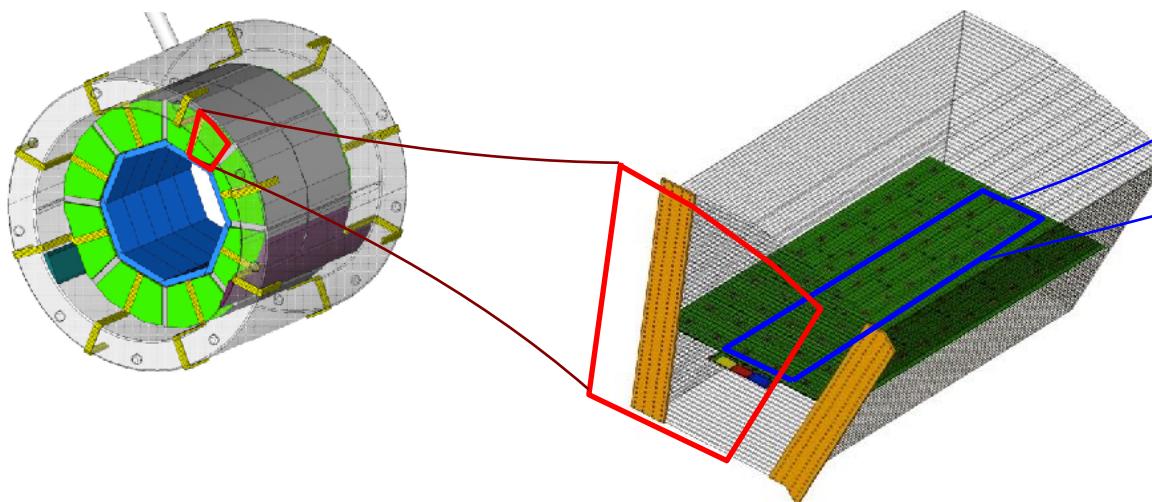
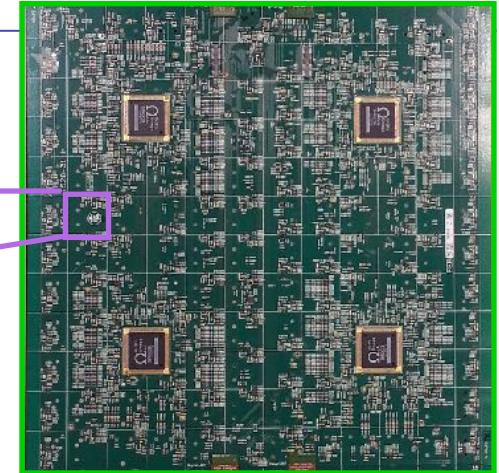
Overview

- New prototype construction effort
- Test beam plans
- Some news on granularity



AHCAL architecture

- Sandwich calorimeter based on scintillator tiles (3x3cm²) readout using Silicon Photomultipliers (SiPM)
- Fully integrated electronics
- HCAL Base Unit (HBU): 36x36cm²,
 - 144 channels readout by 4 ASIC chips
- In total 8M channels, challenge for data concentration
- Technological prototype: demonstrate scalability to full detector
- Improvement in all aspects compared to physics prototype



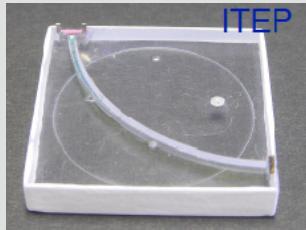
New AHCAL prototype

Felix Sefkow March 23, 2017

Progress in SiPMs and tile design

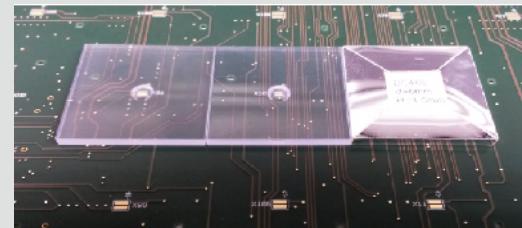
Physics prototype

2006 - 2011



Old ITEP tiles with WLS fibre
1200 px SiPMs

Technological prototype



Surface mounted SiPMs & tiles

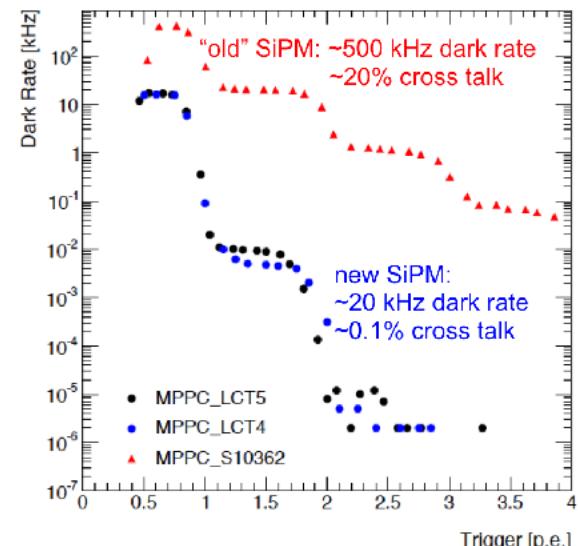
- with MPPC SiPMs 2700 px

Suitable for automated mass assembly

- SiPMs sensitive to blue light → no need for WLS fibres
- New generation of industrial SiPMs: drastically improved over the past years
 - Dramatically reduced dark rate and increased photon detection efficiency
 - Better signal-to-noise ratio, allows simpler tile design
 - After-pulses and inter-pixel cross-talk largely reduced
 - Noise rate decreases quickly with threshold, much more stable operation
- Excellent uniformity (operating voltage, gain)
 - Simplified calibration
- High over-voltage operation
 - Reduced temperature sensitivity

New AHCAL prototype

Felix Sefkow March 23, 2017



For comparison: SiPMs in physics prototype 2 MHz dark rate, 30% cross talk

Electronics and assembly

- Fully integrated electronics for mass production
- Latest generation read-out ASIC SPIROC2E successfully tested
 - reduced power consumption and many improvements
- BGA package of ASIC leads to significant PCB cost reduction and easier soldering
- HBU designed for surface mounted SiPMs & suitable for automated tile assembly
 - LED driver circuit improved channel uniformity: minimise time for test and calibration runs
- Tile assembly and cosmic test procedures established

HCAL Base Unit (HBU)



Tested in beam. Works perfectly!

New AHCAL prototype

Pick-and-place machine

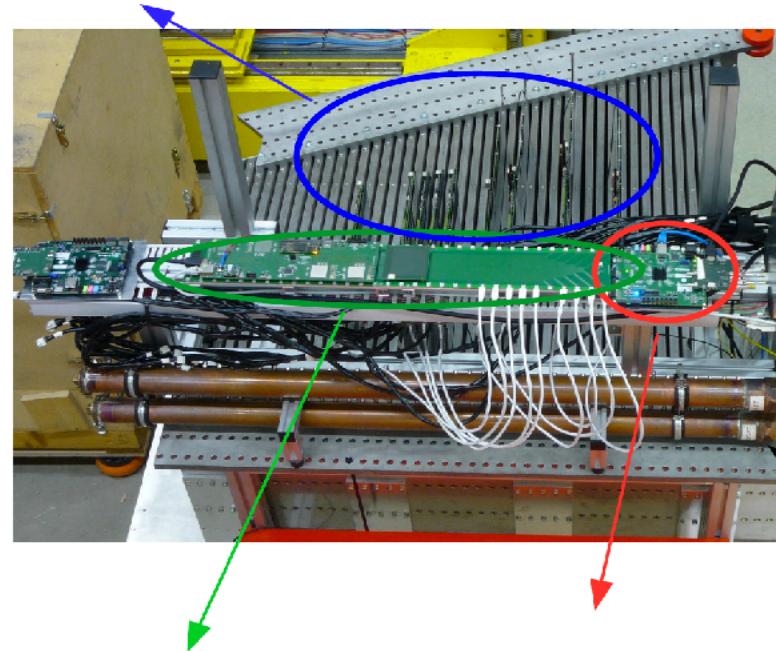


Now used routinely

System integration

- Interface boards POWER, DIF, CALIB
 - can handle full layer of large detector
 - POWER board equipped with capacitor bank for power pulsing, active temperature compensation possible
 - DIF board uses more advanced FPGA to communicate with the ASICs
- Data concentration:
 - Wing-LDA designed for ILD-AHCAL successfully operated
 - Thanks to power pulsing mode, water-cooling only for interface boards needed (leak-less design)
- Data acquisition:
 - Integrated into EUDAQ system (chosen by LC community and actively supported by AIDA-2020): successful operation

Modules (ASIC+SiPMs) and DAQ interfaces (DIF, Calibration and Power Boards)



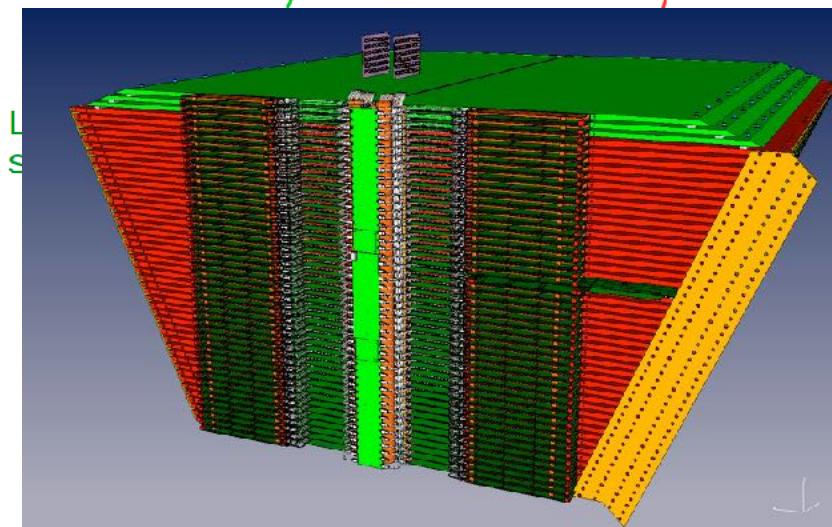
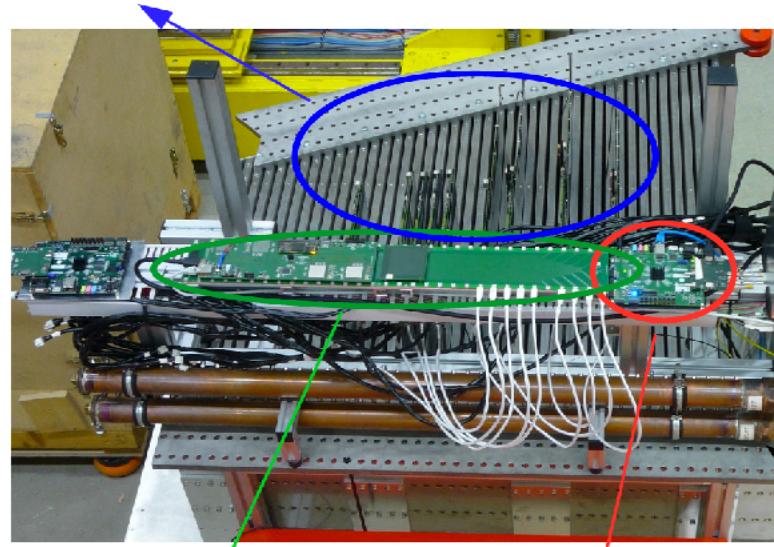
LDA (designed to fit in the space constrains)

CCC

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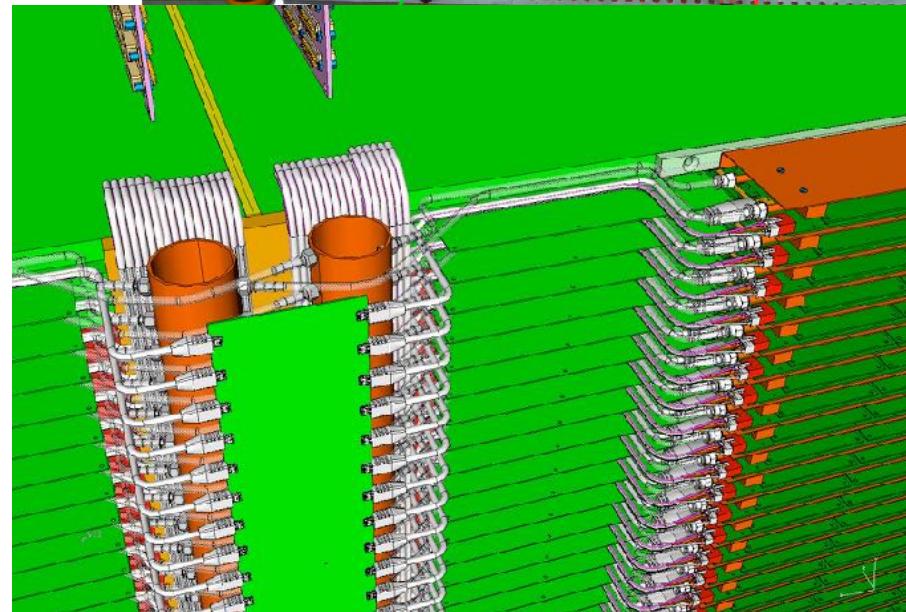
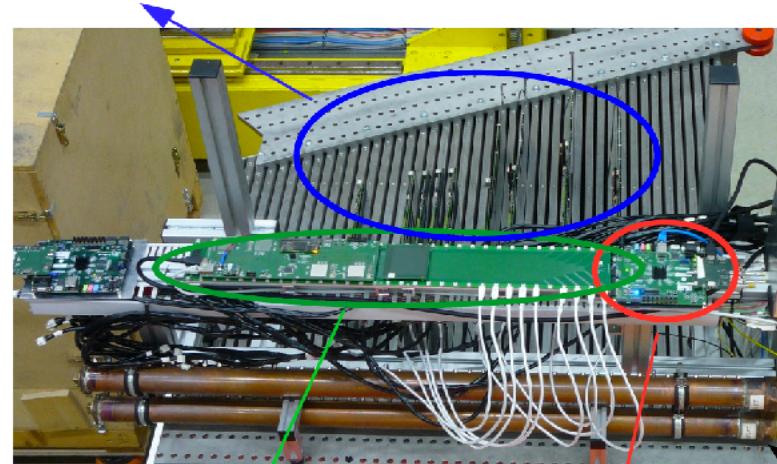
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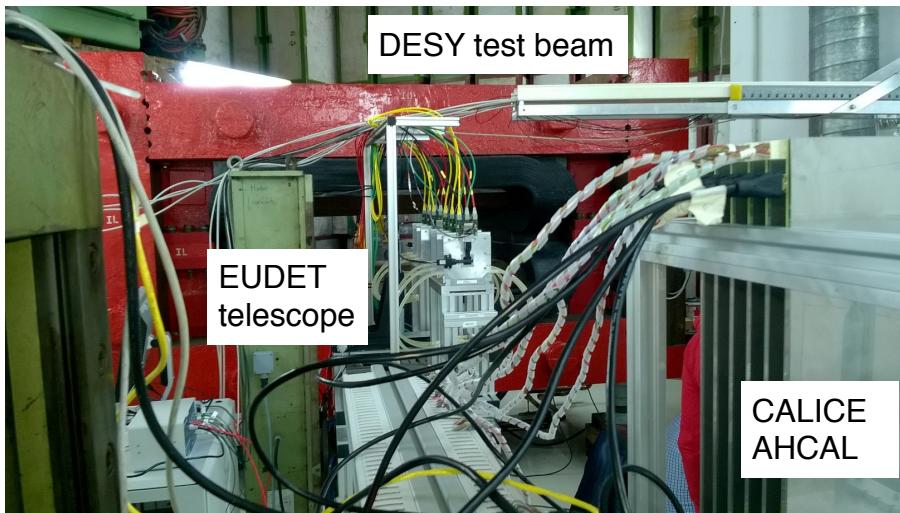
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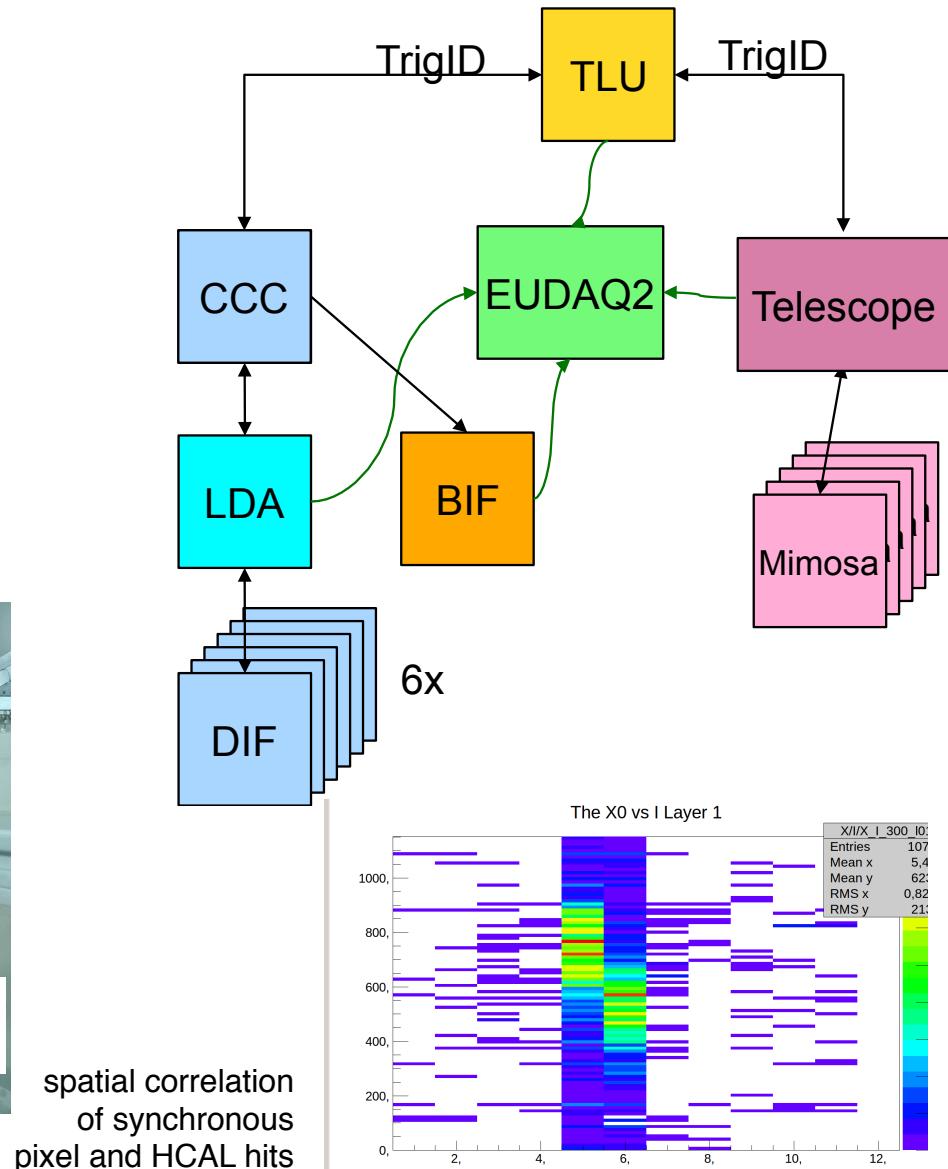


DAQ integration

- Within AIDA-2020 DAQ effort, established combined read-out of trigger-less time-stamped AHCAL and trigger-numbered EUDET telescope
- Opens many possibilities
- Proceeding towards debugging and commissioning of new trigger logic unit (TLU) and EUDAQ-2



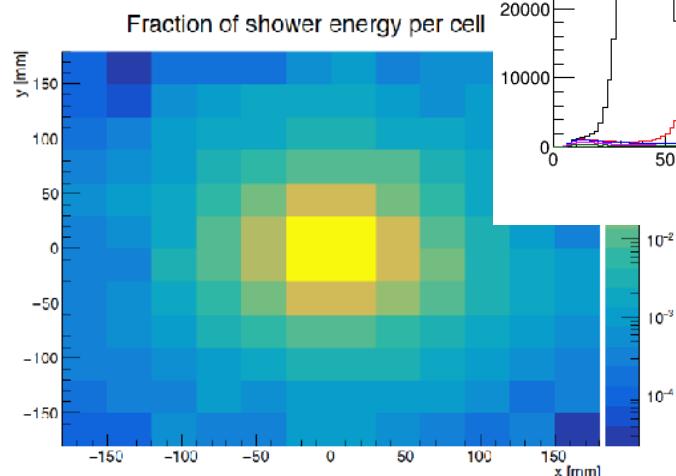
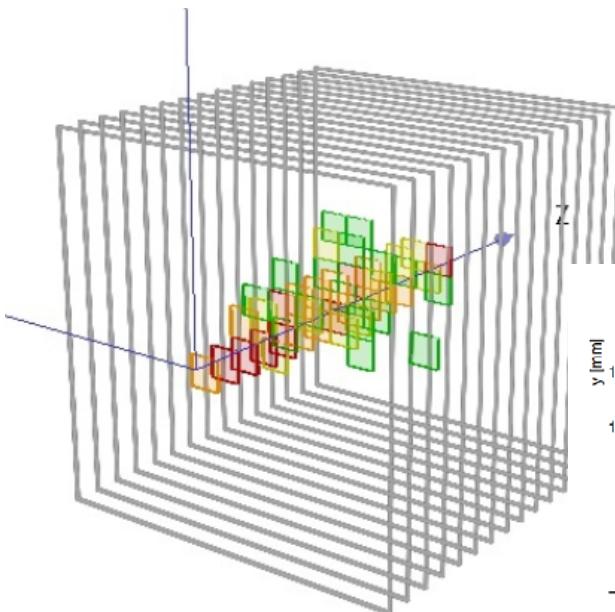
New AHCAL prototype



Felix Sefkow March 23, 2017

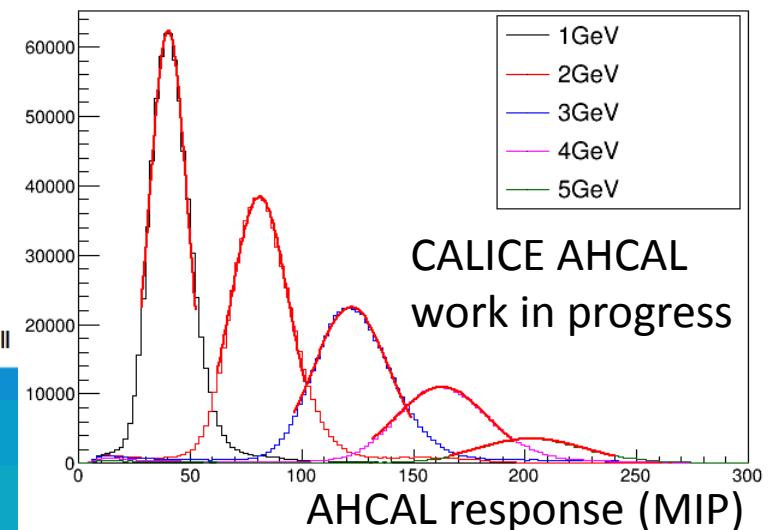
Online monitoring, software & analysis

- Online monitoring based on DQ4HEP framework
 - also handing correlations between detectors
- Quasi-online monitoring after event building and reconstruction
- Analysis in progress: energy and time
 - 2015 CERN and 2016 DESY data



New AHCAL prototype

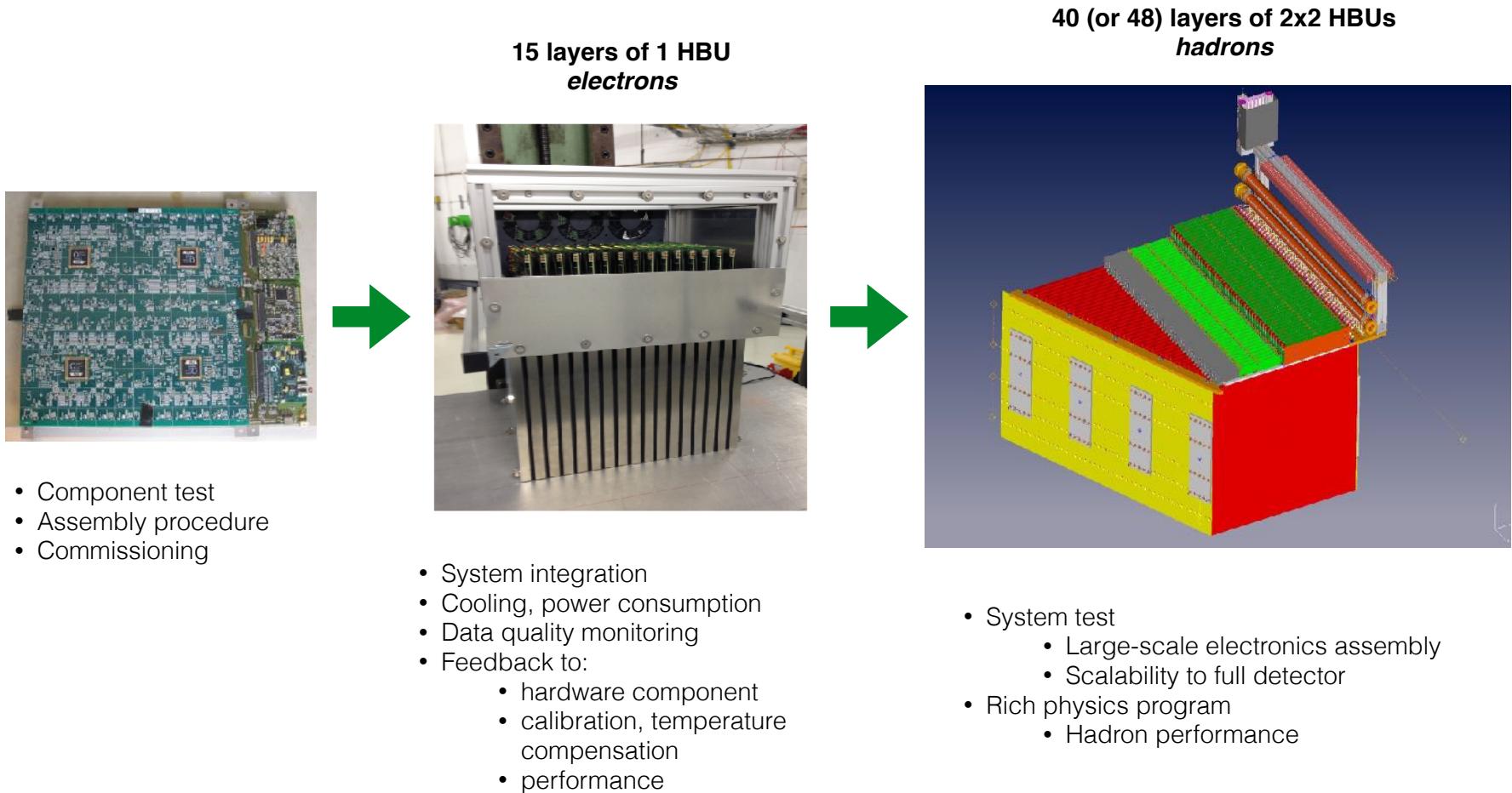
energy spectrum for 1-5 GeV



Felix Setkow March 23, 2017

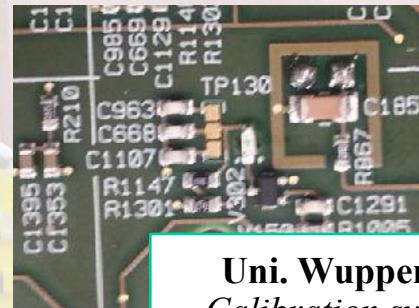
Strategy

- From single HBUs via small to large stack

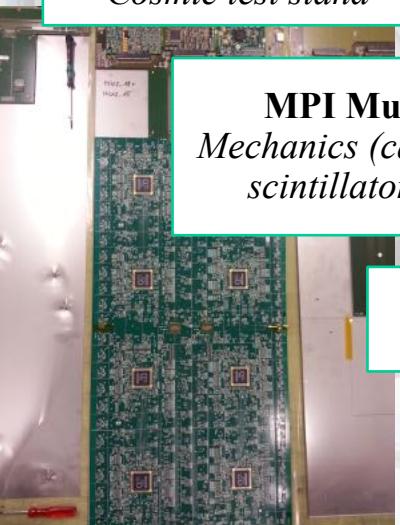


Time line

- **2016:** warming up for the new prototype
 - 1000 MPPCs, 6 HBUs
 - automatised test and assembly procedures
 - small e.m. stack, including 9 other good HBUs
 - electron beam tests at DESY and EUDAQ integration
 - new ASICs, HBUs and interfaces
 - SiPM procurement
- **2017:** construction and commissioning
 - boards in summer, layers in fall, stack in winter
 - small stack tests going on in parallel at DESY and CERN
- **2018:** full hadronic stack test at CERN SPS



Uni. Wuppertal
*Calibration system
ASIC tests*



Uni. Mainz
*DAQ, assembly
Cosmic test stand*

MPI Munich
*Mechanics (cassettes),
scintillator tests*

Prague
DAQ

**Strong contribution from
different international
& German institutes**

DESY in leading role
*Electronics & mechanics design
Commissioning
Testbeam software
Testbeam coordination*

All institutes
Analysis of data

**R&D contribution from
additional partners**

Shinshu Uni, Tokyo Uni (**Japan**)
JINR, Dubna, MEPhI, Moscow (**Russia**)
UT Arlington, Northern Illinois Uni (**USA**)

Uni. Hamburg
Tile & SiPM tests

Uni. Heidelberg
*Tile & SiPM tests
ASICs*

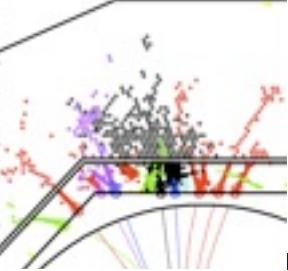


Uni. Sussex
Monitoring

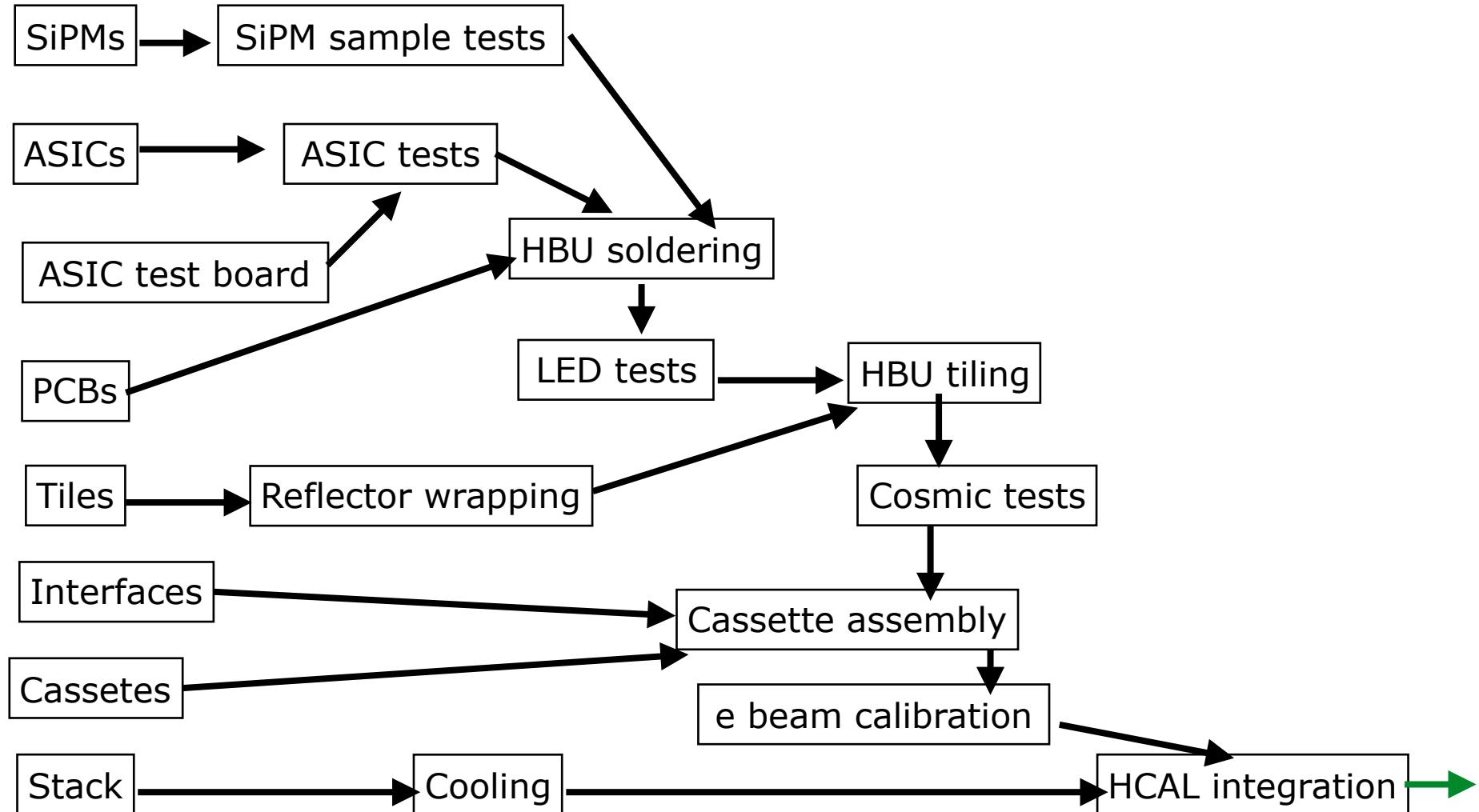
Lebedev I
Tile production

Omega (IN2P3)
ASICs

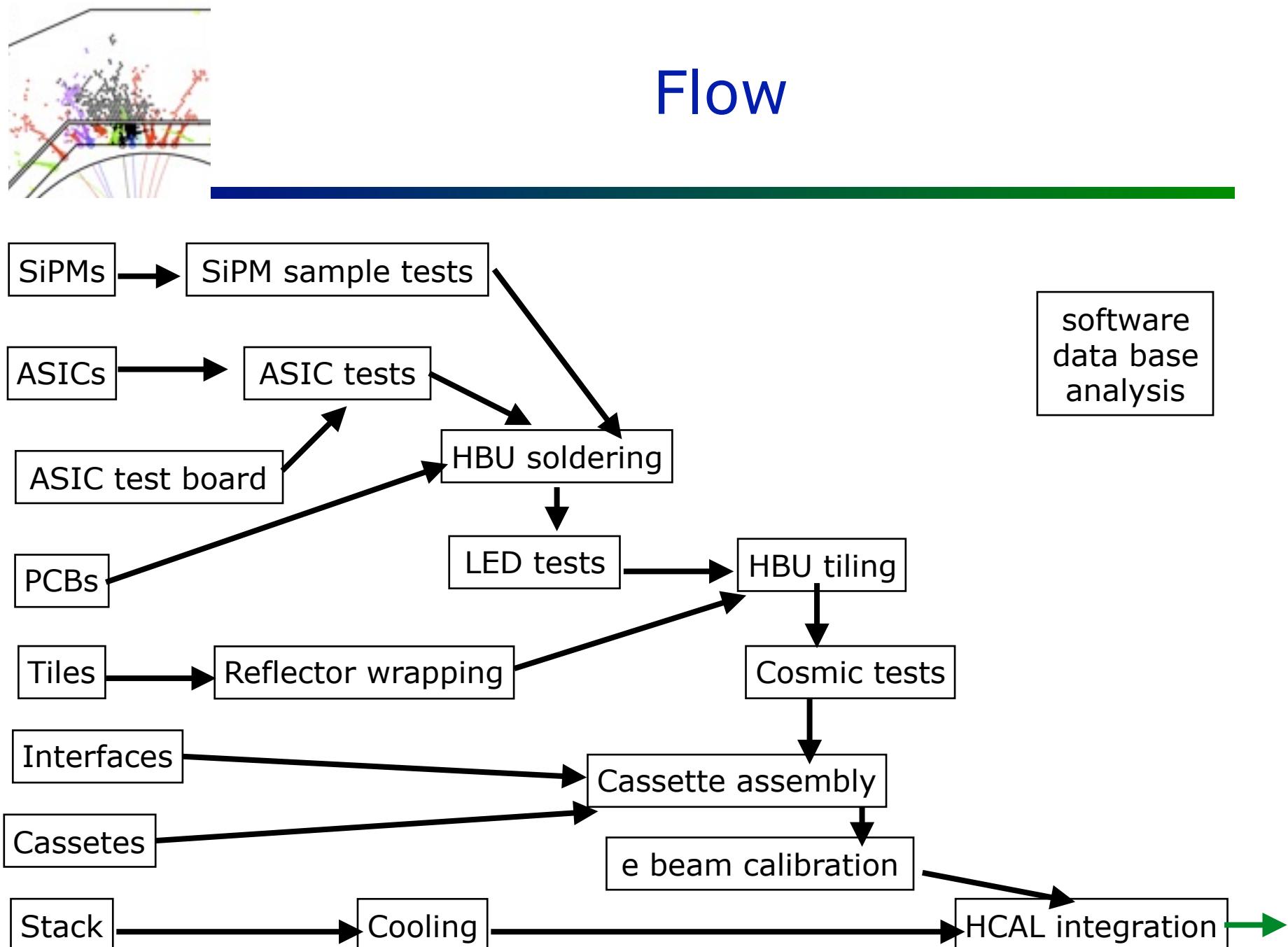
CERN
*Tungsten structure,
test beam, logistics*



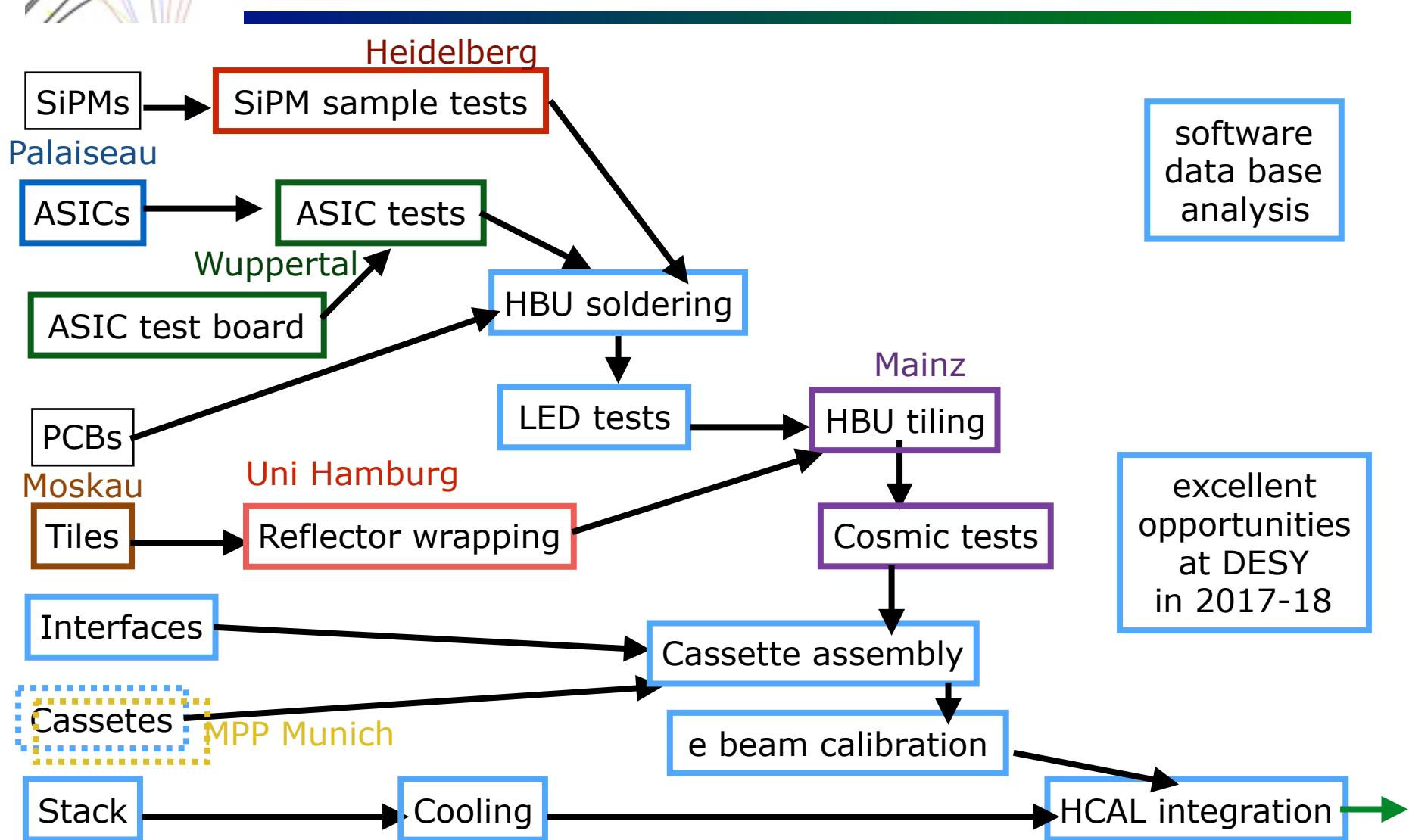
Flow



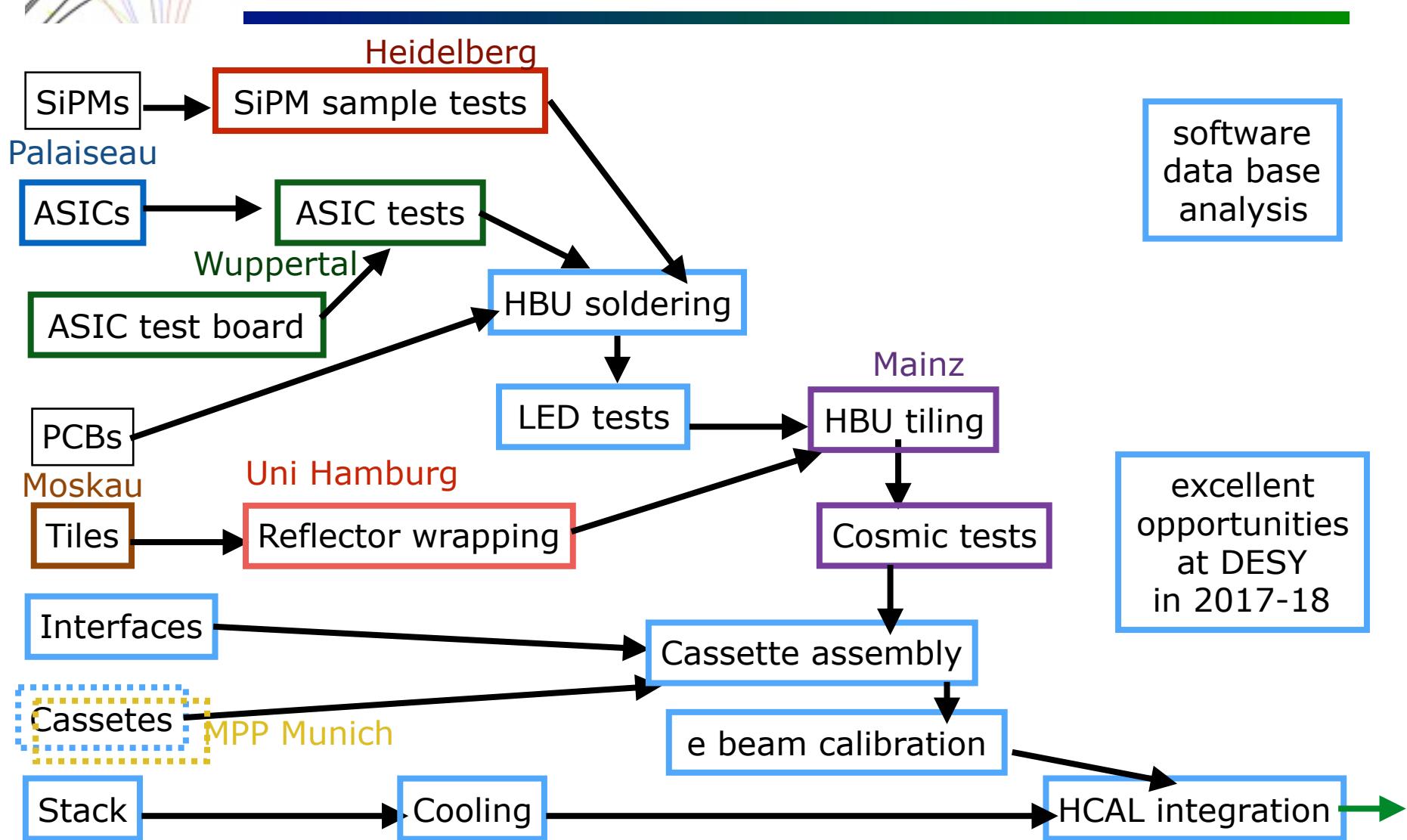
Flow



Flow



Flow



The Gantt chart illustrates the timeline and dependencies for the New AHCAL prototype project. The project begins on 1 Jan 2017 and concludes on 23 March 2018. The chart is organized into several main phases:

- Phase 1 (Jan - Mar 2017):** Includes tasks like AHCAL-ILC, Stack modifications, Cooling, Design, Components, Integration, Power, purchase 3+2 more pods, software integration, Layer, Cassettes, and Interfaces.
- Phase 2 (Mar - Jun 2017):** Focuses on spare CIB series, 20+10 CIB series, 30 piggy backs, SIB proto, 25 + 25 SIBs, HBUs with tiles, and SiPMs.
- Phase 3 (Jun - Sep 2017):** Involves delivery and sample tests for various components, followed by ASICs, packaging, and ASIC test board hardware/software.
- Phase 4 (Sep - Dec 2017):** Handles ASIC tests (1 & 2), HBUs, HBU Prototype 1, PCBs series 1, LEDs, Connectors (series 2), and HBU Prototype 2.
- Phase 5 (Dec - Mar 2018):** Features PCB production, soldering (1 & 2), and HBU test with LEDs.
- Phase 6 (Mar - Apr 2018):** Involves tile molding, wrapping, and tile placement (1 & 2).
- Phase 7 (Apr - May 2018):** Conducts cosmic tests (1 & 2) and layer assembly.
- Phase 8 (May - June 2018):** Completes layer calibration and integration.
- Phase 9 (June - July 2018):** Finishes the AH CAL system test.

Key milestones include the start of the project on 1 Jan 2017 and the completion of the AH CAL system test on 23 March 2018. The chart also shows various sub-tasks and their dependencies, such as the sequential flow from design to integration, and the parallel execution of multiple hardware and software development paths.

New AHCAL prototype

Felix Sefkow

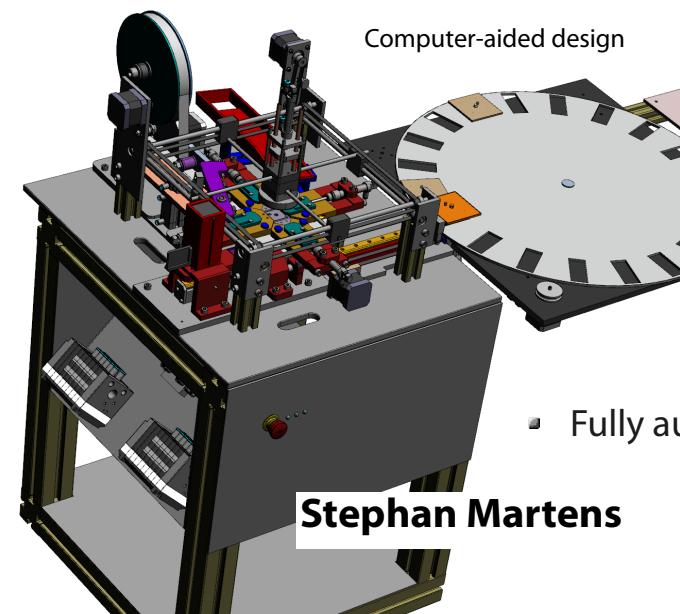
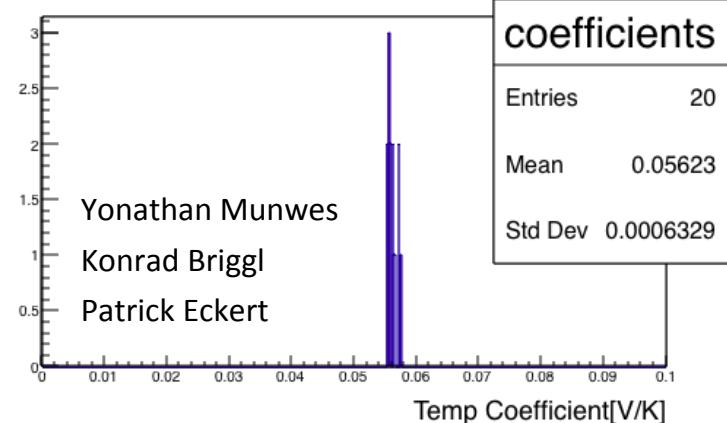
Layer integration

Status as of today

- MPPCs: first 600 delivered
 - characterised at U Heidelberg
 - excellent uniformity
 - mounted on PCBs, awaiting tiles
 - 11'400 more in April, 12'000 in May
- Tiles: 28'000 from Moscow delivered to DESY
 - first 144 to be wrapped manually
 - wrapping machine in preparation at U Hamburg
- ASICs: 400 @ DESY, 400 more to be packaged



New AHCAL prototype



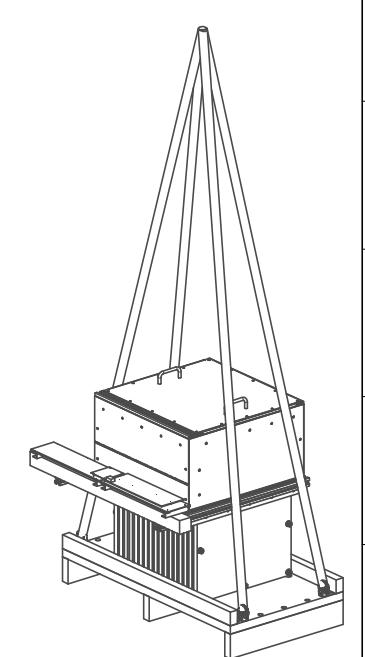
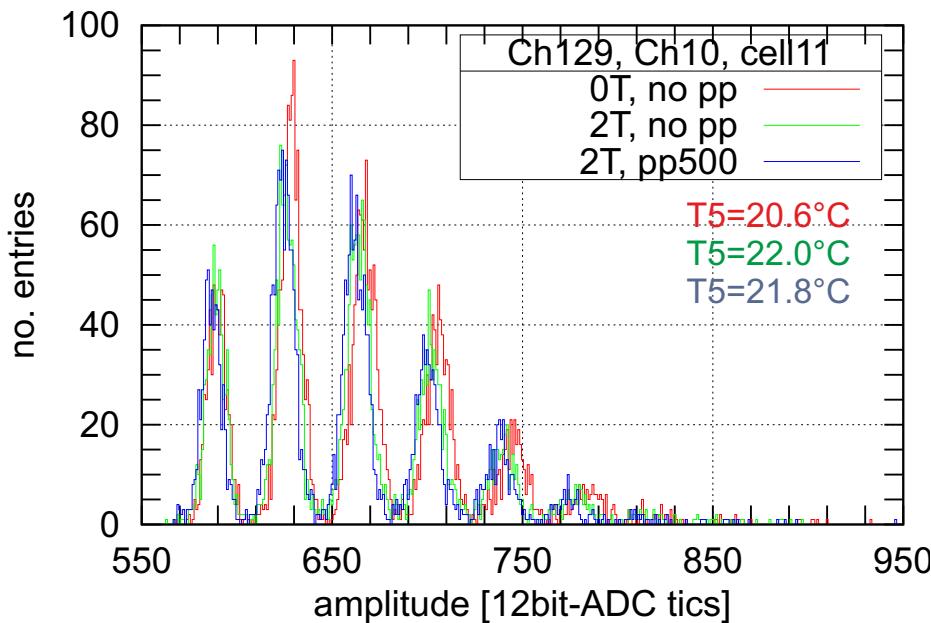
Felix Sefkow March 23, 2017

Tests with small stack

- May 2017: beam test in 3T magnetic field at SPS
 - Electronics tested last week at DESY in 2T (w/o beam)
 - Commissioning of active temperature compensation in preparation

HBU5 BGA test in 2T magnetic field

First Result, DESY, March 3rd, 2017

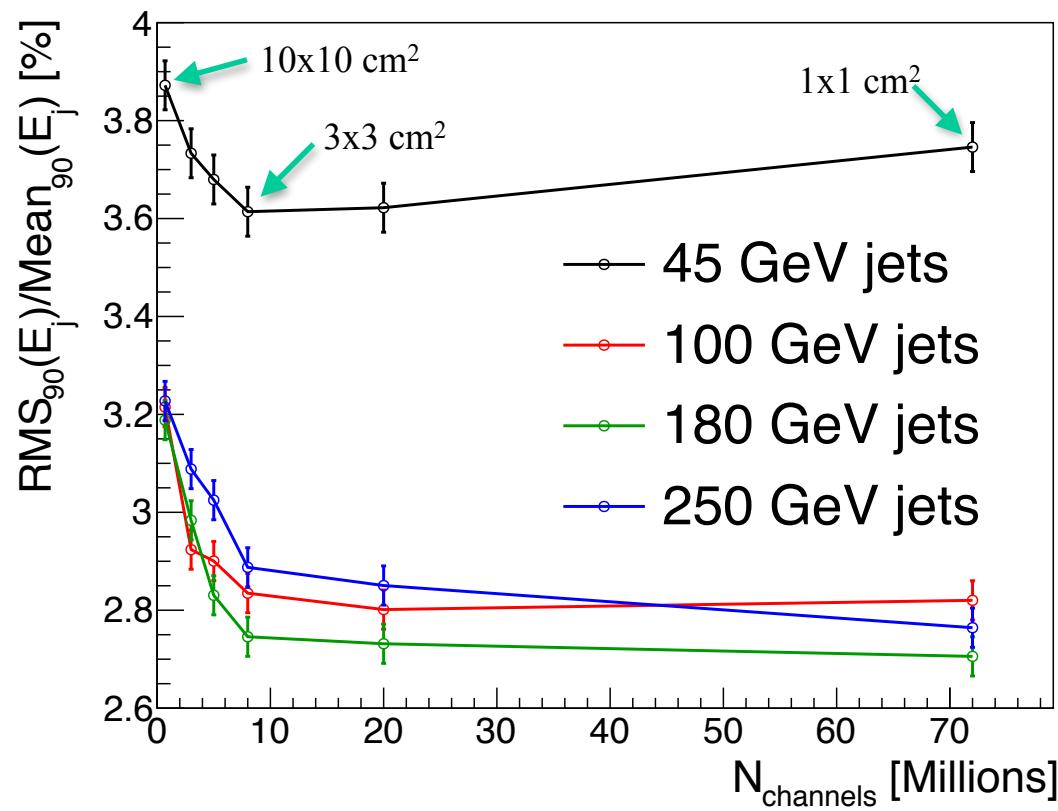
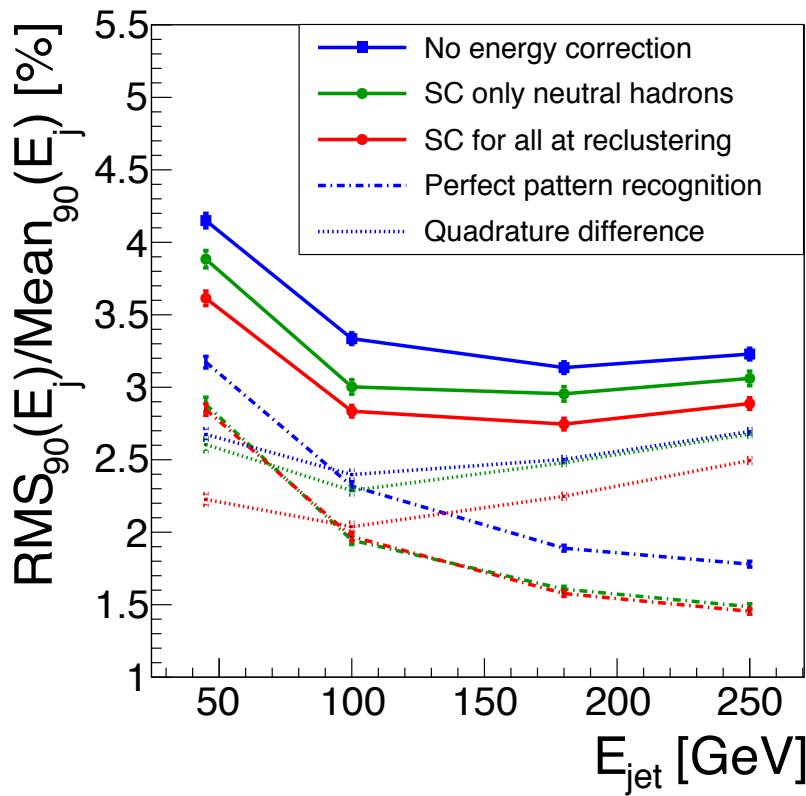


Short update on granularity and resolution

AHCAL studies using Pandora

- Done in collaboration with Cambridge
- Software compensation implemented
 - works also for SDHCAL
 - paper this month
- New study with two granularity regions

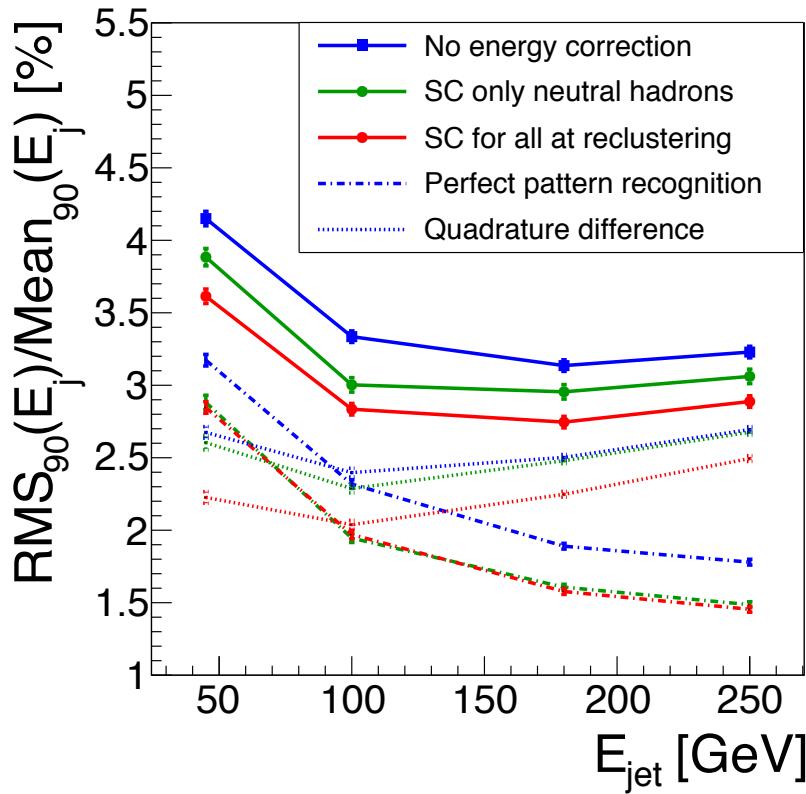
To be done for CLIC
detector with deeper HCAL



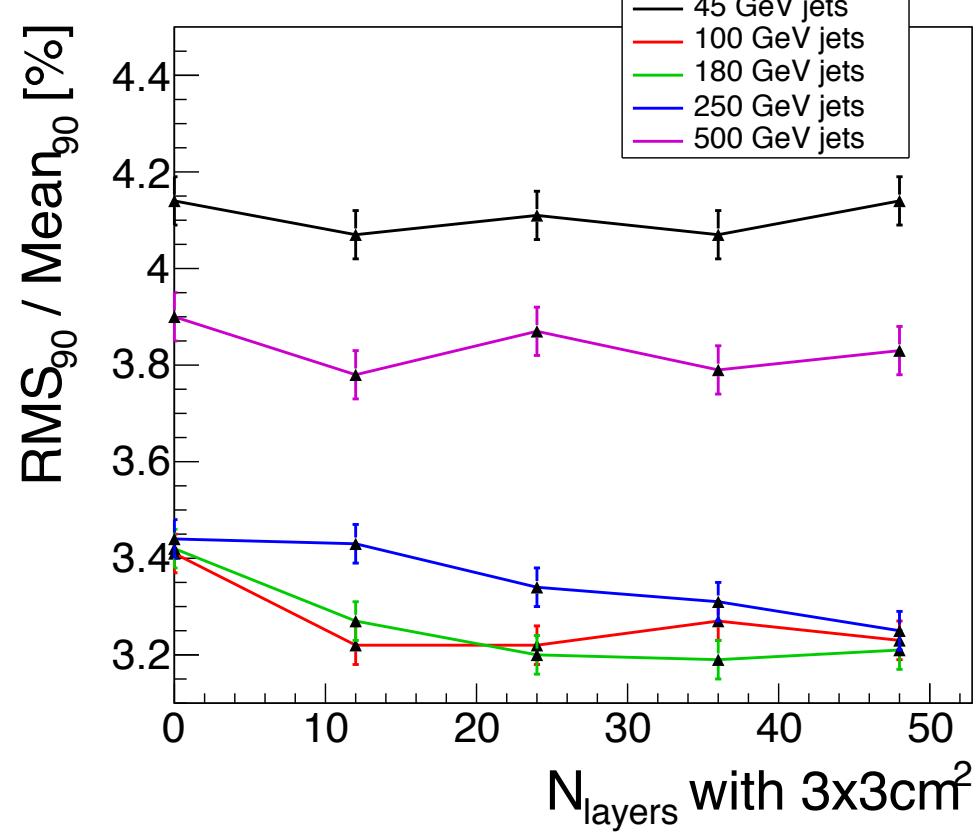
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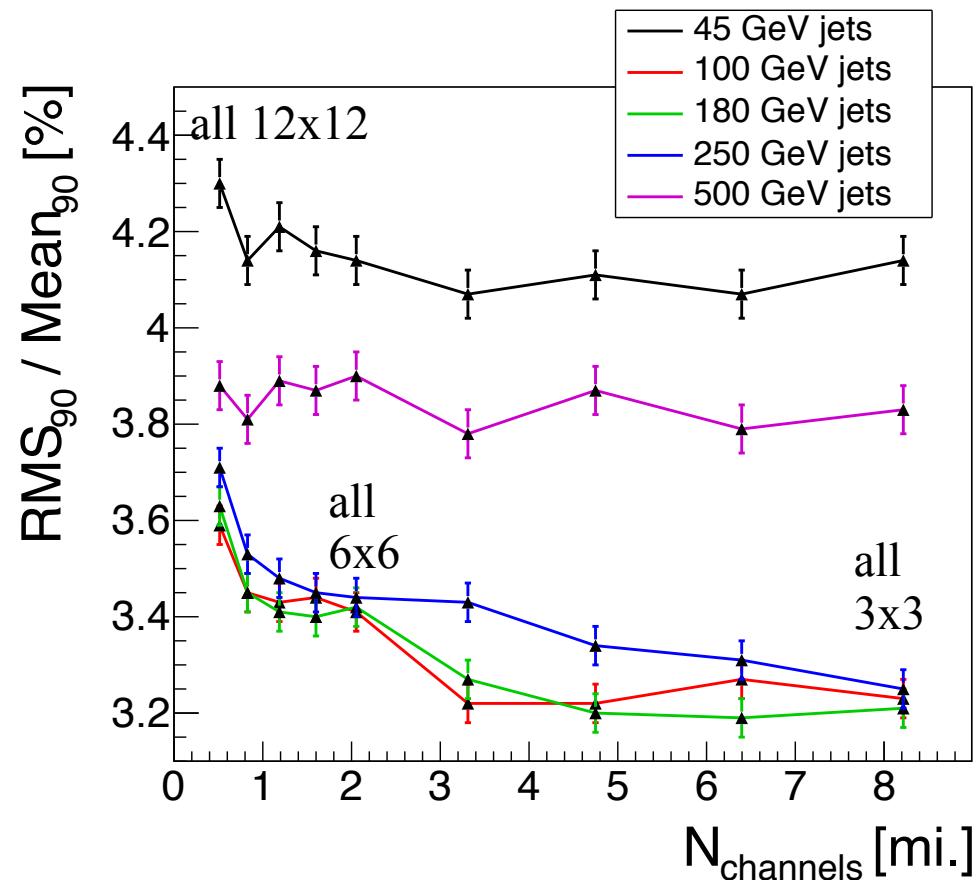
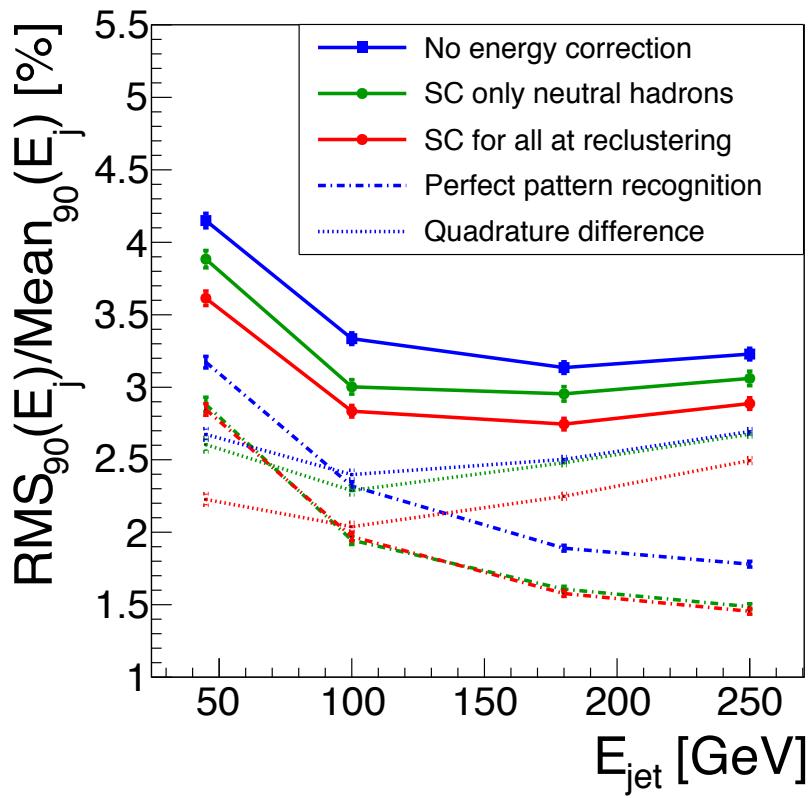
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Summary

- Construction of a new AHCAL prototype with allover improved technologies started for beam test at CERN in 2018
- Tile size optimisation reveals cost saving potential
- R&D continues, e.g. on mega-tiles, ASICs
- Cooperation with CMS HGCal on scintillator read-out electronics and beam test started