Design and Optimization of Multi-Channel Mixed-Mode ASIC:

On Noise, Mismatch and Coupling

Author: Zhenxiong Yuan

Time: 2018.12.12

(Titel der Masterarbeit - deutsch):

(Abstract in Deutsch, max. 200 Worte. Beispiel: lorem ipsum)

Lorem ipsum dolor sit amet, consectetur adipisici elit, sed eiusmod tempor incidunt ut labore et dolore magna aliqua. Ut enim ad minim veniam, quis nostrud exercitation ullamco laboris nisi ut aliquid ex ea commodi consequat. Quis aute iure reprehenderit in voluptate velit esse cillum dolore eu fugiat nulla pariatur. Excepteur sint obcaecat cupiditat non proident, sunt in culpa qui officia deserunt mollit anim id est laborum.

Duis autem vel eum iriure dolor in hendrerit in vulputate velit esse molestie consequat, vel illum dolore eu feugiat nulla facilisis at vero eros et accumsan et iusto odio dignissim qui blandit praesent luptatum zzril delenit augue duis dolore te feugait nulla facilisi. Lorem ipsum dolor sit amet, consectetuer adipiscing elit, sed diam nonummy nibh euismod tincidunt ut laoreet dolore magna aliquam erat volutpat.

Ut wisi enim ad minim veniam, quis nostrud exerci tation ullamcorper suscipit lobortis nisl ut aliquip ex ea commodo consequat. Duis autem vel eum iriure dolor in hendrerit in vulputate velit esse molestie consequat, vel illum dolore eu feugiat nulla facilisis at vero eros et accumsan et iusto odio dignissim qui blandit praesent luptatum zzril delenit augue duis dolore te feugait nulla facilisi.

(Title of Master thesis - english):

(abstract in english, at most 200 words. Example: lorem ipsum)

Lorem ipsum dolor sit amet, consectetur adipisici elit, sed eiusmod tempor incidunt ut labore et dolore magna aliqua. Ut enim ad minim veniam, quis nostrud exercitation ullamco laboris nisi ut aliquid ex ea commodi consequat. Quis aute iure reprehenderit in voluptate velit esse cillum dolore eu fugiat nulla pariatur. Excepteur sint obcaecat cupiditat non proident, sunt in culpa qui officia deserunt mollit anim id est laborum.

Duis autem vel eum iriure dolor in hendrerit in vulputate velit esse molestie consequat, vel illum dolore eu feugiat nulla facilisis at vero eros et accumsan et iusto odio dignissim qui blandit praesent luptatum zzril delenit augue duis dolore te feugait nulla facilisi. Lorem ipsum dolor sit amet, consectetuer adipiscing elit, sed diam nonummy nibh euismod tincidunt ut laoreet dolore magna aliquam erat volutpat.

Ut wisi enim ad minim veniam, quis nostrud exerci tation ullamcorper suscipit lobortis nisl ut aliquip ex ea commodo consequat. Duis autem vel eum iriure dolor in hendrerit in vulputate velit esse molestie consequat, vel illum dolore eu feugiat nulla facilisis at vero eros et accumsan et iusto odio dignissim qui blandit praesent luptatum zzril delenit augue duis dolore te feugait nulla facilisi.

Contents

1	Technology and Components	4
	1.1 Transistor	4
	1.2 Resistor	4
	1.3 Capacitor	4
2	Design overview of current version	5
	2.1 Front-end	5
	2.2 Analog-to-digital converter	5
	2.3 Digital parts	5
3	Optimization on mismatch	6
	3.1 Mismatch of components	6
	3.2 Mismatch of building blocks	
	3.2.1 Current mirror	6
	3.2.2 Operational amplifier	
	3.3 Optimization of uniformity	
4	Optimization on noise	7
	4.1 Noise components of the transistor	7
	4.2 Noise analysis for the ASIC	7
	4.2.1 Input stage	7
	4.2.2 Integration and shaper stage	7
	4.2.3 Baseline hold	7
	4.3 Optimization for the Noise	7
5	Optimization on noise coupling	8
	5.1 Power supply rejection ratio	8
	5.2 Substrate noise	8
ĺ	Appendix	9
Α	Lists	10
^	A.1 List of Figures	
	A.2 List of Tables	10
В	Bibliography	11

1 Technology and Components

This chapter will give a detail view of the technology we used for the ASIC. It is very important to get familiar with the properties of components used in the design. Since functionality of current version has been verified, in this dissertation, we will focus on the optimization. Noise, mismatches between channels and noise coupling are the main issues to be discussed.

- 1.1 Transistor
- 1.2 Resistor
- 1.3 Capacitor

- 2 Design overview of current version
- 2.1 Front-end
- 2.2 Analog-to-digital converter
- 2.3 Digital parts

3 Optimization on mismatch

- 3.1 Mismatch of components
- 3.2 Mismatch of building blocks
- 3.2.1 Current mirror
- 3.2.2 Operational amplifier
- 3.3 Optimization of uniformity

4 Optimization on noise

- 4.1 Noise components of the transistor
- 4.2 Noise analysis for the ASIC
- 4.2.1 Input stage
- 4.2.2 Integration and shaper stage
- 4.2.3 Baseline hold
- 4.3 Optimization for the Noise

5 Optimization on noise coupling

- 5.1 Power supply rejection ratio
- 5.2 Substrate noise

Part I Appendix

A Lists

- A.1 List of Figures
- A.2 List of Tables

B Bibliography

lorem ipsum. URL http://la.wikisource.org/wiki/Lorem_ipsum.

Erklärung:	
Ich versichere, dass ich diese Arbeit sals die angegebenen Quellen und Hilf	selbstständig verfasst habe und keine anderen smittel benutzt habe.
Heidelberg, den (Datum)	