Two Step SAR ADC

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Successive-approximation-register (SAR) analog-to-digital converter (ADC) have been widely used due to its lower power consumption, inherent analog simplicity and compatibility to technology scaling. However, the conversion resolution ($\sim$ 8-10 bits) and speed of SAR ADC is still largely limited by mismatches between elements and its serial decision process. A few works have been reported to combine the pipeline architecture with SAR in an attempt to achieve higher resolution as well as higher conversion speed.

A typical pipelined SAR ADC is shown in figure. , in which two SAR ADC are employed in the first and the second conversion stages connected by a residue amplifier (RA) to enable pipeline. Compared to a conventional pipelined ADC, a SAR typically offers a higher resolution in the first stage due to its simple analog structure. As a result, the front-end matching accuracy as well as the precision specs for the RA are both much relaxed. In addition, since SAR ADC typically utilizes a switched-capacitor DAC to produce the successive decision thresholds during bit cycles, so there is no necessary to introduce additional multiplying DAC (MDAC) as in conventional pipelined ADC.

This article is organized as follows. Section 1 describes the prototype ADC architecture and analysis of the static error source in the two-step ADC. Section 2 introduces the off-line calibration methods. Section 3 describes some of background calibration methods.

1 Static Error Analysis

Figure shows the block diagram of the prototype 12 bit two-step SAR ADC. In this work, we use the 6+8 bit two-step structure with 1 bit inter-stage redundancy. Since the two SAR ADC employ the MCS structure, basically the LSB of the first ADC is the same as the MSB of the second one. Therefore, this structure will give a 12 bit resolution ADC in total.

In the 180 nm process we used to implement the prototype, the inter-stage redundancy can tolerate at most 50 mV non-ideal errors with a 1.8 V reference for both sub-ADC. The nominal inter-stage gain between the two stages is chosen to be 16$\times$ (instead of 32$\times$) to decease te output swing of the residue amplifier, thereby reducing its distortion and providing the 1 bit inter-stage redundancy.

For every input voltage, a single conversion will give us a 6 bit digital output D_{FE} from the first stage, and a 8 bit digital output D_{BE} from the second stage. From these two digital words, we can extract the 12 bit final digital output. In a ideal case, the final output code and LSB of the 12 bit ADC is given below:

$$D_{OUT} = \left\lfloor \frac{D_{FE}}{2} \right\rfloor \times 128 + D_{BE} \tag{1}$$

$$LSB = \frac{LSB_{BE}}{16} \tag{2}$$

where LSB_{BE} is the LSB of the second ADC. However, there are many kinds of static errors which will in turn make a violation to the ideal case. We list some of the static errors below:

1. Non-linearity of the first ADC
2. Offset of the comparator of the first ADC
3. Gain error of residue amplifier
4. Offset of the residue amplifier
5. Offset of the comparator of the second ADC
6. Gain error of the first ADC
7. Gain error of the second ADC
8. Non-linearity of the gain of the residue amplifier
9. Non-linearity of the second ADC

We will analysis some of the static error in detail. In order to demonstrate the effects of the error sources, we take a 4-bit first stage MCS-SAR ADC for example, and plot the amplified residue voltage.

1.1 Gain error of the residue amplifier

Figure. 1 shows the effect of residue amplifier's gain error on the output of the first ADC and on the input voltage of the second SAR ADC.

1.2 Non-linearity of the first ADC

Figure. 2 shows the effect of non-linearity of the first ADC on the output of the first ADC and on the input voltage of the second SAR ADC.

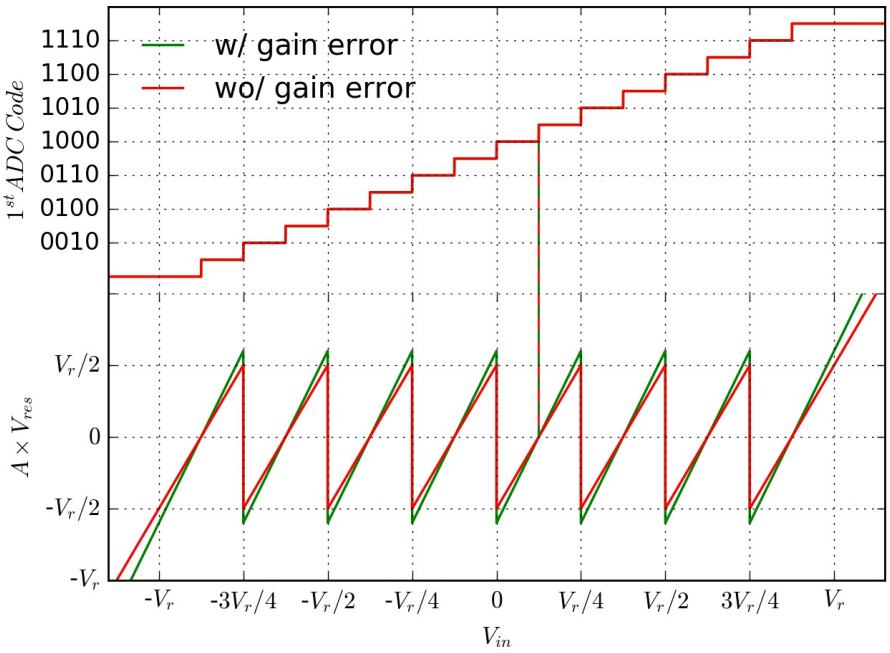

Figure 1: Gain error of the amplifier on the D_{FE} and the amplified residue voltage

2 Off-line Calibration with Ramp Test Signals

3 Background Calibration Methods

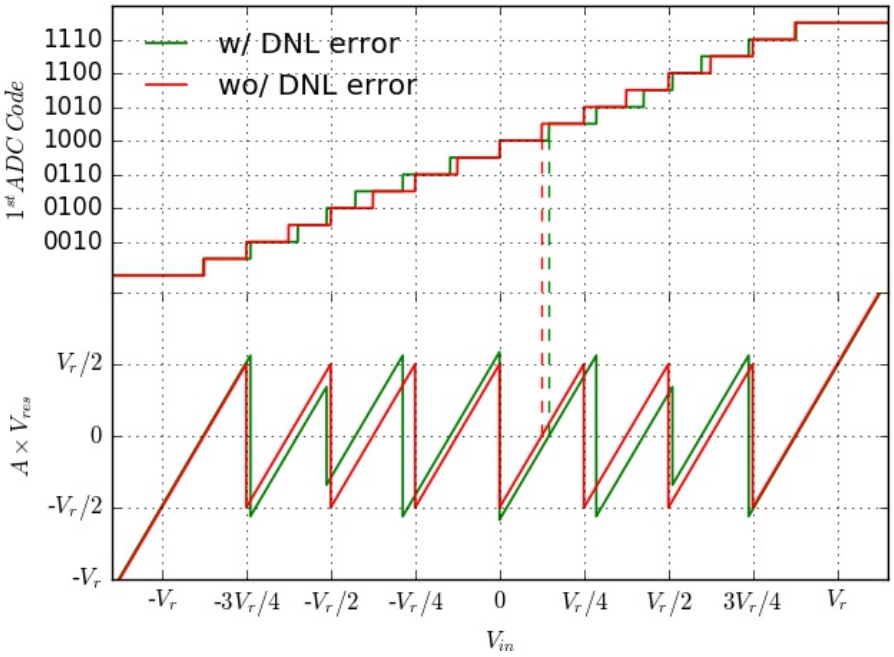

Figure 2: Non-linearity of the first ADC on the D_{FE} and the amplified residue voltage