Digital Integrated Circuit Design

Yu Bi

ELE447 – Digital Integrated Circuit Design I
University of Rhode Island
Spring 2021

ELE447

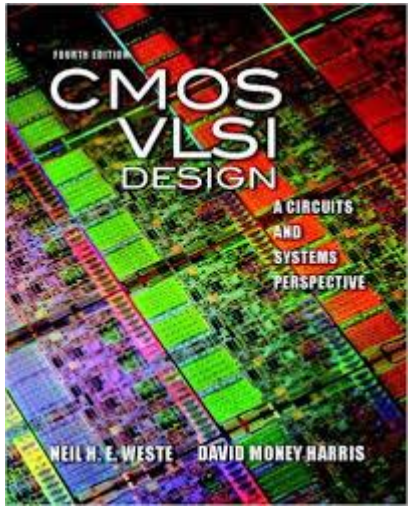
- **Title**: “Digital Integrated Circuit Design I”
- **Instructor**
  - Yu Bi, Assistant Professor, ECBE Department
- **Class Time**
  - 2:00 – 4:45 pm Wednesday, Online (Zoom)
- **Prerequisites**
  - Digital or analog circuit design
  - ELE 338/339, PH204, ELE212, ELE215 or instructor’s permission
  - A brief overview of digital/VLSI design will be provided

ELE447

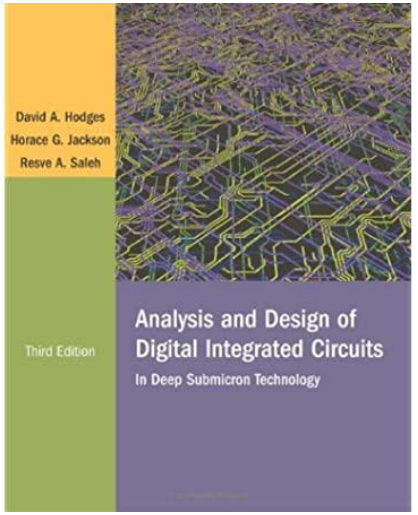
- **Office Hours**
  - 2:00 – 4:00 pm Tuesday&Thursday
  - Fascitelli Center 410
- **Textbooks**:
  - D. Harris and N. Weste, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th edition, Pearson, 2010.
  - D. A. Hodges, H. G. Jackson, R. A. Saleh, Analysis and Design of Integrated Circuits, 3rd edition, McGraw-Hill, 2004. ISBN 0-07-228365-3.
- **Course Websites:**
  - https://yubi-ece.github.io/teaching/ele447_digital_ic.html
- **Supplementary**
  - Opencores, https://opencores.org/

Textbooks and Materials

- Textbooks (not required):
  - CMOS VLSI Design: A Circuits and Systems Perspective, Pearson, 2010.
  - Analysis and Design of Integrated Circuits, McGraw-Hill, 2004.



- Reading Materials
  - Conferences: IEEE ISCAS, IEEE/ACM DAC, DATE, IEEE ICCAD; IEEE SSCC; IEEE CICC; IEEE VLSI Circuits, etc.
  - Journals: IEEE JSSC, IEEE TCAS-I/II, IEEE TCAD, IEEE TC, IEEE TVLSI etc.



Course Objectives

This is an introductory course in CMOS integrated circuit design where you will go from the low-level physical transistor and mask design of your own cell library, all the way to the design, implementation, and fabrication of a significant CMOS digital integrated circuit.

Course Topics

- CMOS Logic, Switch Models & Simple RC Models;
- IC Fabrication, Layout & Design Rules;
- Device Physics, MOS Models, Device Scaling & Short-channel effects;
- Static CMOS & Pseudo NMOS Logic Gates;
- Pass Transistor Logic;
- Dynamic Logic & Other CMOS Logic Families;
- Static/Dynamic Flip-Flops, Registers, Semiconductor Memory, Counters & Arithmetic Elements;
- …

Work required by this course

- Lectures
  - Read sections in text and slides before class
- Lab Assignments
  - Six major exercises dealing with various aspects of VLSI design
  - Complete each section before the deadline
- Final Project
  - Your opportunity to design a chip of interest to you
  - Design could be completed to the point where it could be fabricated by following process covered this course
- This course includes a large amount of useful information and skill practice that will help you for your future career

Grading

- Grading
  - Lab Assignments and Reports: 60%
  - Student Final Projects and Reports: 40%

- Project
  - Individual
  - Propose or select from a given list of projects.

Collaboration is good! Cheating is not!

- Collaboration is good!
  - Discussing issues with your classmates is a good way to learn and a study group is a very effective learning tool. Feel free to discuss lab exercises with classmates, TAs and the instructors
  - Helping each other learn is particularly satisfying
  - But Individual assignments and projects must be done by individuals

- Cheating is a serious breach of trust and will not be tolerated
  - If ever in doubt, don’t do it or ask me immediately for a clarification
  - Don’t cheat, its not worth it.

IC Design - The Big Picture

- Today we are generally designing IC systems for a particular embedded application:
  - Need to decompose design into sub-functions
  - Need to integrate the various sub-functions into a System-on-a-Chip
  - Guess what? Also need to write 1 million lines of code to make your system work.

- What do you do with a billion transistors?
  - The real question is how do you test a billion transistors to make sure they were manufactured correctly?
  - How do you co-verify a million lines of software and the billion transistors?

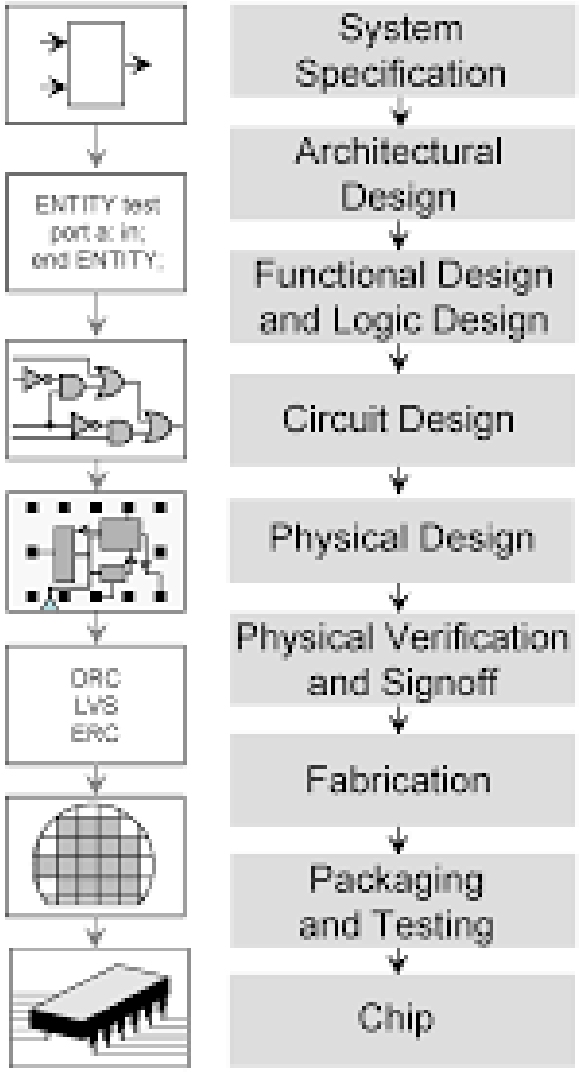
Types of IC Designs

- IC Designs can be **Analog** or **Digital** or both!!

- Digital designs can be one of three groups
  - **Full Custom**
    - Every transistor designed and laid out by hand
  - **ASIC** (Application-Specific Integrated Circuits)
    - Designs synthesized automatically from a high-level language description
  - Semi-Custom or structured custom
    - Mixture of custom and synthesized modules

- Analog designs are generally full custom
  - Digitally assisted Analog is a combination of full custom and ASIC

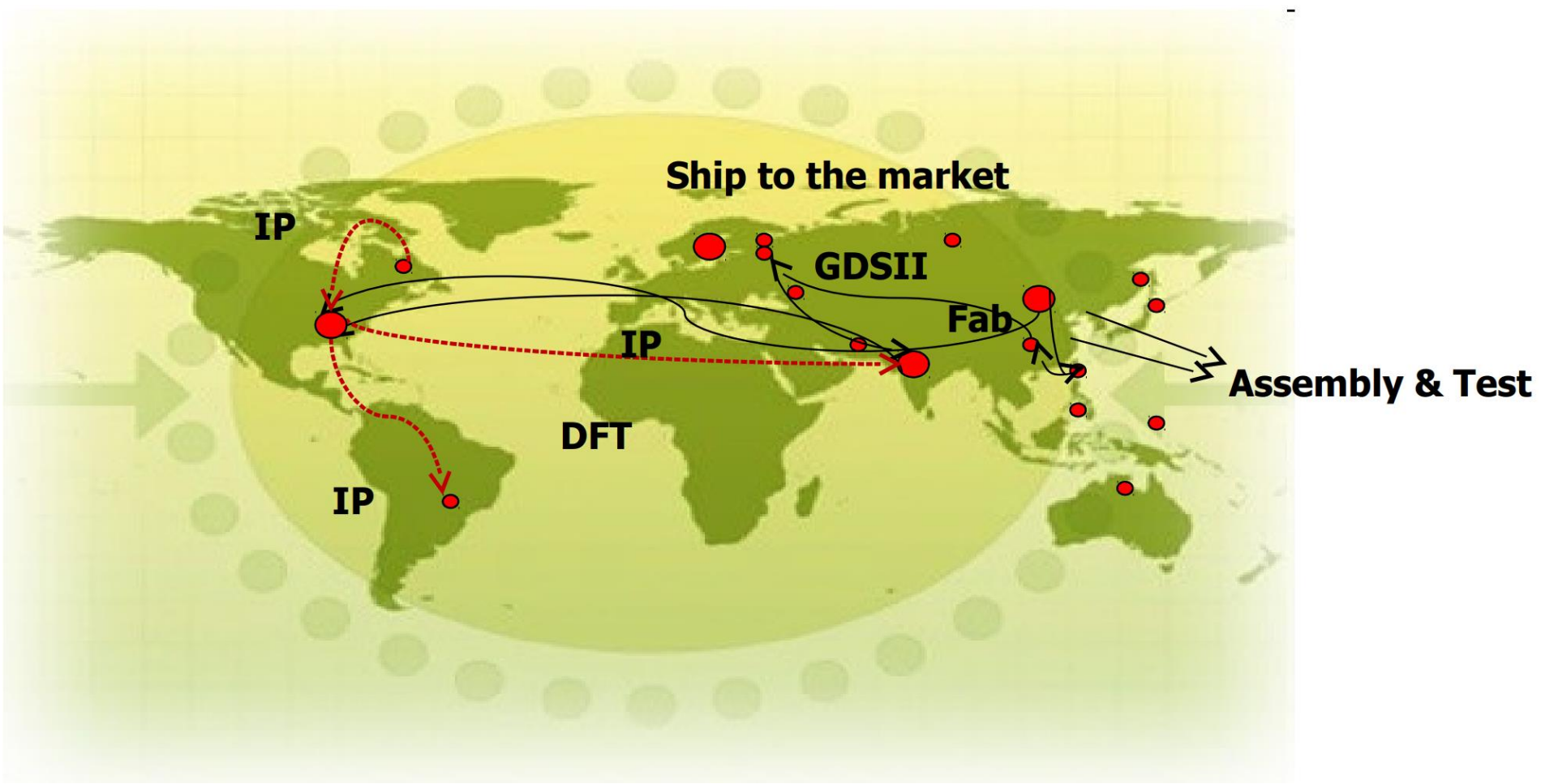
Digital IC Design Flow



Old IC Landscape

-

IC Globalization



Laboratory Design Tools

- We will use commercial CAD tools
  - **Cadence**, Synopsys, etc.

- Commercial software is powerful, but very complex
  - Designers sent to long training classes
  - Students will benefit from using the software, but we don’t have the luxury of long training
  - TAs have experience with the software

- Start work early in the lab
  - Plan designs carefully and save your work frequently.

Tools for Lab/Projects

- Tools
  - Circuit Simulation: Cadence Virtuoso
  - Remote Access: MobaXterm; Xpra
    - MobaXterm: https://mobaxterm.mobatek.net/
  - Linux commands, Bash and Shell etc.

- Hardware
  - URI Engineering Servers

URI Linux Account

ECBE Portal Link: https://portal.ele.uri.edu/

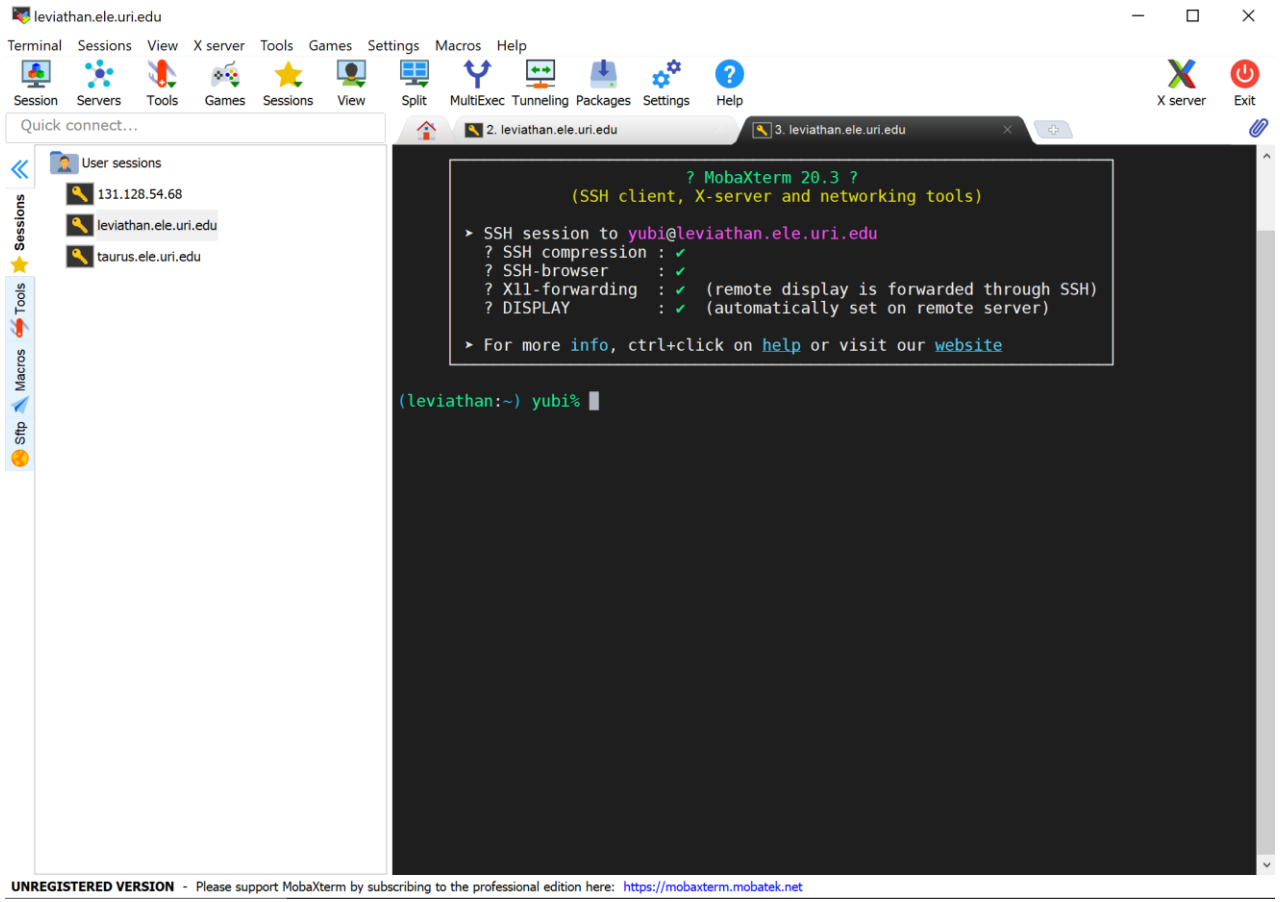
Instruction:

1) Visit the ECBE Portal
2) Log in with their URI G-Suite accounts
3) Use the Portal's "Create/Reset ELE Account" function to create their ELE accounts

The Portal's account creation form has a text field for justification for the new account. Simply enter "ELE448" in the justification field.

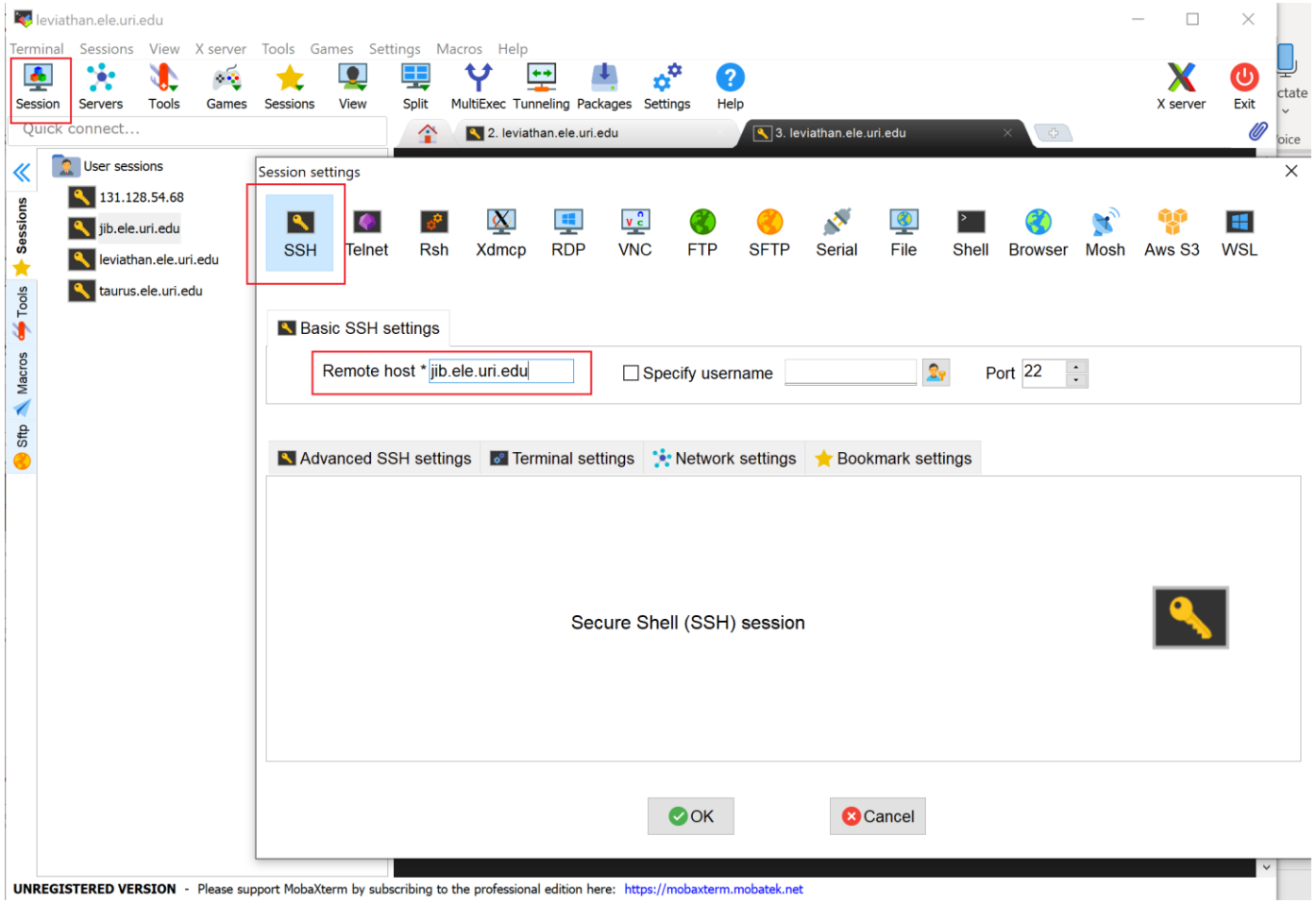
Remote Access

- MobaXterm
  - https://mobaxterm.mobatek.net/



Remote Access

- MobaXterm
  - Connect to URI engineering servers (e.g. jib.ele.uri.edu)



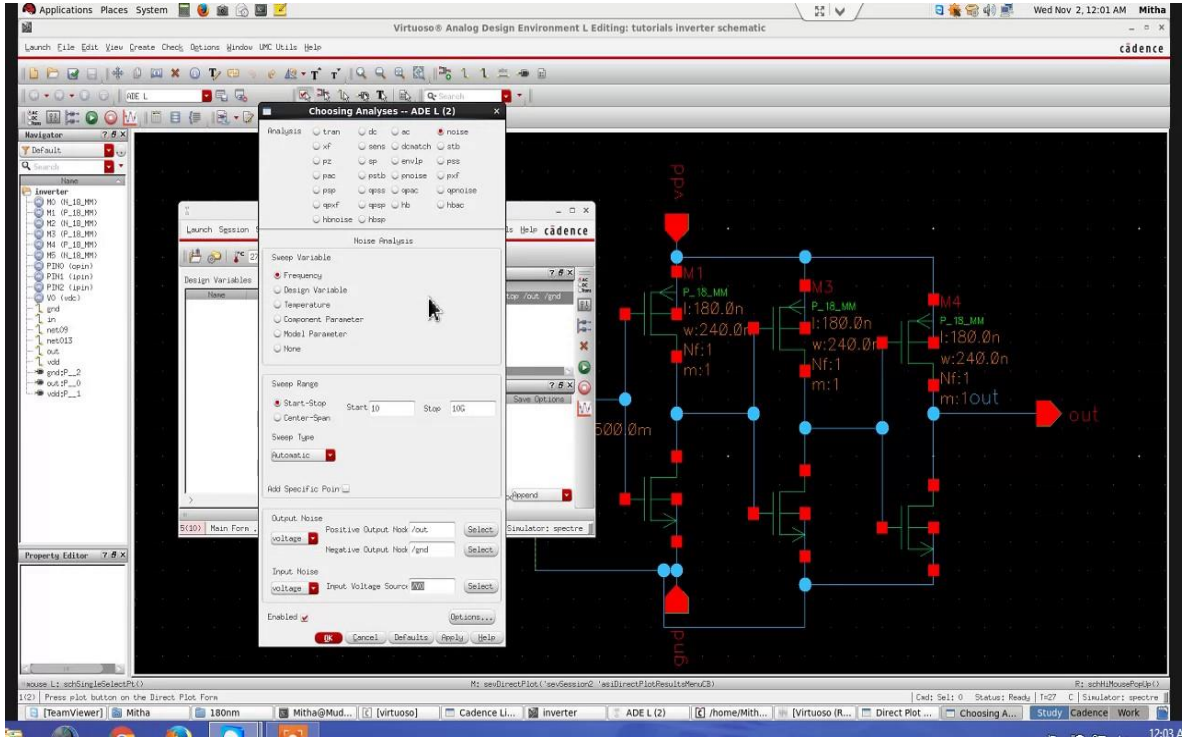
Remote Access

- URI Engineering Server Lists
  - *.ele.uri.edu (* is computer name)
- Students will be assigned to each computer

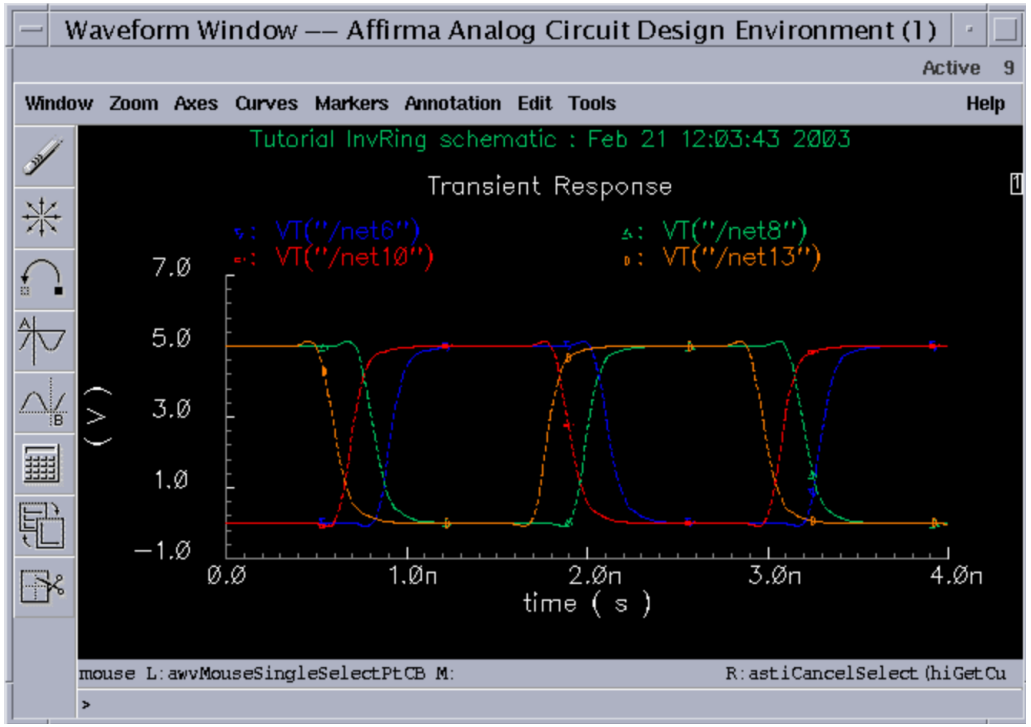
Computer Name
jib
fin
keel
bow
oar
rudder
anchor
sail
mast
shark
sans
papyrus
toriel
eddie
undyne

Cadence

- Circuit Schematic and Simulation



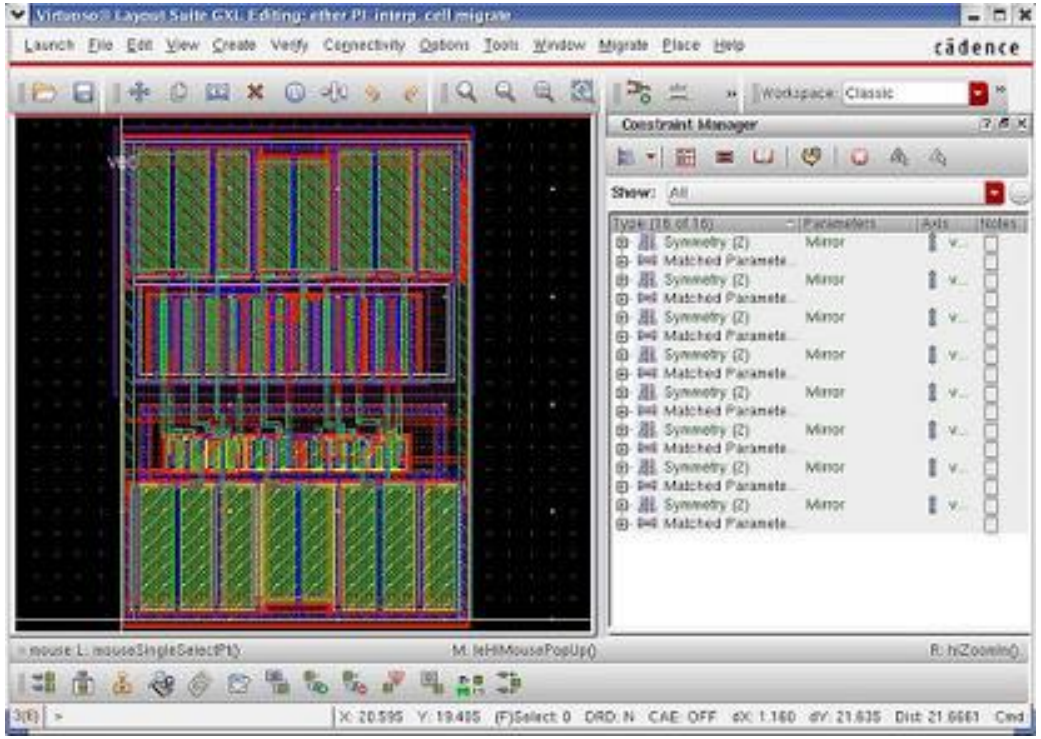
Circuit Schematic



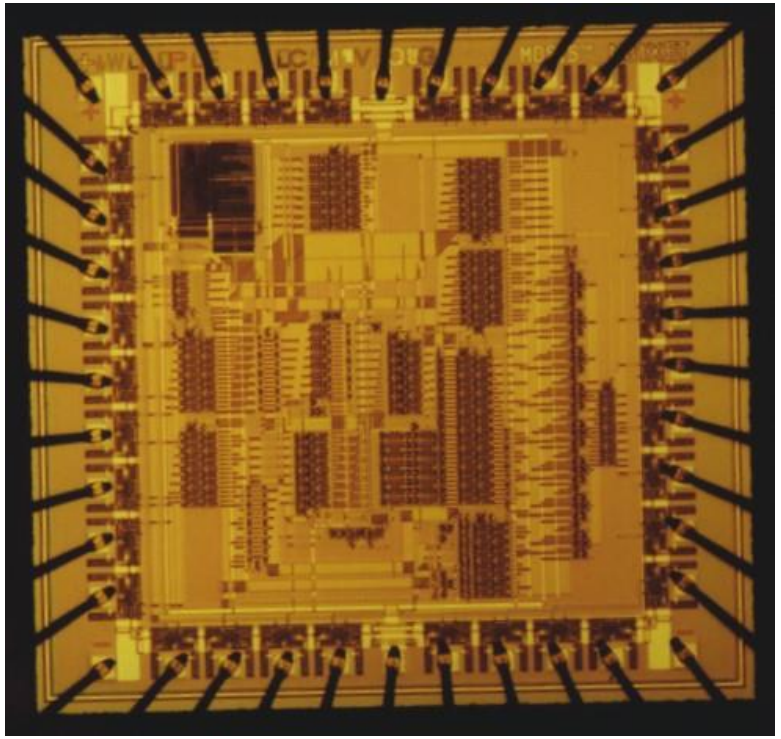
Circuit Simulation

Cadence Virtuoso

- Circuit Layouts and Fabrication



Circuit Layouts

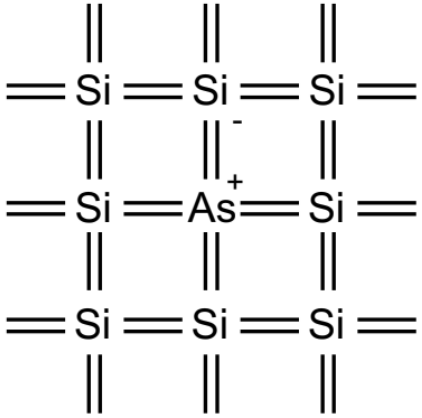


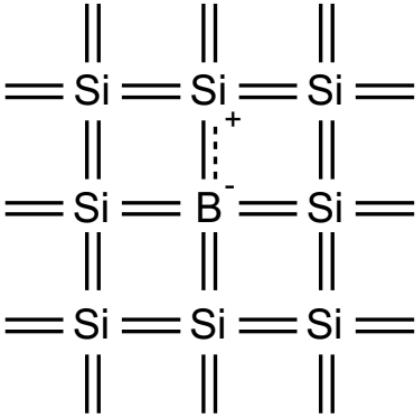
Chip Image

Take a Break!

Silicon (Si)

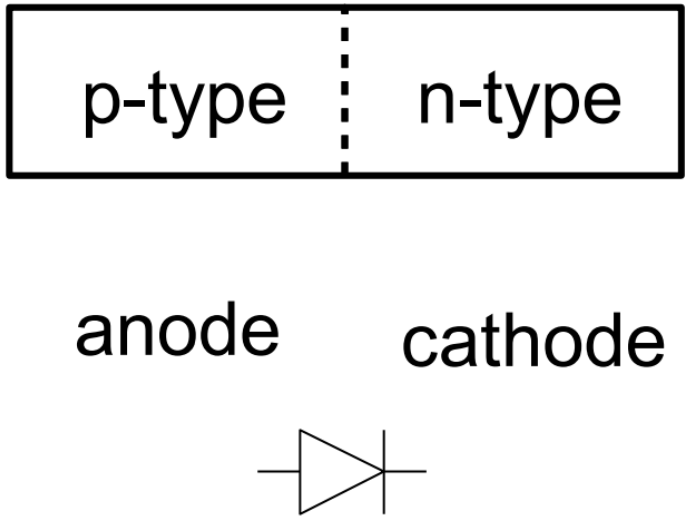
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)





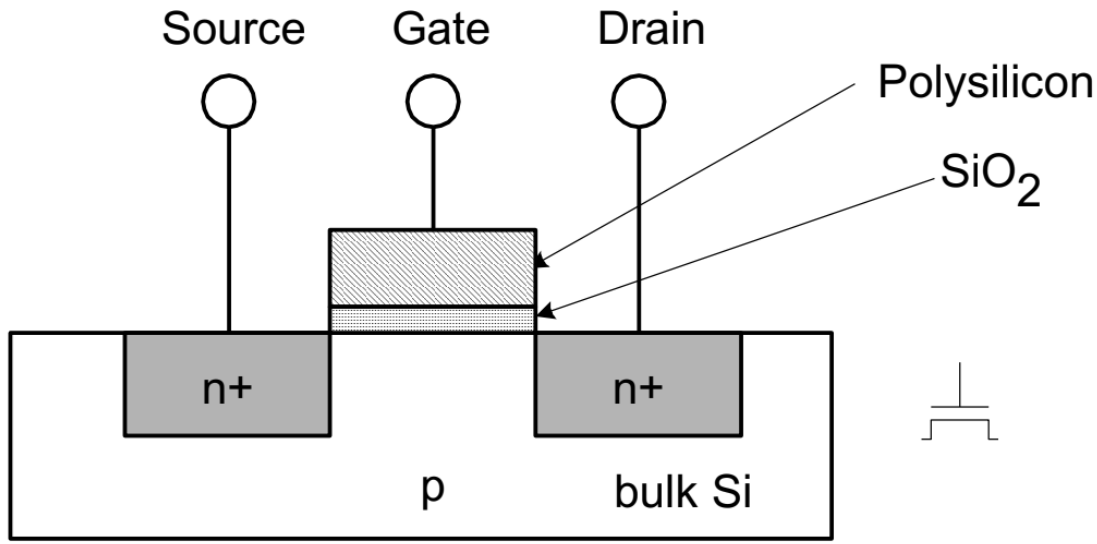
P-N Junctions

- **A junction between p-type and n-type semiconductor forms a diode.**
- **Current flows only in one direction**



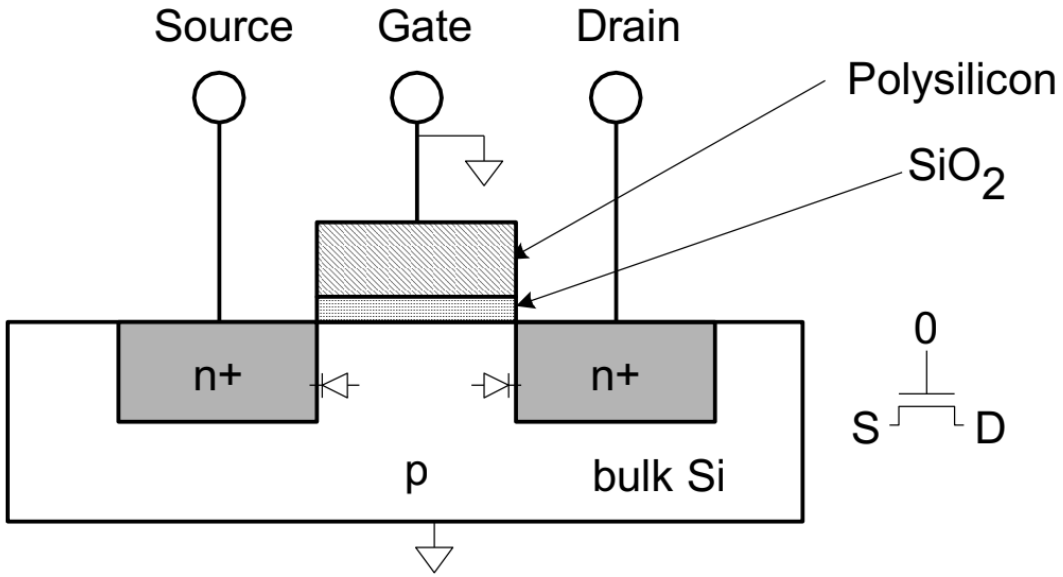
nMOS Transistor

- **Four terminals: gate, source, drain, body**
- **Gate – oxide – body stack looks like a capacitor**
  - **Gate and body are conductors**
  - **SiO_2 (oxide) is a very good insulator**
  - **Called metal – oxide – semiconductor (MOS) capacitor**
  - **Even though the gate is no longer made of metal**
    - **Not true for 45nm and beyond.**



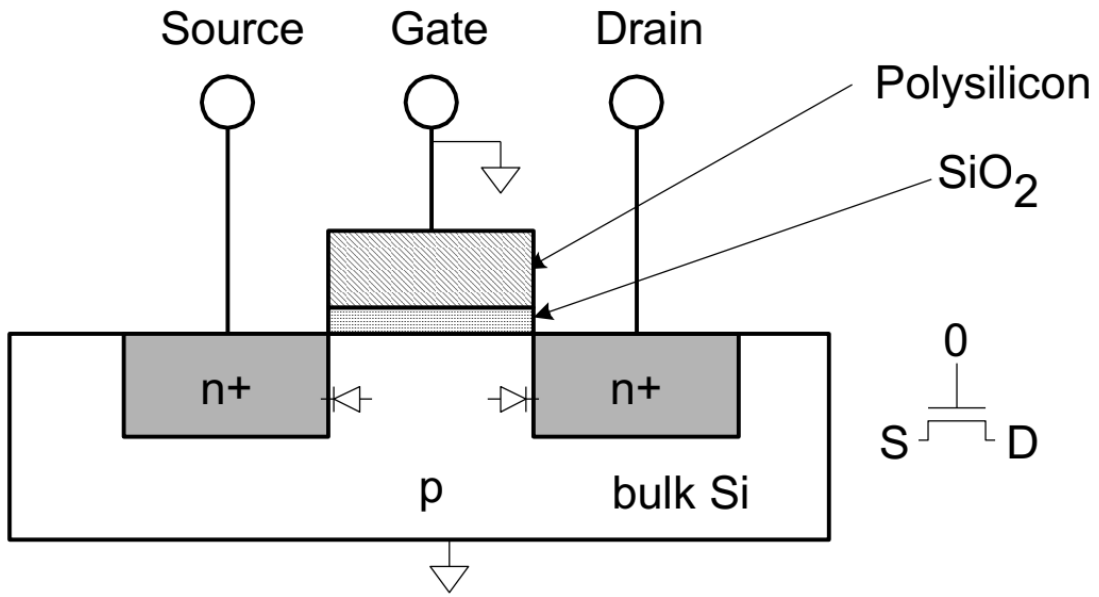
nMOS Operation

- **Body is commonly tied to ground (0 V)**
- **When the gate is at a low voltage:**
  - **P-type body is at low voltage**
  - **Source-body and drain-body diodes are OFF**
  - **No current flows, transistor is OFF**



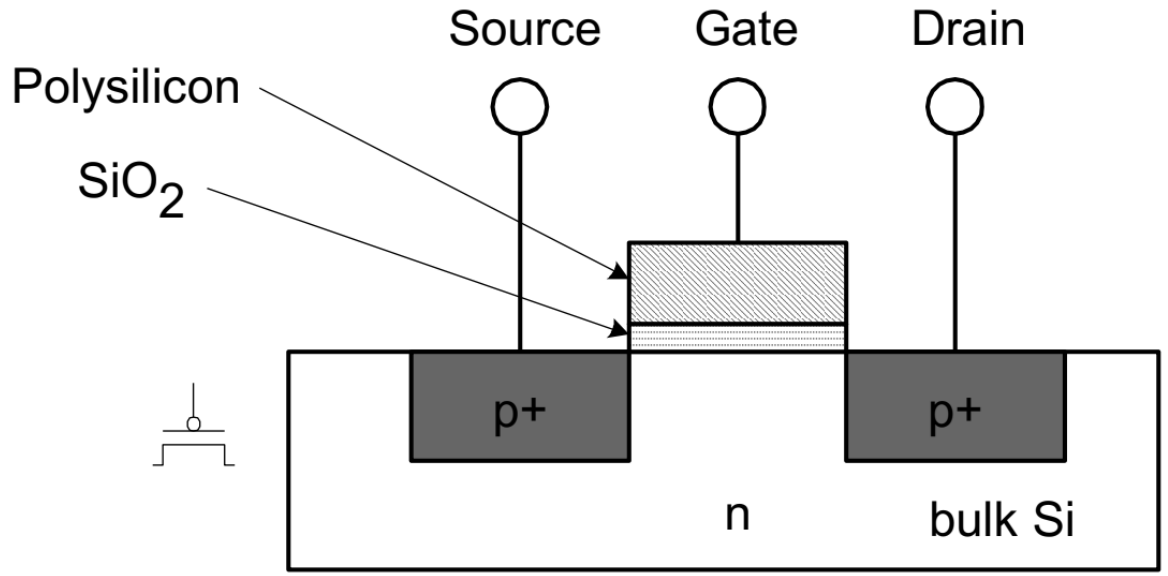
nMOS Operation

- **When the gate is at a high voltage:**
  - **Positive charge on gate of MOS capacitor**
  - **Negative charge attracted to body**
  - **Inverts a channel under gate to n-type**
  - **Now current can flow through n-type silicon from source through channel to drain, transistor is ON**



pMOS Transistor

- **Similar, but doping and voltages reversed**
  - **Body tied to high voltage (VDD)**
  - **Gate low: transistor ON**
  - **Gate high: transistor OFF**
  - **Bubble indicates inverted behavior**

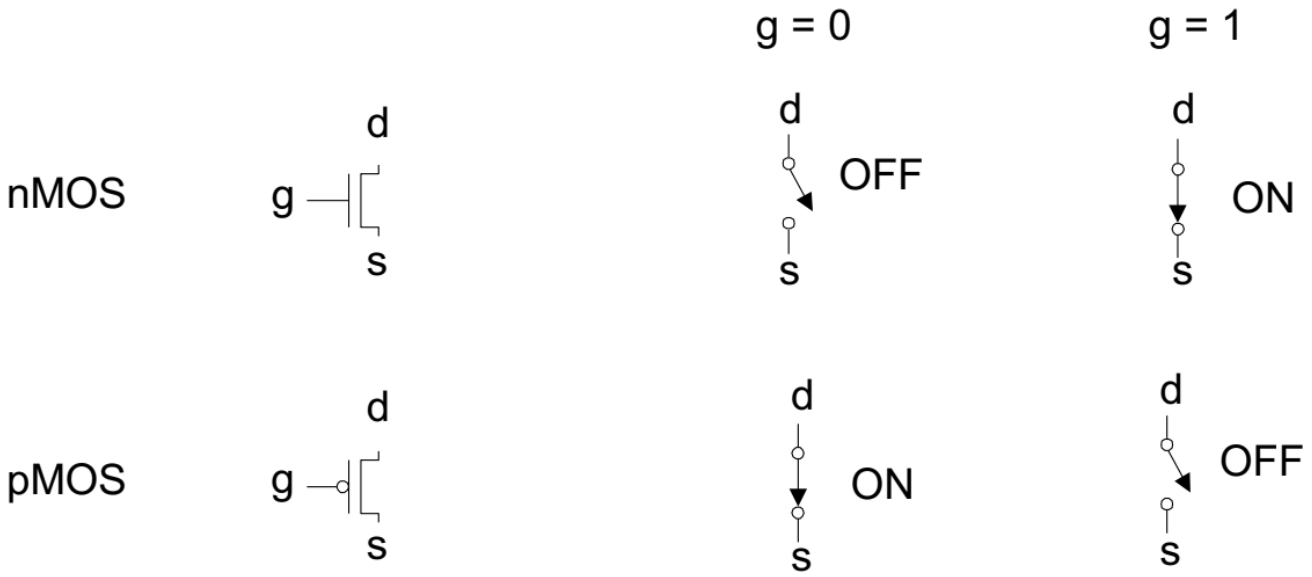


Power Supply Voltage

- In 1970's VDD = 12-18V for Metal Gate CMOS
- In 1980's, VDD = 5V
- VDD has decreased in modern processes
  - High VDD would damage modern tiny transistors
  - Lower VDD saves power
- VDD = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, 0.8, 0.7, 0.6
- GND = 0 V

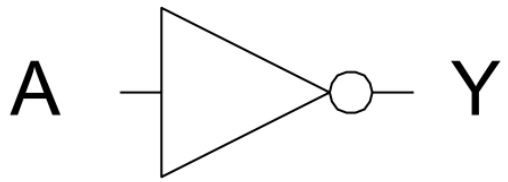
Transistors as Switches

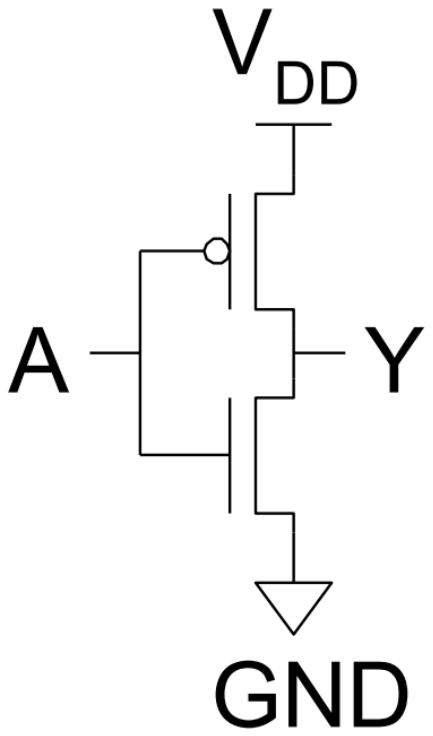
- **We can view MOS transistors as electrically controlled switches**
- **Voltage at gate controls path from source to drain**



CMOS Inverter

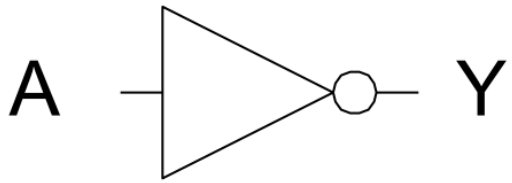
A	Y
0	
1	

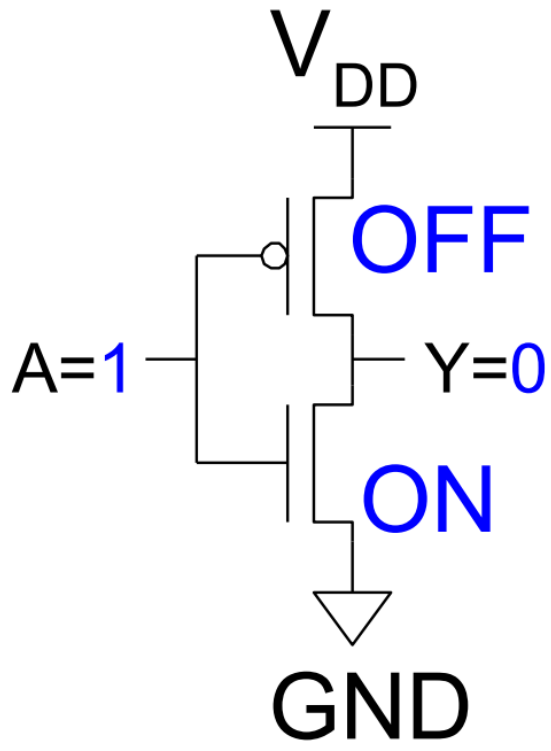




CMOS Inverter

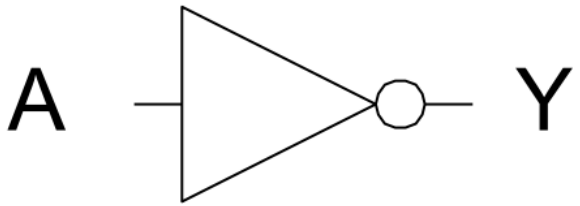
A	Y
0	
1	**0**

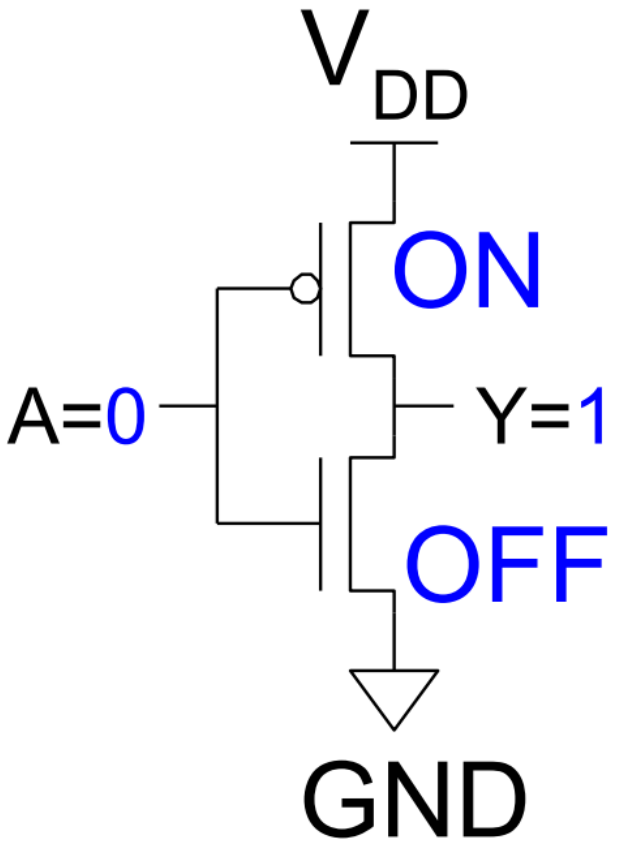




CMOS Inverter

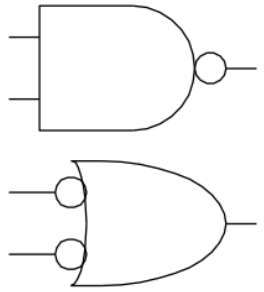
A	Y
0	**1**
1	0

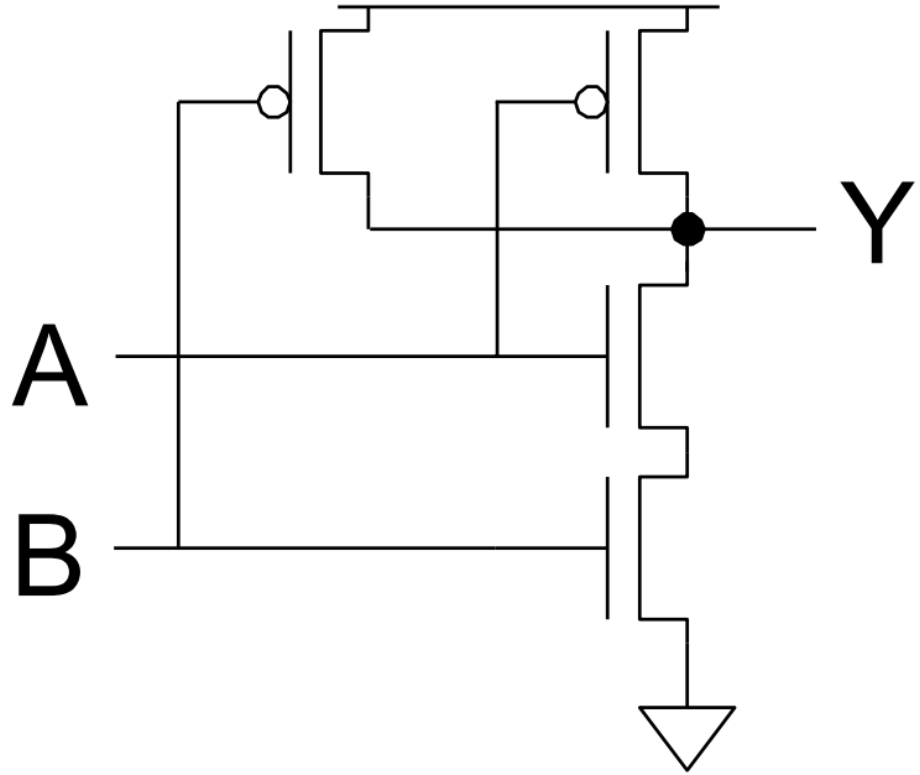




CMOS NAND Gate

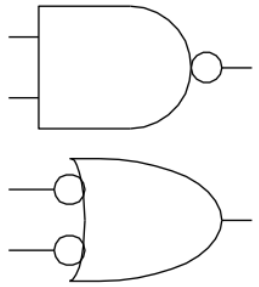
A	B	Y
0	0	
0	1	
1	0	
1	1	

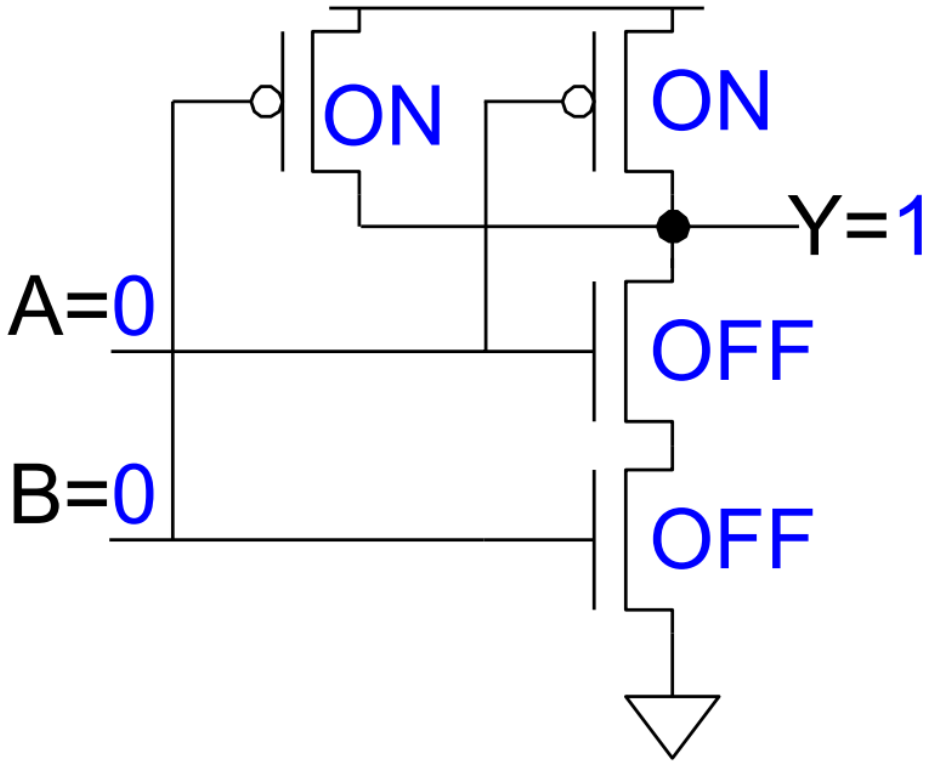




CMOS NAND Gate

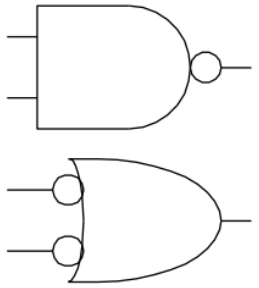
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

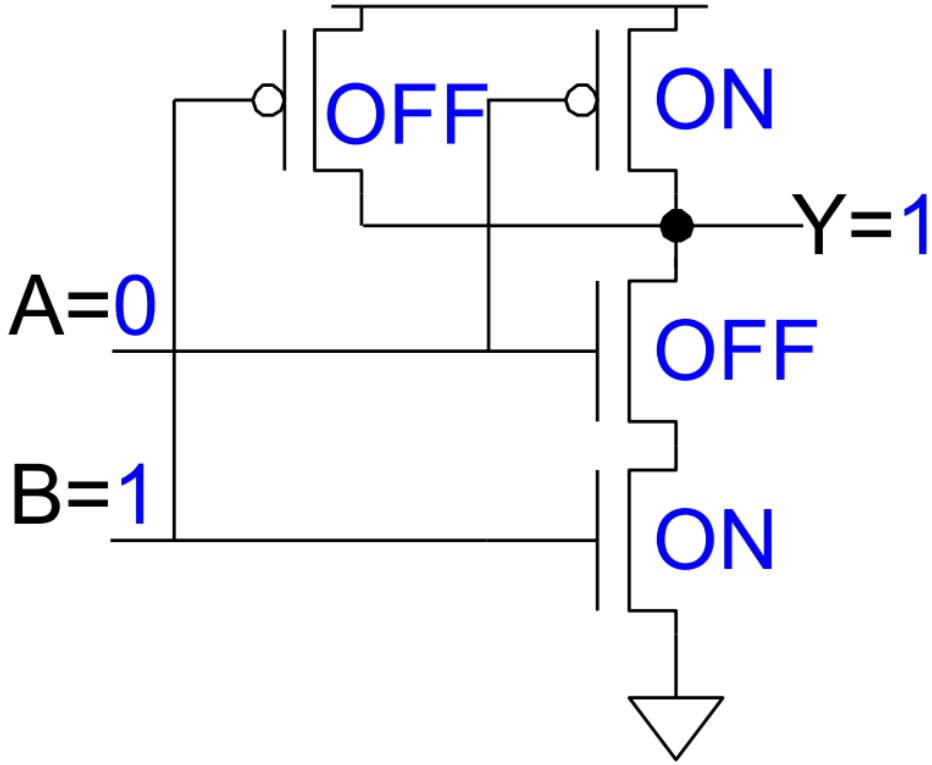




CMOS NAND Gate

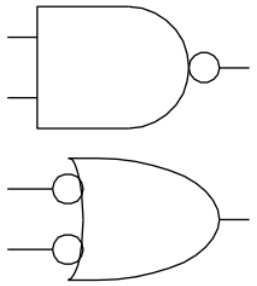
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

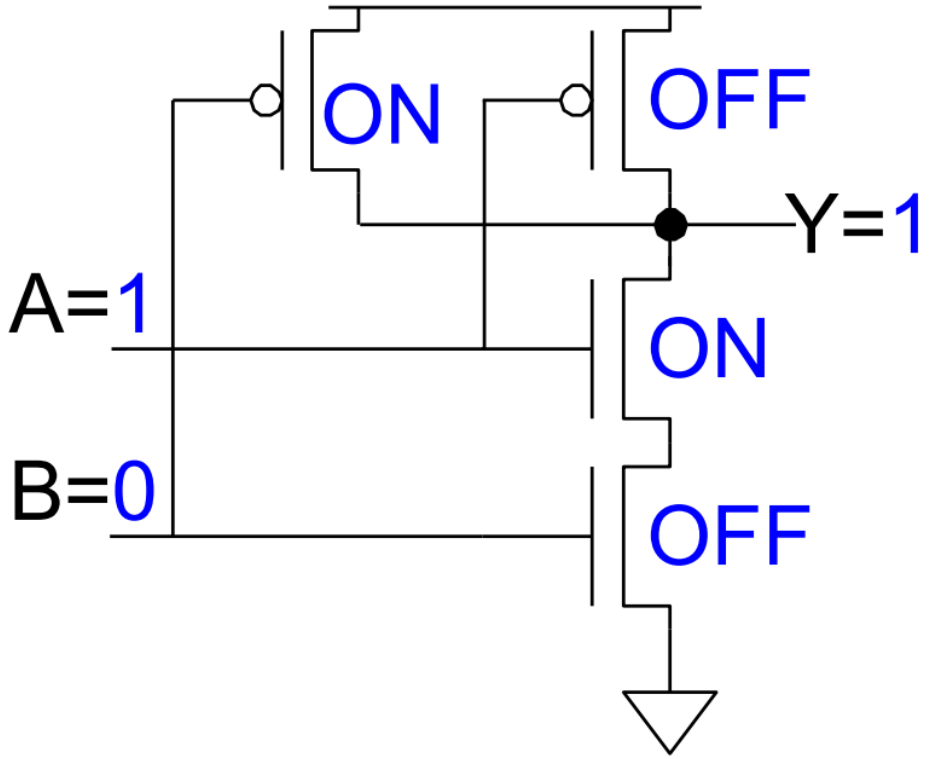




CMOS NAND Gate

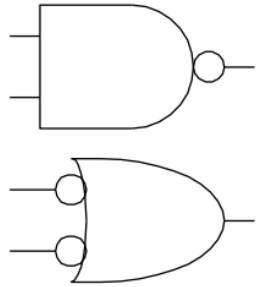
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

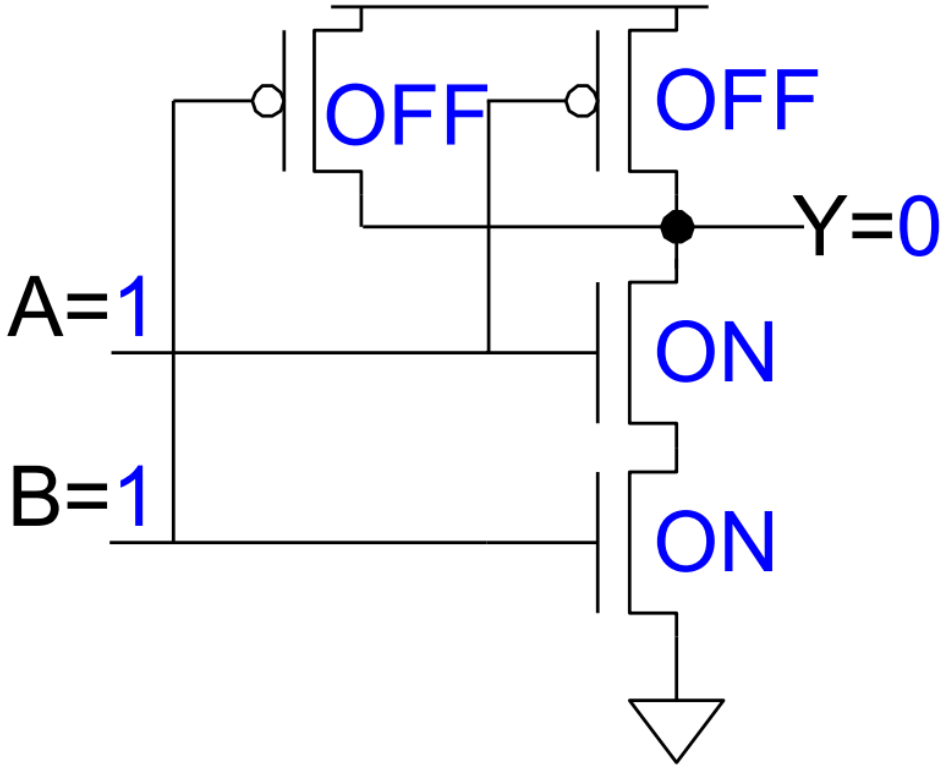




CMOS NAND Gate

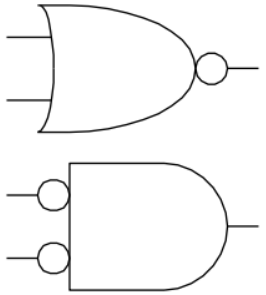
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

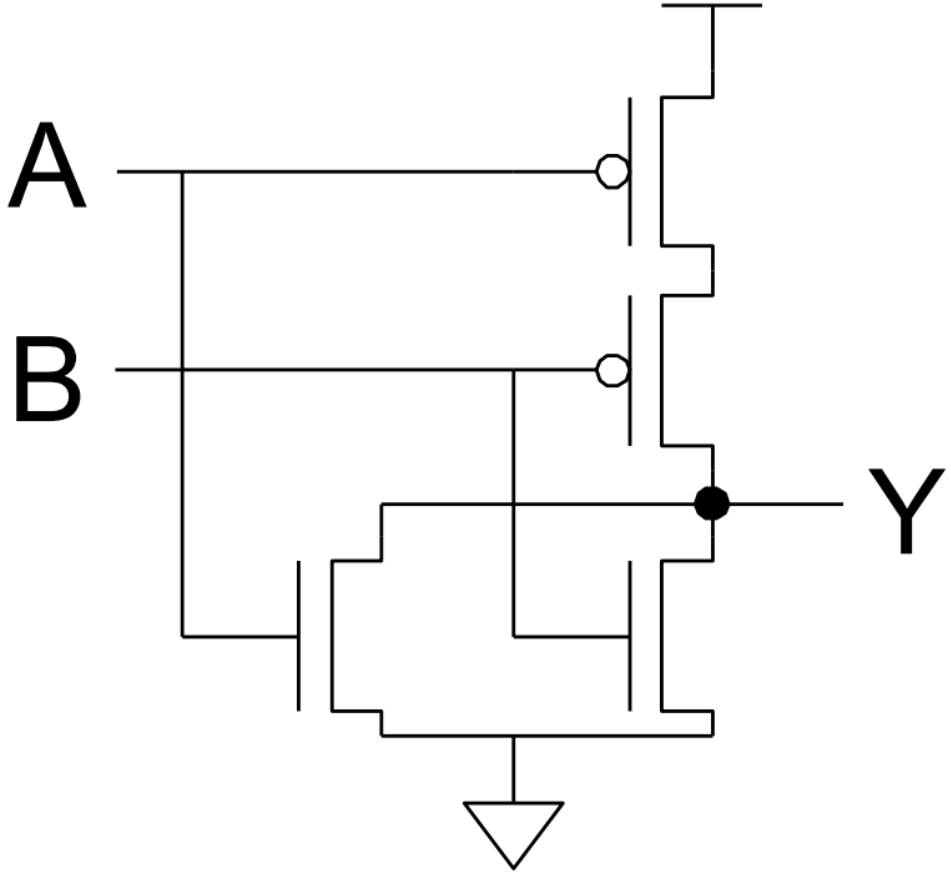




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



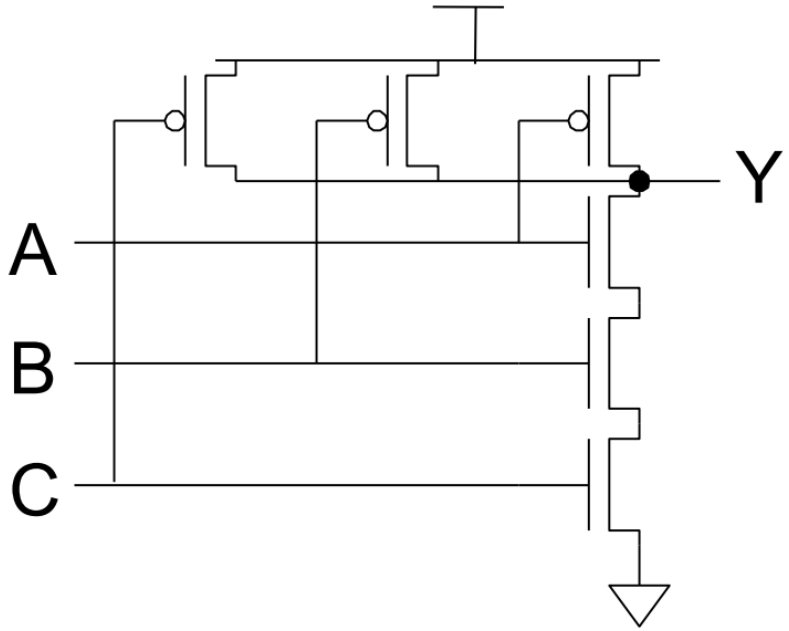


3-input NAND Gate

- **Y pulls low if ALL inputs are 1**
- **Y pulls high if ANY input is 0**

3-input NAND Gate

- **Y pulls low if ALL inputs are 1**
- **Y pulls high if ANY input is 0**



Characteristics of CMOS Gates

- **In general, when the circuit is stable**
  - **There is a path from one supply (VSS or VDD) to the output (low static power dissipation)**
  - **There is NEVER a path from one supply to another**
- **There is a momentary drain of current when a gate switches from one state to the other**
  - **Dynamic power dissipation**
- **If a node has no path to power or ground, the previous value retained due to the capacitance of the node.**
  - **Don't count on it though. Leakage is so bad in DSM that the charge will be lost.**