

# Embedded System Design

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## Lab 1 Report

## Modeling in MATLAB and Simulink

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# 1 BPCU Design and Implementation

## 1.1 Introduction

Lab 1 requires us to design and implement the Bus Power Control Unit (BPCU) of an aircraft Electrical Power System (EPS).

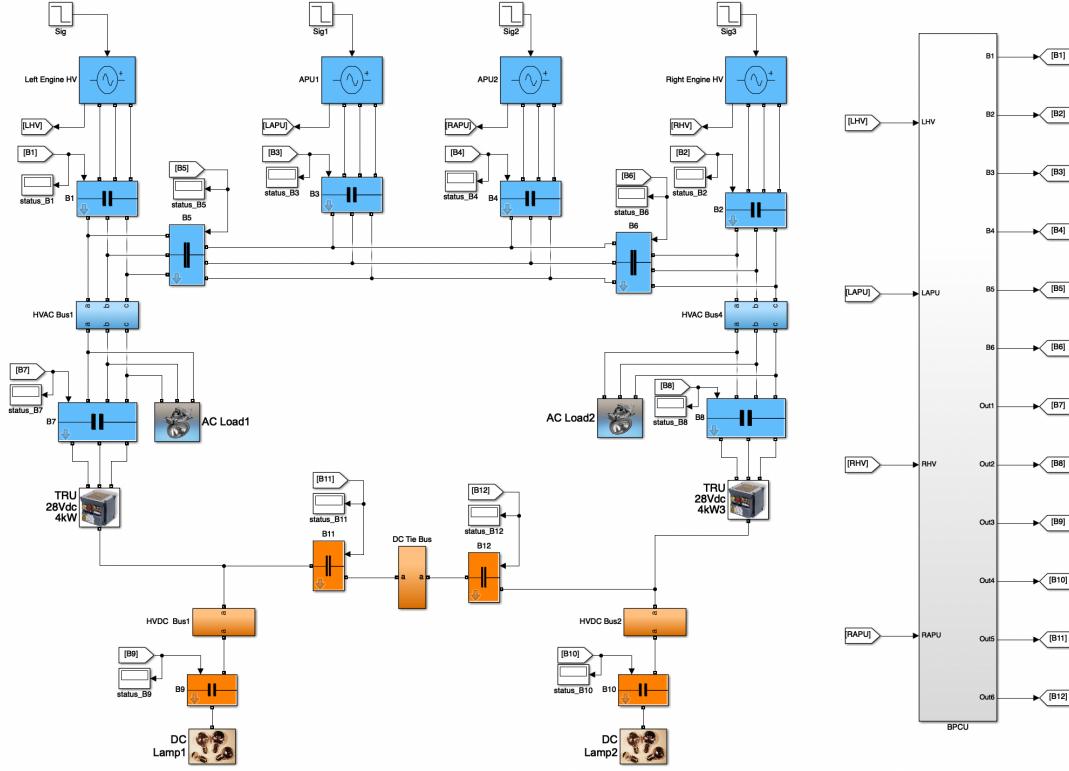


Figure 1. An Aircraft Electrical Power System (EPS)

As Fig. 1 shows, the aircraft EPS is consisted of a set of generators (GL and GR), auxiliary power units (AL and AR), power switches (B1 to B12), rectifier units (HVAC and HVDC), and loads (AC and DC loads). Under some situations (these are specified as environment assumptions), the power generators might malfunction, and auxiliary power units should be connected with loads to ensure that they are always powered and the aircraft stays safe.

BPCU is used to control the buses between power supply and loads when such crisis happens. When the system detects some unexpected power generator malfunction, BPCU controls the power switches to be on or off to connect the healthy power supply with loads. The objective of BPCU is specified by 8 guarantees and our design is based on these 8 guarantees.

## 1.2 BPCU Guarantees Interpretation

Our BPCU control logic is based on 8 guarantees, here is the interpretation of them.

- **G1:** This means B1 to B12 are on during the start-up phase.
- **G2:** This means B1 and B2 are on but B5 and B6 are off when GL, GR are working.
- **G3:** We must control B1 to B6 to prevent paralleled AC power sources connection.
- **G4:** This means AL and AR can not be used in parallel, so when B3 is open, B4 is off; when B4 is open, B3 is off.
- **G5:** We must control B1 to B6 to ensure AC buses are empowered.
- **G6:** We must control B1 to B6 to ensure DC buses are empowered.
- **G7:** This means the leftmost healthy power supply empowers the left AC bus. For example, if GL and AL are healthy, GL empowers the left AC bus; if AL and AR are healthy, AL empowers the left AC bus.
- **G8:** This means the rightmost healthy power supply empowers the right AC bus. For example, if GL and AL are healthy, AL empowers the right AC bus; if AL and AR are healthy, AR empowers the right AC bus.

## 1.3 BPCU Control Logic and Implementation

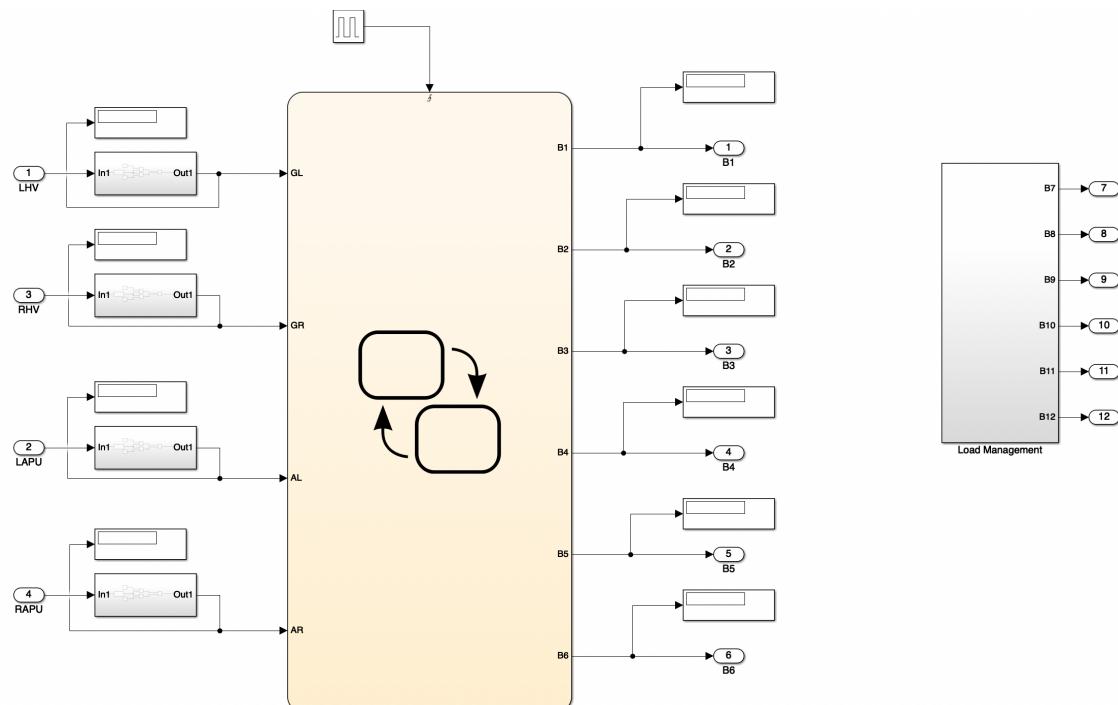


Figure 2. BPCU Overview

Our BPCU is implemented by Stateflow, a graphical and programmable state machine toolbox in Simulink. Before we introduce its control logic, we first give an overview of our BPCU.

Fig.2 shows the layout of our BPCU. On the left side there are LHV, RHV, LAPU, RAPU signals that represent power supply. Since there is an environment assumption which states that "an AC bus is correctly powered if the root-mean-square (RMS) voltage at its loads is between 110 V and 120 V and the frequency is 400 Hz", so the controller switches at a rate of 2.5 ms and a voltage monitor is used to ensure that the RMS voltage is within the desired range (see Fig.3 below).

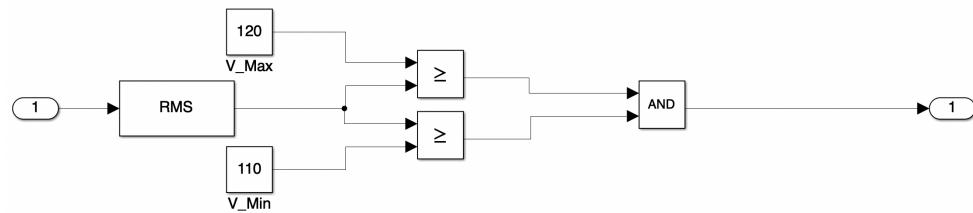


Figure 3. The Voltage Monitor Module

On the right side of Fig.2 are the output signals generated by the controller. The controller is visualized in Fig. 4.

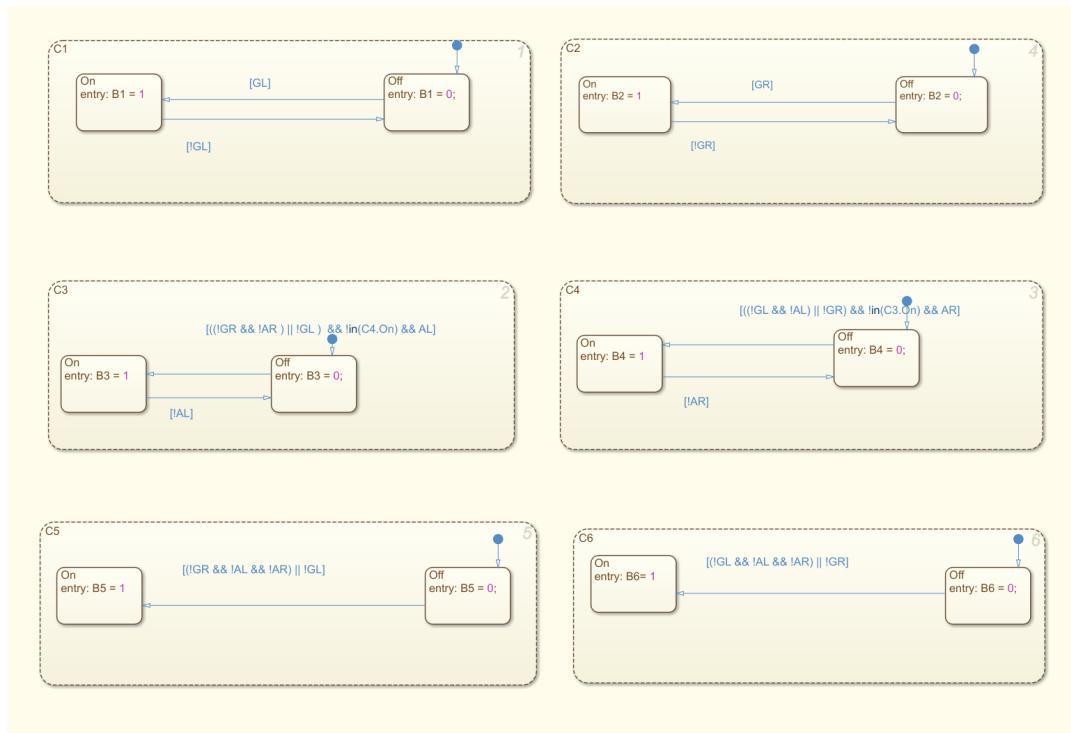


Figure 4. The Controller

There are 6 modules that control B1 to B6.

- **C1:** B1 changes from 0 to 1 when  $GL$ , B1 changes from 1 to 0 when  $\neg GL$ , because if GL functions well B1 is open to power the left AC bus.
- **C2:** B2 changes from 0 to 1 when  $GR$ , B2 changes from 1 to 0 when  $\neg GR$ , because if GR functions well B2 is open to power the right AC bus.
- **C3:** B3 changes from 0 to 1 when  $\neg AL$ , B3 changes from 1 to 0 when  $((\neg GR \& \& \neg AR) \mid\mid \neg GL) \&\& \neg C4 \&\& AL$ , because B3 is open when (1) AL functions well; (2) B4 is off since B3 and B4 cannot be open at the same time because of G4; (3) GL is not working so AL empowers the left AC bus, or GR and AR are both not working so AL empowers the right AC bus.
- **C4:** B4 changes from 0 to 1 when  $\neg AR$ , B4 changes from 1 to 0 when  $((\neg GL \& \& \neg AL) \mid\mid \neg GR) \&\& \neg C3 \&\& AR$ , because B4 is open when (1) AR functions well; (2) B3 is off since B3 and B4 cannot be open at the same time because of G4; (3) GR is not working so AR empowers the right AC bus, or GL and AL are both not working so AR empowers the left AC bus.
- **C5:** B5 changes from 0 to 1 when  $((\neg GR \& \& \neg AL \& \& \neg AR) \mid\mid \neg GL)$ , because B5 is open when GL is not working so some power supply on the right of GL empowers the left AC bus or GR, AL, and AR are all not working so GL empowers the right AC bus.
- **C6:** B6 changes from 0 to 1 when  $((\neg GL \& \& \neg AL \& \& \neg AR) \mid\mid \neg GR)$ , because B6 is open when GR is not working so some power supply on the left of GR empowers the right AC bus or GL, AL, and AR are all not working so GR empowers the left AC bus.

## 2 Simulation Results and Design Verification

### 2.1 General Idea

In this section, we introduce how to use simulation to verify that our design meets all system guarantees. We have totally 10 cases to consider:

- **Case 1:** GR, GL are working
- **Case 2:** GR is not working
- **Case 3:** GL is not working
- **Case 4:** GR, AR are not working
- **Case 5:** GL, AL are not working
- **Case 6:** GR, GL are not working
- **Case 7:** GR, GL, AR are not working
- **Case 8:** GR, GL, AL are not working
- **Case 9:** GR, AR, AL are not working
- **Case 10:** GL, AR, AL are not working

The basic case is that the system works well, which means GR and GL are working (regardless of the status of AR and AL). If the basic case gives a desired result, it proves that G2 is satisfied.

The second and third cases handle the situation when one of GR and GL fails and others are not. Because of G4, G7, G8, only one APU is inserted into the network and the leftmost available APU empowers the left AC bus and the rightmost available APU empowers the right AC bus, the results are definite. For the second case, AR empowers the right AC bus; for the third case, AL empowers the left AC bus.

Based on the second and third cases, the fourth and fifth cases verify if AL empowers the right AC bus if both GR and AR fail, AR empowers the left AC bus if both GL and AL fail.

The rest four cases verify if the system can use only one generator to empower both AC buses. Since there is an environment assumption that states "at least one power source is always healthy", BPCU does not need to handle the case that all generators fail. Finally, G1, G3, G5, and G6 are proved if all the above cases are satisfied.

## 2.2 Case 1: GR, GL Are Working

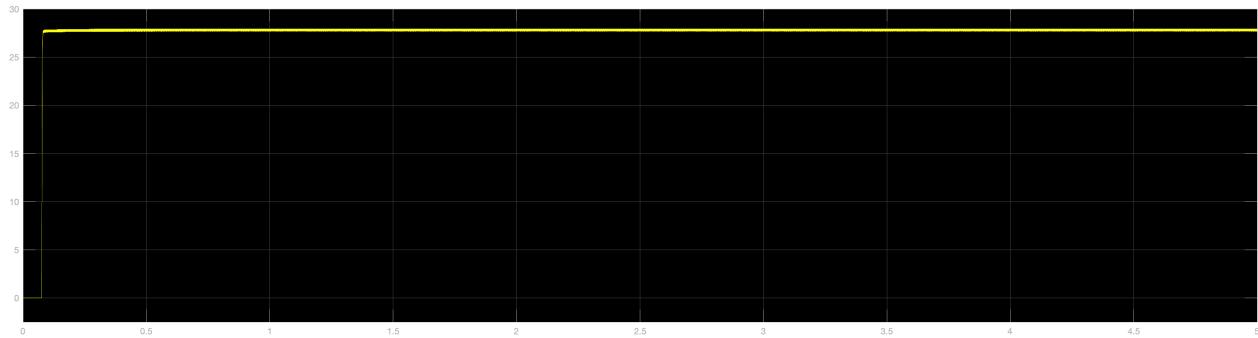


Figure 2.2.1 Left DC Load Waveform

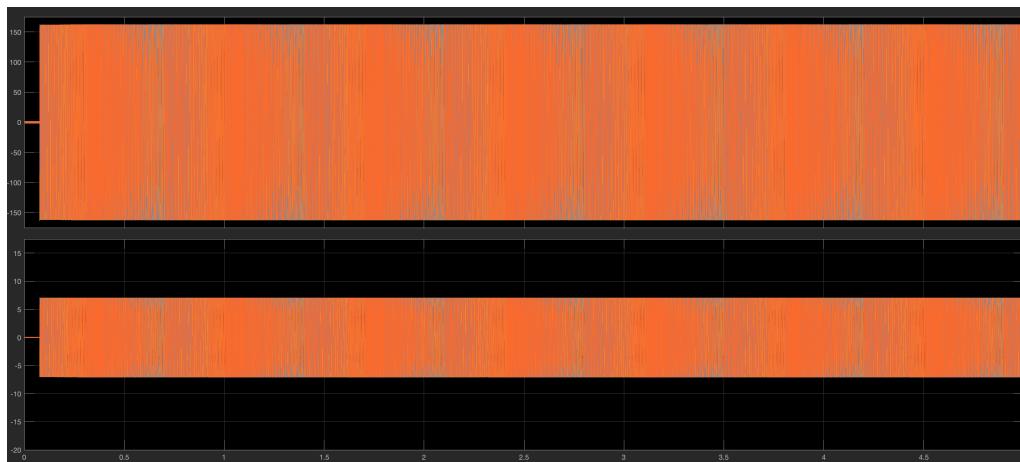


Figure 2.2.2 Left AC Load Waveform

We include an AC load waveform in this case to show that DC waveform is corresponding to AC waveform, so we just include DC waveforms in the following cases.

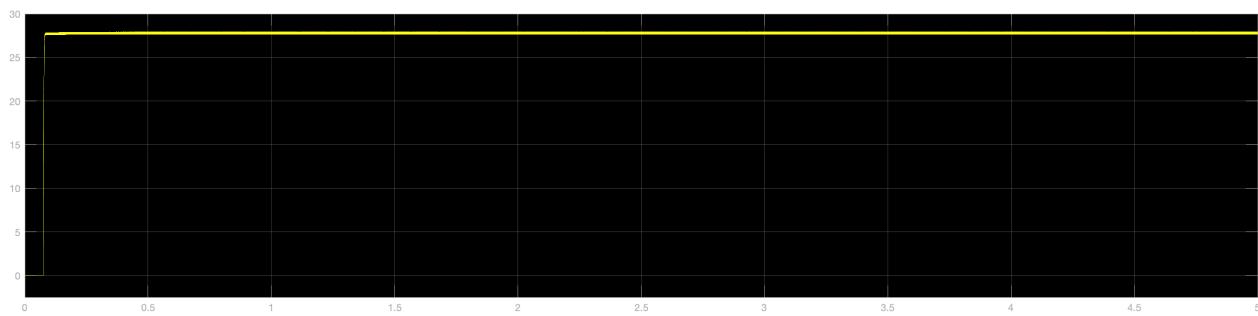


Figure 2.2.3 Right DC Load Waveform

Symbols

TYPE	NAME	VALUE	PORT
BL	B1	1	1
BL	GL	1	1
BL	B2	1	2
BL	B3	0	3
BL	B4	0	4
BL	B5	0	5
BL	B6	0	6
BL	GR	1	2
BL	AL	1	3
BL	AR	1	4

Figure 2.2.4 BPCU Output Control Signals

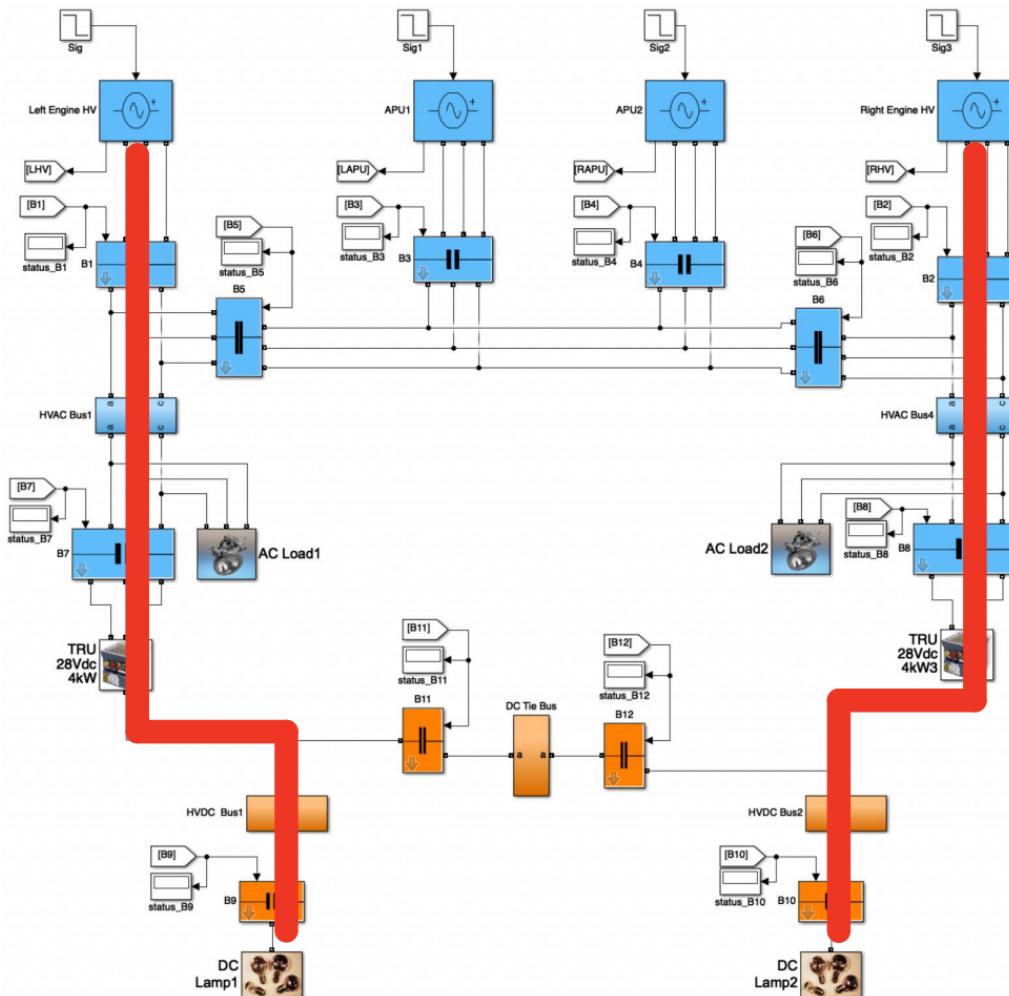


Figure 2.2.5 EPS Connection

Under normal conditions, GL empowers the left AC bus, GR empowers the right AC bus.

## 2.3 Case 2: GR Not Working

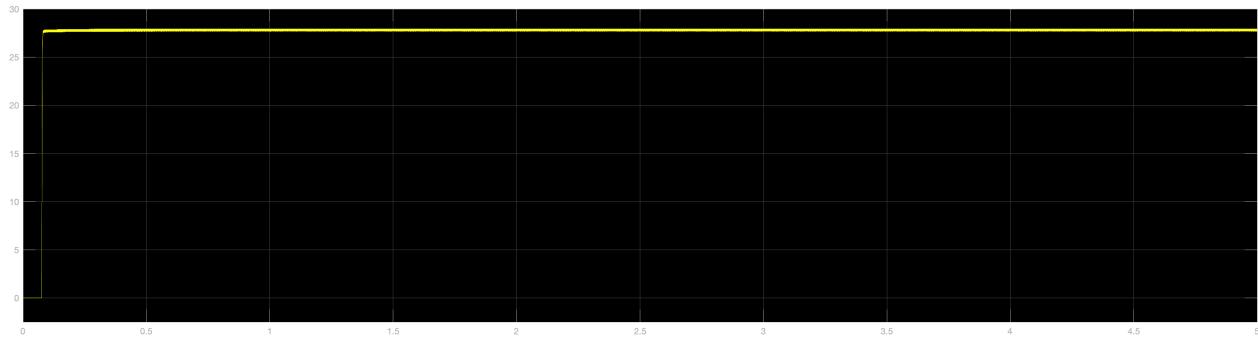


Figure 2.3.1 Left DC Load Waveform

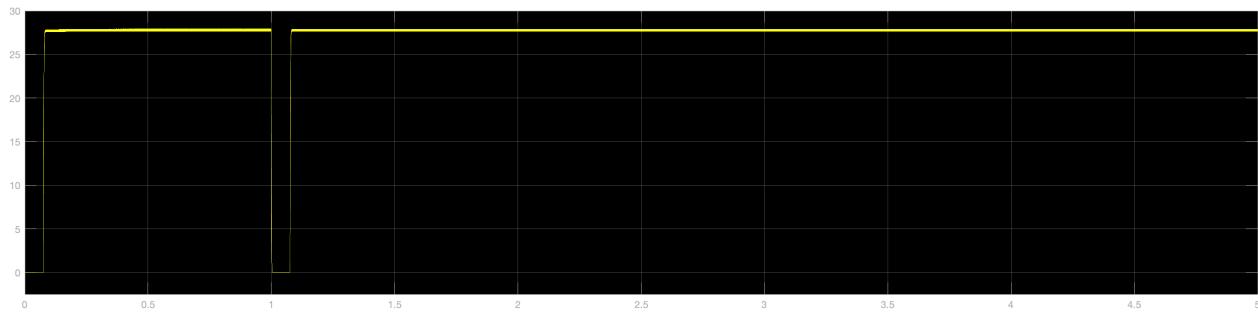


Figure 2.3.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	1	1
	GL	1	1
	B2	0	2
	B3	0	3
	B4	1	4
	B5	0	5
	B6	1	6
	GR	0	2
	AL	1	3
	AR	1	4

Figure 2.3.3 BPCU Output Control Signals

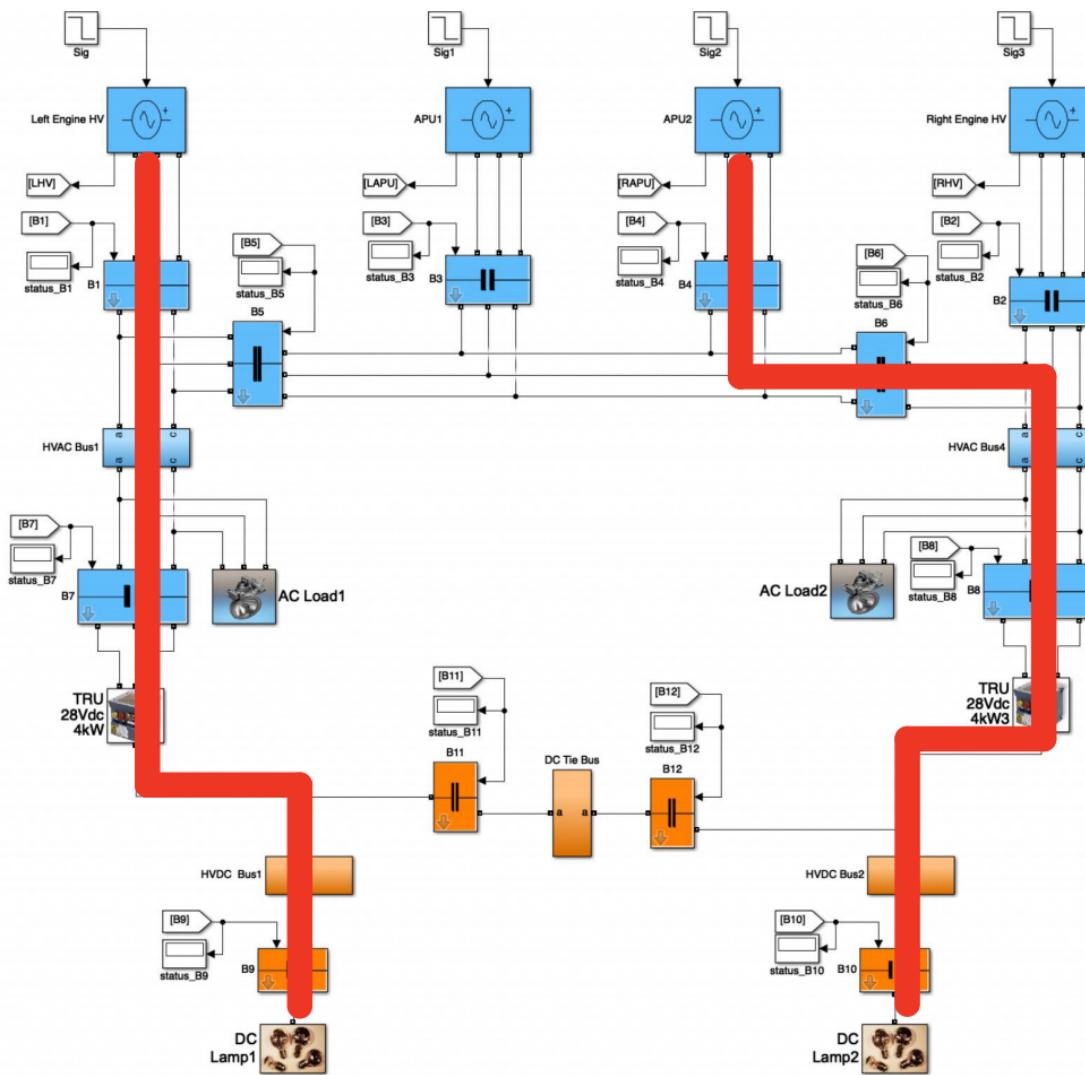


Figure 2.3.4 EPS Connection

When only GR fails, the rightmost available power supply AR empowers the right AC bus based on system guarantee G8. Only one APU, AR, is used based on system guarantee G4.

## 2.4 Case 3: GL Not Working

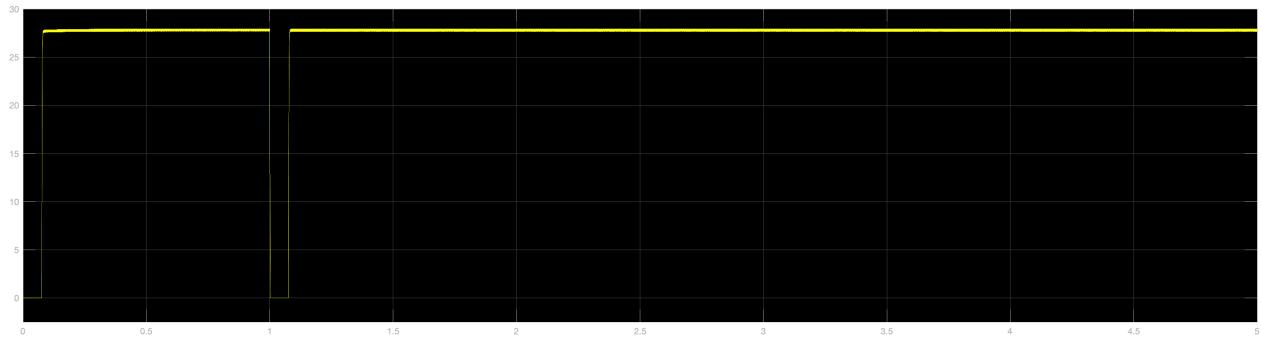


Figure 2.4.1 Left DC Load Waveform

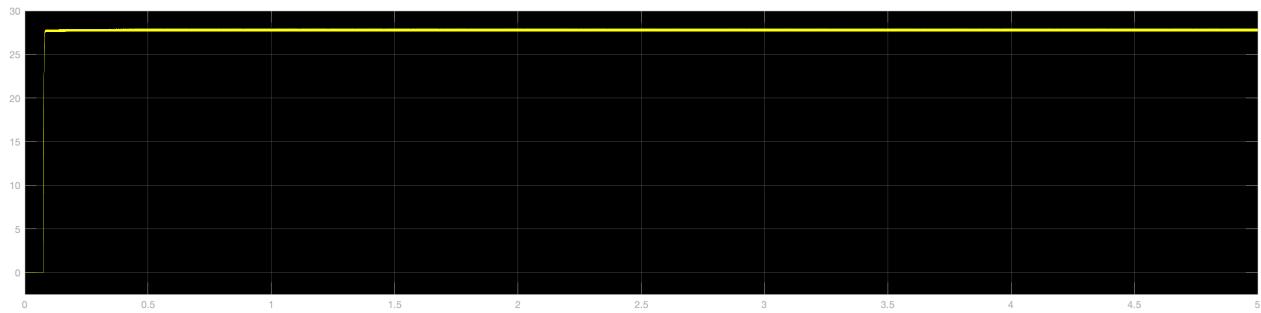


Figure 2.4.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	1	2
	B3	1	3
	B4	0	4
	B5	1	5
	B6	0	6
	GR	1	2
	AL	1	3
	AR	1	4

Figure 2.4.3 BPCU Output Control Signals

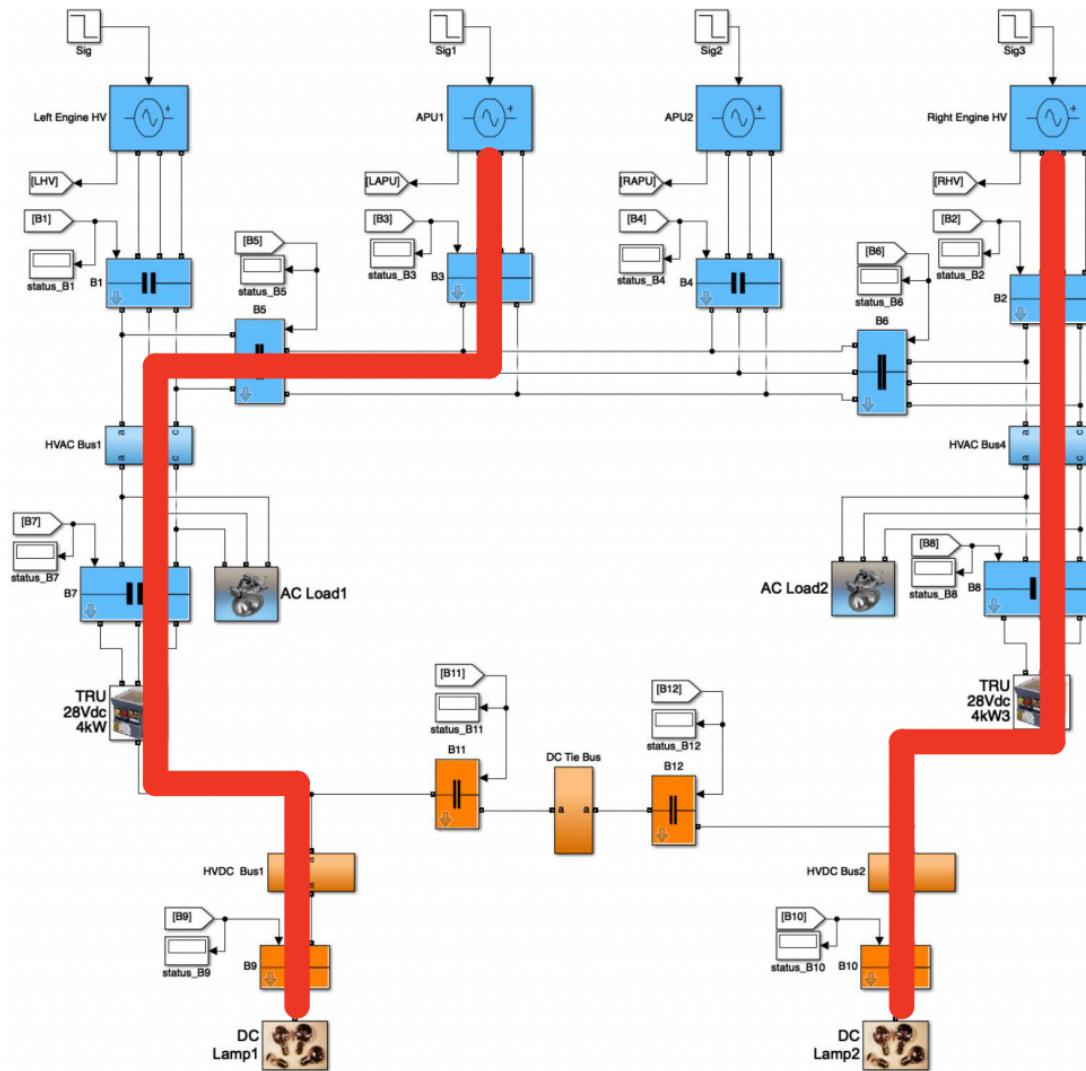


Figure 2.4.4 EPS Connection

When only GL fails, the leftmost available power supply AL empowers the left AC bus based on system guarantee G7. Only one APU, AL, is used based on system guarantee G4.

## 2.5 Case 4: GR, AR Not Working

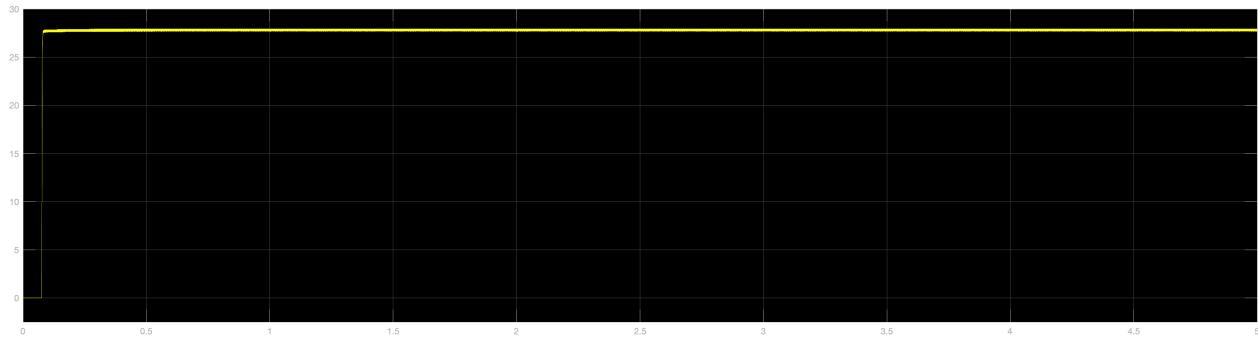


Figure 2.5.1 Left DC Load Waveform

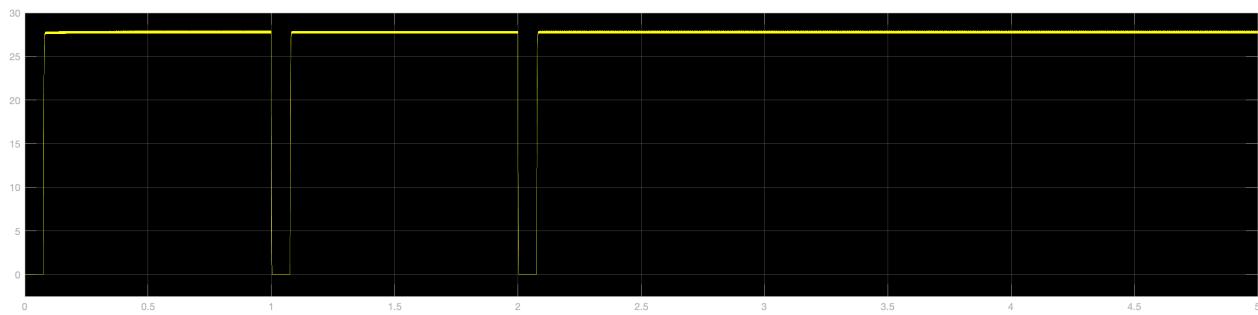


Figure 2.5.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	1	1
	GL	1	1
	B2	0	2
	B3	1	3
	B4	0	4
	B5	0	5
	B6	1	6
	GR	0	2
	AL	1	3
	AR	0	4

Figure 2.5.3 BPCU Output Control Signals

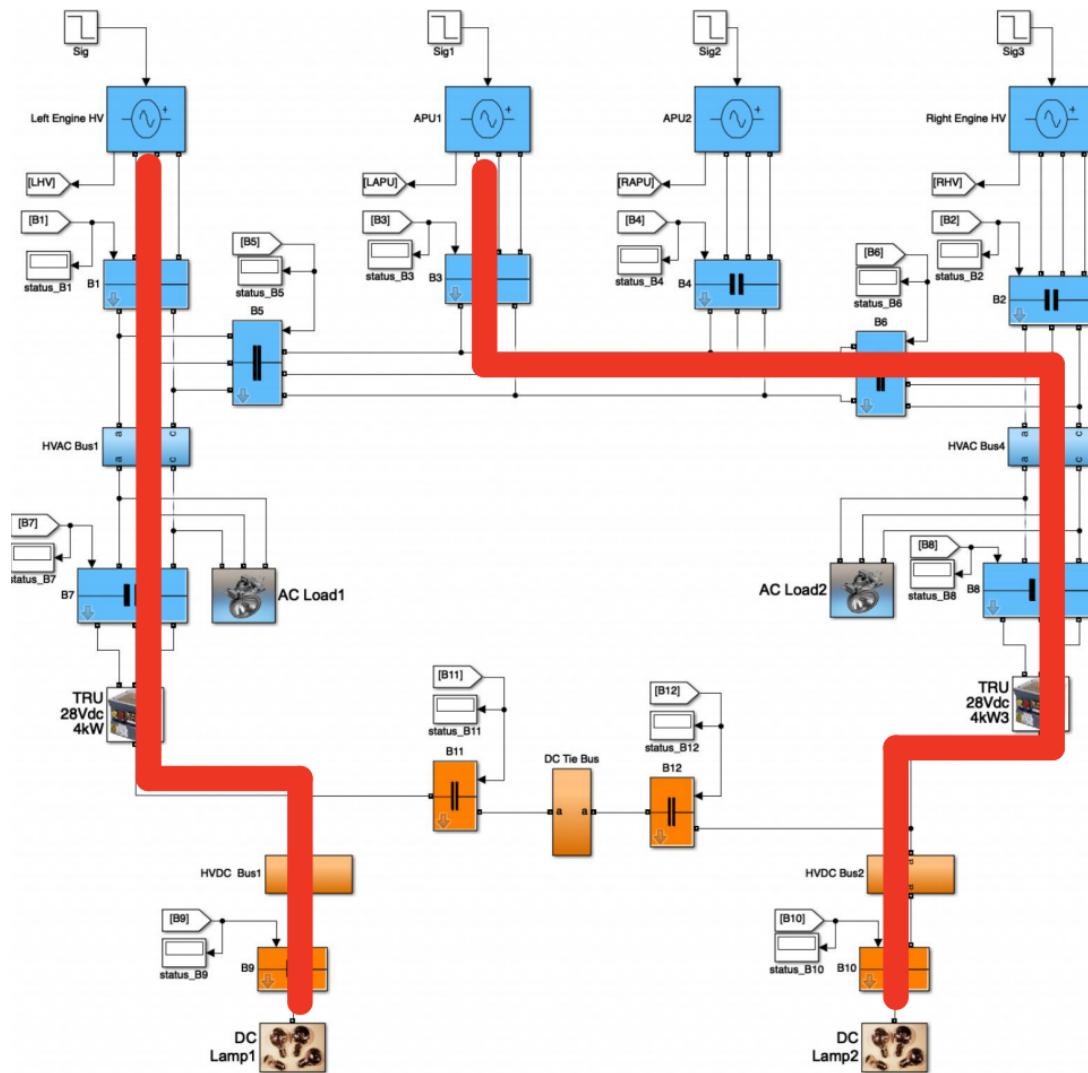


Figure 2.5.4 EPS Connection

When GR and AR fail, the rightmost available power supply AL empowers the right AC bus based on system guarantee G8. Only one APU, AL, is used based on system guarantee G4.

## 2.6 Case 5: GL, AL Not Working

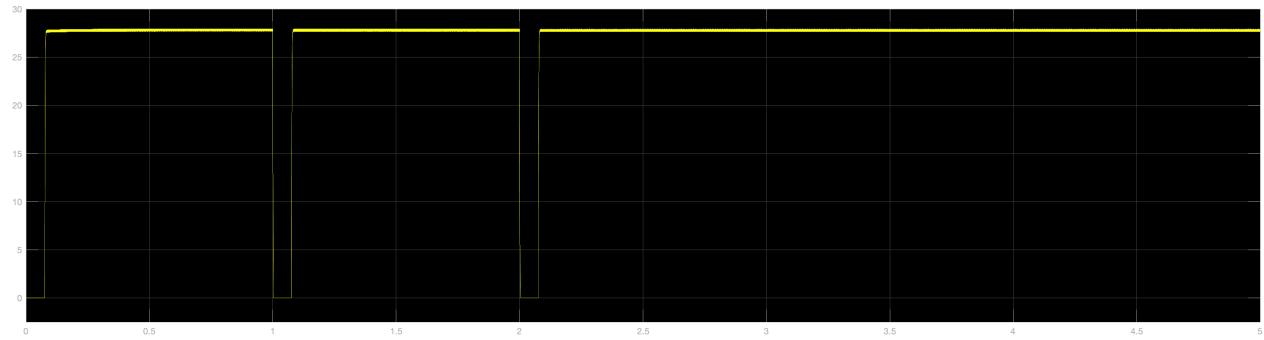


Figure 2.6.1 Left DC Load Waveform

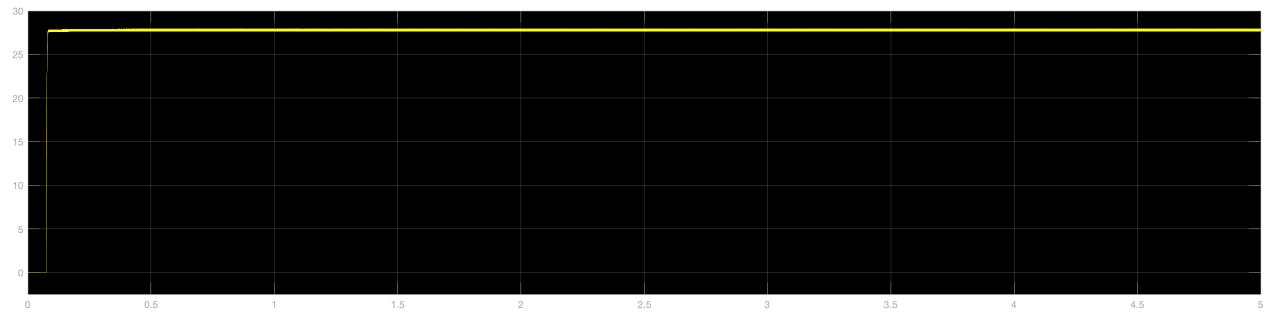


Figure 2.6.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	1	2
	B3	0	3
	B4	1	4
	B5	1	5
	B6	0	6
	GR	1	2
	AL	0	3
	AR	1	4

Figure 2.6.3 BPCU Output Control Signals

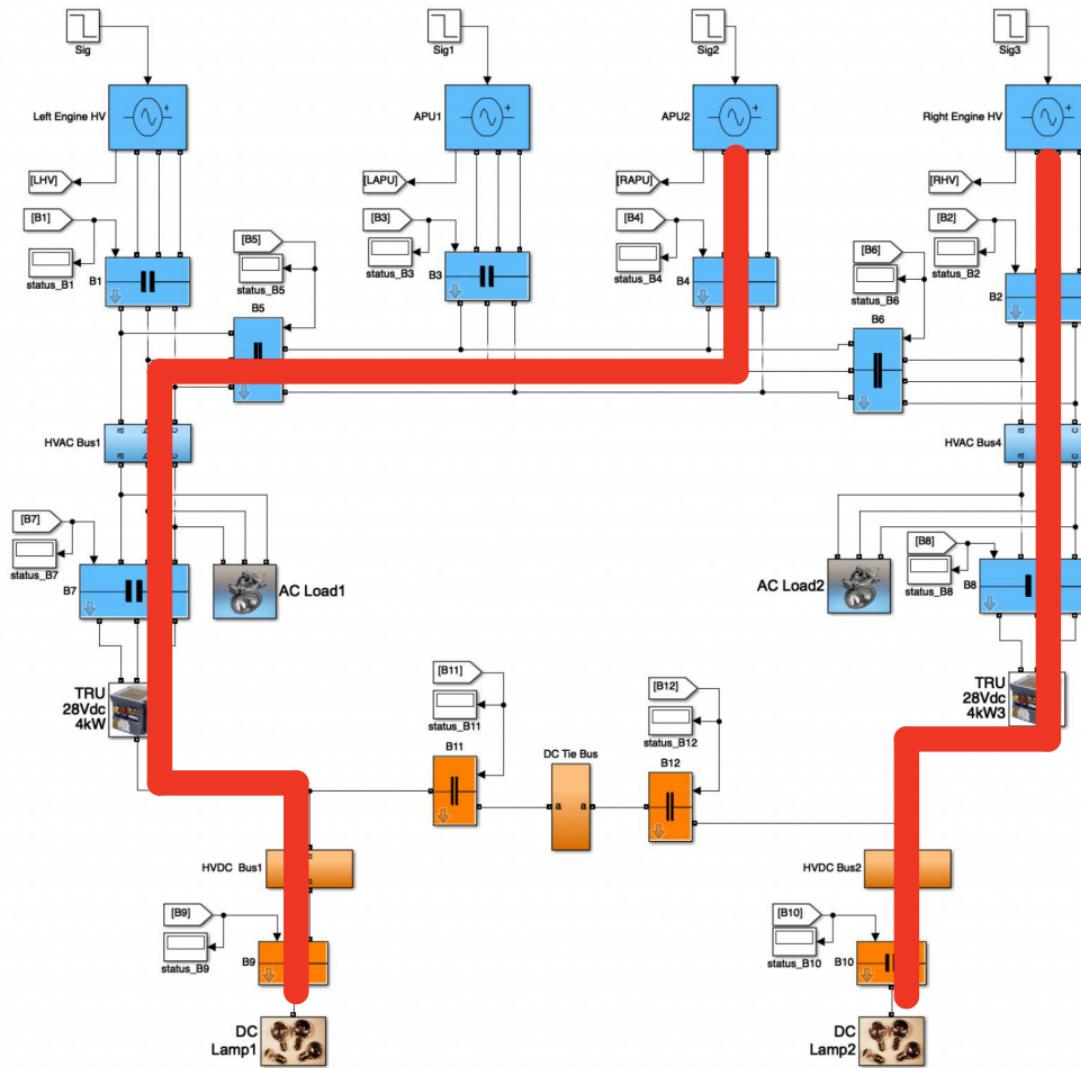


Figure 2.6.4 EPS Connection

When GL and AL fail, the leftmost available power supply AR empowers the left AC bus based on system guarantee G7. Only one APU, AR, is used based on system guarantee G4.

## 2.7 Case 6: GR, GL Not Working

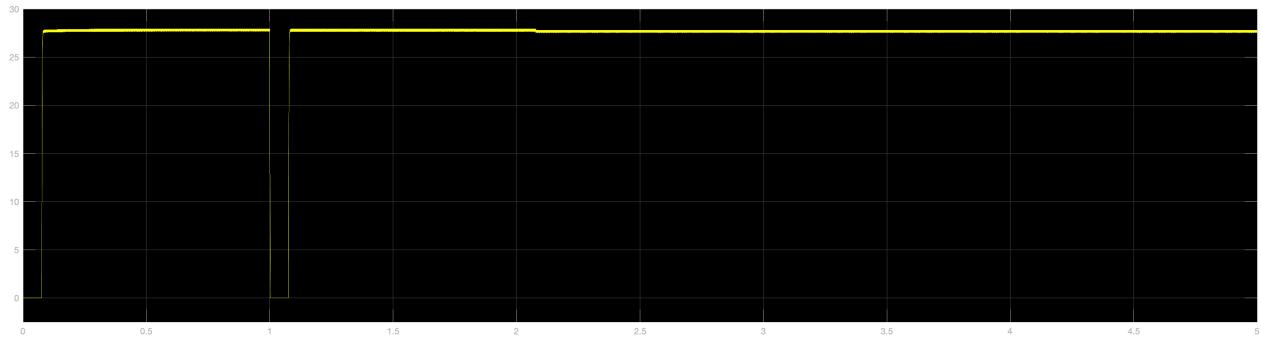


Figure 2.7.1 Left DC Load Waveform

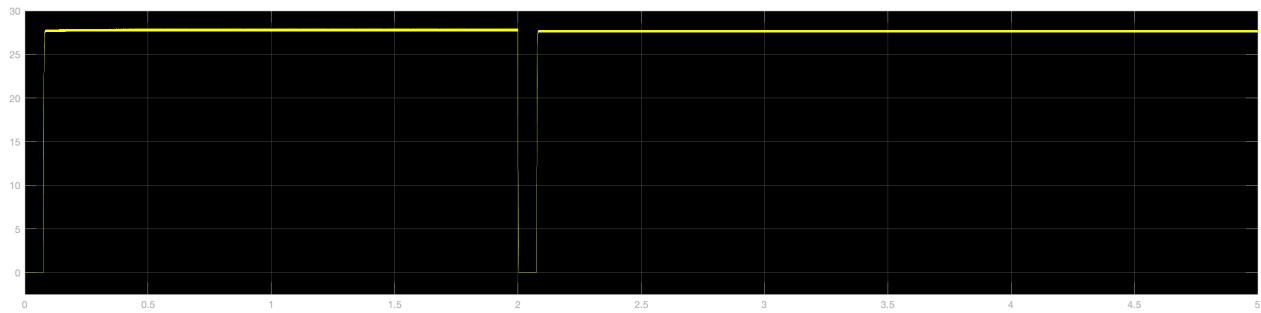


Figure 2.7.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	0	2
	B3	1	3
	B4	0	4
	B5	1	5
	B6	1	6
	GR	0	2
	AL	1	3
	AR	1	4

Figure 2.7.3 BPCU Output Control Signals

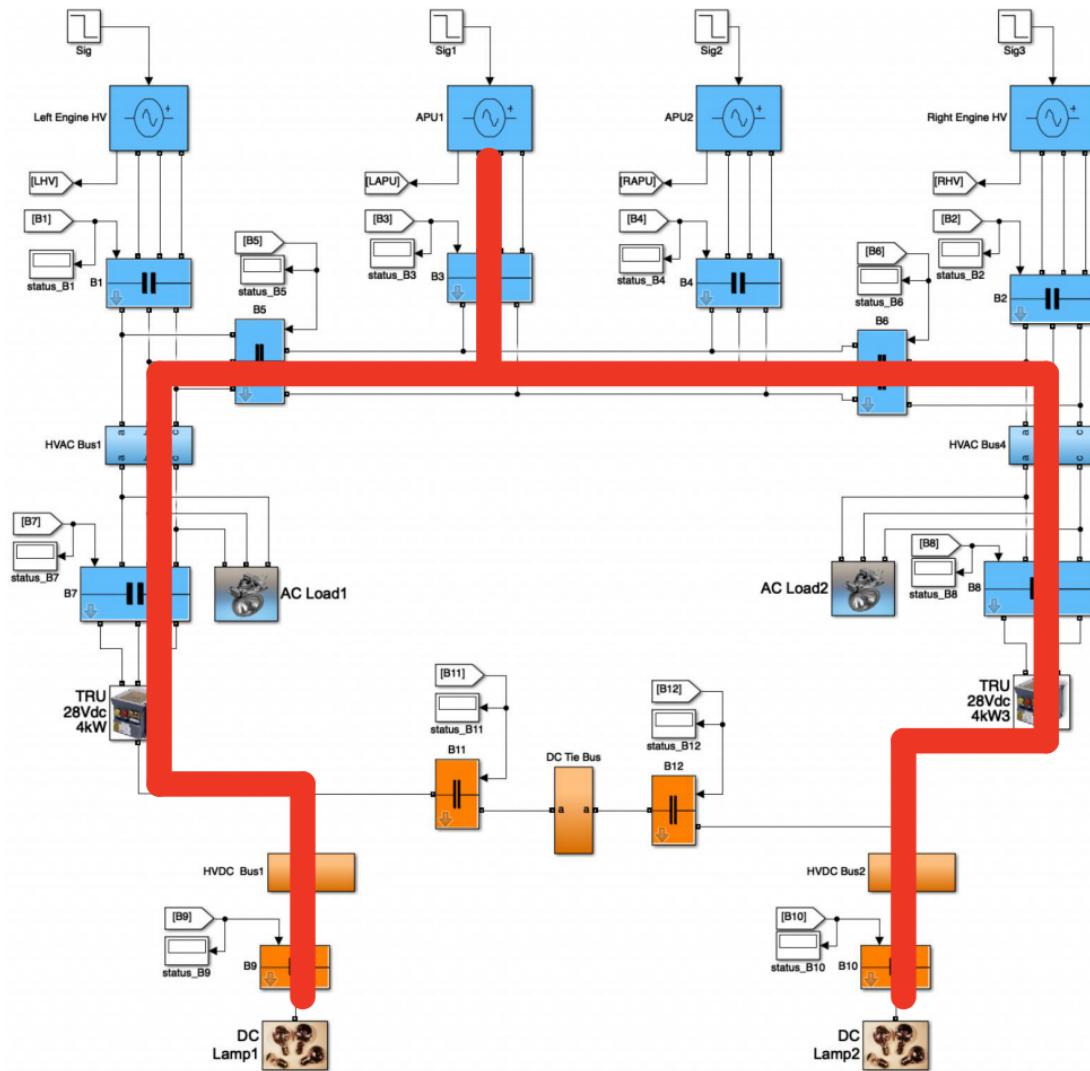


Figure 2.7.4 EPS Connection

When both GR and GL fail, only one APU, AL, is inserted into the network and empowers both AC buses based on system guarantee G4, G7, and G8.

## 2.8 Case 7: GR, GL, AR Not Working

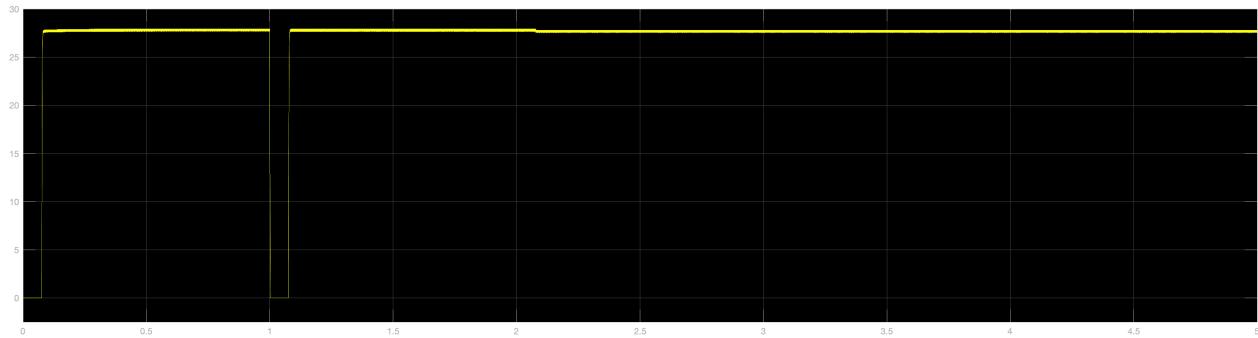


Figure 2.8.1 Left DC Load Waveform

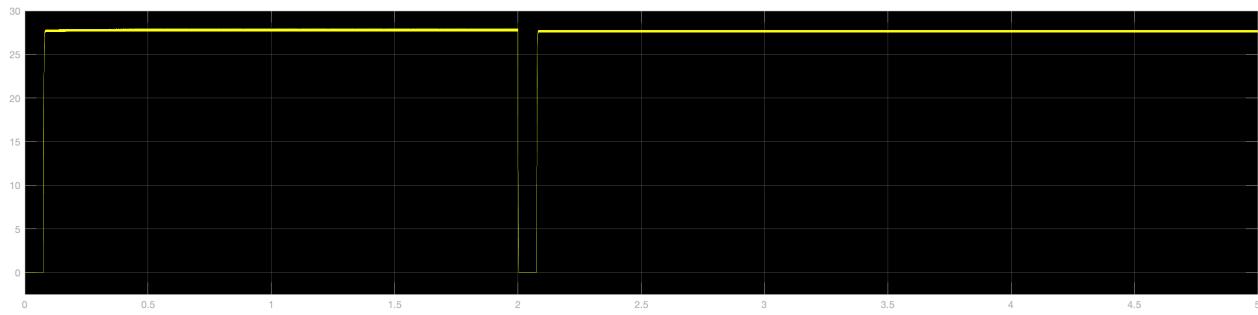


Figure 2.8.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	0	2
	B3	1	3
	B4	0	4
	B5	1	5
	B6	1	6
	GR	0	2
	AL	1	3
	AR	0	4

Figure 2.8.3 BPCU Output Control Signals

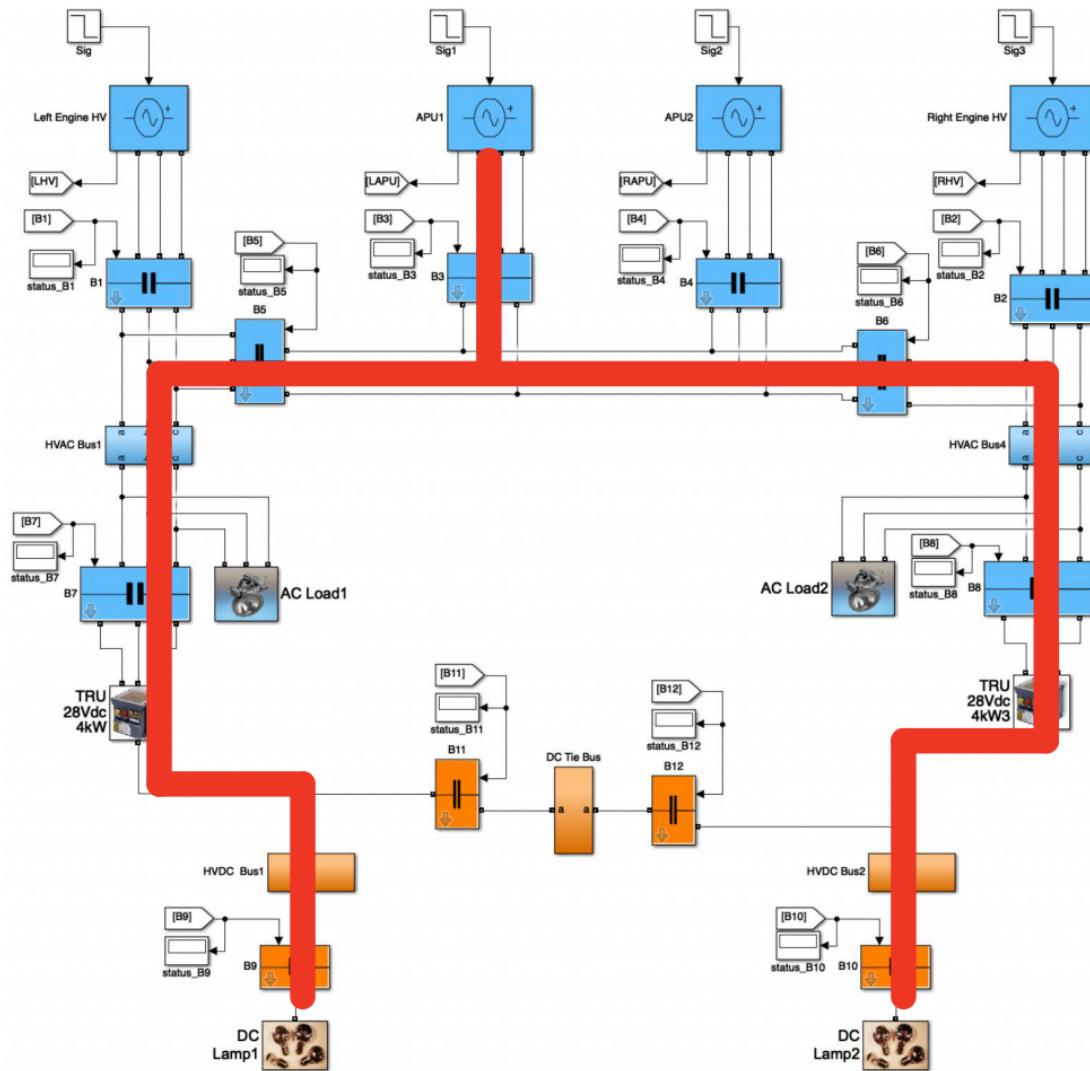


Figure 2.8.4 EPS Connection

When GR, GL, and AR fail, the only power supply left, AL, is inserted into the network and empowers both AC buses based on system guarantee G4, G7, and G8.

## 2.9 Case 8: GR, GL, AL Not Working

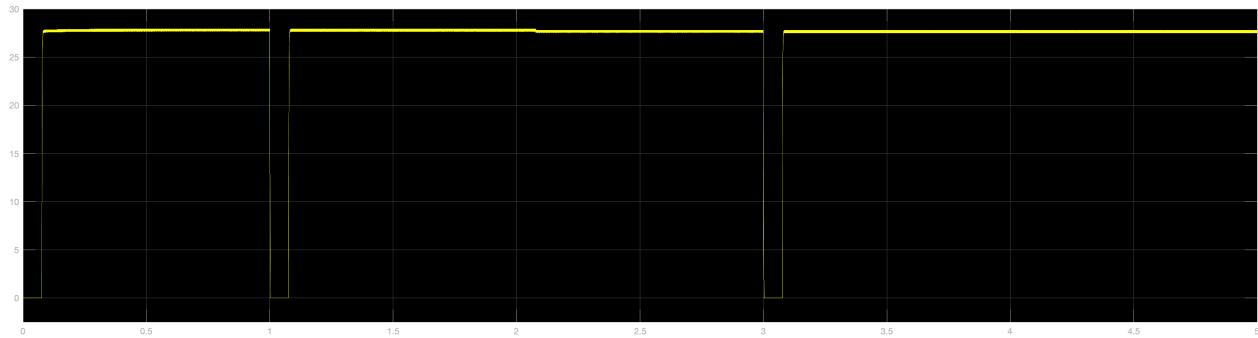


Figure 2.9.1 Left DC Load Waveform

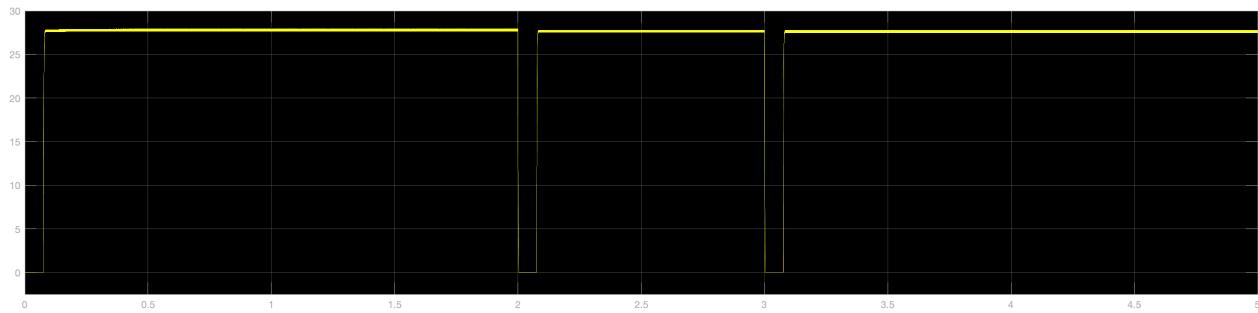


Figure 2.9.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	0	2
	B3	0	3
	B4	1	4
	B5	1	5
	B6	1	6
	GR	0	2
	AL	0	3
	AR	1	4

Figure 2.9.3 BPCU Output Control Signals

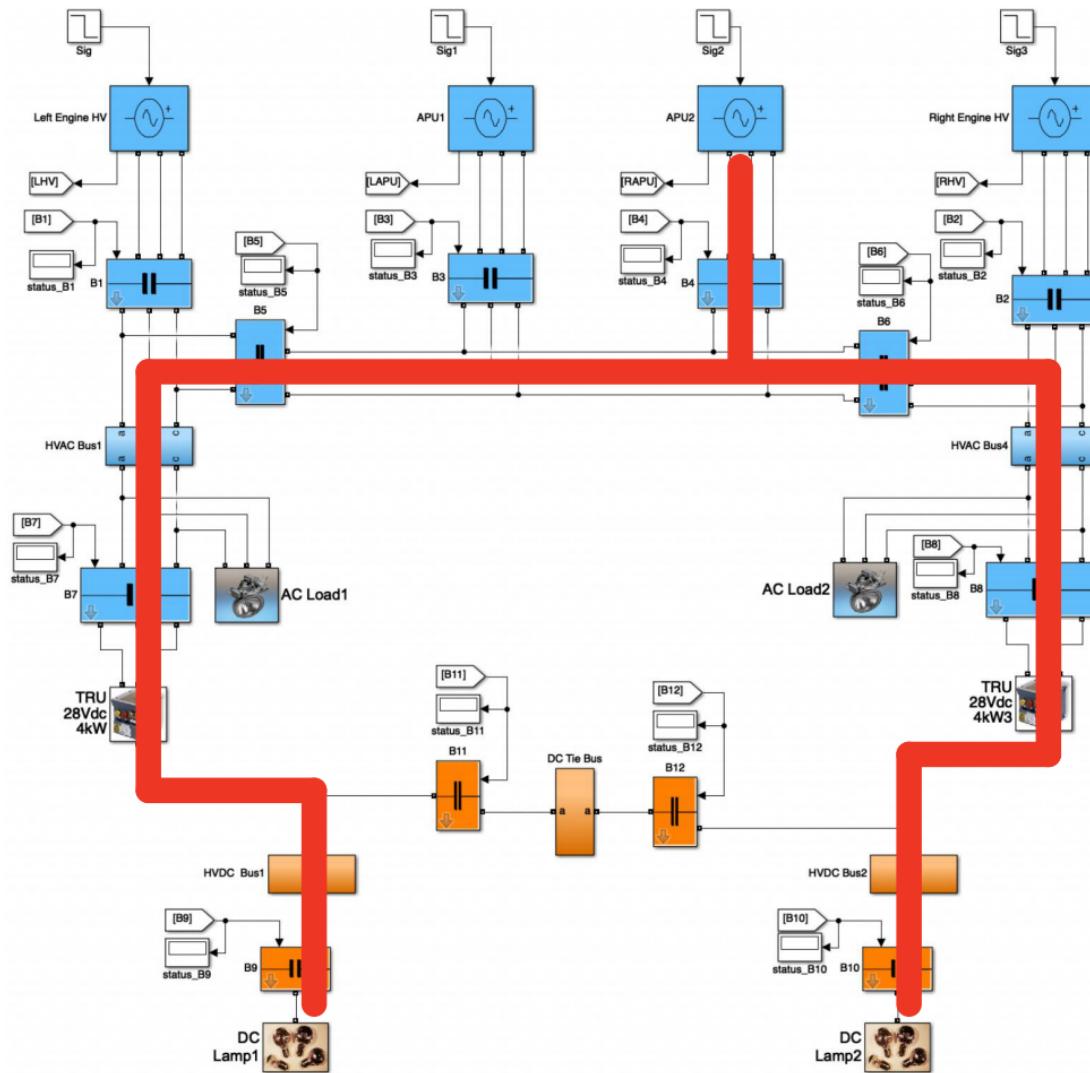


Figure 2.9.4 EPS Connection

When GR, GL, and AL fail, the only power supply left, AR, is inserted into the network and empowers both AC buses based on system guarantee G4, G7, and G8.

## 2.10 Case 9: GR, AR, AL Not Working

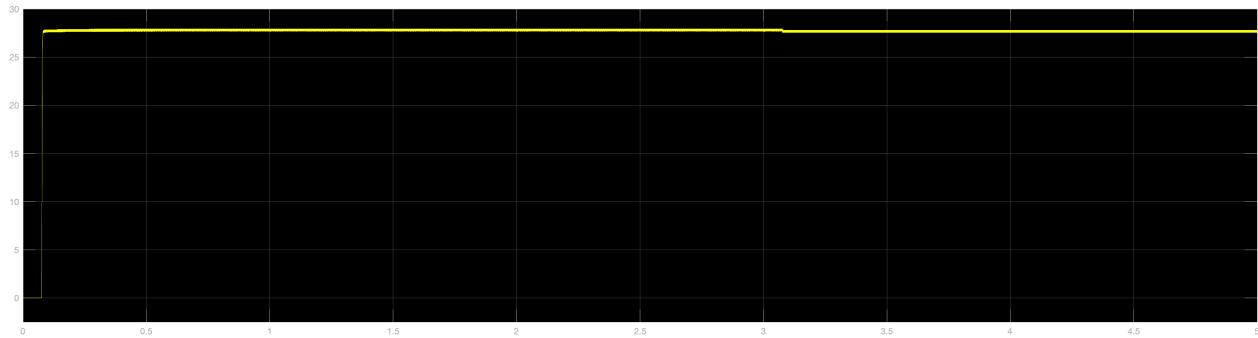


Figure 2.10.1 Left DC Load Waveform

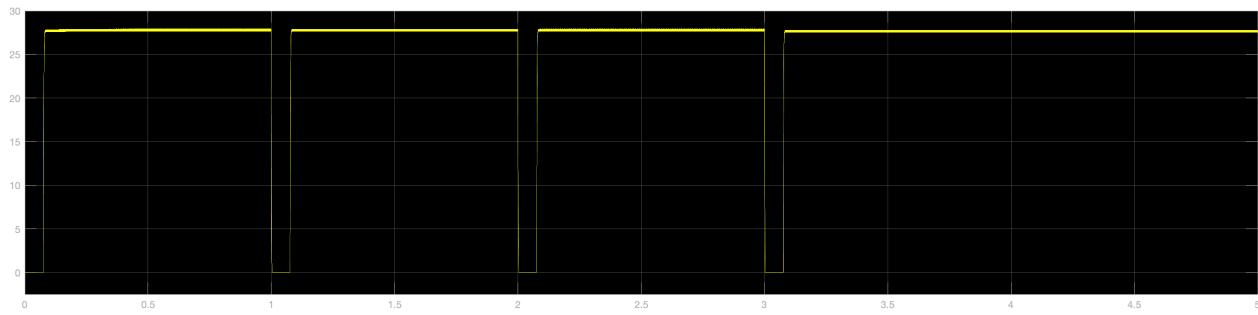


Figure 2.10.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	1	1
	GL	1	1
	B2	0	2
	B3	0	3
	B4	0	4
	B5	1	5
	B6	1	6
	GR	0	2
	AL	0	3
	AR	0	4

Figure 2.10.3 BPCU Output Control Signals

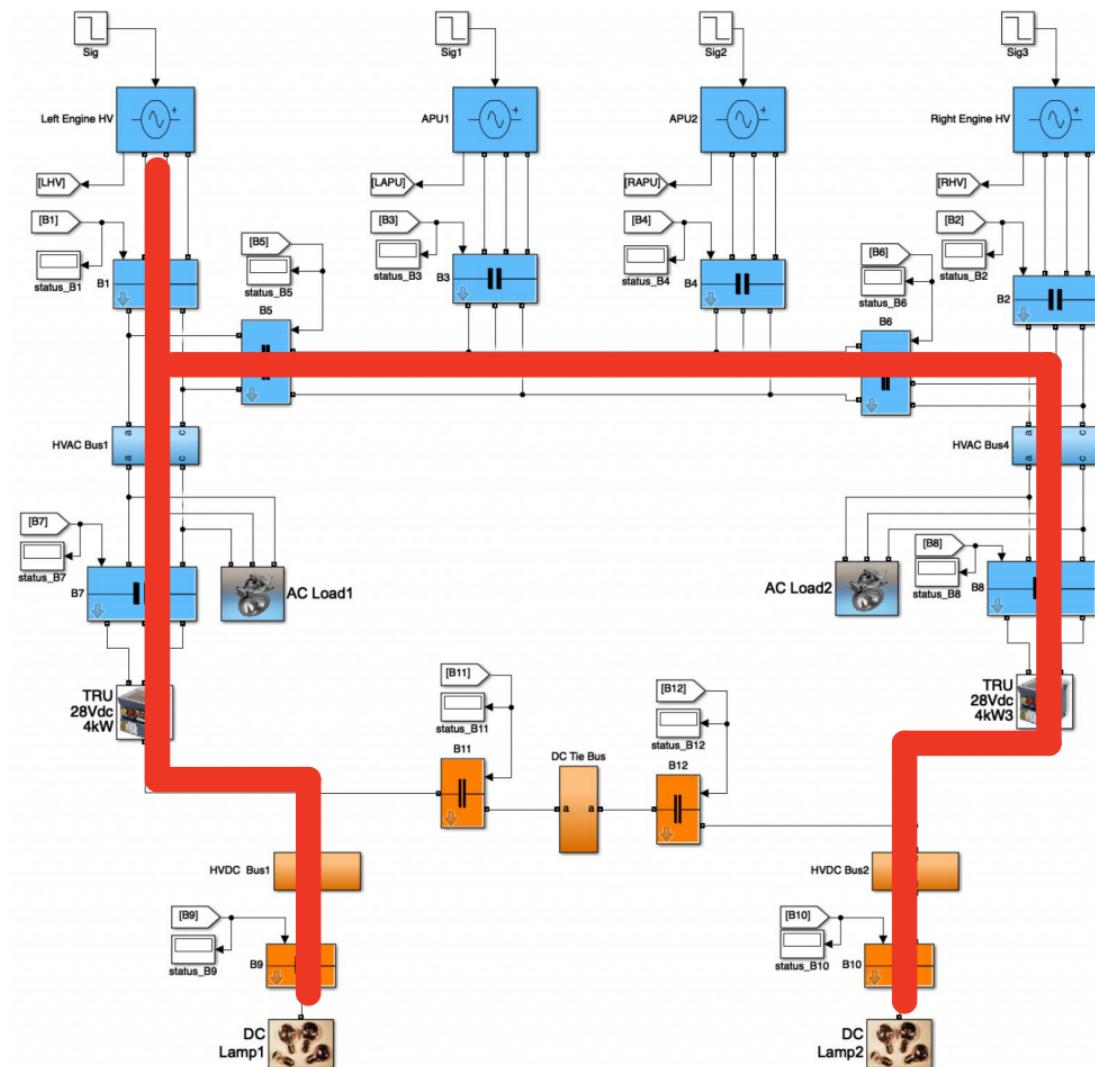


Figure 2.10.4 EPS Connection

When GR, AR, and AL fail, the only power supply left, GL, is inserted into the network and empowers both AC buses based on system guarantee G7 and G8.

## 2.11 Case 10: GL, AR, AL Not Working

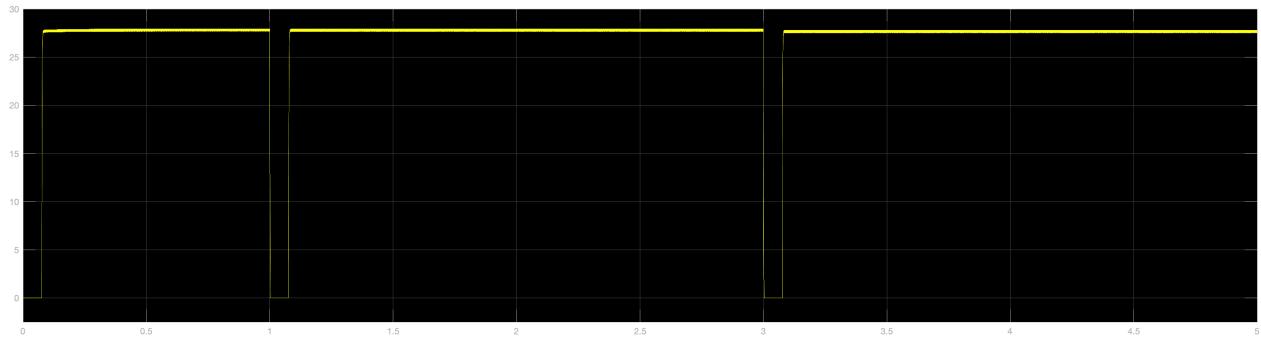


Figure 2.11.1 Left DC Load Waveform

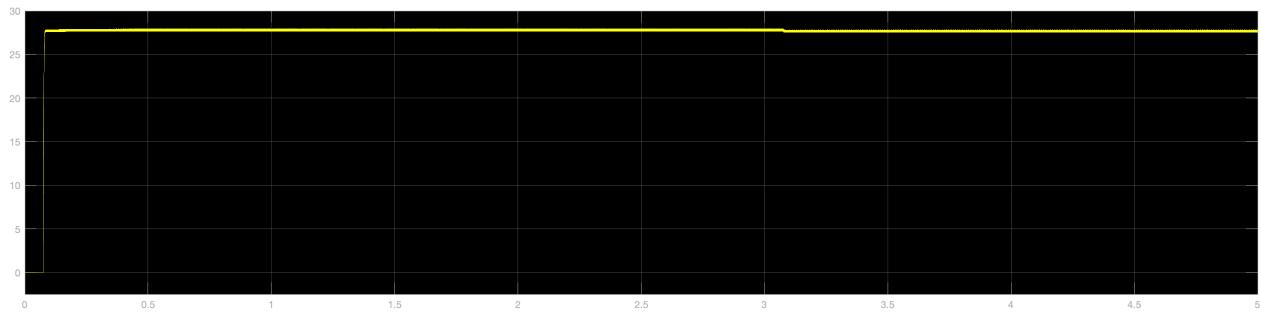


Figure 2.11.2 Right DC Load Waveform

Symbols			
Type	Name	Value	Port
	B1	0	1
	GL	0	1
	B2	1	2
	B3	0	3
	B4	0	4
	B5	1	5
	B6	1	6
	GR	1	2
	AL	0	3
	AR	0	4

Figure 2.11.3 BPCU Output Control Signals

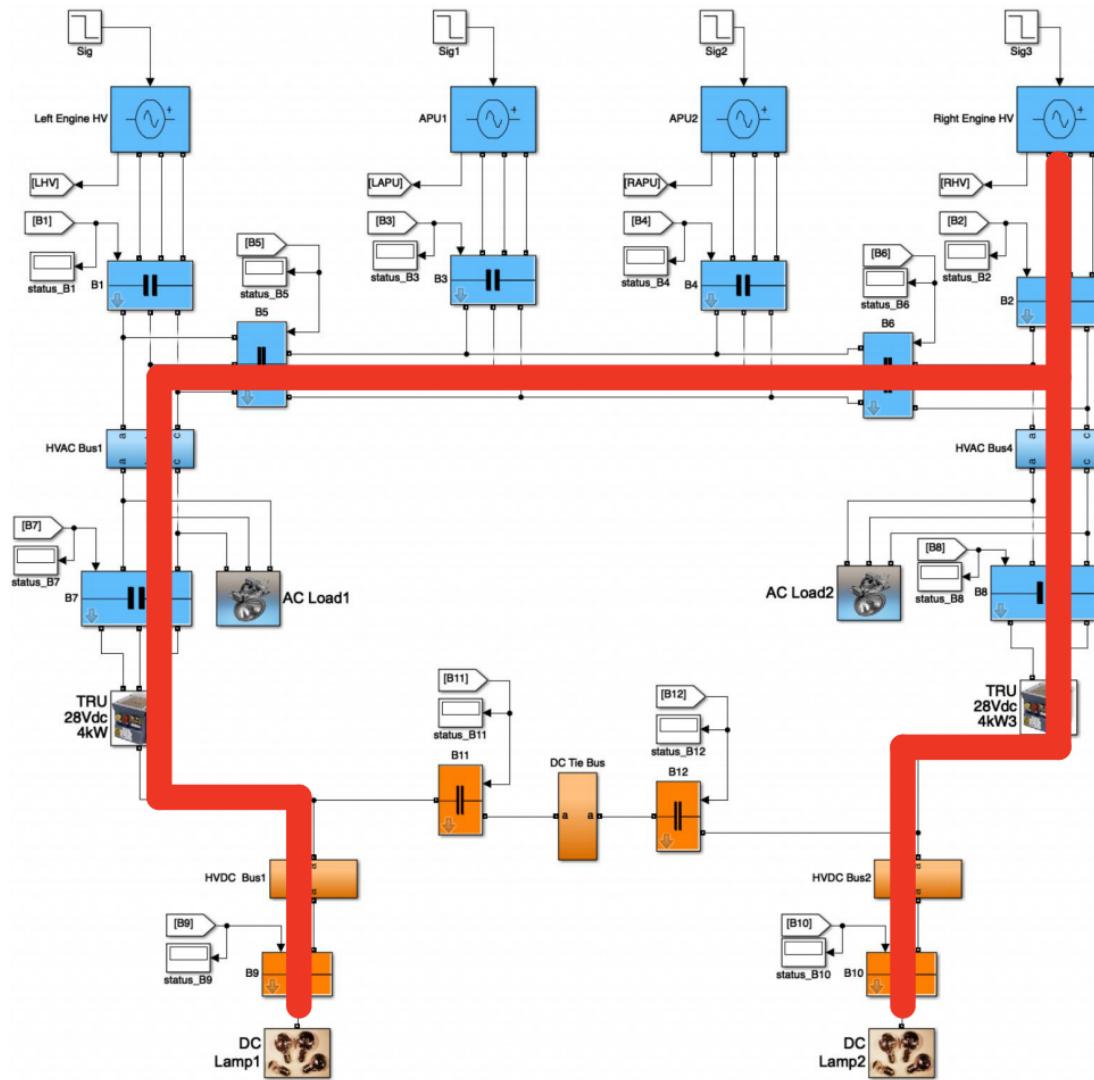


Figure 2.11.4 EPS Connection

When GL, AR, and AL fail, the only power supply left, GR, is inserted into the network and empowers both AC buses based on system guarantee G7 and G8.

### 3 Learning Experience with Simulink

The learning experience with Simulink was time-consuming but satisfactory for us. We self-studied how to build control logic with Stateflow toolbox, how to generate and observe digital waveforms, and how to write and run tests for simulation. In addition, we improved our time management ability, learned how to cooperate well within the team, and experienced with a lot of Simulink trouble-shooting and debugging. The characteristics of Simulink that we like most are its graphical user interface that is friendly for beginners and its large number of built-in functions, waveforms, and modules within Simulink libraries. However, Simulink is not intelligent enough, for example, we have to manually choose correct input and output ports for variables, which might cause a lot of confusion because the variables and ports are not automatically paired. This is the aspect that we dislike most.