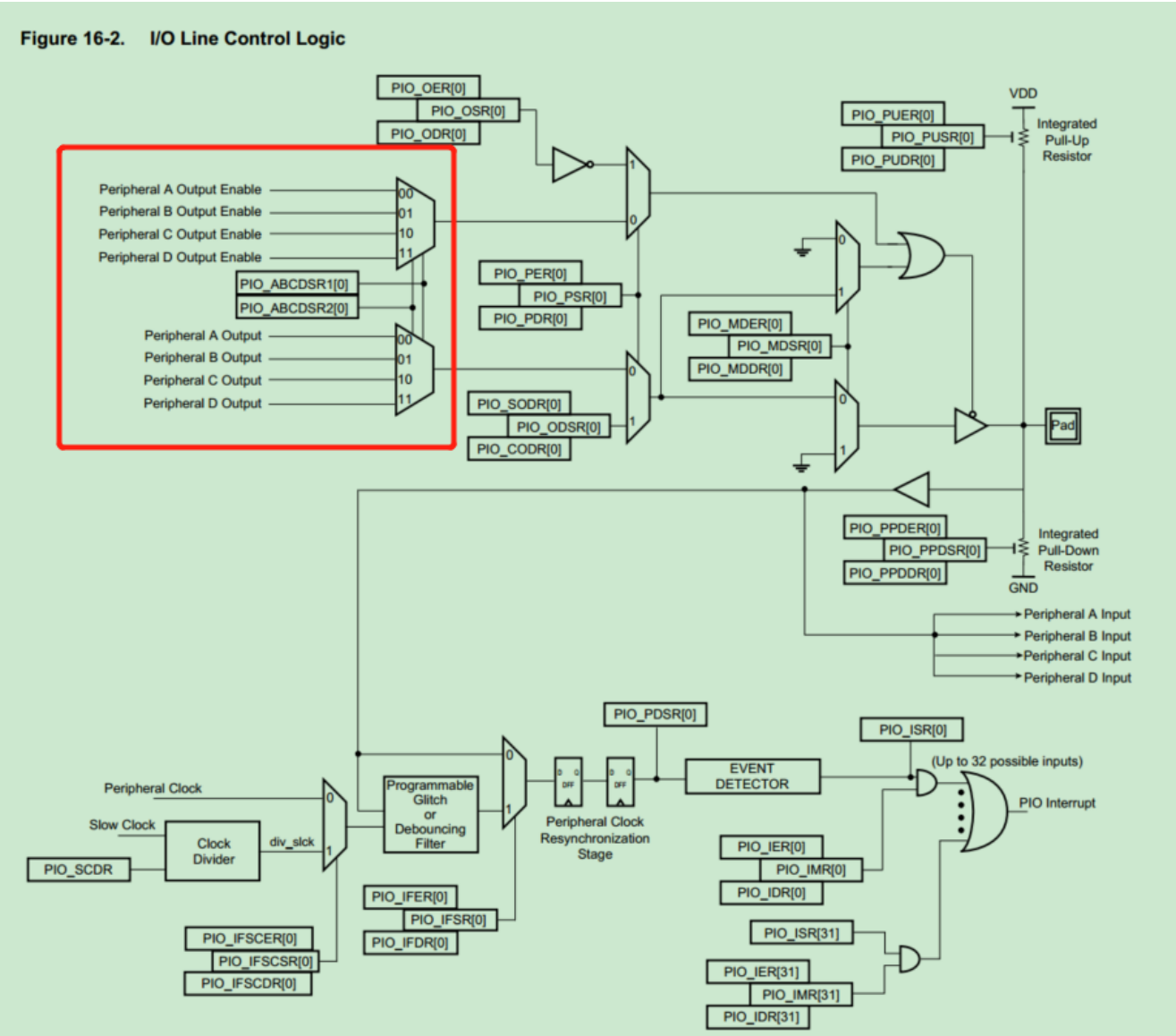
如何配置SAMG55 管脚复用功能

1.注意在I/O line control logic里的"PIO_ABCDSR1","PIO_ABCDSR2"寄存器使用



2.

16.6.24 PIO Peripheral ABCD Select Register 1

Name: PIO_ABCDSR1

Address: 0x400E0E70 (PIOA), 0x400E1070 (PIOB)

Access: Read/Write

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

- **P0–P31: Peripheral Select**

If the same bit is set to 0 in PIO_ABCDSR2:

0: Assigns the I/O line to the Peripheral A function.

1: Assigns the I/O line to the Peripheral B function.

If the same bit is set to 1 in PIO_ABCDSR2:

0: Assigns the I/O line to the Peripheral C function.

1: Assigns the I/O line to the Peripheral D function.

3.

16.6.25 PIO Peripheral ABCD Select Register 2

Name: PIO_ABCDSR2

Address: 0x400E0E74 (PIOA), 0x400E1074 (PIOB)

Access: Read/Write

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

- **P0–P31: Peripheral Select**

If the same bit is set to 0 in PIO_ABCDSR1:

0: Assigns the I/O line to the Peripheral A function.

1: Assigns the I/O line to the Peripheral C function.

If the same bit is set to 1 in PIO_ABCDSR1:

0: Assigns the I/O line to the Peripheral B function.

1: Assigns the I/O line to the Peripheral D function.

有图1.2.3的相关说明可以得出如下结论

第一步

当需要将一个某一PIN口复用为外设功能时，需要将PIO_PER相应的位打开，同时PIO_PSR相应位会被置1或置0，用来表示相应的PIN口是被相应的外设控制，还是被PIO controller控制。

第二步

PIO_ABCDSR1[x] 与PIO_ABCDSR2[x]的组合确定对应Px口线的功能。比如

1.PIO_ABCDSR1[0] bit位为0，PIO_ABCDSR2[0]bit位为0，就决定了P0 这个line口线对应外设功能A.

1.PIO_ABCDSR1[1] bit位为0，PIO_ABCDSR2[0]bit位为0，就决定了P0 这个line口线对应外设功能B.

第三部

那这个外设功能A, 外设功能B到底是指什么呢？

如下图所示：PA0脚的 A外设对应的是I2SCK0功能，B外设对应的是TIOA0功能。

9.2.1 PIO Controller A Multiplexing

Table 9-3. Multiplexing on PIO Controller A (PIOA)

I/O Line	Peripheral A	Peripheral B	Extra Function	System Function
PA0	I2SCK0	TIOA0	WKUP0(1)	–
PA1	I2SWS0	TIOB0	WKUP1(1)	–
PA2	TCLK0	I2SDI0	WKUP2(1)	–
PA3	TXD3/SPI3_MOSI/TWD3	I2SDO0	WKUP9(1)	–
PA4	RXD3/SPI3_MISO/TWCK3	I2SMCK0	WKUP10(1)	–
PA5	RXD2/SPI2_MISO/TWCK2	SPI5_NPCS1/RTS5	WKUP4(1)	–
PA6	TXD2/SPI2_MOSI/TWD2	PCK0	–	–
PA7	–	–	–	XIN32(2)
PA8	–	ADTRG	WKUP5(1)	XOUT32(2)
PA9	RXD0/SPI0_MISO/TWCK0	PDMIC_DAT	WKUP6(1)	–
PA10	TXD0/SPI0_MOSI/TWD0	PDMIC_CLK	–	–
PA11	SPI5_NPCS0/CTS5	–	–	–
PA12	RXD5/SPI5_MISO/TWCK5	–	–	–
PA13	TXD5/SPI5_MOSI/TWD5	–	–	–
PA14	SCK5/SPI5_SPCK	–	WKUP8(1)	–
PA15	SPI2_NPCS1/RTS2	SCK2/SPI2_SPCK	–	–
PA16	SPI2_NPCS0/CTS2	TIOB1	WKUP7(1)	–
PA17	I2SDO0	PCK1	AD0(3)	–
PA18	I2SMCK0	PCK2	AD1(3)	–
PA19	TCLK1	I2SCK1	AD2(3)	–
PA20	TCLK2	I2SWS1	AD3(3)	–
PA21	TIOA2	PCK1	–	DM
PA22	TIOB2	I2SDI1	–	DP
PA23	I2SDO1	TIOA1	WKUP3(1)	–
PA24	I2SMCK1	SCK2/SPI2_SPCK	WKUP11(1)	–
PA25	SPI0_NPCS0/CTS0	I2SDO1	–	–
PA26	SPI0_NPCS1/RTS0	I2SMCK1	–	–
PA27	SCK1/SPI1_SPCK	RXD7/SPI7_MISO/TWCK7	–	–

疑问：

所有的PIO_PER, PIO_PSR, PIO_ABCDSR1,PIO_ABCDSR2寄存器都是对应32个pin脚，怎么区分是PA01 还是PB01呢，就是说，如何区分不同的pin组，其实每组PIN口都对应有一组的寄存器。如下图所示，每个PIO_PER其实有两个实际的寄存器地址，分别对应PIOA, PIOB.

16.6.1 PIO Enable Register

Name: PIO_PER

Address: 0x400E0E00 (PIOA), 0x400E1000 (PIOB)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

- **P0–P31: PIO Enable**

0: No effect.

1: Enables the PIO to control the corresponding pin (disables peripheral control of the pin).