2023 Digital IC Design Homework 1

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| NAME | | 王昱承 | | | | | | |
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| **Functional Simulation Result** | | | | | | | | |
| Stage 1 | Pass | | Stage 2 | Pass | Stage 3 | Pass | Stage 4 | Pass |
| **Stage 1** | | | | | | | | |
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| **Stage 2** | | | | | | | | |
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| **Stage 3** | | | | | | | | |
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| **Stage 4** | | | | | | | | |
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| **Description of your design** | | | | | | | | |
| * MMS\_4num.v   先令兩個wire temp1以及temp2，接著透過assign先比較大小，再來才比較select，以避免產生多餘大小比較器。可由下面截圖發現只使用3個 ”>”單元，如果是先比較select才比較大於則會產生6個 ”>” 單元。   * MMS\_8num.v   Include上面寫好的.v檔，再令兩個wire temp1以及temp2，一樣先透過assign先比較大小，再來才比較select。 | | | | | | | | |