VLSI System Design (Graduate Level)

Fall 2018

HOMEWORK IV

REPORT

Must do self-checking before submission:

Compress all files described in the problem into one tar

All SystemVerilog files can be compiled under SoC Lab environment

All port declarations comply with I/O port specifications

Organize files according to File Hierarchy Requirement

No any waveform files in deliverables

Student name: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

Student ID: \_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_

Rtl0

L1Cache hit = 0.964

L2Cache hit = 0.4

Ipc = 0.702

Rtl1

L1Cache hit = 0.999

L2Cache hit = 0.986

Ipc = 0.798

Rtl2

L1Cache hit = 0.999

L2Cache hit = 0.90

Ipc = 0.775

Rtl3

L1Cache hit = 0.992

L2Cache hit = 0.87

Ipc = 0.654