EECS31L
Lab3
Dr. Kavianpour

A. MOD-32 Up/Down-Counter

1. Write VHDL codes for MOD-32 up/down counter. Use an input DIR, to specify the direction of the count when DIR = 0, the count increments; when DIR = 1, the count decrements.

2. Simulate your codes for both up and down cases using CLK for a period of 40 ns.

B. MOD-21 Up/Down-Counter

1-Modify VHDL in part A to have MOD 21 up/down counter.

Lab submission

a-Doc/pdf report

Write if your code is working or partially working.
-Paste copy of VHDL files for parts A and B
-Paste copy of VHDL test bench files for parts A and B
-Paste Screenshot of simulation results for parts A and B.

b-Submit VHDL and test bench files for parts A and B