© 2019 Dr. Kavianpour

These notes are protected by copy rights. Students are not allowed to reproduce, distribute, sell, or publicly post this course materials without faculty permission

Final Project EECS31L Dr. Kavianpour

Use VHDL design a 4-bit ALU (Arithmetic logic Unit) with the 8 instructions:

ADD, REVERSE, MUL, INC, XNOR, NOT, RROTATION, LROTATION.

- 1-Assume codes for instructions are: 000=ADD, 001=REVERSE, 010=MUL, 011=INC, 100=XNOR, 101=NOT, 110= RROTATION, and 111= LROTATION
- 2- Assume input numbers are unsigned.
- 3- For instructions REVERSE, NOT, RROTATION and LROTATION use number  $A_3A_2A_1A_0$
- 4-For addition result will be in C<sub>3</sub>C<sub>2</sub>C<sub>1</sub>C<sub>0</sub> and carry in CO
- 4-For multiplication use repeated addition such as A+A+A+... ( B times) and outputs are in  $D_3D_2D_1D_0,\,C_3C_2C_1C_0$  ,
- 5-Inputs are clock,  $A_3A_2A_1A_0$ ,  $B_3B_2B_1B_0$ , and code for instruction. Output is  $C_3C_2C_1C_0$  and CO in case of add and  $D_3D_2D_1D_0$ ,  $C_3C_2C_1C_0$ in case of multiplication

## **Example:**

A=0111, B=0101, code=000

Means add A+B and the result is C=0111+0101=1100 and CO=0 If code is 101

Means NOT of A

A=0111, C=1000

If code is 001

Means REVERSE

A=0111, C=1110

If code is 010

Means Multiplication

A=0111, B=0101,

A\*B=100011 D=0010 C=0011

## For your report:

## 1-Report

a--Write if your code is working or partially working b-Paste Screenshot of simulation results. For 8 instructions for A=1000 and B=0111 c--Paste copy of VHDL file d-Paste copy of VHDL test bench

## 2-Submit VHDL and test bench files

,