Lab report For Lab 2 of EECS 31L 2019 Fall

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Lab Session Hours: LAB A2 16442 M 6:00 – 8:50 P.M.

T.A.: CHOOKHACHIZADE.M.

This project is working properly

Objective:

This lab asks us to design a 4-1 MUX and then use this 4-1 mux to design a 16-1 mux. For lab part, I just simply define two select bit as bit type and input as std\_logic. Then I use a signal named “sel” to combine two select bits into bit vector. And use “with” and “when” method to select all possible cases.

Lab\_2 mux14 part:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.numeric\_std.ALL;

entity mux41 is

-- Port ( );

port(S0,S1 : IN BIT;

D0,D1,D2,D3 : IN STD\_LOGIC;

Y : OUT STD\_LOGIC);

end mux41;

architecture Behavioral of mux41 is

SIGNAL sel: BIT\_vector(1 downto 0);

begin

sel <= S0&S1;

WITH sel SELECT

Y <= D0 WHEN "00",

D1 WHEN "01",

D2 WHEN "10",

D3 WHEN "11";

end Behavioral;

lab\_2 test bench tb\_mux14 part:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity tb\_MUX41 is

-- Port ( );

end tb\_MUX41;

architecture Behavioral of tb\_MUX41 is

COMPONENT MUX41 IS

PORT(S0,S1 : IN BIT;

D0,D1,D2,D3 : IN STD\_LOGIC;

Y : OUT STD\_LOGIC );

END COMPONENT;

SIGNAL S0,S1 : BIT;

SIGNAL D0,D1,D2,D3 : STD\_LOGIC;

SIGNAL Y : STD\_LOGIC;

begin

uut:MUX41

PORT MAP(

S0 => S0,

S1 => S1,

D0 => D0,

D1 => D1,

D2 => D2,

D3 => D3,

Y => Y);

stimu\_proc : process

begin

wait for 20ns;

S0 <= '0';

S1 <= '1';

D0 <= '1';

D1 <= '0';

D2 <= '1';

D3 <= '1';

wait for 20ns;

S0 <= '1';

S1 <= '1';

D0 <= '1';

D1 <= '0';

D2 <= '1';

D3 <= '1';

end process;

end Behavioral;

Simulation run for mux41 output:

A screenshot of a computer

Description automatically generated

Lab\_2 16 1 mux code:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

entity mux161 is

-- Port ( );

PORT( A: IN STD\_LOGIC\_VECTOR(15 DOWNTO 0);

S: IN BIT\_VECTOR(3 DOWNTO 0);

Y: OUT STD\_LOGIC);

end mux161;

architecture Behavioral of mux161 is

SIGNAL Y1,Y2,Y3,Y4 : STD\_LOGIC;

COMPONENT mux41 IS

PORT(

S0,S1 : IN BIT;

D0,D1,D2,D3 : IN STD\_LOGIC;

Y:OUT STD\_LOGIC);

END COMPONENT;

begin

MUX1 : mux41 port map(s0=>S(0),s1=>S(1),D0=>A(0),D1=>A(1),D2=>A(2),D3=>A(3),y=>Y1);

MUX2 : mux41 port map(s0=>S(0),s1=>S(1),D0=>A(4),D1=>A(5),D2=>A(6),D3=>A(7),y=>Y2);

MUX3 : mux41 port map(s0=>S(0),s1=>S(1),D0=>A(8),D1=>A(9),D2=>A(10),D3=>A(11),y=>Y3);

MUX4 : mux41 port map(s0=>S(0),s1=>S(1),D0=>A(12),D1=>A(13),D2=>A(14),D3=>A(15),y=>Y4);

MUX5 : mux41 port map(s0=>S(2),s1=>S(3),D0=>Y1,D1=>Y2,D2=>Y3,D3=>Y4,y=>Y);

end Behavioral;

Lab\_2 16 1mux test bench tb\_161mux code:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity tb\_mux161 is

-- Port ( );

end tb\_mux161;

architecture Behavioral of tb\_mux161 is

component mux161

port(

A: IN STD\_LOGIC\_VECTOR(15 DOWNTO 0);

S: IN BIT\_VECTOR(3 DOWNTO 0);

Y: OUT STD\_LOGIC);

END COMPONENT;

component mux41

port(

S0,S1 : IN BIT;

D0,D1,D2,D3 : IN STD\_LOGIC;

Y : OUT STD\_LOGIC);

END COMPONENT;

SIGNAL A: STD\_LOGIC\_VECTOR(15 DOWNTO 0);

SIGNAL S: BIT\_VECTOR(3 DOWNTO 0);

SIGNAL Y: STD\_LOGIC;

begin

uut: mux161 port map(

A => A,

S => S,

Y => Y);

uut1: mux41 port map(

S0 => S(0),

S1 => S(1),

D0 => A(0),

D1 => A(1),

D2 => A(2),

D3 => A(3),

Y => Y);

stimus\_proc : process

begin

wait for 20ns;

A <= X"7DAB";

S <= "0011";

wait for 20ns;

A <= X"7DAB";

S <= "1010";

wait for 20ns;

A <= X"7DAB";

S <= "1110";

END PROCESS;

end Behavioral;

16 to 1 Mux test bench simulation screenshots:

A screenshot of a computer

Description automatically generated