Lab report For Lab 4 of EECS 31L 2019 Fall

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Lab Session Hours: LAB A2 16442 M 6:00 – 8:50 P.M.

T.A.: CHOOKHACHIZADE.M.

The code is working properly.

1. Objective:

This project is asking us to design a elevator control machine. Using the requirement in the lab’s description. I defined 6 states s0,s1,s2,s3,s4,s5. Each States has 3 variables to represent direction motion and door. S0 is “000”, S1 is “100”,S2 is “101” AND after S2, arrive1 becomes 1,arrive2 becomes 0. S3 is “010”, S4 is “ 011” and finally s5 is “111” AND after s5, arrive1 becomes0, arrive2 becomes 1 indicate the elevator arrives at higher level.

1. Elevator Code for State Diagram:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity elevator is

port( clk : in bit;

Q: buffer bit\_vector(2 downto 0);

arrive1: BUFFER bit;

arrive2: BUFFER bit

);

-- Port ( );

end elevator;

architecture Behavioral of elevator is

type STATE\_TYPE IS(S5,S4,S3,S2,S1,S0);

SIGNAL state : STATE\_TYPE;

begin

process(CLK)

begin

IF(CLK'EVENT AND CLK = '1')THEN

CASE state IS

WHEN S0 => state <= s1;

WHEN S1 => state <= S2;

WHEN S2 =>

arrive2 <= '0';

arrive1 <= '1';

if ARRIVE1 = '1' THEN

state <= s3;

else state <= s2;

end if;

when s3 => state <=s4;

when s4 => state <=s5;

when s5 =>

arrive1 <= '0';

arrive2 <= '1';

if arrive2 = '1' THEN

state <= s0;

else state <= S5;

end if;

end case;

end if;

end process;

with state select

Q <= "000" WHEN S0,

"100" when s1,

"101" when s2,

"010" when s3,

"110" when s4,

"111" when s5;

end Behavioral;

1. Code for tb\_elevator test bench:

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity tb\_elevator is

-- Port ( );

end tb\_elevator;

architecture Behavioral of tb\_elevator is

component elevator is

port(

clk : in bit;

q: buffer bit\_vector(2 downto 0);

arrive1: BUFFER bit;

arrive2: BUFFER bit

);

end component;

signal CLK,arrive1,arrive2 : BIT;

signal Q : bit\_vector(2 downto 0);

begin

uut : elevator

port map(

clk => clk,

arrive1 => arrive1,

arrive2 => arrive2,

q => q

);

clk\_proces : process

begin

wait for 40ns;

if CLK = '0'then

clk <= '1';

else

clk <= '0';

end if;

end process;

stimu\_process : process

begin

wait for 2000ns;

end process;

end Behavioral;

1. Screenshots of the testing simulation output:

The total simulation was set to 2000ns;

A close up of a computer

Description automatically generated