Lab report For Lab 5 of EECS 31L 2019 Fall

Student Name: Yuchen Yan

Student ID:28249722

Lab Session Hours: LAB A2 16442 M 6:00 – 8:50 P.M.

T.A.: CHOOKHACHIZADE.M.

The code is working properly.

1. Objective:

This lab asks us to design a 4-bit ALU with the function of add, reverse, mul, rotation, not, xnor. In this lab, I use case when to select different functions with different codes input. For add and multiplication function, I use variable instead of signal to process the value to output c3c2c1c in order to make it within one clock cycle, and use while loop to achieve multiplication function for ALU.

1. Code for ALU

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**-- Company:**

**-- Engineer:**

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**-- Create Date: 11/18/2019 06:06:09 PM**

**-- Design Name:**

**-- Module Name: ALU - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**use IEEE.numeric\_std.all;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity ALU is**

**-- Port ( );**

**port ( clk : in bit;**

**A: in std\_logic\_vector(3 downto 0);**

**C: OUT std\_logic\_vector(3 downto 0);**

**D: OUT std\_logic\_vector(3 downto 0);**

**B: IN std\_logic\_vector(3 downto 0);**

**CODE : IN std\_logic\_vector(2 DOWNTO 0);**

**CO : out std\_logic**

**);**

**end ALU;**

**architecture Behavioral of ALU is**

**begin**

**process(A,B,clk,code)**

**variable tmp: std\_logic\_vector(4 downto 0);**

**variable ALU\_RESULT\_3 : std\_logic\_vector(7 downto 0);**

**variable tmp1: std\_logic\_vector(7 downto 0):=(others => '0');**

**variable n:integer;**

**begin**

**tmp1 := "00000000";**

**if(clk'event and clk ='1') then**

**case code is**

**when "000" =>---add**

**tmp := std\_logic\_vector(unsigned("0"&A) + unsigned("0"&B));**

**C <= tmp(3 downto 0);**

**Co <= tmp(4);**

**when "001" =>---reverse**

**C <= A(0)&A(1)&A(2)&A(3);**

**when"101" =>---not**

**C <= NOT A;**

**when "110" =>---right R**

**C <= A(0)&A(3 downto 1);**

**when "111"=>---left R**

**C <= A(2 downto 0)&A(3);**

**when "010" => ---mul**

**while (n < unsigned(b)) loop**

**tmp1 := std\_logic\_vector(to\_unsigned(to\_integer(unsigned(tmp1))+ to\_integer(unsigned("0000"&A)),8));**

**n := n + 1;**

**end loop;**

**alu\_result\_3 := tmp1;**

**C <= std\_logic\_vector(alu\_result\_3(7 downto 4));**

**D <= std\_logic\_vector(alu\_result\_3(3 downto 0));**

**when "100" => --- xnor**

**C <= A XNOR B;**

**when "011"=> --- increment**

**C <= std\_logic\_vector(unsigned(A)+B"0001");**

**when others =>**

**null;**

**end case;**

**end if;**

**end process;**

**end Behavioral;**

1. Testbench for ALU tb\_alu:

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**-- Company:**

**-- Engineer:**

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**-- Create Date: 11/29/2019 08:37:54 PM**

**-- Design Name:**

**-- Module Name: tb\_alu - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity tb\_alu is**

**-- Port ( );**

**end tb\_alu;**

**architecture Behavioral of tb\_alu is**

**component ALU is**

**port(**

**clk : in bit;**

**A: in std\_logic\_vector(3 downto 0);**

**C: OUT std\_logic\_vector(3 downto 0);**

**D: OUT std\_logic\_vector(3 downto 0);**

**B: IN std\_logic\_vector(3 downto 0);**

**code: IN std\_logic\_vector(2 downto 0);**

**CO : out std\_logic**

**);**

**end component;**

**signal CLK: bit;**

**signal A,B,C,D : std\_logic\_vector(3 downto 0);**

**signal CO:std\_logic;**

**signal code: std\_logic\_vector(2 downto 0);**

**begin**

**uut: ALU**

**port map(**

**clk => clk,**

**A => A,**

**B => B,**

**C => C,**

**D => D,**

**code => code,**

**CO => CO);**

**clk\_proces : process**

**begin**

**wait for 175 ns;**

**if clk = '0' then**

**clk <= '1';**

**else**

**clk <= '0';**

**end if;**

**end process;**

**stimu\_process : process**

**begin**

**A <= "0111";**

**B <= "0101";**

**CODE <= "000";**

**wait for 375ns;**

**CODE <= "001";**

**wait for 375ns;**

**code <= "010";**

**wait for 375ns;**

**code <= "011";**

**wait for 375ns;**

**code <= "100";**

**wait for 375ns;**

**code <= "101";**

**wait for 375ns;**

**code <= "110";**

**wait for 375ns;**

**code <= "111";**

**wait;**

**end process;**

**end Behavioral;**

1. Simulation run for ALU’S output:

**A close up of a computer

Description automatically generated**