

國立中興大學

108 學年度

碩士班考試入學招生

試 題

學系：資訊科學與工程學系

甲組

科目名稱：資訊概論

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**PART 1. Introduction to Computer Science****A. Multiple Choice (3 points each)**

1. Assuming that  $a$  is an array and  $aPtr$  is a pointer to that array and no errors are encountered during the compilation. What expression refers to the address of the  $k$ -th element?  
 A compilation. What expression refers to the address of the  $k$ -th element?  
 (a)  $*(a + k)$  (b)  $\&aPtr[k]$  (c)  $\&a[k-1]$  (d)  $*(a + k-1)$
2. We have stored the two-dimensional array *student* in memory. The array is  $100 \times 4$ , i.e., 100 rows and 4 columns. Assume the following three conditions for this array.  
 (1) The element *student* [1][1] is stored in the memory location with address 1000;  
 (2) Each element occupies only one memory location;  
 (3) The computer uses row-major storage, which means an entire row of an array is stored in memory before the next row.  
 What will be address of the element *students* [5][3]?  
 (a) 1013 (b) 1014 (c) 1017 (d) 1018
3. Assuming no compilation error occurs in the program shown below. What will be the output of the following C program?  
 (a) unknown garbage value (b) Excellent (c) The address of the string *str*[25]  
 (d) cellent

```
#include<stdio.h>
int main()
{
    char str[25] = "Excellent";
    printf("%s\n", (str+2));
    return 0;
}
```

4. What will be the output of the following C program?  
 (a) 20, 2, 4 (b) 16, 4, 4 (c) 16, 4, 2 (d) 20, 4, 4

```
#include<stdio.h>
int main()
{
    int arr[] = {12, 13, 14, 15, 16};
    printf("%d, %d, %d\n", sizeof(arr), sizeof(*arr), sizeof(arr[0]));
    return 0;
}
```

5. What will be the output of the following C program?  
 (a) -3, 3, 1, 1 (b) -3, 2, 0, 1 (c) -2, 3, 0, 1 (d) -2, 3, 1, 1

```
#include<stdio.h>
int main()
{
    int i=-3, j=2, k=0, m;
    m = ++i && ++j || ++k;
    printf("%d, %d, %d, %d\n", i, j, k, m);
    return 0;
}
```

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6. In \_\_\_\_ traversal of a binary tree, the left subtree is processed last.  
(a) preorder (b) inorder (c) postorder (d) none of the above
7. To prevent \_\_\_\_, an operating system can put resource restrictions on processes.  
(a) starvation (b) synchronization (c) paging (d) deadlock
8. What is the highest TCP/IP layer responsible for each of the following activities?  
(a) sending a frame to the next node (b) sending a packet from the source to the destination (c) delivery of a long message from the source computer to the destination computer (d) logging in to a remote computer

## B. Short Answer Questions

1. A multiprogramming operating system uses paging. The available memory is 100 MB divided into 25 frames, each of 4 MB. The first program needs 13 MB, the second program needs 17 MB, and the third program needs 30 MB.

- (a) How many frames are unused? (2 pts) 17  
(b) What percentage of memory wasted? (2 pts)  $\frac{8}{17} = 46.4\%$

2. The bit pattern  $(1100101000000000111000100001111)_2$  is stored in Excess\_127 format. Show the value in decimal. (6 pts)

3. Using an 8-bit allocation, first convert each of the following number to sign-and-magnitude representation, do the operation, and then convert the result to decimal.

- a. 19-23 (4 pts)  
b. -19-23 (4 pts)

$$\begin{array}{r} 001001 \\ 110100 \\ \hline 111100 \end{array} \Rightarrow 1000100 \#$$

$$\begin{array}{r} 110101 \\ 110100 \\ \hline 101011 \end{array}$$

4. Please derive the corresponding time complexity (Big-O) for the following programs. (8 pts)

- (A) Program a:  $O(n)$   
(B) Program b:  $O(n^2)$   
(C) Program c:  $O(n^3)$   
(D) Program d:  $O(\log n)$

Program a	Program b
<pre>int dot() {     int sum = 0;     for (int i=0; i&lt;n; ++i)         sum += a[i] * b[i];     return sum; }</pre>	<pre>int factorial(int n) {     if (n &lt;= 1)         return 1;     else         return n * factorial(n-1); }</pre>
Program c	Program d
<pre>int factorial (int n) {     if (n &lt;= 1)         return 1;     else {         fact = 1;         for (k = 2; k &lt;= n; k++)             fact * = k;         return fact;     } }</pre>	<pre>int binarysearch(int a[], const int x, const int n){     int left = 0, right = n - 1;     while (left &lt;= right) {         int middle = (left + right) / 2;         if (x &gt; a[middle])             left = middle + 1;         else if (x &lt; a[middle])             right = middle - 1;         else return middle;     }     return -1; }</pre>

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## PART 2. Computer Organizations

Multiple choice question. (50%. For each, 5 point for right answer, 0 point for blank, -3 point for wrong answer)

- (1) The basic performance equation is

$$CPU\ time = Instruction\ count \times CPI \times Clock\ cycle\ time,$$

in which the factor Clock cycle time can be affected by

- (a) Machine language.  
(b) Cycles per instruction.  
(c) Instruction level parallelism.  
(d) Instruction set architecture.

IL CPI CCT  
software hardware  
ISA

- (2) A program  $P$  runs in 20 seconds on computer A, which has a 2 GHz clock rate. We try to build a computer B, that will run the program  $P$  in 10 seconds. We have determined that a substantial increase in the clock rate is possible, but this increase will cause computer B to require 1.5 times as many clock cycles as computer A for the program  $P$ . What clock rate should the computer B have?

- (a) 4 GHz  
(b) 6 GHz  
(c) 8 GHz  
(d) 10 GHz

0.5ns

A: 20s,  $\frac{20}{0.5 \times 10^{-9}} = 40 \times 10^9$  clock

B: 10s,  $\frac{10}{x \times 10^{-9}} = 1.5 \times 40 \times 10^9$  clock

$\frac{10}{x} = 200 \quad (x = \frac{1}{8})$

clock  
IL CPI CCT  
IL

- (3) About the addressing mode, which of the following statements is false?

- (a) PC-relative addressing, where the desired operand is at the memory location whose address is the sum of the PC and a constant in the instruction.  
(b) Register indirect addressing, where the instruction contains the number of a register that contains the memory address of the desired operand.  
(c) Immediate addressing, where the desired operand can be fetched from the instruction cache immediately.  
(d) Base or displacement addressing, where the desired operand is at the memory location whose address is the sum of a register and a constant in the instruction.

不用抓 register 在指令裡

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- (4) Below is the outcome of a branch during the program execution, where T for taken and N for not taken.

T-T-N-T-T-N-T

What's the prediction result for a 2-bit predictor initialized to weakly predict not taken?

- (a) 3 right, 4 wrong  
(b) 4 right, 3 wrong  
(c) 5 right, 2 wrong  
(d) 6 right, 1 wrong

T	T	N	T	T	N	T
01	10	11	00	01	10	11
X	✓	X	✓	✓	X	✓

- (5) Suppose we have a processor with a clock rate of 2 GHz, and a base CPI of 1.0 if all references hit in the primary cache. Assume a main memory access time of 100ns, including all the miss handling. If the miss rate per instruction at the primary cache is 2%, what's the total CPI?

- (a) 2.0  
(b) 3.0  
(c) 4.0  
(d) 5.0

$$1 + \frac{2}{100} \times 200 = 5$$

- (6) About the reservation station, which of the following statements is true?

- (a) The buffer within a functional unit that holds the operands and operation.  
(b) A small memory that is indexed by the lower portion of the address of the branch instruction and that contains one or more bits indicating whether the branch was recently taken or not.  
(c) The buffer that holds results in a dynamically scheduled processor until it is safe to store the results to memory or a register.  
(d) A table that keeps track of recently used address mappings to avoid an access to the page table.

- (7) Assume a cache has 64K words, block size is 8-word, and word size is 4-byte. For a 32-bit address, what's the tag length in case of 8-way set associative.

- (a) 15-bit  
(b) 16-bit  
(c) 17-bit  
(d) 18-bit

$$2^{16} = 2^3 \times 2^{13} \text{ Block} \quad 2^{13} = 2^3 \times 2^{10} \text{ set}$$

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(8) The simplest SOP expression for the function  $f(x_1, x_2, x_3) = \sum m(1, 2, 3, 5)$  is

- B
- (a)  $x_1\bar{x}_2 + \bar{x}_1x_3$
  - (b)  $\bar{x}_1x_2 + \bar{x}_2x_3$
  - (c)  $\bar{x}_1x_2 + x_1\bar{x}_3$
  - (d)  $\bar{x}_1x_2 + x_1\bar{x}_2$

(9) Which statement is not the key feature of write-back used in the cache?

- D
- (a) Individual words can be written by the processor at the rate that the cache, rather than the memory, can accept them.
  - ✓ (b) Multiple writes within a block require only one write to the lower level in the hierarchy.
  - ✓ (c) When blocks are written back, the system can make effective use of a high-bandwidth transfer, since the entire block is written.
  - (d) When blocks are written back, the write allocate policy is usually used to improve the write performance.

(10) Assume that the operation times for the major functional units are the following:

>Memory units (read or write): 200 ps

>ALU and adders: 100ps

>Register file (read or write): 50ps

Please compute the total execution time for the instruction class: R-type, Load word, and Jump.

- D
- (a) 550ps, 600ps, 350ps
  - (b) 450ps, 650ps, 350ps
  - (c) 450ps, 500ps, 250ps
  - (d) 400ps, 600ps, 200ps

Handwritten calculations:

$$200 + 50 + 100 + 50 = 400$$

$$200 + 100 + 50 + 200 + 50 = 600$$