

國立中興大學 112 學年度碩士班招生考試試題

科目：計算機組織與作業系統

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請於答案卡上作答，否則不予計分。

本科目不得使用計算機

本科目試題共 6 頁

共有 25 題，每一題都是單選題，每題 4 分，答錯則該題倒扣 1 分。

1. Consider the following page reference string:
1, 2, 3, 4, 2, 1, 5, 6, 2, 1, 2, 3, 7, 6, 3, 2, 1, 2, 3, 6.
For the LRU replacement algorithm, how many times does the page fault occur? Assume that there are three page frames in the physical memory. Besides, assume that all frames are initially empty, so your first unique pages will all cost one fault each.
A. 11
B. 12
C. 13
D. 14
E. 15
2. Continued from above question, how many page faults would occur for the optimal replacement algorithms, again assuming there are three page frames in the physical memory? And all frames are initially empty.
A. 11
B. 12
C. 13
D. 14
E. 15
3. Followings are statements about differences/relationship between system calls and APIs. Which statement is wrong?
A. APIs provides a wrapper for system calls.
B. Actual system calls can often be more detailed to work with than the APIs
C. APIs provide more program portability than system calls
D. The former is a function definition that specifies how to obtain a given service, while the latter is an explicit request to the kernel made via a software interrupt.
E. System calls and APIs are one-to-one mapping.
4. Following statements are about local variables. Which statement is wrong?
A. They make efficient use of memory because their storage space is dynamically allocated and can be released.
B. They can only be accessed inside the function that declares it.
C. They are created in the stack segment.
D. The same local variable name can appear in two different procedures.
E. Threads in the same process can share the local variables.

5. Which statement is wrong?
- A. The page table is often kept in memory. As a result, two memory accesses are needed to access a byte. The standard solution to this problem is to use a special hardware cache, called a translation look-aside buffer, so that we may bypass the page table lookup in memory.
 - B. If a translation look-aside buffer does not have an address-space identifier (ASID) in each entry, using translation look-aside buffer may increase the context switch time since the content must be saved and restored when context switch occurs.
 - C. If you want to set a file as memory-mapped, you must invoke the *mmap()* system call.
 - D. The implementation of system calls relies on a special instruction that could trigger a trap.
 - E. Inverted page tables often require that an address-space identifier be stored in each entry of the page table.
6. Which statement is wrong?
- A. To support demand paging, we must have the valid/invalid bit in each page table entry.
 - B. The valid/invalid bit is set by MMU and looked up by the OS.
 - C. To eliminate the page fault overhead, each page table entry can be associated with a dirty bit. If the dirty bit is clear, the page can be directly replaced without paging out.
 - D. The dirty bit is set by MMU and looked up by the OS.
7. 如果我們要求程式中某一個變數其起始位址必須為 4 的倍數，請問實現此一要求的技術被稱為？
- A. Alignment
 - B. Binding
 - C. Linking
 - D. Spooling
 - E. None of above
8. Several processes access the same data concurrently and the result of the execution depends on the particular order in which the access takes places. We call this as ____
- A. Critical section
 - B. Race condition
 - C. Mutually exclusive
 - D. Writing ordering
 - E. None of above
9. Which statement is wrong?
- A. Traps are triggered by CPU or by external devices
 - B. Interrupts are triggered by external devices
 - C. Applications can invoke a trap but cannot trigger an interrupt
 - D. Page fault is a kind of traps.
10. Which statement is wrong?
- A. Using semaphore as the synchronization mechanism does not allow context switches during critical sections.
 - B. Usually, each process has an associated page table. In contrast, only one inverted page table is in the system.
 - C. Read ahead and free behind are useful for sequential accesses.
 - D. Process Control Block (PCB) or Thread Control Block (TCB) are kernel data structures for keeping processes or threads' information.

11. Which statement is incorrect?
- A. Both polling and interrupts usually associates with context switches.
 - B. If the I/O device is ready for service, polling can be much more efficient than is catching and dispatching an interrupt.
 - C. Using interrupts may increase the CPU cache miss rates comparing with polling. This is because, upon interrupts, the CPU must jump to the OS to execute the interrupt service routine and then other processes, if the scheduler schedules other processes for running. As a result, the cache must re-populate with the data/code of the interrupt service routine or other processes.
 - D. When an interrupt occurs, CPU jumps to the OS, asking OS to serve the interrupt. Usually, OS must first save the state of the interrupted process.
12. Consider a process that uses a user level threading library to spawn 20 user level threads. The library maps these 20 user threads onto 10 kernel threads. The process is executing on an 8-core computer. What is the maximum number of user threads of the process that can be executed in parallel?
- A. 20
 - B. 10
 - C. 8
 - D. 1

13. The following code is shown to you:

```
int main(int argc, char *argv[]) {  
    printf("a");  
    fork();  
    printf("b");  
    return 0;  
}
```

Assuming *fork()* succeeds and *printf()* prints its outputs immediately (no buffering occurs), what are possible outputs of this program?

- A. a
 - B. ab
 - C. abb
 - D. aabb
 - E. abbb
14. Regarding the DMA, how many of the following statement is/are true?
- [1] The CPU isn't concerned with the time DMA takes to transfer the data.
 - [2] DMA controller would complete the memory bus with CPU, called cycle stealing, for transferring data to/from memory.
 - [3] The CPU can start a DMA block transfer, and do other work in parallel with the DMA operation.
 - [4] DMA can offload expensive memory operations, such as large copies or scatter-gather operations, from the CPU to a dedicated DMA engine.
- A. 0
 - B. 1
 - C. 2
 - D. 3
 - E. 4

15. Which statement is wrong?
- A. Pipeline improves throughput but cannot improve instruction latency.
 - B. A left shift instruction can replace an integer multiply by a power of 2.
 - C. Forwarding resolves data hazard by adding extra hardware to retrieve the missing item early from the internal resources.
 - D. Capacity misses is caused by the first access to a block that has never been in the cache.
16. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. Which processor has the highest performance expressed in instructions per second?
- A. P1
 - B. P2
 - C. P3
 - D. All the same
17. What is the decimal value of this 32-bit two's complement number?
1111 1111 1111 1111 1111 1111 1111 1100
- A. -4
 - B. -8
 - C. -2
 - D. -1
18. When a planned instruction cannot execute in the proper clock cycle because the hardware does not support the combination of instructions that are set to execute. We call this as _____
- A. Structural hazard
 - B. Data hazards
 - C. Control hazard
 - D. Branch hazard
19. Programs exhibit the tendency to reference data items that are close to other recently accessed items. We call this as _____
- A. Temporal locality
 - B. Spatial locality
 - C. Interleaved executions
 - D. Working set model.
20. A cache that has a fixed number of locations (at least two) where each block can be placed. We call this as _____
- A. Fully associative cache
 - B. Direct mapped cache
 - C. Set-associative cache
 - D. Multi-level cache

21. Figures 1 and 2 show two programs, programs A and B. How many "k" will be printed on the screen?

```
int global_var = 10 ;
int main(){
    int local_var = 20;
    if(fork()==0){
        execlp("./b.sh", "5", NULL);
        local_var++;
        fork();
    }
    wait(NULL);
    if(fork()==0){
        fork();
        fork();
    }
    printf("k\n");
    return 0;
}
```

Figure 1. Program A

```
#!/bin/sh

echo "$0"
```

Figure 2. Program A

- A. 1.
 - B. 2
 - C. 3
 - D. 4
 - E. 5
22. Continued from the above question, in addition to a number of *k*, what will be printed on the screen after the execution of program A?
- A. ./b.sh
 - B. 5
 - C. \$0
 - D. 0
 - E. 1
23. Continued from the above question, after the execution of the program A, what's the value of *local_var* variable in A?
- A. 20.
 - B. 21
 - C. 22
 - D. 23
 - E. 24
24. Followings are statements about handling writes. Which statement is wrong?
- A. Write through scheme always updates both the cache and the next lower level of the memory hierarchy.
 - B. Write back scheme updates values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.
 - C. Write through scheme ensures that data is always consistent between the cache and memory.
 - D. Write back scheme can use a write buffer to improve the performance. A write buffer stores the data while it is waiting to be written to memory. After writing the data into the cache and into the write buffer, the processor can continue execution.

25. Assume that a computer is an 8-bit computer (i.e., the logical address length is 8 bits). A computer with 32 bytes of physical memory uses paging as its memory management scheme. Suppose the size of page is 4 bytes. The page table is shown as follows.

0	5
1	6
2	1
3	2

Which statement is wrong?

- A. If logical address is 00001101, the page number is 3 and the page offset is 1
- B. If logical address is 00000000, the page number is 0 and the page offset is 0
- C. If logical address is 00001011, the corresponding physical address is 7
- D. If logical address is 00000101, the corresponding physical address is 21