## 4.3 EM78P520NL48

| Pin | Pin No. | I/O Type | Description |
|---|---|---|---|
| P70~P77 | 1~4, 39~42 | I/O | 8-bit bidirectional I/O pins.<br>P70 ~ P73 are pin-shared with SEG12 ~ SEG15, respectively.<br>P74 is pin-shared with external Interrupt 0 or SEG18.<br>P75 is pin-shared with external Interrupt 1 or T1OUT or PWM1.<br>P76 is pin-shared with external Interrupt 2 or T1CK.<br>P77 is pin-shared with external Interrupt 3 or T1CAP. |
| P81~P87 | 12~18 | I/O | 7-bit bidirectional I/O pins.<br>P81 is pin-shared with RESET pin.<br>P82 is pin-shared with Interrupt 8 or AD8 input.<br>P83 is pin-shared with COM7 or Interrupt 9 or AD7 input.<br>P84 is pin-shared with A/D reference input pin.<br>P85 is pin-shared with COM6 or AD6 input.<br>P86 is pin-shared with COM5 or AD5 input.<br>P87 is pin-shared with COM4 or AD4 input. |
| P90~P97 | 19~26 | I/O | 8-bit bidirectional I/O pins.<br>P90 is pin-shared with AD3 input or PWM2.<br>P91 is pin-shared with AD2 input or BUZ.<br>P92 ~P93 are pin-shared with AD1 ~ AD0 input, respectively.<br>P94 ~P97 are pin-shared with COM3 ~ COM0, respectively. |
| PA0~PA7 | 27~34 | I/O | 8-bit bidirectional I/O pins.<br>PA0 ~ PA3 are pin-shared with SEG0 ~ SEG3, respectively.<br>PA4 is pin-shared with SEG4 or SPI SI pin.<br>PA5 is pin-shared with SEG5 or SPI SO pin.<br>PA6 is pin-shared with SEG6 or SPI SCK pin.<br>PA7 is pin-shared with SEG7 or SPI /SS pin. |
| PB0~PB7 | 35~38, 43~46 | I/O | 8-bit bidirectional I/O pins.<br>PB0 is pin-shared with SEG8 or external Interrupt 4 or AD9 input.<br>PB1 is pin-shared with SEG9 or external Interrupt 5 or AD10 input.<br>PB2 is pin-shared with SEG10 or external Interrupt 6 or AD11 input.<br>PB3 is pin-shared with SEG11 or external Interrupt 7.<br>PB4 is pin-shared with SEG16 or UART RX pin.<br>PB5 is pin-shared with SEG17 or UART TX pin.<br>PB6 ~ PB7 are pin-shared with SEG19 ~ SEG20, respectively. |
| PC0~PC3 | 47~48 10~11 | I/O | 4-bit bidirectional I/O pins.<br>PC0 ~ PC1 are pin-shared with SEG21 ~ SEG22, respectively.<br>PC2 ~PC3 are pin-shared with Xin ~ Xout, respectively. |
| OSCI | 8 | I | Crystal mode: crystal input<br>RC mode: pull-high resistor<br>PLL mode: connect 0.01μF capacitance to GND.<br>Connect 0.01μF capacitor to GND and code option select PLL mode when high oscillator is not used. |
| OSCO | 7 | O | Crystal mode: crystal output<br>RC mode: instruction clock output |
| Test | 9 | I | Test signal import pin (must be connected to VDD) |
| Xin | 10 | I | Crystal mode: input pin for sub-oscillator. Connect to a 32.768kHz crystal.<br>RC mode: pull-high resistor |
| Xout | 11 | O | In crystal mode: connect to a 32.768kHz crystal. |
| /RESET | 12 | I | Input pin with Schmitt Trigger. If this pin remains at logic low, the controller will also remain in rest condition. |
| VDD | 5 | I | Power supply pin |
| VSS | 6 | I | System ground pin |

**Note:** When using common pin I/O and LCD (P70~74, P83, P85~87, P94~97, PA0~A7, PB0~B7 and PC0~C1), it is recommended to use a circuit sink.

# 5 Block Diagram

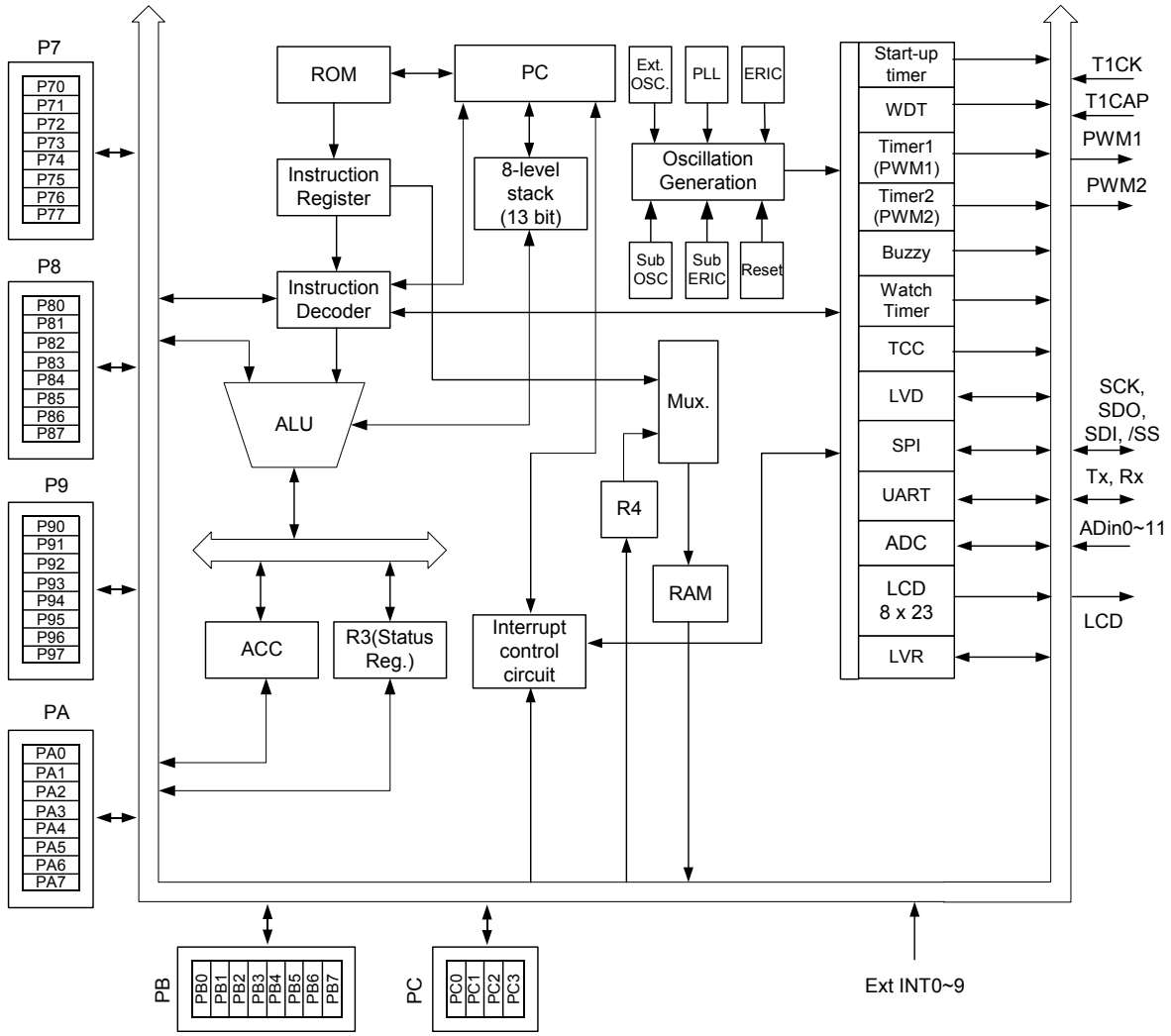


*Figure 5 EM78P520N Block Diagram*

# 6 Function Description

## 6.1 Register Configuration

### 6.1.1 R PAGE Register Configuration

| Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 | Bank 6 |
|---|---|---|---|---|---|---|
| R0 (IAR) | | | | | | |
| R1 (TCC) | | | | | | |
| R2 (PC) | | | | | | |
| R3 (SR) | | | | | | |
| R4 (RSR) | | | | | | |
| RBSR | LCDCR | T1CR | URC | LEDDCR | Reserve | Reserve |
| Reserve | LCDAR | TSR | URS | WBCR | URC2 | LVRCR |
| PORT7 | LCDBR | T1PD | URRD | IOC7 | P7PHCR | P7ODCR |
| PORT8 | LCDVCR | T1TD | URTD | IOC8 | P8PHCR | P8ODCR |
| PORT9 | LCDCCR | T2CR | ADCR | IOC9 | P9PHCR | P9ODCR |
| PORTA | LCDSCR0 | T2PD | ADICH | IOCA | PAPHCR | PAODCR |
| PORTB | LCDSCR1 | T2TD | ADICL | IOCB | PBPHCR | PBODCR |
| SCCR | LCDSCR2 | SPIS | ADDH | IOCC | PCPHCR | PORTC |
| TWTCR | Reserve | SPIC | ADDL | Reserve | Reserve | Reserve |
| IMR | EIMR | SPIR | EIESH | Reserve | Reserve | Reserve |
| ISR | EISR | SPIW | EIESL | WKCR | Reserve | Reserve |
| R10 | | | | | | |
| . | | | | | | |
| . | | | | | | |
| R1F | Bank 1 . . . . . | | | Bank 7 | | |
| R20 | General Purpose RAM | | | R20 | | |
| . | . | | | . | | |
| . | . | | | . | | |
| . | . | | | . | | |
| R3F | . | | | R3F | | |

*Figure 6-1 Data Memory Configuration*

## 6.2 Register Operations

### 6.2.1 R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

### 6.2.2 R1 (TCC)

Incremented by the main oscillator clock (Fm) or sub oscillator clock (Fs) (controlled by TWTCR register). Written and read by the program as any other register.

### 6.2.3 R2 (Program Counter)

The structure is depicted in Figure 6-2. Generates 8K × 13 on-chip ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

"CALL" instruction loads the low 10 bits of the PC and PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and contents of the ninth and tenth bits don't change.

"ADD R2, A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits don't change.

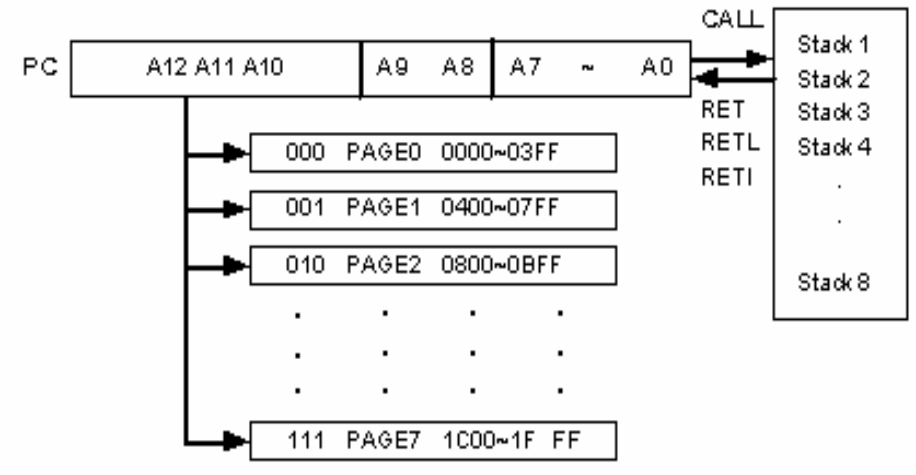


*Figure 6-2 Program Counter Organization*

User can use the Long jump (LJMP) or long call (LCALL) instructions to program user's code. And the program page is maintained by ELAN's compiler. It will change user's program by inserting instructions within the program.