EM198850AW

2.4GHZ Low Data Rate RF Transceiver

Application Note

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Outline

1. Description of Operation Mode

Operation Mode	Register Setting	CE (pin)	CSn (pin)	MOSI (pin)	MISO (pin)	IRQ (DR) (pin)
Power Down	Reference to the state machine of operation modes on P.12	0	X	SPI_{in}	SPI_{out}	
Idle		0	X	SPI_{in}	SPI_{out}	
Configuration		1	0	SPI_{in}	SPI_{out}	
Standby I		1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Buffered		1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
Standby II		1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Direct		1	1	SPI_{in}	SPI_{out}	$Data_{in}$
RX Buffered		1	1	SPI_{in}	$FIFO_{out}$	IRQ_{out}
RX Direct		1	1	SPI_{in}	SPI_{out}	$Data_{out}$

Configuration

When CSn=0 and CE = 1, the SPI interface may be activated to program the SPI register value.

Power Down Mode

When the pin CE sets to 0 and R0x00[0] sets to 1, EM198850AW is disabled with minimal current consumption. When entering the power down mode, EM198850AW is not active including voltage regulators and crystal block, and the values of the all registers are clear.

Idle

In Idle Mode, the contents of all registers are retained by internal power supply. It will reduce the initialization time on next start up.

Standby I

For Rx or Tx device, we can turn off all the RF blocks and mini Mac baseband system clock to save power consumption. Only regulator and Xtal buffer keep on to speed up start-up time.

TX Buffered Mode (BUF)

As a transmitter with the function of FIFO and packet handling

Standby II

Without any raw data input into the TX FIFO in TX Buffer Mode, the Tx device would stay at standby II mode. At this mode, regulator, Xtal buffer clock and mini Mac baseband system clock is available. No any start-up time is need.

TX Direct Mode (DR)

As a transmitter without the function of the FIFO and packet handling

RX Buffered Mode (BUF)

As a receiver with the function of FIFO and packet handling

RX Direct Mode (DR)

As a receiver without the function of the FIFO and packet handling

2. State Machine of Operation Mode

The Figure is the state machine of operation modes. The MCU can follow the register sequence to write SPI registers into the desired operation mode through digital SPI interface.

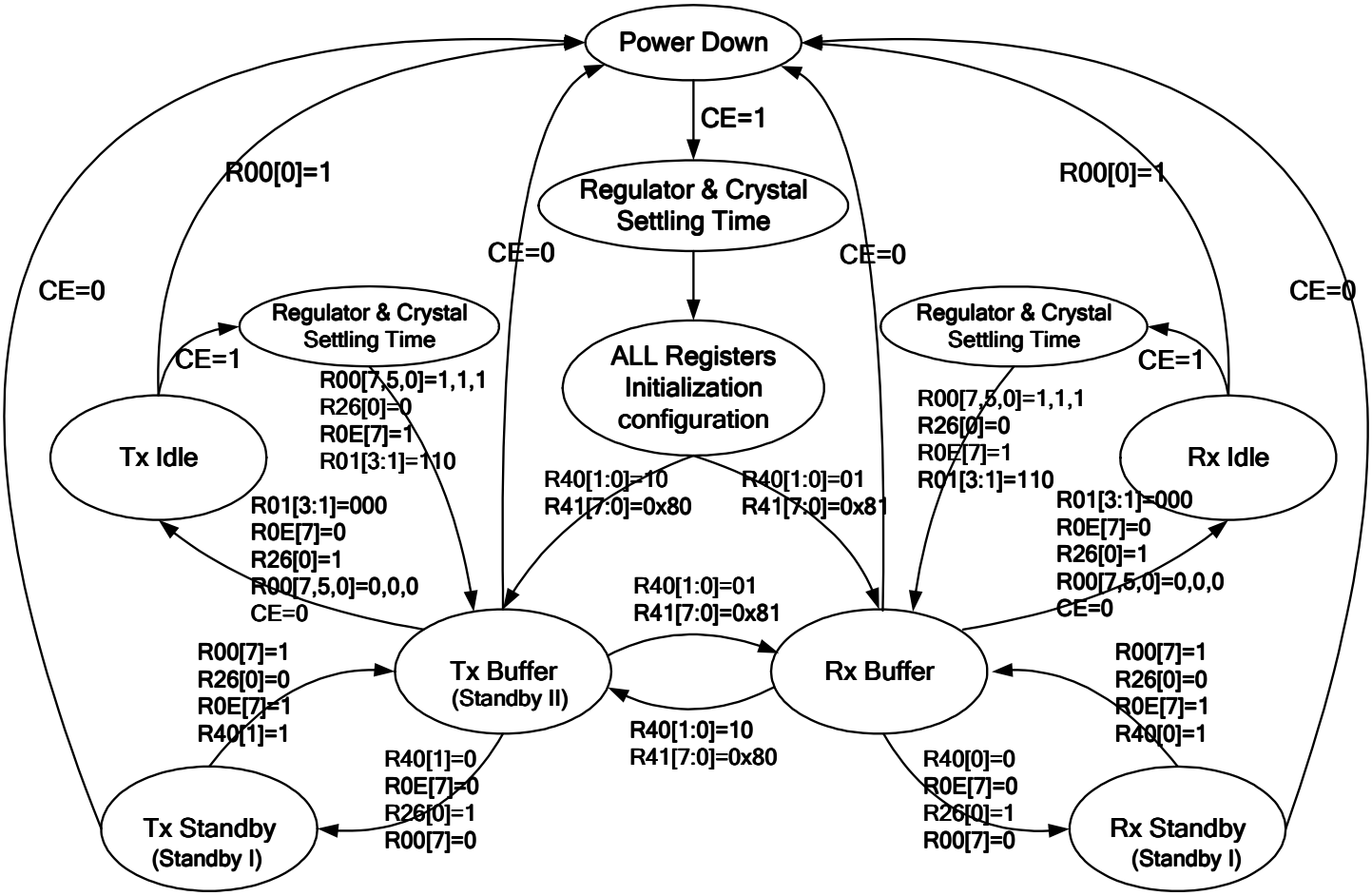


Figure 1 .EM198850AW state machine diagram

3. System Flowchart

- **Tx operation**

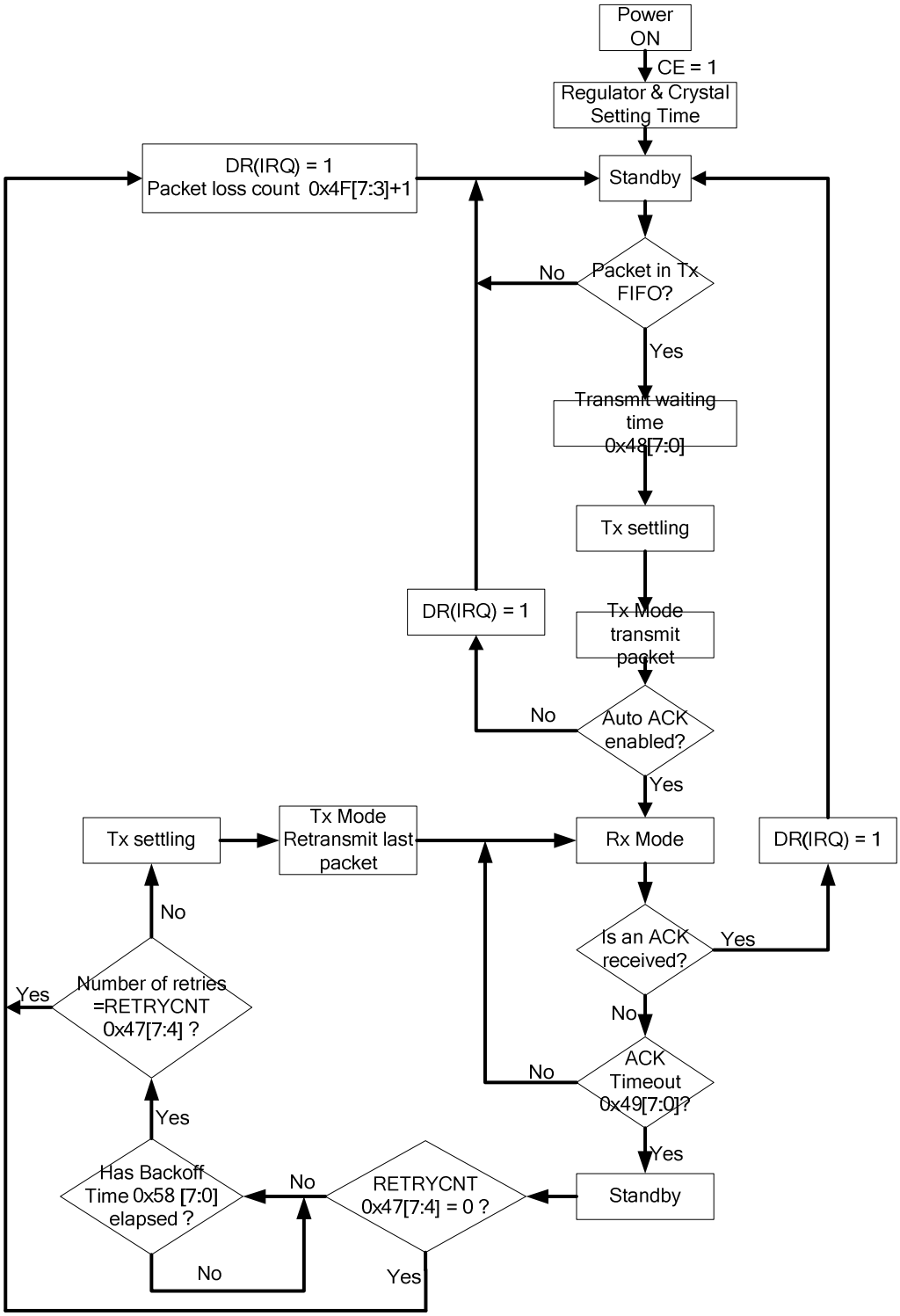


Figure 2 .Operation flowchart of Tx

If there is a packet present in Tx FIFO, the EM198850AW enters Tx Buffer mode and transmits the packet. If Auto ACK is enabled, the EM198850AW enters Rx mode to receive an ACK packet.

If the ACK packet is not received before timeout occurs, the EM198850AW returns to Tx standby II mode. It stay in Tx standby II mode until the Backoff Time(0x58[7:0]) has elapsed. If number of retransmits has not reached the ETRYCNT(0x47[7:4]), the EM198850AW start to transmit the last packet once more. When number of retransmits reach the maximum number, the EM198850AW assert DR(IRQ) and automatically add one to packet loss count(0x4F[7:3]) . EM198850AW return to standby II mode wait for next new packet input.

- **Rx operation**

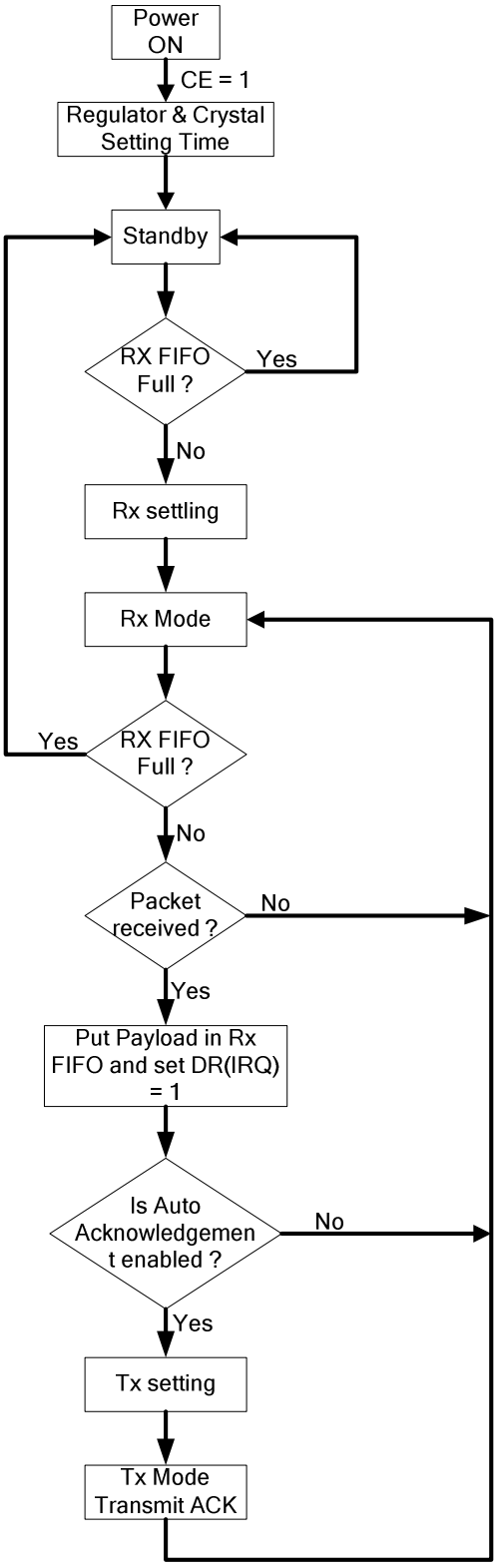
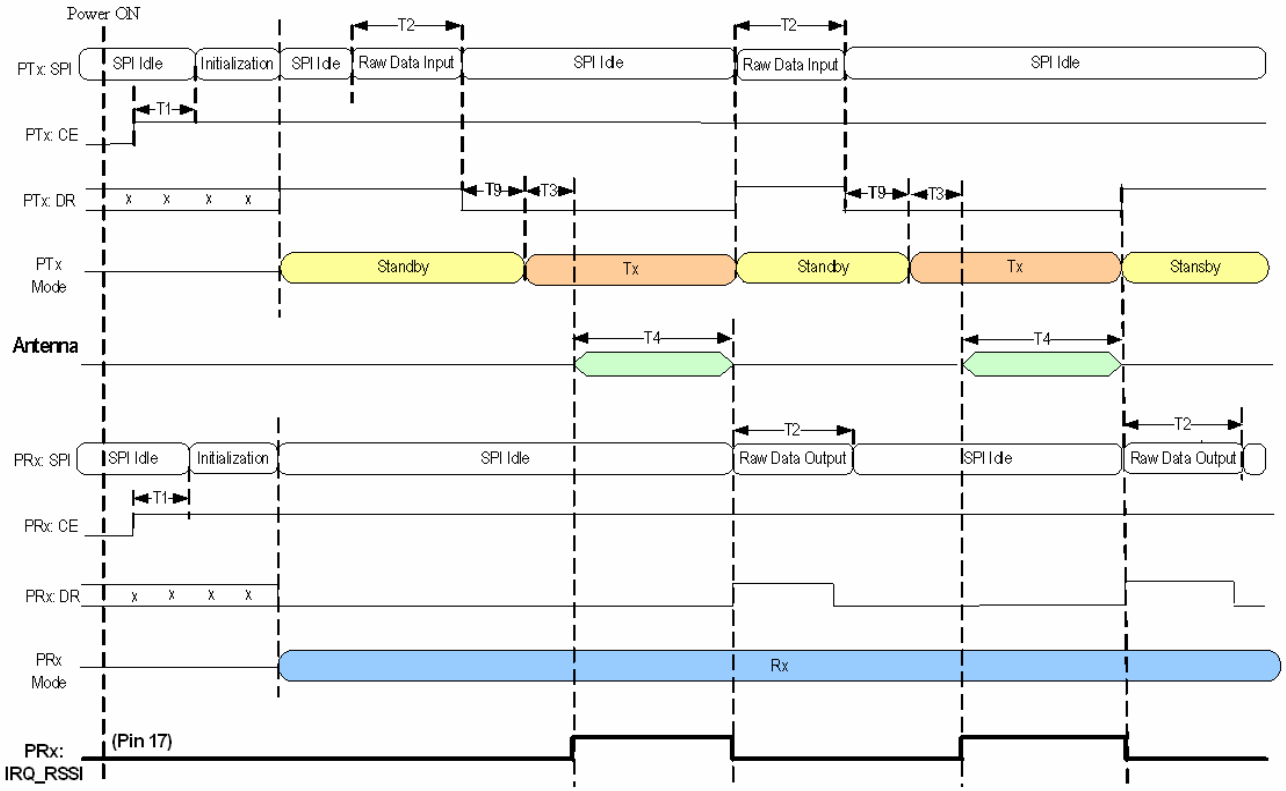


Figure 3 .Operation flowchart of Rx

If a packet is received from transmitter, the EM198850AW assert DR(IRQ) and put receive packet in Rx FIFO. If Auto ACK is enabled, the EM198850AW enters Tx mode to transmit an ACK packet. After ACK packet is transmitted, the EM198850AW return to Rx mode. When the FIFO is full, number of payload equal to PKTCNT, all the RF circuits will turn off automatically to save power consumption. RF circuits will turn on when the FIFO is not full.

- **RSSI operation in Rx**



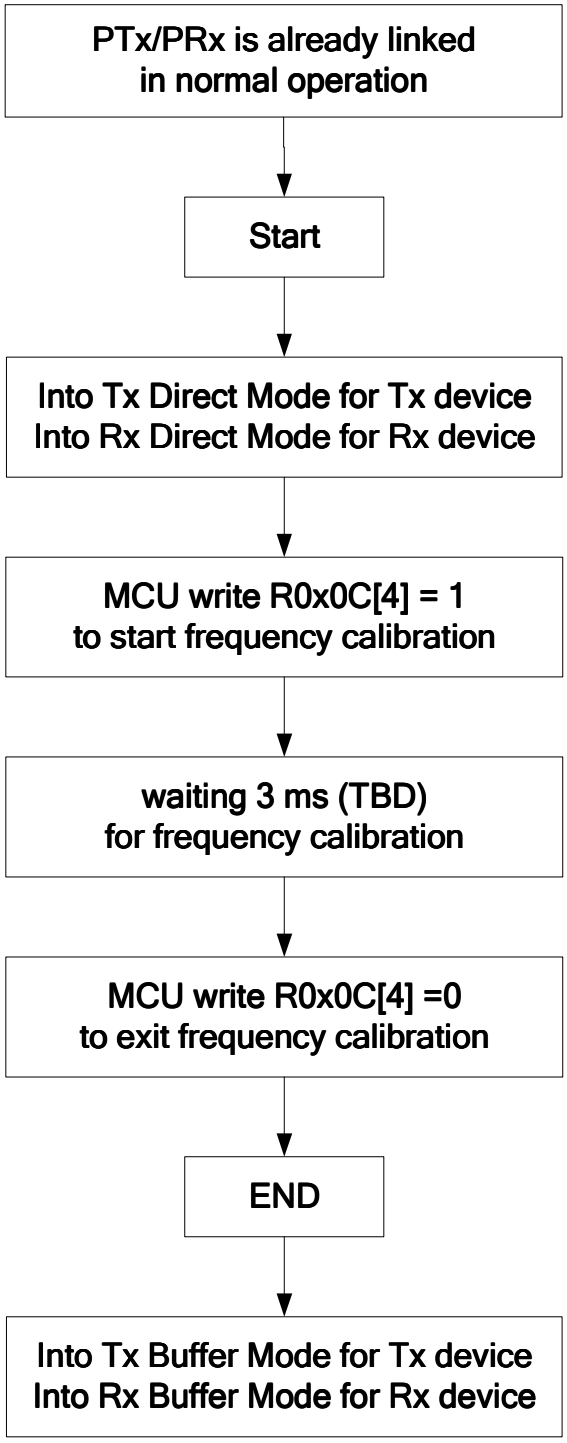
In Rx device, pin 17, sets as IRQ_RSSI, is high to indicate that it is available for the MCU to read the RSSI registers, R0x4B[5:0] through the SPI interface. RSSI values are only valid during receiving signal.

Xtal Frequency Offset Calibration

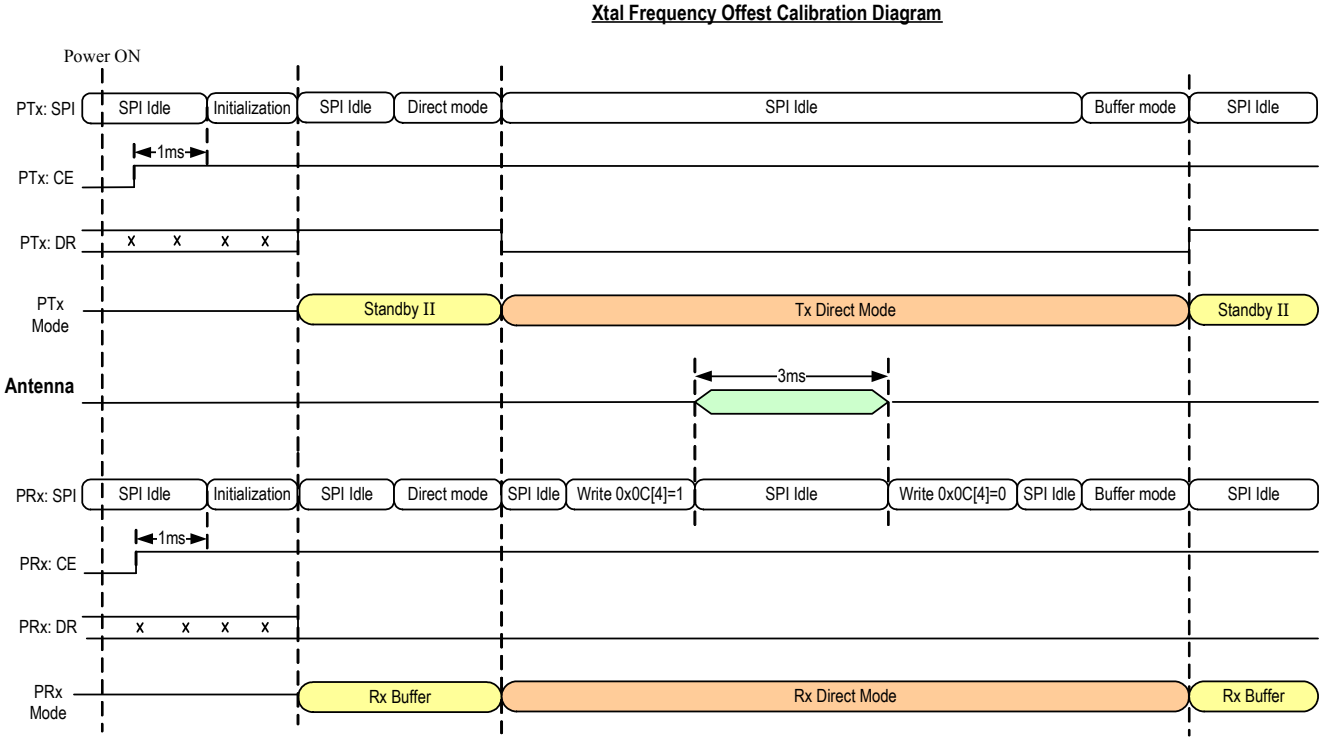
If the EM198850AW uses the external Xtal with internal oscillator to create the system clock, the EM198850AW provide the auto frequency tuning engine to fine the Xtal frequency.

Calibration Flow

1. Start
2. Set registers into Direct Mode
3. For Rx device, write R0x0C[4]=1 to start frequency calibration. For Tx device, it outputs a single carrier as reference frequency for Rx device
4. Waiting 3 msec for the timing of frequency calibration (TBD)
5. For Rx device, write R0x0c[4]=0 to finish the calibration flow
6. End
7. Recover to the normal operation mode



Xtal Frequency Offset Calibration Timing Diagram



Note: When the devices go into POWER DOWN mode, all the calibration result will be refreshed

4. Star Network

An EM198850AW configured as primary RX will be able to receive data through 6 different data pipes. A data pipe will have a unique address but share the same frequency channel. This means that up to 6 different EM198850AW configured as primary TX can communicate with one EM198850AW configured as RX, and the EM198850AW configured as RX will be able to distinguish between them. Only one data pipe can receive a packet at a time.

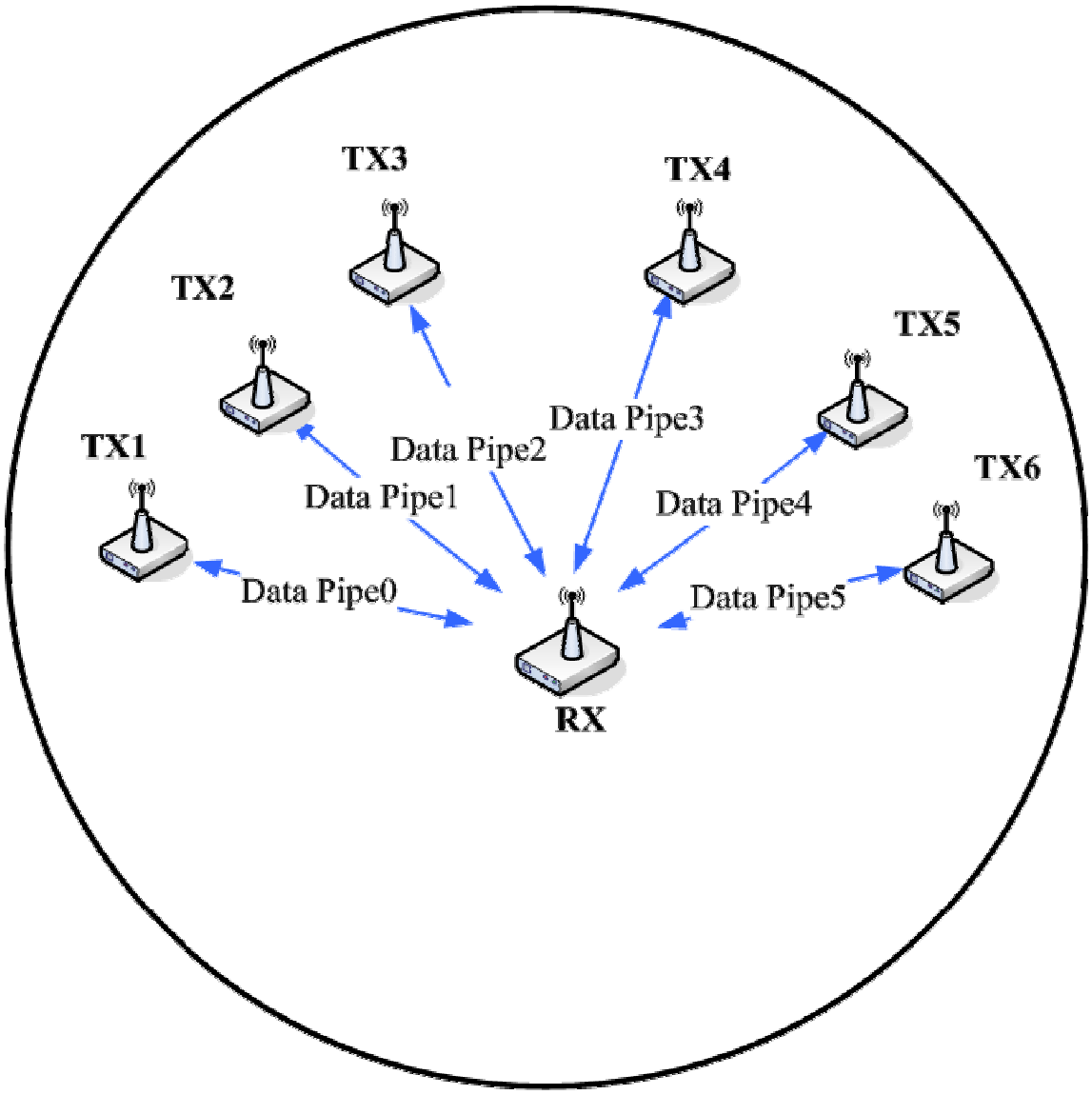


Figure 4 .EM198850AW in a star network Configuration

The following settings are common to all data pipes:

- Auto ACK enable
- STARTNET enable
- CRC encoding scheme
- Tx / Rx Address width
- Frequency channel
- Air data pipe
- RF data rate

The data pipes are enabled with the bits in the 0x41[5:0] register.

Each data pipe address is configured in the RXADR0 ~ RXADR5. Each data pipe can have up to 2 byte configurable address. Data pipe 0 has a unique 2 byte address. Data pipe 1~5 shares the 8 most significant address bits. Figure 5. is an example of how data pipes 0~5 are addressed.

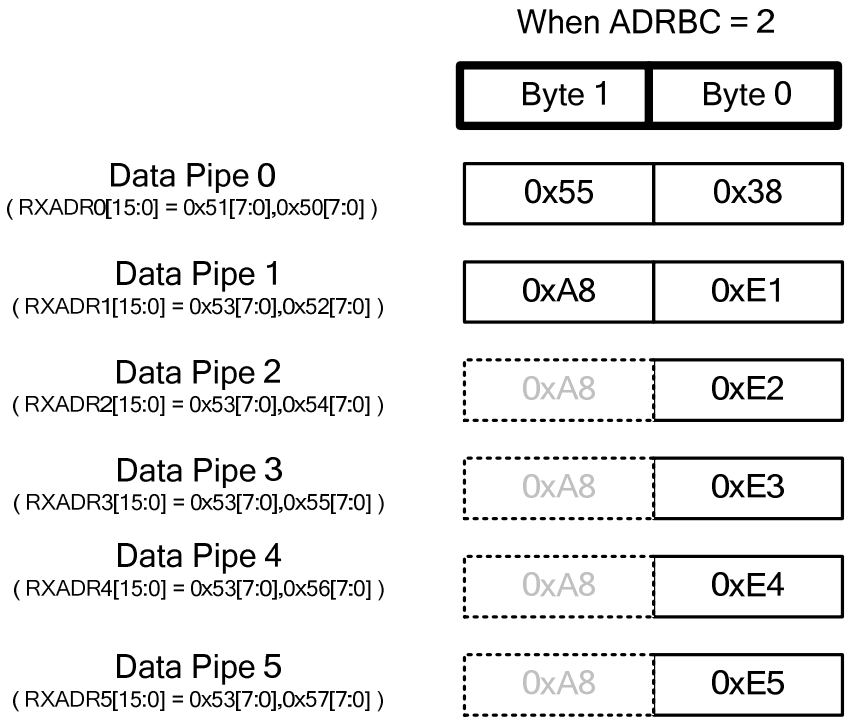


Figure 5 .Addressing Data Pipes 0~5

The Rx receives packet from more than one Tx. To ensure that the ACK packet from the Rx is transmitted to the correct Tx, the Rx takes the data pipe address where it received the packet and use it as the Tx address when transmitting the ACK packet. On the Tx device, the TXADR must be same as the RXADR0. On the Rx device, the RXADR0~RXADR5, defined as the data pipe address, must be unique. Figure 6. is an example of data pipe addressing for the Tx and Rx.

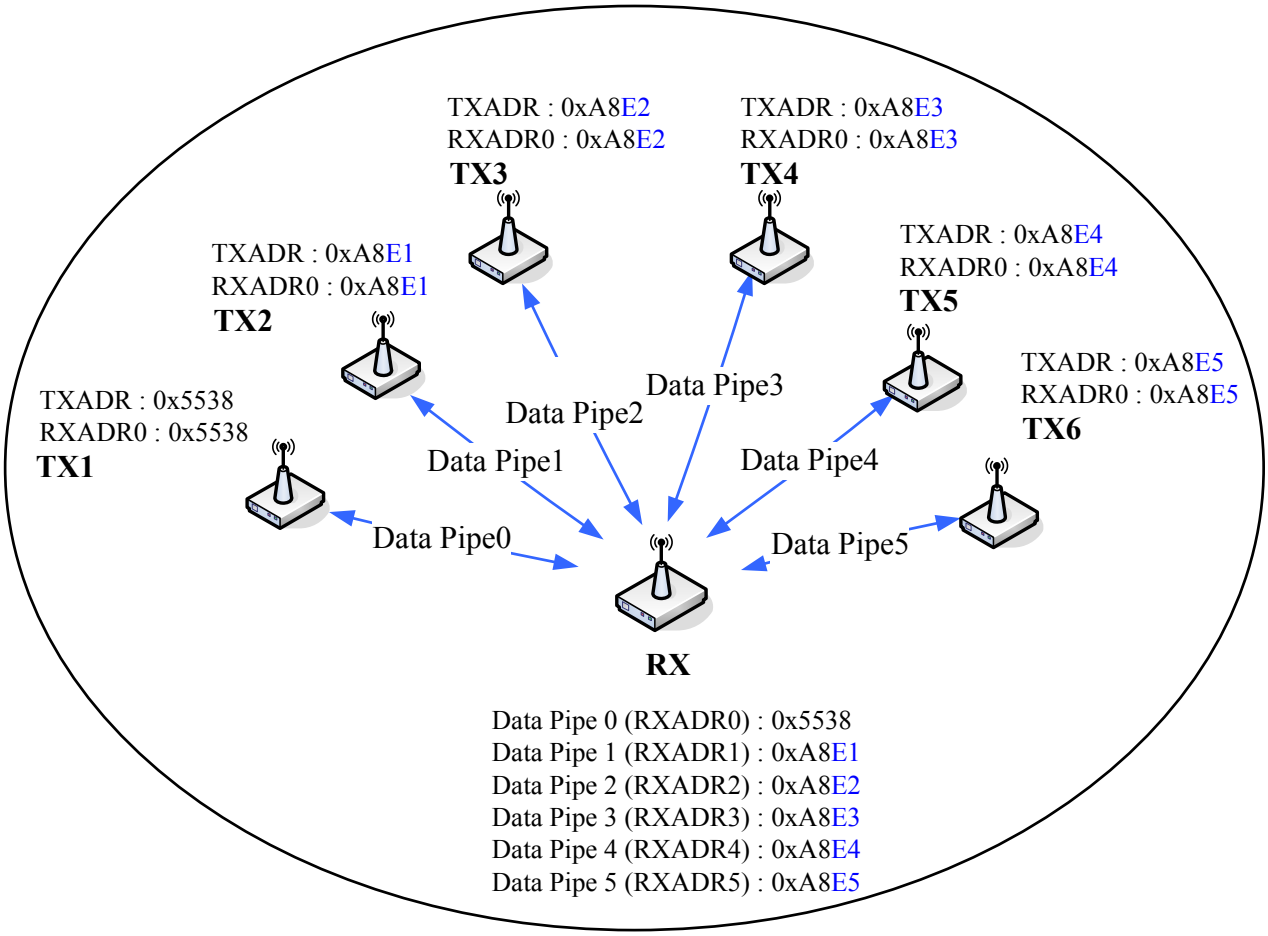


Figure 6 .Example of data pipe addressing

5. Frame-Structure

Data Frame-structure

sync	SOF	address	PID	payload	CRC

ACK Frame-structure

sync	SOF	address	PID	CRC

- **Sync: 4**-12 bytes (Default 4 bytes)
- **SOF:** Start of Frame (1byte)
- **Address:** Programmable byte length (1-2 Byte)
- **PID:** 1 byte

  When STARNET 0x40[7] is enabled, PID is adding to frame structure.

  When STARNET 0x40[7] is disabled, PID is removing from frame structure.

  Example:

  If STARNET 0x40[7] is enabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),

  → PID= 1 byte, the available payload = 3 bytes

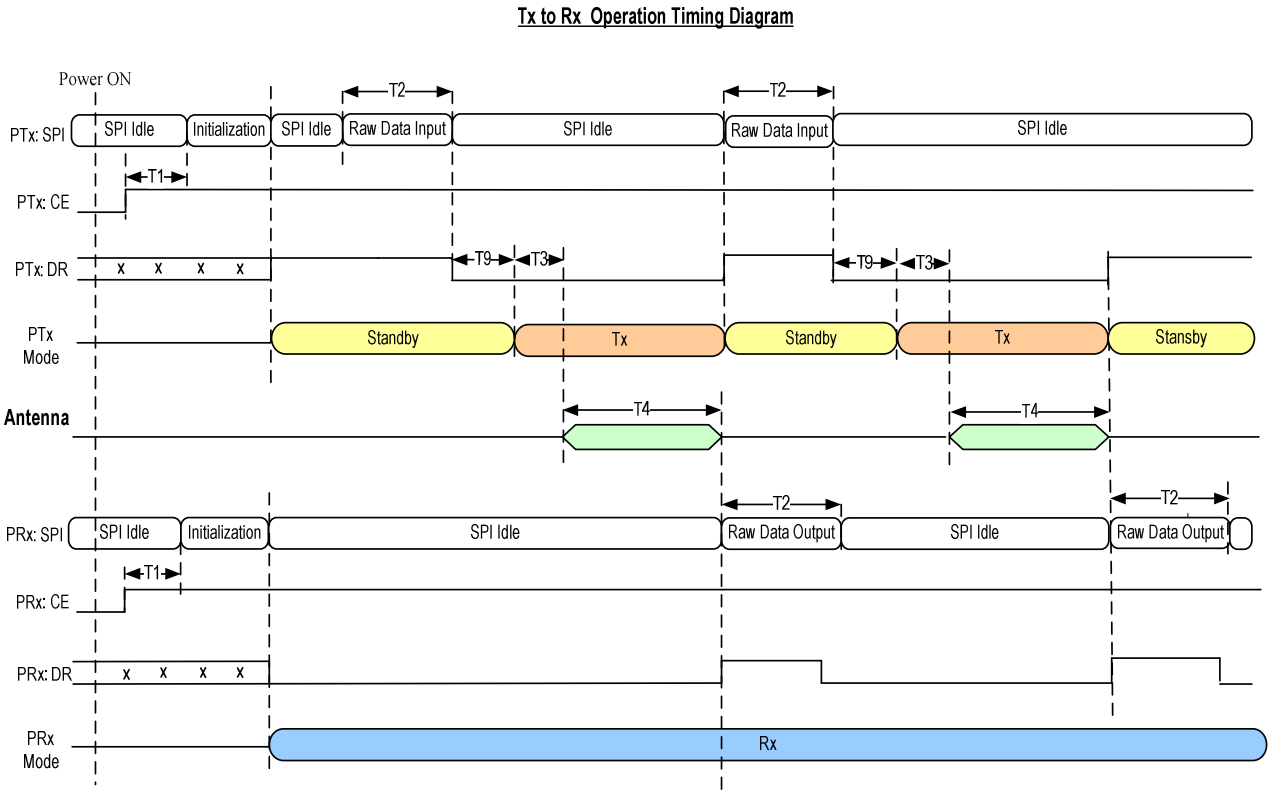
  If STARNET 0x40[7] is disabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),

  → PID= 0 byte, the available payload = 4 bytes

  - [7]: Packet type, auto generate by HW
    - 1'b0 : Data packet (needs ACK or not)
    - 1'b1: ACK packet
  - [6:4]: 000~101 Pipe data number, auto generate by HW
  - [3:0]: Packet sequence number, It is used by the Rx device to determine if a packet is new or retransmitted. It defined by user.
- **Payload:** Programmable byte length (1-64 Byte)
- **CRC:** Programmable length(0,1,2,4 Byte)

6. Operation Timing Diagram

Tx/Rx Link Operation Timing Diagram in Buffer Mode



Condition: Disable Auto ACK 0x40[3:2] = 00

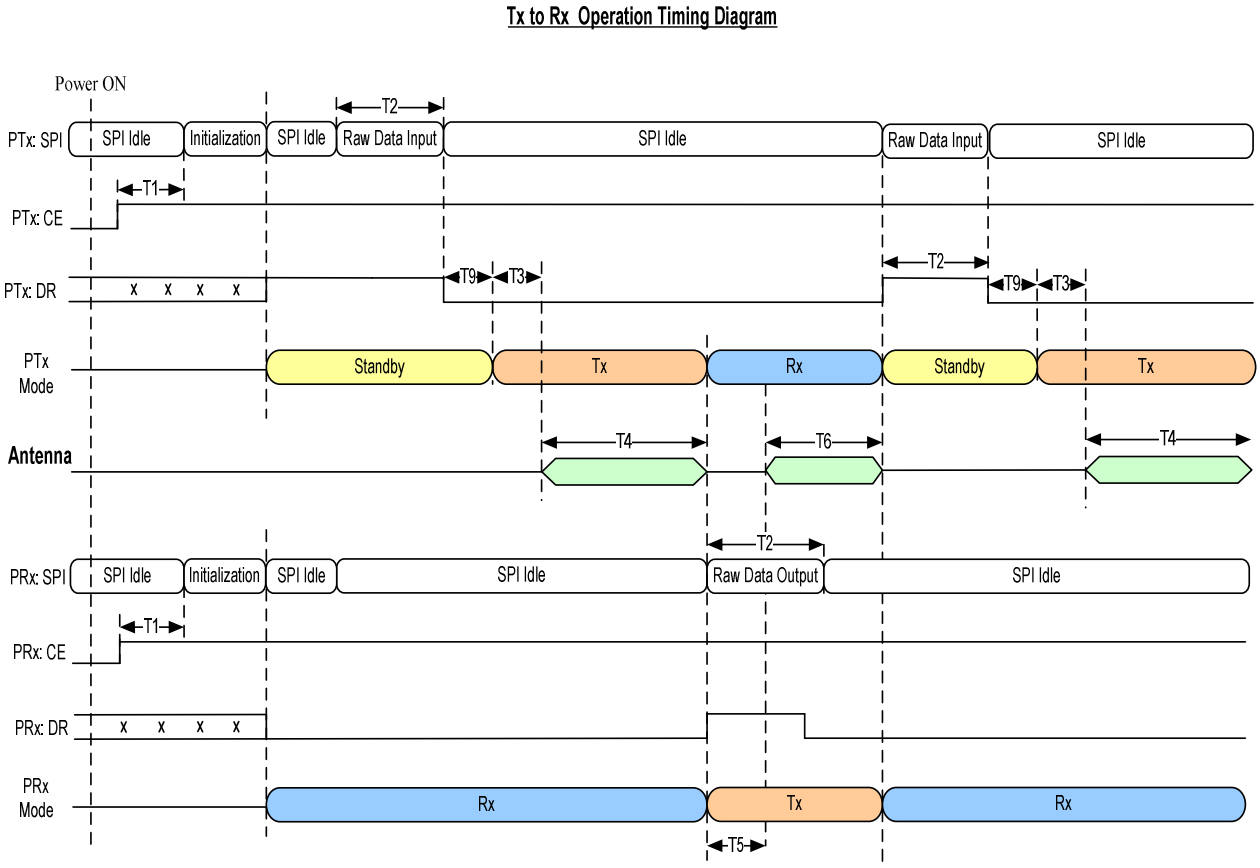
PKTCNT 0x45[7:4] = 0001

Enable RXEN0 0x41[5:0] = 000001

The PTx DR is asserted after the packet is transmitted by the PTX.

The PRx DR is asserted after the packet is received by the PRX.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode



Condition: Enable Auto ACK 0x40[3:2] = 11

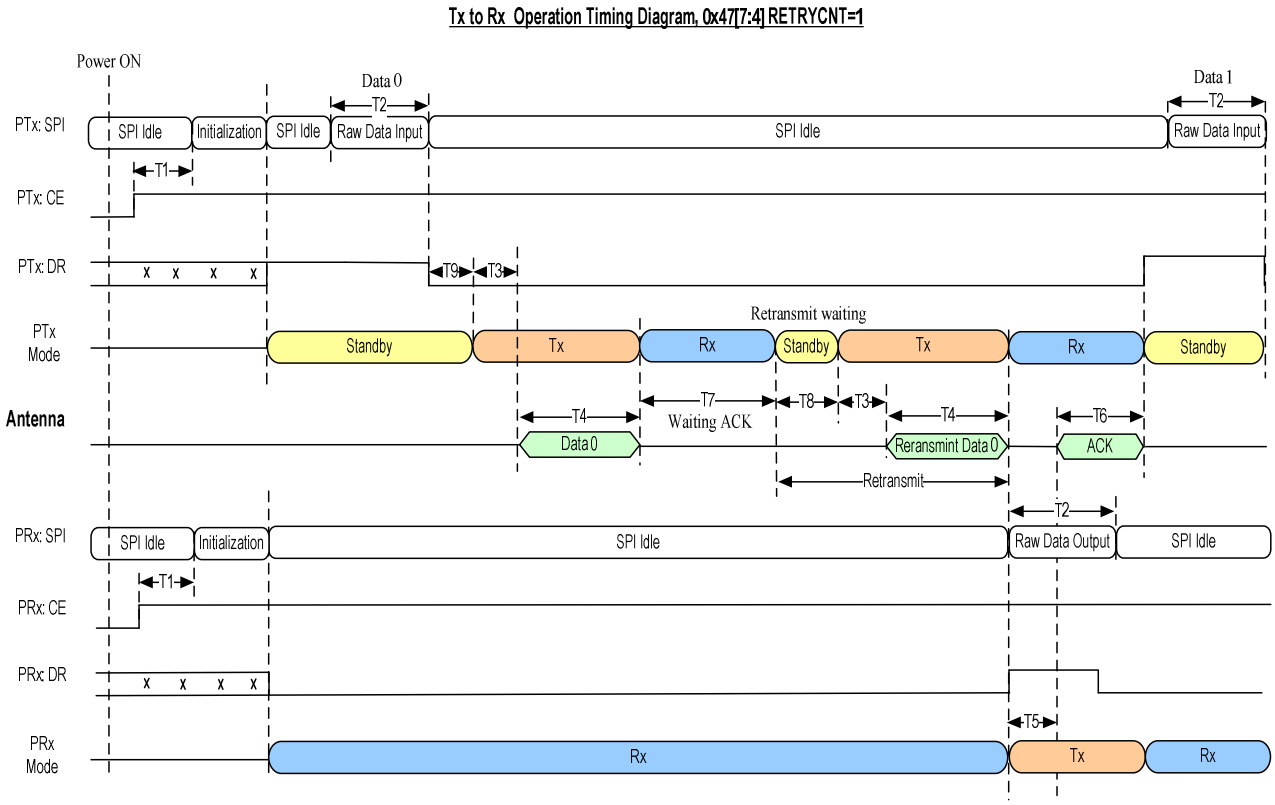
PKTCNT 0x45[7:4] = 0001

Enable RXEN0 0x41[5:0] = 000001

When the transmission ends the PTX device automatically switches to Rx mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to MCU. When the PRX device receives the packet it responds with an interrupt to MCU.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode

ACK Lost Condition: PTx transmits Data ➔ PTx doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTx receives ACK

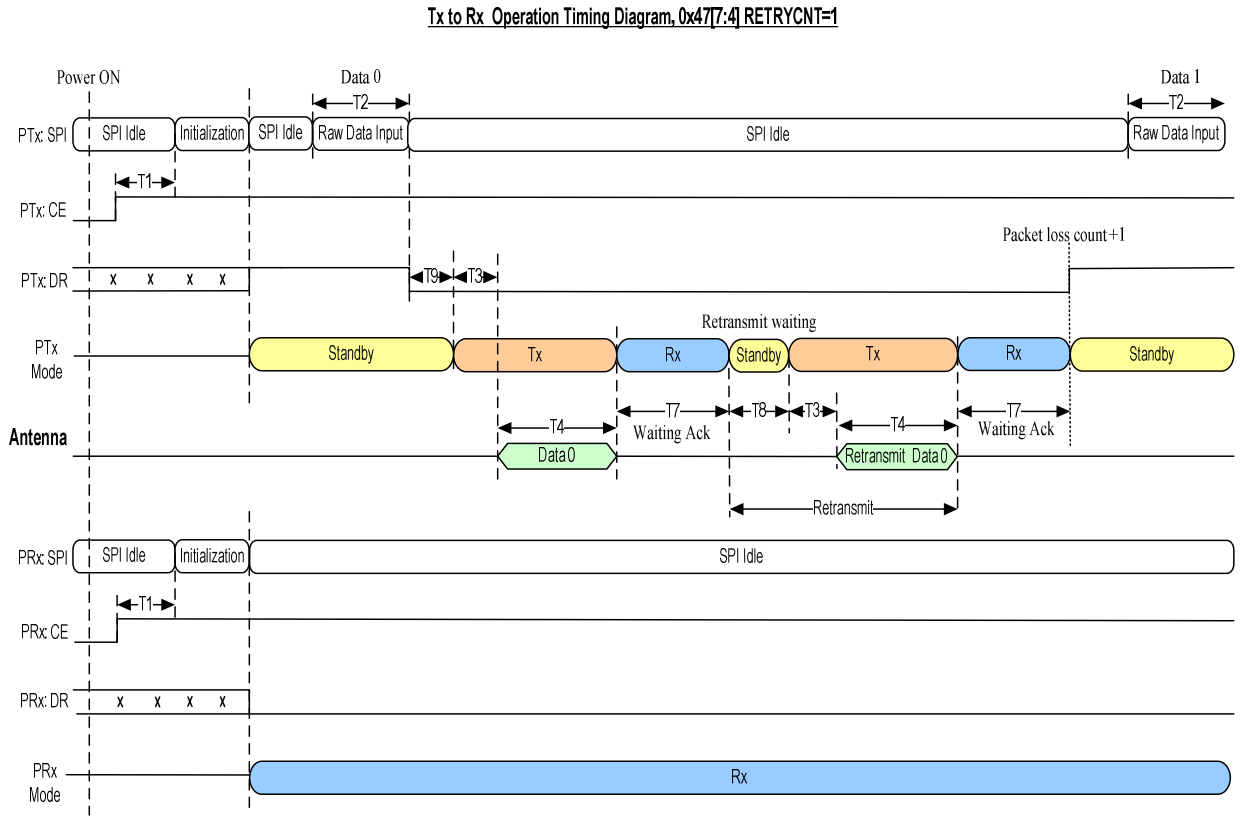


Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

After Data 0 is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits specified time for ACK packet (T7), if it is not in specified time slot, the PTX retransmit the Data 0. When the retransmitted packet is received by the PRX, the PRX DR is asserted and ACK is transmitted back to the PTX. When the ACK is received by the PTX, the PTX DR is asserted.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode

ACK Lost Condition: PTx transmits Data ➔ PTx doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTx doesn't receive ACK again ➔ Packet Loss Count + 1

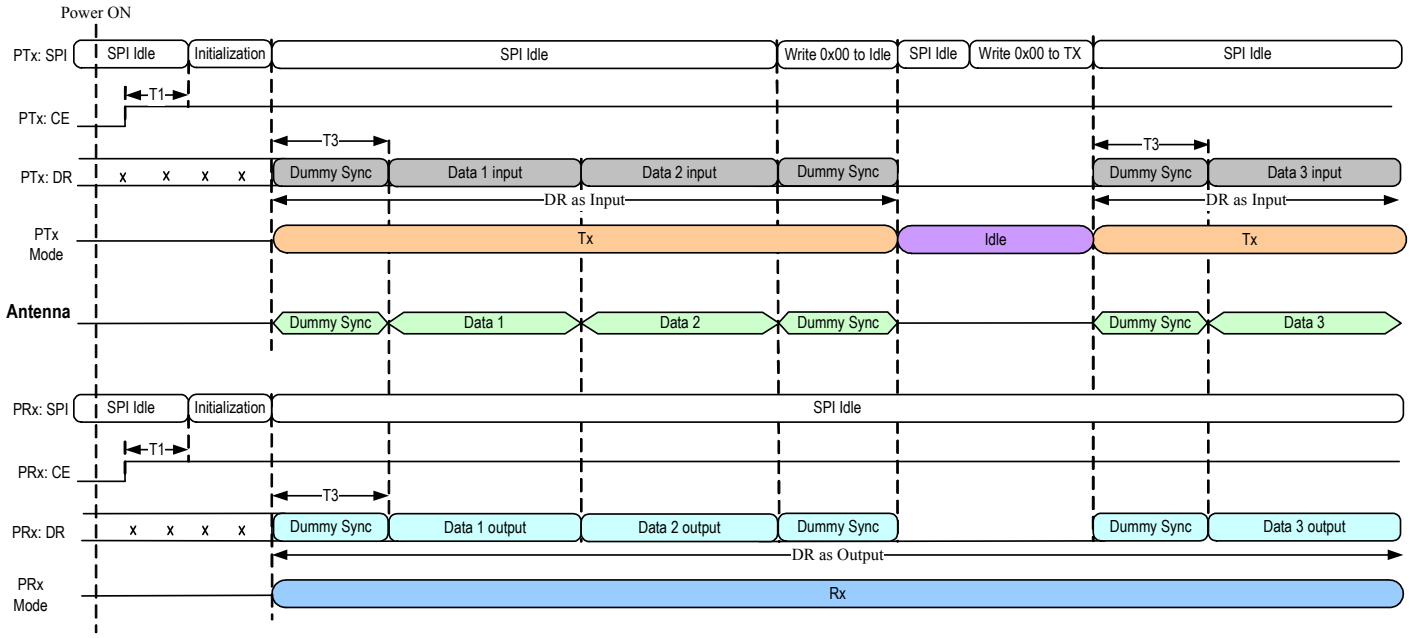


Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

If the PTX retransmit counter exceeds the RETRYCNT 0x47[7:4], the PTX DR is asserted and automatically add one to packet loss count (0x4F[7:3]). The payload in PTX FIFO is removed.

Tx/Rx Link Operation Timing Diagram in Direct Mode

TX DR Mode to Idle Timing Diagram



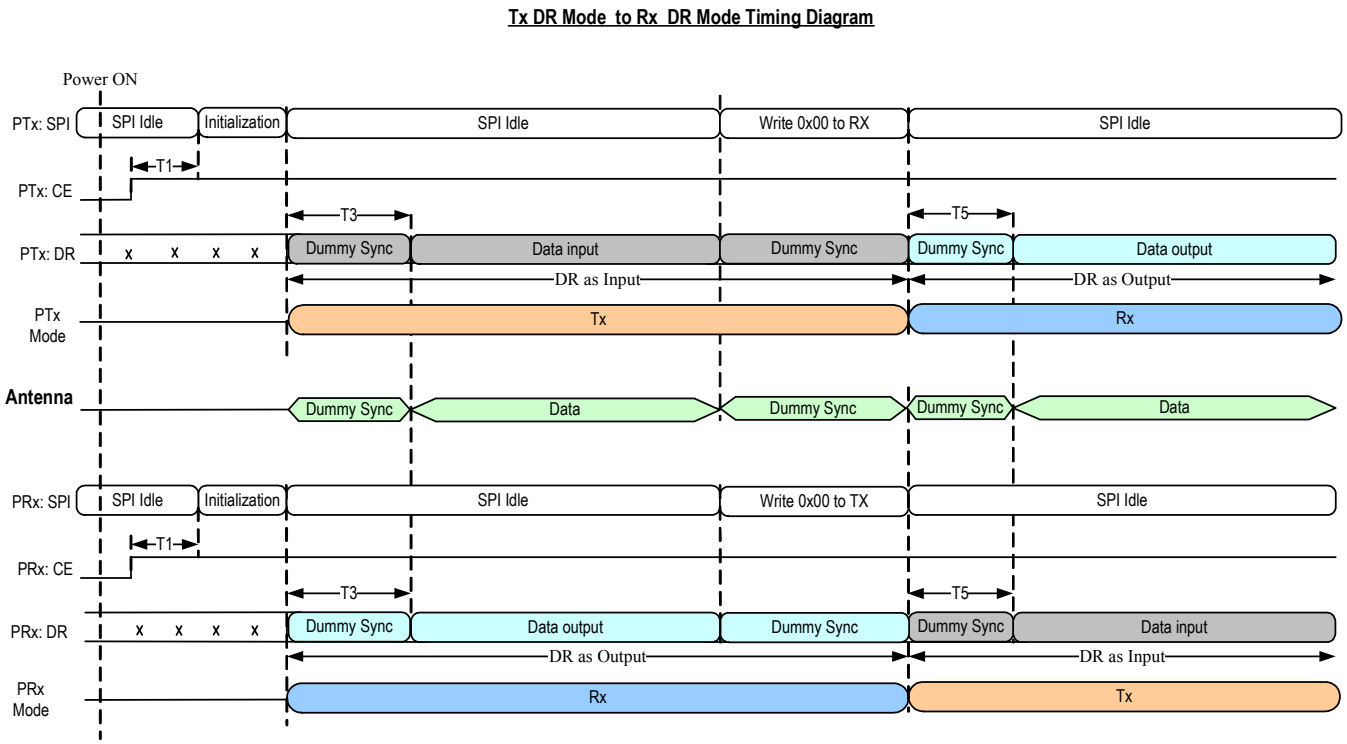
Condition: Set 0x00[6] = 0, 0x00[1] = 1

Set 0x00[4:3] = 10 for Rx device

Set 0x00[4:3] = 01 for Tx device

When RF blocks are active in Tx device, we need to write dummy sync from pin of DR. It can reduce the Rx receiving settling time. The figure shows the timing diagram from direct mode into idle mode, then into direct mode again.

Tx/Rx Switching Operation Timing Diagram in Direct Mode



Condition: Set 0x00[6] = 0, 0x00[1] = 1

Set 0x00[4:3] = 10 for Rx device

Set 0x00[4:3] = 01 for Tx device

When RF blocks are active in Tx device, we need to write dummy sync from pin of DR. It can reduce the Rx receiving settling time. The figure shows the timing diagram for Rx/Tx switching operation. If the devices change from Tx(Rx) into Rx(Tx) directly, the devices don't go into standby mode. Besides, the PLL block only takes the time T5 not T3 for PLL settling time.

Time Formula Description:

Payload Length: **n**
Data rate: **rate**
Sync 0x43 [4:0]: **s**
Address 0x42[7:6]: **a**
SCK Frequency: **SCK**
CRC Check 0x43 [6:5]: **r**
SOF: 1 byte
PID: When STARNET 0x40[7] =1, PID = 1 byte, else PID=0
Slot time 0x47 [3:0]: **SLT**
ACKTOSLOT 0x49 [7:0]: **ATS**
BACKOFFWIN 0x58 [7:0]: **BFW**

Formula Description
• T1 must be over 1ms for Xtal and regulator settling. • Only 500us is needed for regulator settling when system reference clock is shared with MCU
Burst Mode : T2 = (n+1) *8 /SCK Non-Burst Mode : T2 = (2*n) *8 /SCK
T3 = 120us
T4 = (s+SOF+a+n+r)*8/rate
T5 =60us
T6=(s+SOF+PID+a+r)*8/rate
T7= ATS*SLT*10us
T8= BFW*SLT*10us
T9= 10us

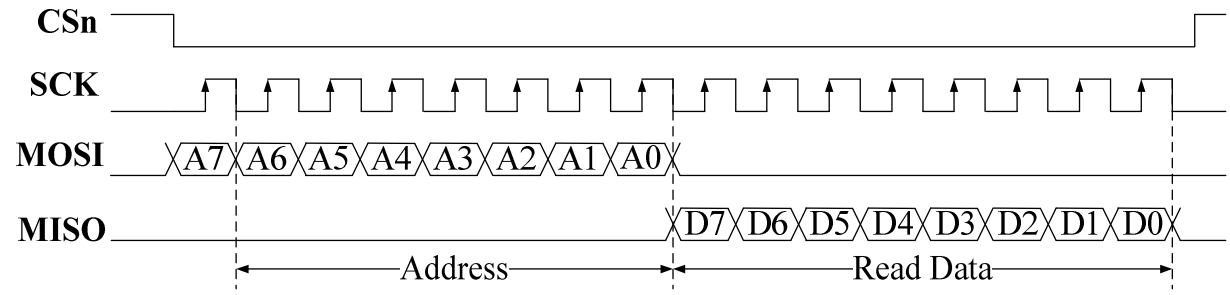
T1: Initiation setting time
T2: TX: Write data to FIFO; RX: Read data from FIFO
T3: RF delay time for transmit data. (Waiting for PLL settling)
T4: Packet Input Data Transmission Time
T5: RF delay for transmit ACK data. (Waiting for PLL settling)
T6: ACK packet Data Transmission Time
T7: ACK waiting time, must be larger then T5+T6, programmable from 10us to 32ms.
T8: Retransmit waiting time, programmable from 0 to 32ms
T9: Packet Handling Time

7. SPI Interface Timing Diagram

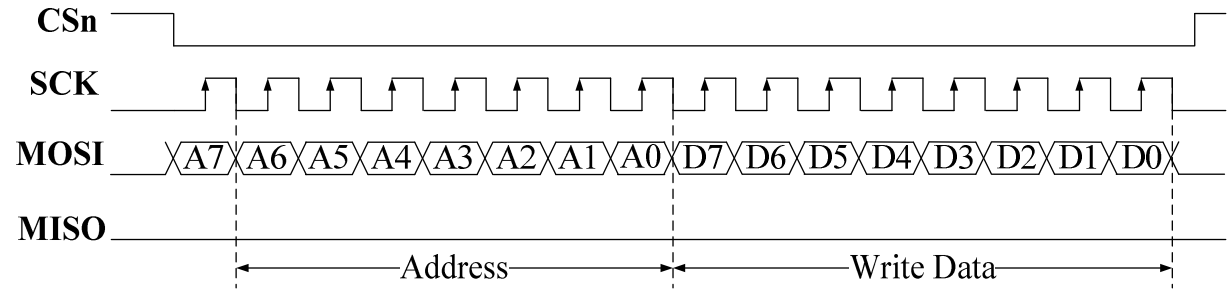
A. SPI interface Read / Write for Register

When A7 = 1, MCU read value from EM198850AW register.
When A7 = 0, MCU write value to EM198850AW register.

SPI Read **A7=1**



SPI Write **A7=0**

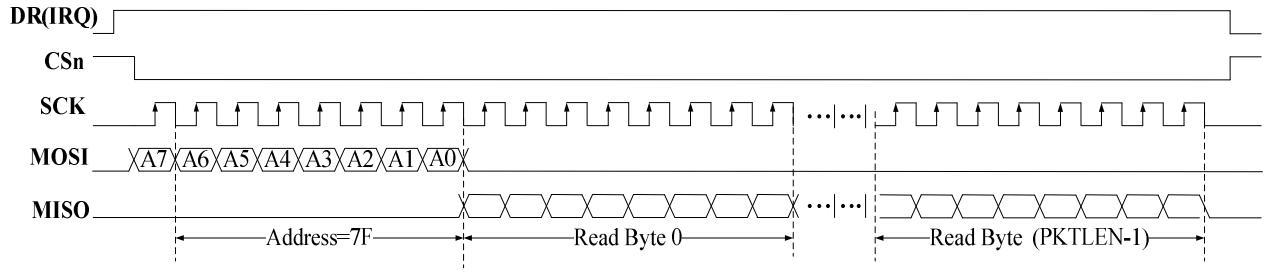


B. SPI interface Read / Write for Buffer mode

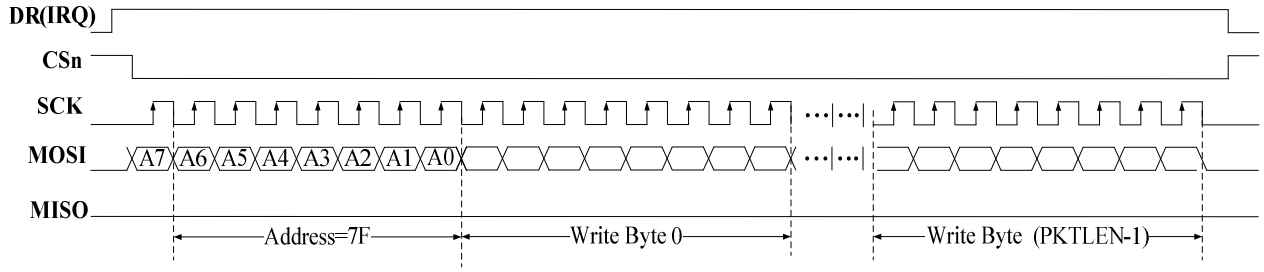
✓ When 0x40[6] = 1, SPI interface switch to Burst mode.

Burst Mode:

Buffer Read **A7=1** (PKTCNT=1)



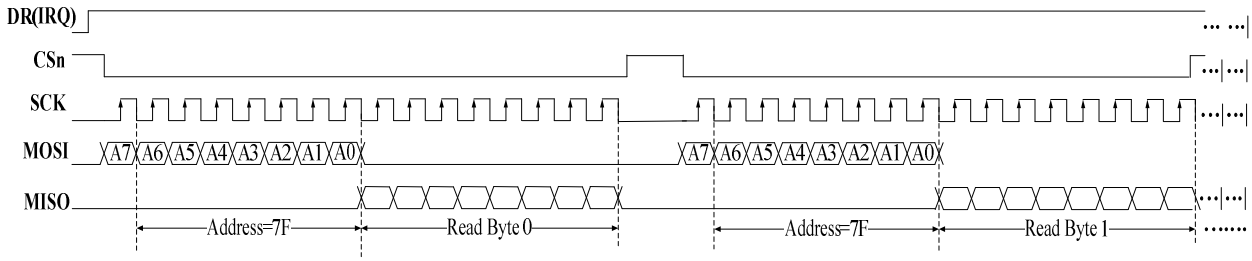
Buffer Write **A7=0** (PKTCNT=1)



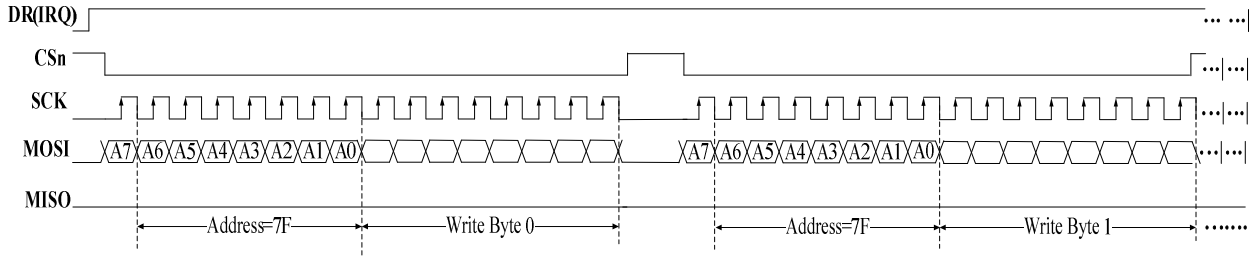
✓ When 0x40[6] = 0, SPI interface switch to Non-Burst mode.

Non-Burst Mode:

Buffer Read **A7=1** (PKTCNT=1)



Buffer Write **A7=0** (PKTCNT=1)



8. SPI Programmable Function Description

1. Data Rate & Crystal Frequency Register Setting

Table 1: Date Rate & Crystal Frequency Register Setting Table																				
Data Rate	XO Freq.	R00	R01	R29	R03						R0A	R4E	R42	R46	R2D	R29	R2E	R2D	R26	R0C	R4A
(Mbps)	(MHz)	5	0	5	5	4	3	2	1	0	5	[7:0]	[5:0]	[5:3]	[2:0]	[3:2]	0	5	3	5	[7:0]
1.6	12	1	0	1	0	0	0	1	1	0	1	10	01111	110	100	10	0	1	0	0	00100111
1	12	1	0	1	0	0	0	1	1	0	0	10	11000	001	010	10	1	0	1	1	00111111
1.6	16	1	1	x	0	0	1	0	0	0	1	01	1010	110	100	10	0	1	0	0	00100111
1	16	1	1	x	0	0	1	0	0	0	0	01	10000	001	010	10	1	0	1	1	00111111
1.6	24	0	1	1	0	0	1	1	0	0	1	10	01111	110	100	10	0	1	0	0	00100111
1	24	0	1	1	0	0	1	1	0	0	0	10	11000	001	010	10	1	0	1	1	00111111

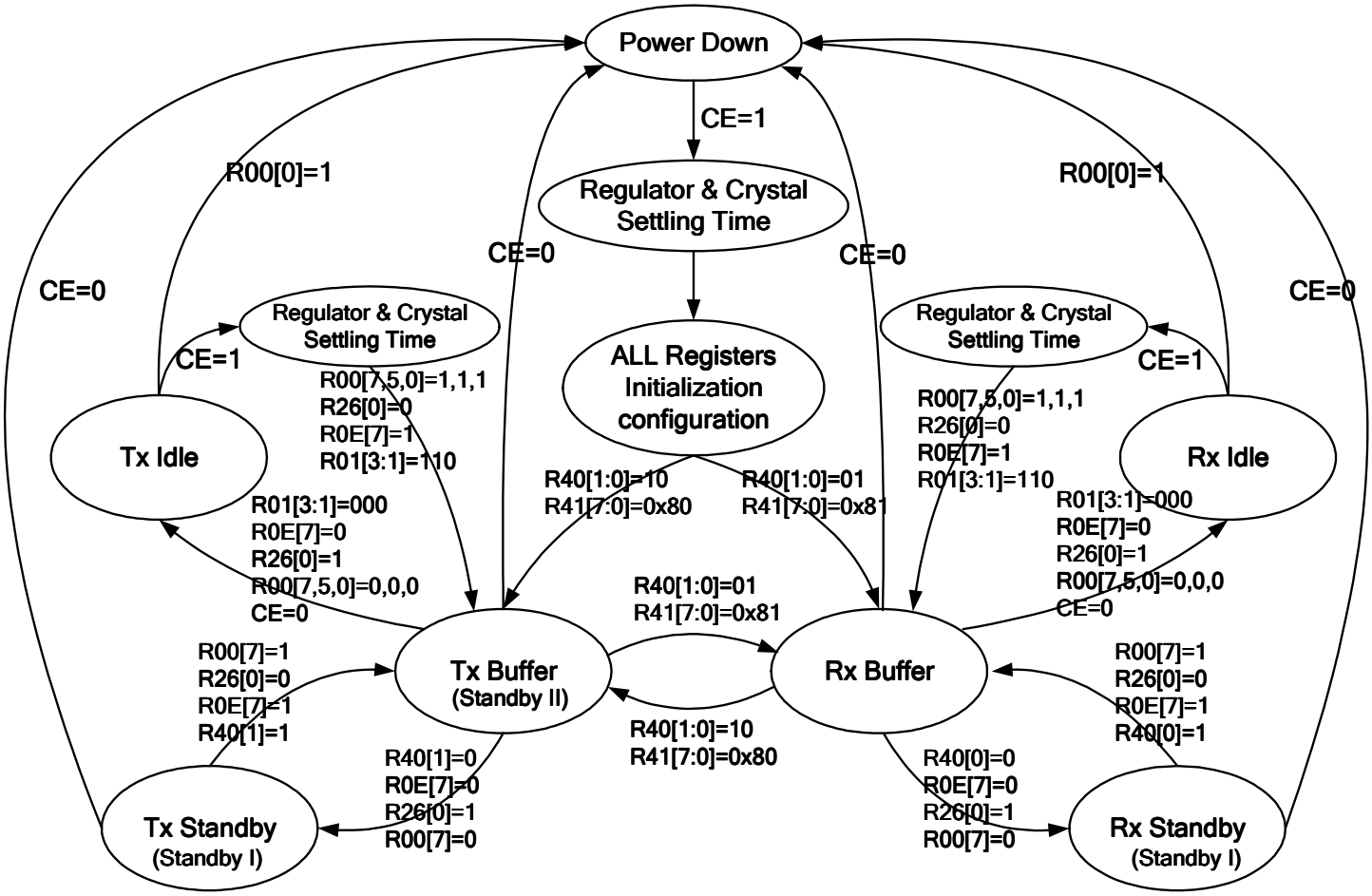
According to the date rate and crystal frequency, find out the corresponding register values before write registers. When write the initial register values, set the relative register values.

2. Operation Mode Register Setting in Direct Mode

Table 2-1: Operation Mode Register Setting Table																
Operation Mode	R0E	R26	R0E	R44	R43	R00					R40		R41	R01	R7F
	7	0	7	[6:0]	[4:0]	6	4	3	1	0	1	0	[7:0]	[3:1]	[7:0]
Tx Device in Direct Mode	0	0	1	1	0x00	0	0	1	1	1	1	0	0x80	110	0x00
Rx Device in Direct Mode	0	0	1	0x08	0x04	0	1	0	1	1	0	1	0x81	110	x

Write Register Sequence from R0E → R26 → R0E → R44 → R43 → R00 → R40 → R41 → R01 → R7F into direct mode

3. Operation Mode Register Setting *in Normal Operation Condition*



4. Tx Output Power Control

Table 4: Tx Output Power Control Table				
Tx Output Power	R06	R0F	R2A	R2B
	[3:1]	[3,0]	[7:0]	[2]
0dBm	110	1,1	01111000	0
-6dBm	011	0,0	00001001	1

5. Channel Change in Buffer Mode:

– write 0x02[6:0] as the table listed below

CH_No.	0x02[6:0]
0	0x00
1	0x01
2	0x02
⋮	⋮
62	0x3E
63	0x3F
⋮	⋮
81	0x51
82	0x52
83	0x53

9. Serial Register Format of Power ON Initialization

Follow the serial register addresses showed below to initialize the EM198850AW RF transceiver. The register address 0x40[7:0] and 0x41[7:0] are used to set the device into Tx or Rx mode.

The values showed in table is for the condition listed below:

- Date Rate = 1Mbps
- Xtal Frequency = 12MHz
- Tx/Rx Buffer Mode
- Package Length = 8 bytes
- Syn. Length = 4 bytes
- Enable Auto ACK Function
- Disable Star Network

Register Address	Initialization Register		Description
	Tx	Rx	
0x4E	0x02		Value reference to Table1
0x4D	0x01		
0x42	0x98		Value reference to Table1
0x43	0xC4		
0x44	0x08		
0x45	0x10		
0x46	0x09		
0x47	0x11		
0x48	0x01		
0x49	0x8A		
0x4A	0x27		Value reference to Table1
0x4B	0xC0		
0x4C	0x06		
0x50	0x00		
0x51	0x11		
0x52	0x22		
0x53	0x33		
0x54	0x44		
0x55	0x55		
0x56	0x66		

0x57	0x77	
0x58	0x08	
0x00	0xE5	Value reference to Table1
0x01	0x8C	Value reference to Table1
0x02	0x00	
0x03	0xC6	Value reference to Table1
0x04	0x00	
0x05	0x40	
0x06	0x5D	
0x07	0x38	
0x08	0x40	
0x09	0x18	
0x0A	0x47	Value reference to Table1
0x0B	0x0B	
0x0C	0xEF	Value reference to Table1
0x0D	0x4F	
0x0E	0x11	
0x0F	0x1B	
0x20	0xAD	
0x21	0x64	
0x22	0x00	
0x23	0xC3	
0x24	0xBD	
0x25	0xA2	
0x26	0x1A	Value reference to Table1
0x27	0x09	
0x28	0x00	
0x29	0x38	Value reference to Table1
0x2A	0x78	
0x2B	0x00	
0x2C	0x92	
0x2D	0x0A	Value reference to Table1
0x2E	0x03	Value reference to Table1
0x2F	0x24	
0x30	0xC0	
0x31	0x00	
0x32	0x40	

0x33	0x39	
0x00	0xA7	
0x32	0x48	
0x00	0xE5	Value reference to Table1
0x0E	0x91	

Note: ***The register setting will be updated after fine tune.***