EM198850AW
2.4GHz Digital RF Module
Application Note

Elan Microelectronics Corp.
Office:
NO. 12, Innovation 1st. RD.,
Science-Based Industrial Park, Hsinchu City,
Taiwan, R.O.C.
TEL: (03) 563-9977
FAX: (03) 563-0118
http://www.emc.com.tw

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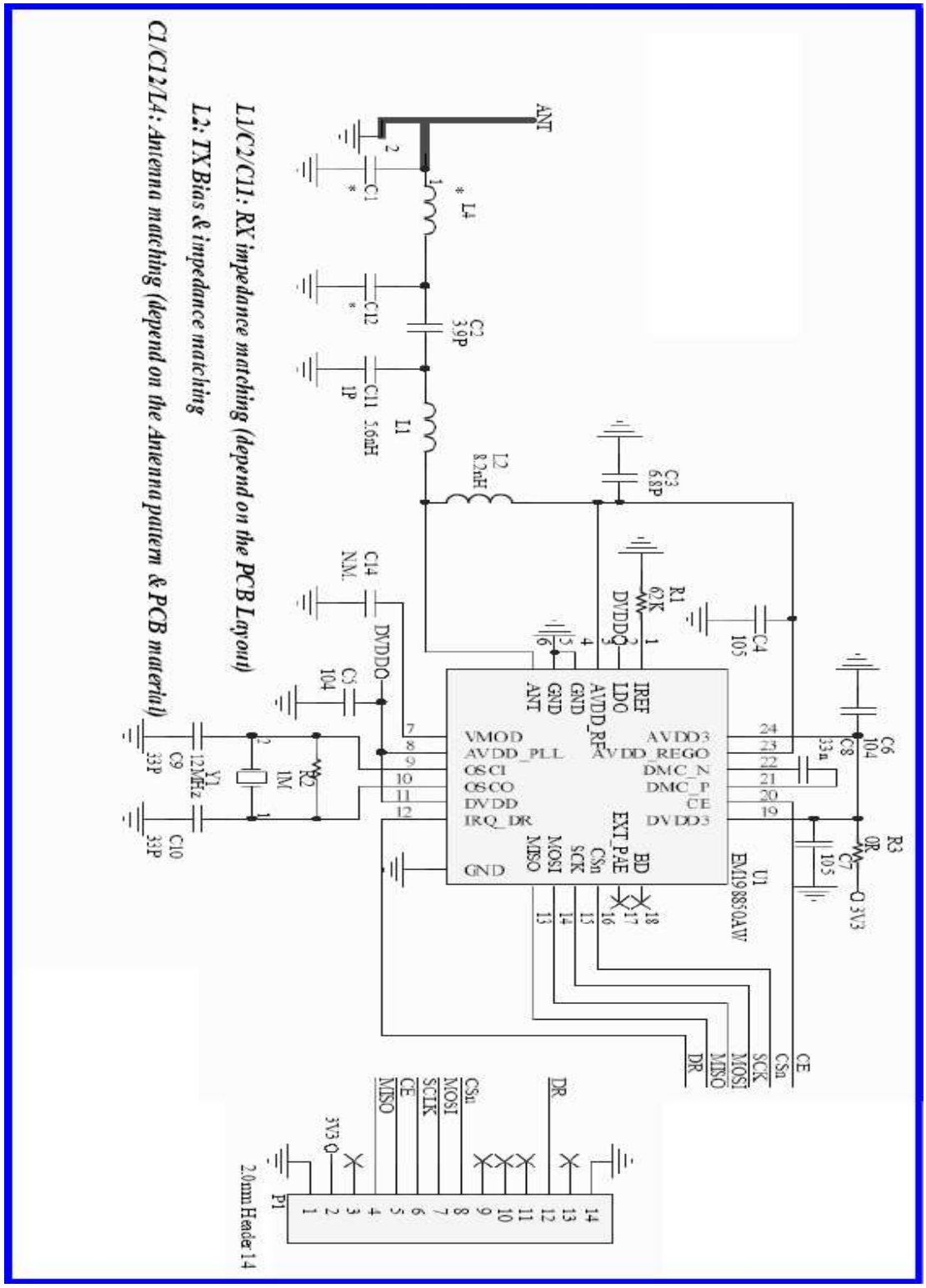


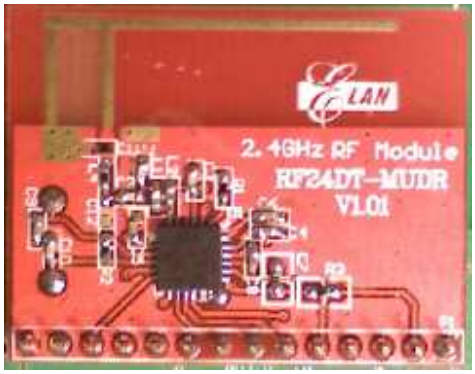


Figure 1: Module PCB Board

Pin Assignment for Connector

PIN	Description	PIN	Description
1	GND	8	SPI_CSn
2	VDD	9	NC
3	NC	10	NC
4	SPI_MISO	11	NC
5	CE	12	DR_IRQ
6	SPI_CLK	13	NC
7	SPI_MOSI	14	GND

Table 1: Module Pin out

PCB Layout Consideration

1. Standard FR4 material is used in a two-layer PCB
2. Resistor for pin 10 and pin11 must close with pin.
3. Pin6 connects to L1 with the shortest distance. L2 places close to pin3.
4. In order to secure isolation between pin3 and pin6, short pin5 and pin4 to ground.
5. RF IO's trace must use 50 ohm transmission line.
6. The trace doesn't pass through below RF_IO's path.

COMPONENT LIST

Comment	Description	Tolerance	Designator	Quantity	Recommend Vendor
1.0P/10V	1005 NPO Ceramic Capacitor	**±0.25P**	C11.	1	Darfon or Murata or equal
3.9P/10V	1005 NPO Ceramic Capacitor	**±0.25P**	C2.	1	Darfon or Murata or equal
6.8P/10V	1005 NPO Ceramic Capacitor	**±0.25P**	C3.	1	Darfon or Murata or equal
33P/10V	**1005 NPO Ceramic Capacitor**	**±5%**	**C9, C10.**	**2**	Darfon or Murata or equal
33n	1005 X7R Ceramic Capacitor	**±10%**	**C8.**	**1**	**Darfon or Murata or equal**
100n/10V	1005 X7R Ceramic Capacitor	**±10%**	C5, C6.	2	**Darfon or Murata or equal**
1u/6.3V	1005 Y5V Ceramic Capacitor	**±20%**	C4, C7.	2	Darfon or Murata or equal
5.6nH	1005 Multilayer Ceramic Chip Inductor	**±0.3nH**	L1.	1	Darfon or Murata or equal
8.2nH	1005 Multilayer Ceramic Chip Inductor	**±5%**	L2.	1	Darfon or Murata or equal
0R	1005 Carbon Film Resistor	**±5%**	L4.	1	Darfon or Murata or equal
4R7	1005 Carbon Film Resistor	**±5%**	R3.	1	Yageo or equal
62K	1005 Carbon Film Resistor	**±5%**	R1.	1	Yageo or equal
1M	1005 Carbon Film Resistor	**±5%**	R2.	1	Yageo or equal
EM198850H	RFIC DICE form		U1	1	Elan
12MHz	DIP HC-49S/CL18P	**±20ppm**	Y1.*	1	TXC or equal
PCB	28X22mm/0.8mm FR-4		PCB	1	ε≒4.5
Total				19	

Table 2: Module BOM

2. Description of Operation Mode

Operation Mode	0x40	0x41	0x00				0x01	CE Pin	CSn Pin	MOSI Pin	MISO Pin	IRQ Pin
	[1:0]	[7:0]	[7]	[6]	[5]	[0]	[3:1]					
Power Down	x	x	x	x	x	1	X	0	x	**SPI**in	**SPI**out	
Idle	x	x	0*a	1	0	0	101	0	x	**SPI**in	**SPI**out	
Configuration	x	x	1	1	x	1	010	1	0	**SPI**in	**SPI**out	
Standby I	00	x	0	1	1	1	110	1	1	**FIFO**in	**SPI**out	**IRQ**out
TX Buffered	10	0x80	1	1	1	1	010	1	1	**FIFO**in	**SPI**out	**IRQ**out
Standby II	10	0x80	1	1	1	1	010	1	1	**FIFO**in	**SPI**out	**IRQ**out
TX Direct	10	0x80	1	0	0	1	010	1	1	**SPI**in	**SPI**out	**Data**in
RX Buffered	01	0x81	1	1	1	1	010	1	1	**SPI**in	**FIFO**out	**IRQ**out
RX Direct	01	0x81	1	0	0	1	010	1	1	**SPI**in	**SPI**out	**Data**out

Table 3: Operation Mode

*a: When using external Xtal with internal oscillator, (i.e. R00[2]=1), MCU write 0. When using external clock from MCU, (i.e. R00[2]=0), register R00[7] don't care.

For detail register setting, refer to the state machine of operation modes. Please follow the register sequence order showed from up to down when you write the register setting. The symbol "x" means that don't write the registers when you change the operation mode.

Configuration
When CSn=0 and CE = 1, the SPI interface may be activated to program the SPI register value. For the detail timing diagram, you can refer to the Figure 16 ~ Figure 18.

Power Down Mode
When the pin CE sets to 0 and 0x00[0] sets to 1, the EM198850AW is disabled with the minimal current consumption. When entering the power down mode, EM198850AW is not active including voltage regulators and crystal block, and the values of all registers are clear.

Idle
Idle mode is used to minimize average current consumption while maintaining short start up times. In this mode, the contents of all registers are maintained by internal power supply voltage. It will reduce the register initialization time on the next start up time from idle mode into buffer mode. EM198850AW is not active including voltage regulators and crystal block.

Standby I
For RX or TX device, all the RF blocks and mini Mac baseband system clock will be turned off to save average current consumption. In this mode, only voltage regulators, crystal oscillator and clock buffers are active to speed up the start-up time. The configuration word content is maintained during standby I mode.

TX Buffered Mode (BUF)
As a transmitter with the function of FIFO and packet handling

Standby II
When TX FIFO is empty in TX buffer mode, the TX device would stay in the standby II mode. In

this mode, the regulators, crystal oscillator, clock buffers and mini Mac baseband system clock are activated. No any start-up time is need.

TX Direct Mode (DR)
As a transmitter without the function of the FIFO and packet handling

RX Buffered Mode (BUF)
As a receiver with the function of FIFO and packet handling

RX Direct Mode (DR)
As a receiver without the function of the FIFO and packet handling

3. State Machine of Operation Mode

The Figure is the state machine of operation modes. The MCU can follow the register sequence to write SPI registers into the desired operation mode through digital SPI interface.

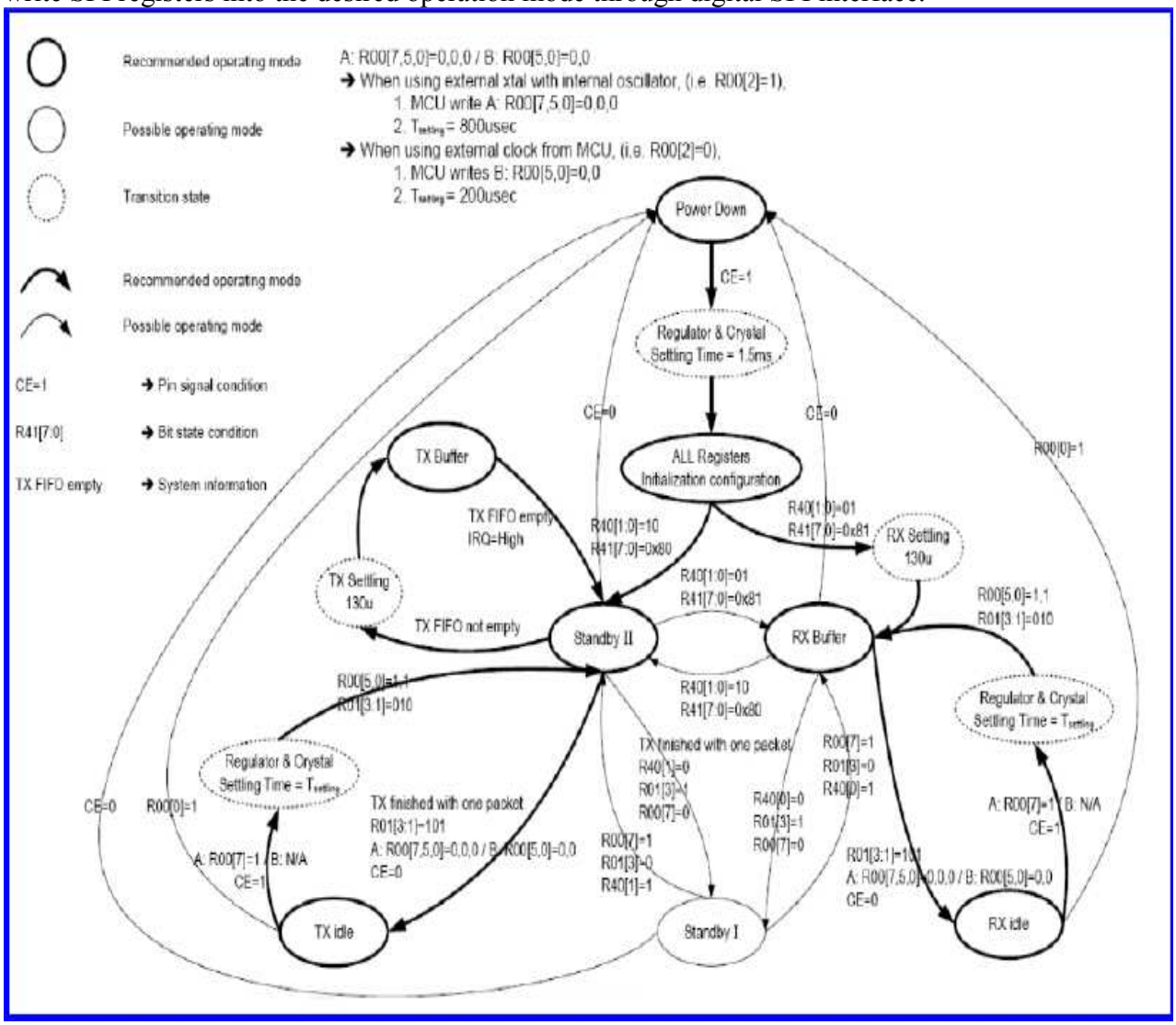


Figure 2: State machine diagram

4. System Flowchart

- **Tx operation**

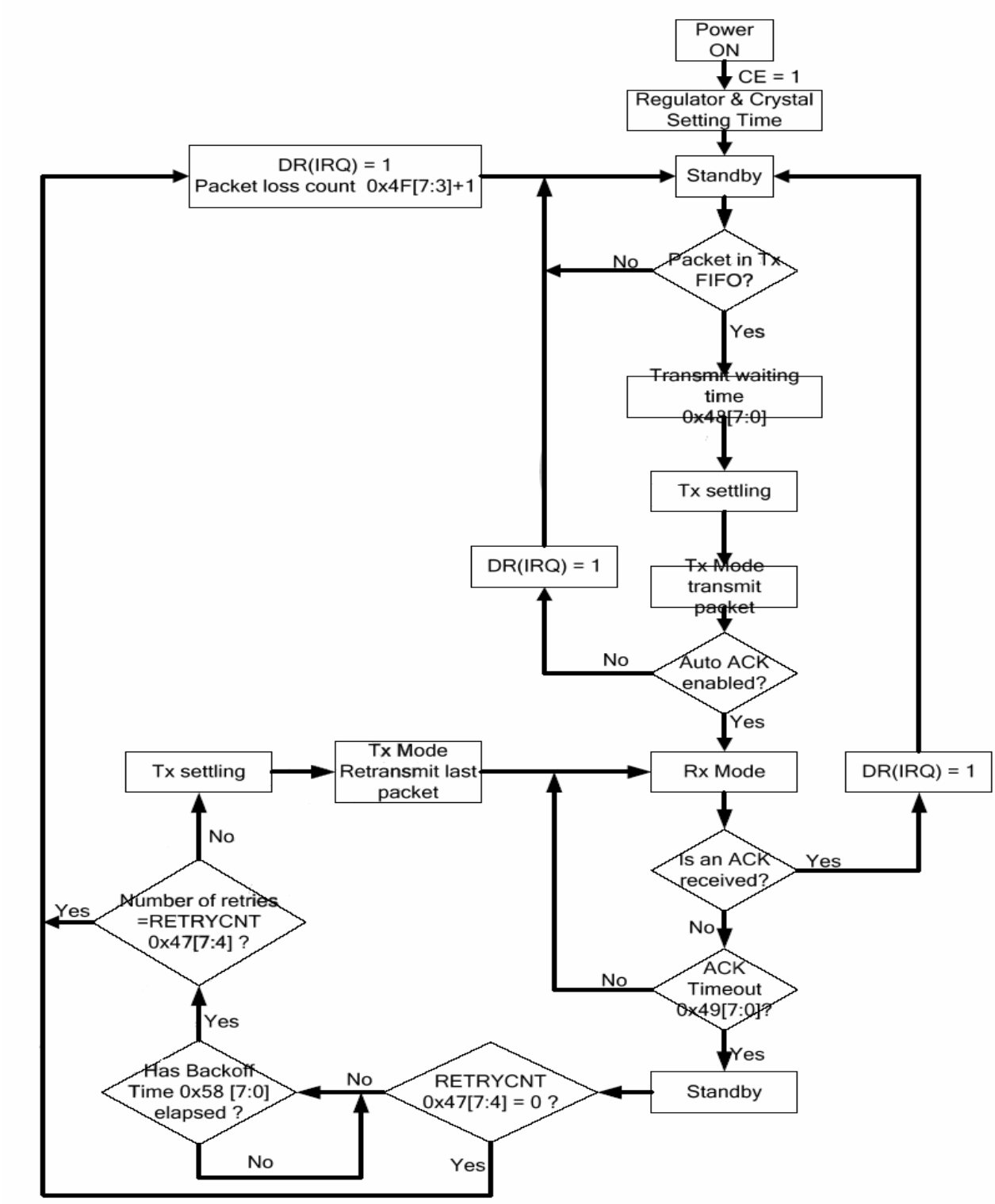


Figure 3: Operation flowchart of Tx

If there is a packet present in Tx FIFO, the EM198850AW enters Tx Buffer mode and transmits the packet. If Auto ACK is enabled, the EM198850AW enters Rx mode to receive an ACK packet.
If the ACK packet is not received before timeout occurs, the EM198850AW returns to Tx standby II mode. It stay in Tx standby II mode until the Backoff Time(0x58[7:0]) has elapsed. If number of retransmits has not reached the ETRYCNT(0x47[7:4]), the EM198850AW start to transmit the last packet once more. When number of retransmits reach the maximum number, the EM198850AW assert DR(IRQ) and automatically add one to packet loss count(0x4F[7:3]) . EM198850AW return to standby II mode wait for next new packet input.

- **Rx operation**

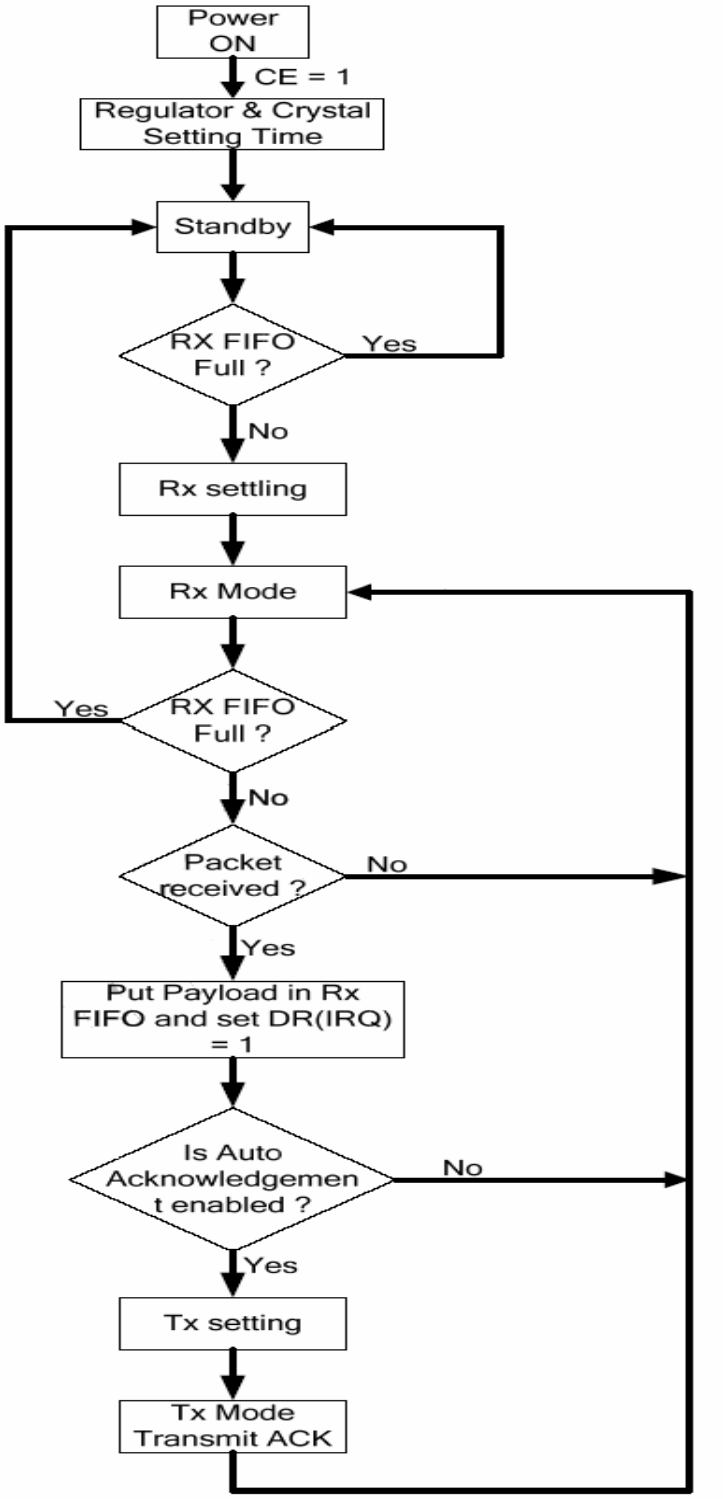


Figure 4: Operation flowchart of Rx

If a packet is received from transmitter, the EM198850AW assert DR(IRQ) and put receive packet in Rx FIFO. If Auto ACK is enabled, the EM198850AW enters Tx mode to transmit an ACK packet. After ACK packet is transmitted, the EM198850AW return to Rx mode. When the FIFO is full, number of payload equal to PKTCNT, all the RF circuits will turn off automatically to save power consumption. RF circuits will turn on when the FIFO is not full.

- **RSSI operation in Rx**

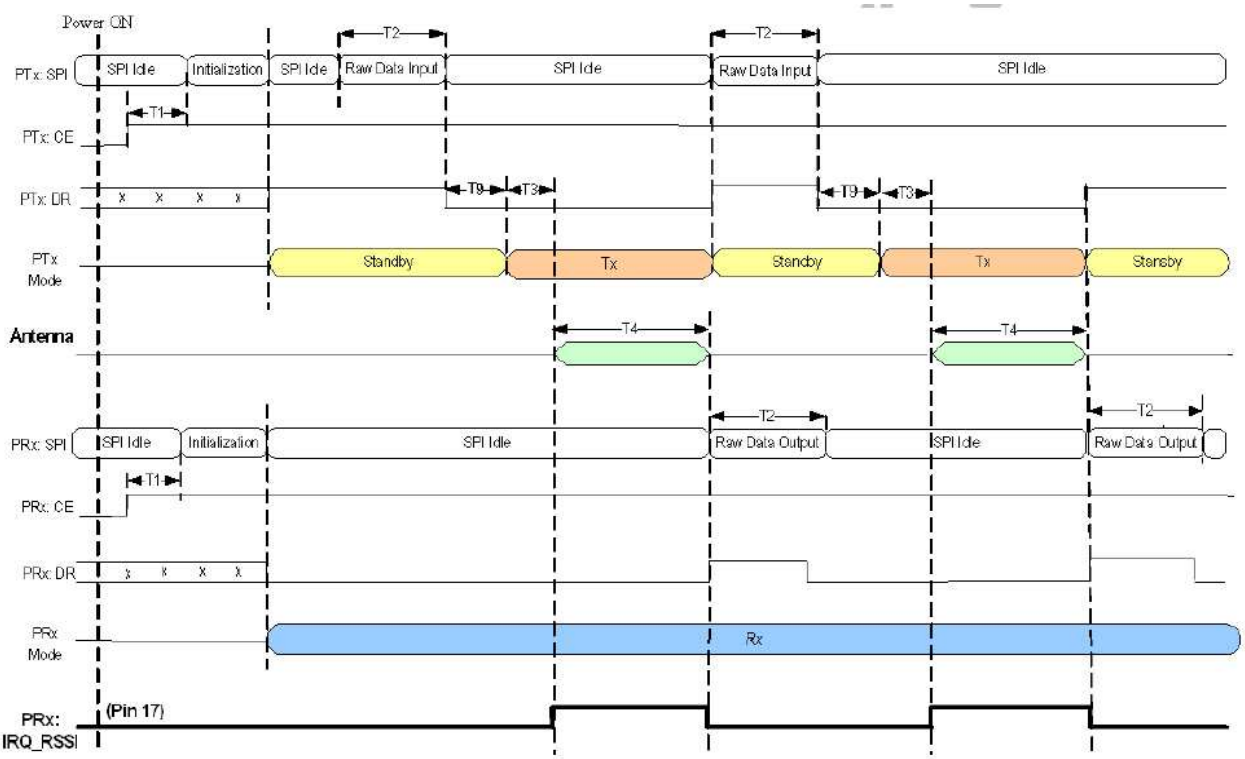


Figure 5: RSSI operation timing diagram in Rx

In Rx device, pin 17, sets as IRQ_RSSI, is high to indicate that it is available for the MCU to read the RSSI registers, R0x4B[5:0] through the SPI interface. RSSI values are only valid during receiving signal.

- **Xtal Frequency Offset Calibration**

If the EM198850AW uses the external Xtal with internal oscillator to create the system clock, the EM198850AW provide the auto frequency tuning engine to fine the Xtal frequency.

Calibration Flow

1. Start

2. Set registers into Direct Mode

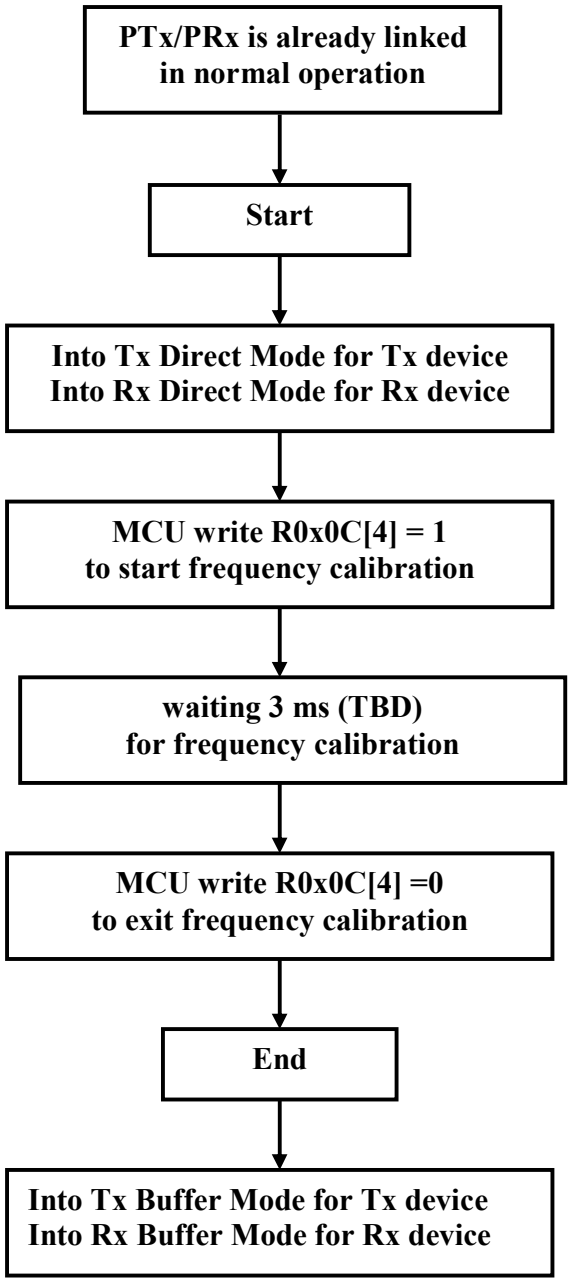
3. For Rx device, write R0x0C[4]=1 to start frequency calibration. For Tx device, it outputs a single carrier as reference frequency for Rx device

4. Waiting 3 msec for the timing of frequency calibration (TBD)

5. For Rx device, write R0x0c[4]=0 to finish the calibration flow

6. End

7. Recover to the normal operation mode



Xtal Frequency Offset Calibration Timing Diagram

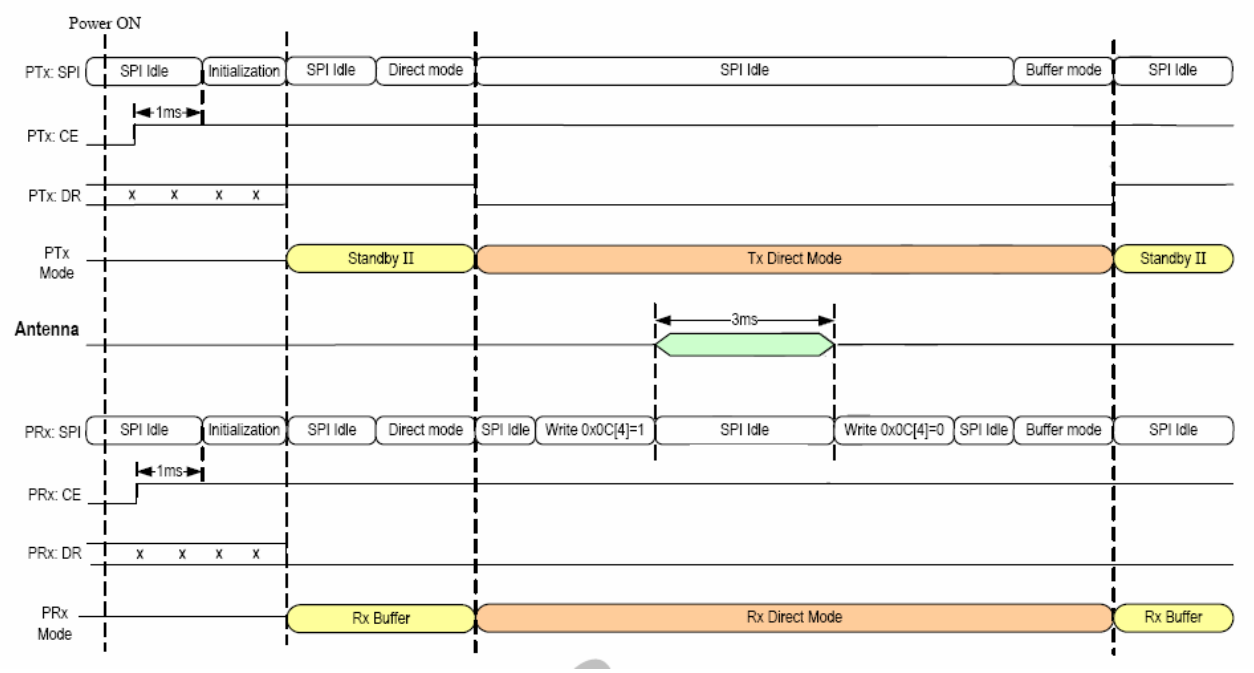


Figure 6: Xtal Frequency Offset Calibration Timing Diagram

Note: When the devices go into POWER DOWN mode, all the calibration result will be refreshed

EM198850AW sharing crystal with a MCU

When using a MCU to drive the crystal reference pin XC2 of the EM198850AW transceiver, some rules must be followed. First, the register R0x00[2] is set to Low. When MCU drives the EM198850AW clock input pin, XC2, the requirement of load capacitance CL is set by the MCU only.

The frequency accuracy of +/-60ppm is still required to get a functional radio link. The input signal should not have amplitudes exceeding any rail voltage, but any DC voltage within this is OK. To achieve low current consumption and also good SNR ratio when using an external clock from MCU, it is recommended to use an input signal larger than 0.4 V-peak. When clocked externally, XC2 is the input pin, and XC1 is not used. XC1 must be connected to ground.

5. Star Network

An EM198850 configured as primary RX will be able to receive data through 6 different data pipes. A data pipe will have a unique address but share the same frequency channel. This means that up to 6 different EM198850 configured as primary TX can communicate with one EM198850 configured as RX, and the EM198850 configured as RX will be able to distinguish between them. Only one data pipe can receive a packet at a time.

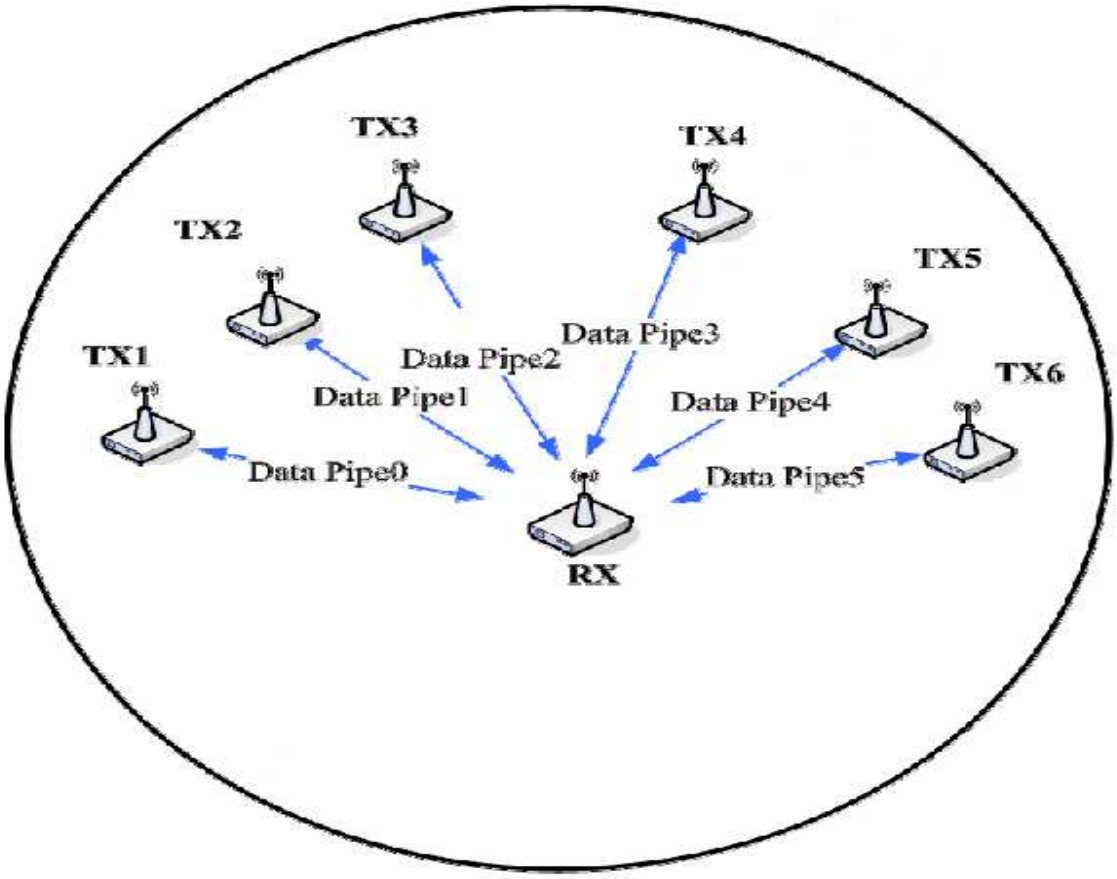


Figure 7: in a star network Configuration

The following settings are common to all data pipes:

- Auto ACK enable
- STARTNET enable
- CRC encoding scheme
- Tx / Rx Address width
- Frequency channel
- Air data pipe
- RF data rate

The data pipes are enabled with the bits in the 0x41[5:0] register.
Each data pipe address is configured in the RXADR0 ~ RXADR5. Each data pipe can have up to 2 byte configurable address. Data pipe 0 has a unique 2 byte address. Data pipe 1~5 shares the 8 most

significant address bits. Figure 8. is an example of how data pipes 0~5 are addressed.

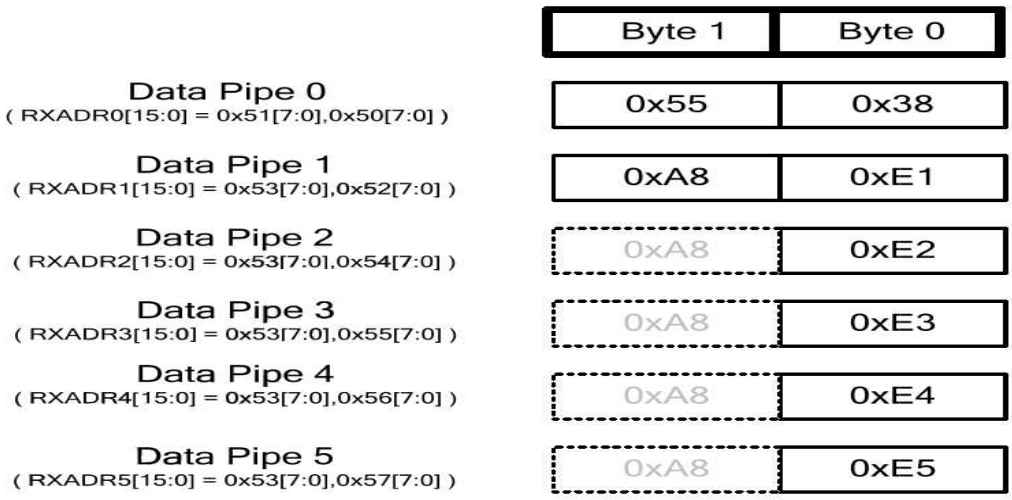


Figure 8: Addressing Data Pipes 0~5

The Rx receives packet from more than one Tx. To ensure that the ACK packet from the Rx is transmitted to the correct Tx, the Rx takes the data pipe address where it received the packet and use it as the Tx address when transmitting the ACK packet. On the Tx device, the TXADR must be same as the RXADR0. On the Rx device, the RXADR0~RXADR5, defined as the data pipe address, must be unique. Figure 2. is an example of data pipe addressing for the Tx and Rx.

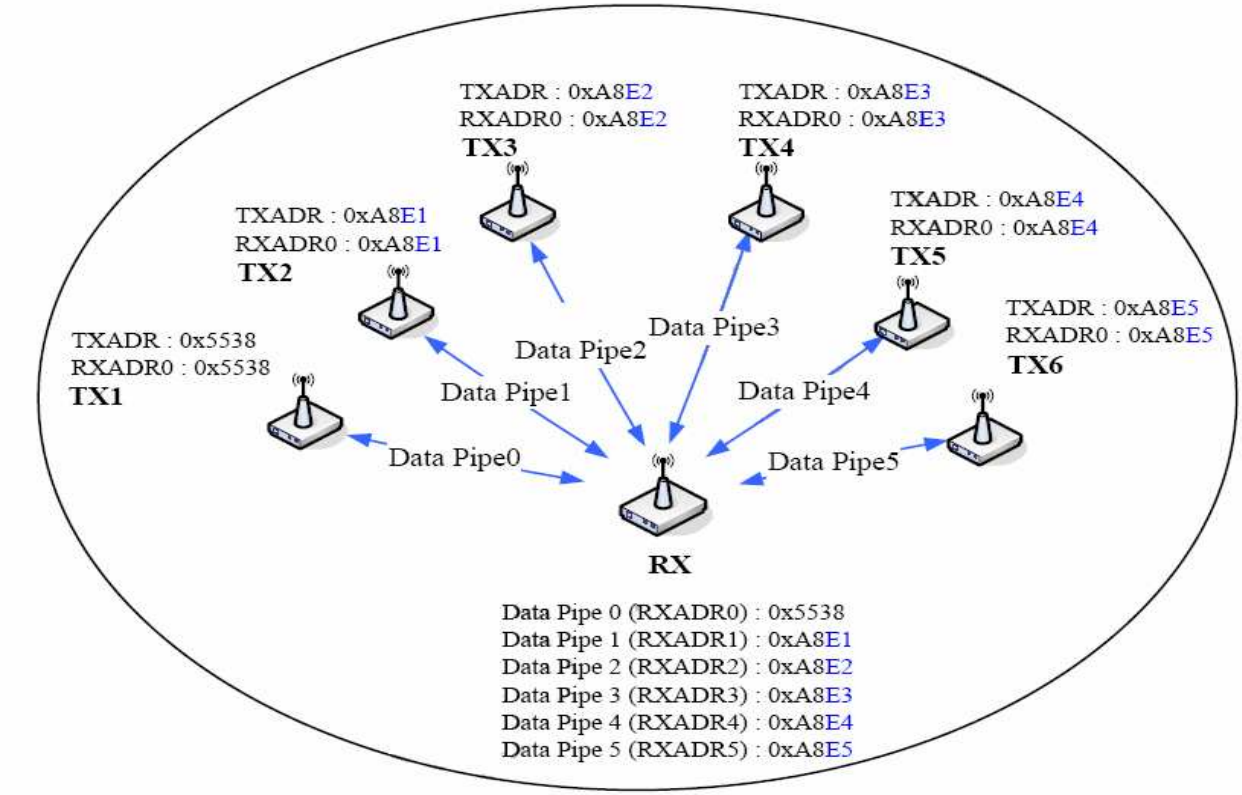


Figure 9: Example of data pipe addressing

6. Frame Structure

Data Frame-structure

sync	SOF	address	PID	payload	CRC

ACK Frame-structure

sync	SOF	address	PID	CRC

Table 4: Frame Structure

Sync: 4-12 bytes (Default 4 bytes)
- **SOF:** Start of Frame (1byte)
- **Address:** Programmable byte length (1-2 Byte)
- **PID:** 1 byte

When STARNET 0x40[7] is enabled, PID is adding to frame structure.
When STARNET 0x40[7] is disabled, PID is removing from frame structure.

Example:
If STARNET 0x40[7] is enabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),
→ PID= 1 byte, the available payload = 3 bytes
If STARNET 0x40[7] is disabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),
→ PID= 0 byte, the available payload = 4 bytes

- [7]: Packet type, auto generate by HW
  - 1'b0 : Data packet (needs ACK or not)
  - 1'b1: ACK packet

- [6:4]: 000~101 Pipe data number, auto generate by HW
- [3:0]: Packet sequence number, It is used by the Rx device to determine if a packet is new or retransmitted. It defined by user.

- **Payload:** Programmable byte length (1-64 Byte)
- **CRC:** Programmable length(0,1,2,4 Byte)

7. Operation Timing Diagram

Tx/Rx Link Operation Timing Diagram without Auto-ACK in Buffer Mode

Tx to Rx Operation Timing Diagram

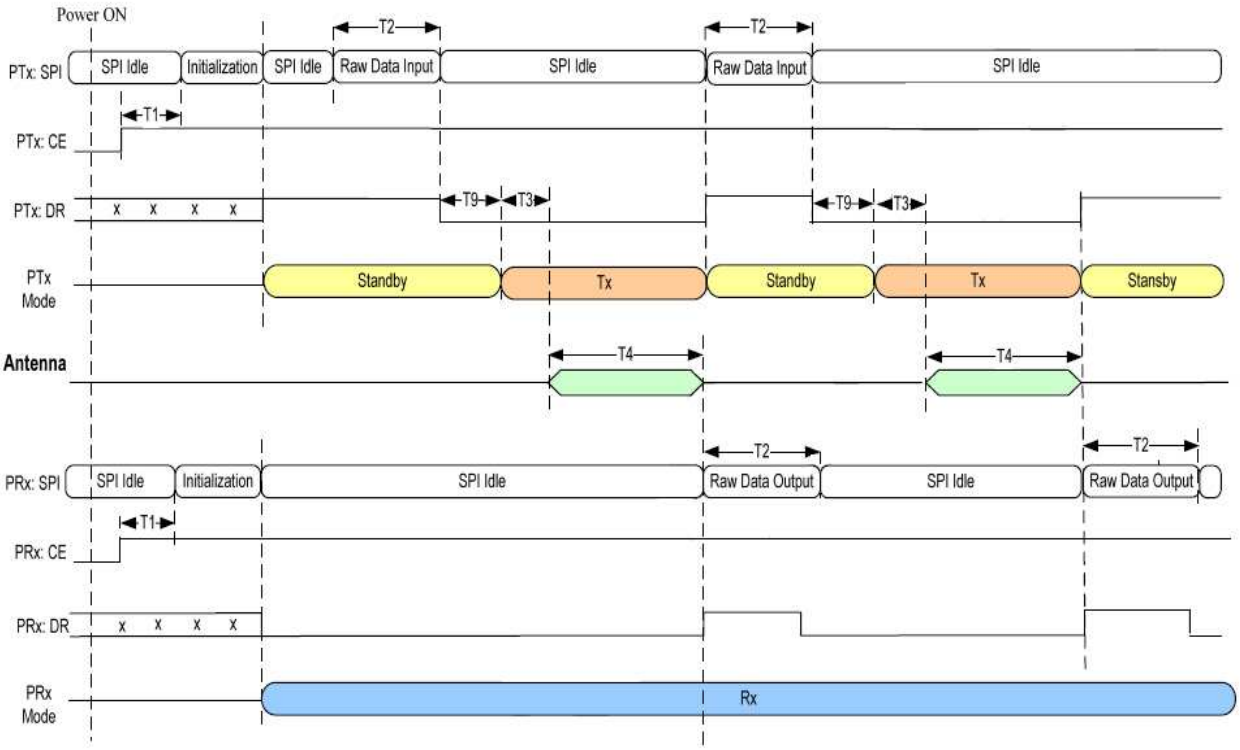


Figure 10: Tx/Rx Link Operation Timing Diagram without Auto-ACK in Buffer Mode

Condition: Disable Auto ACK 0x40[3:2] = 00
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

The PTx DR is asserted after the packet is transmitted by the PTX.
The PRx DR is asserted after the packet is received by the PRX.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode

Tx to Rx Operation Timing Diagram

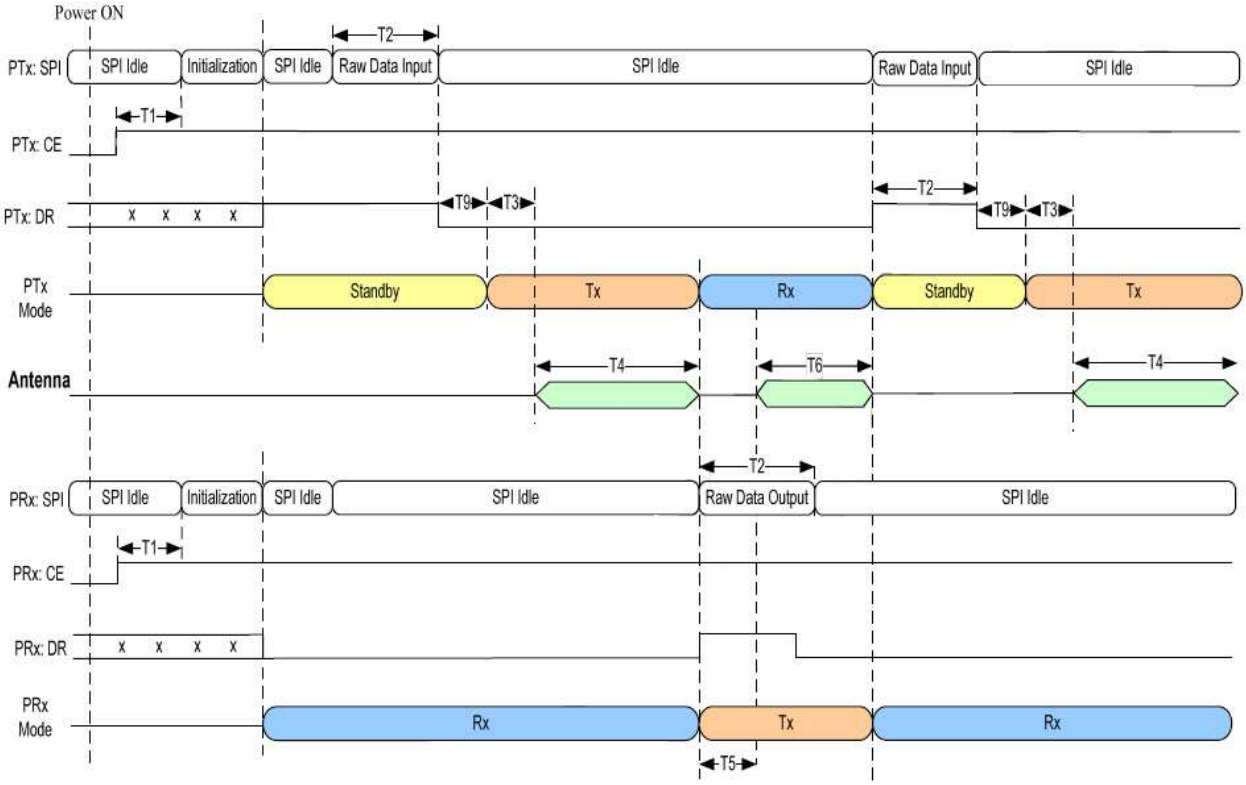


Figure 11: Tx/Rx Link Operation Timing Diagram with Auto-ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

When the transmission ends the PTX device automatically switches to Rx mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to MCU. When the PRX device receives the packet it responds with an interrupt to MCU.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode
ACK Lost Condition: PTx transmits Data → PTx doesn't receive ACK → Retransmit Data (Retransmit time=1) → PTx receives ACK

Tx to Rx Operation Timing Diagram, 0x47[7:4]RETRYCNT=1

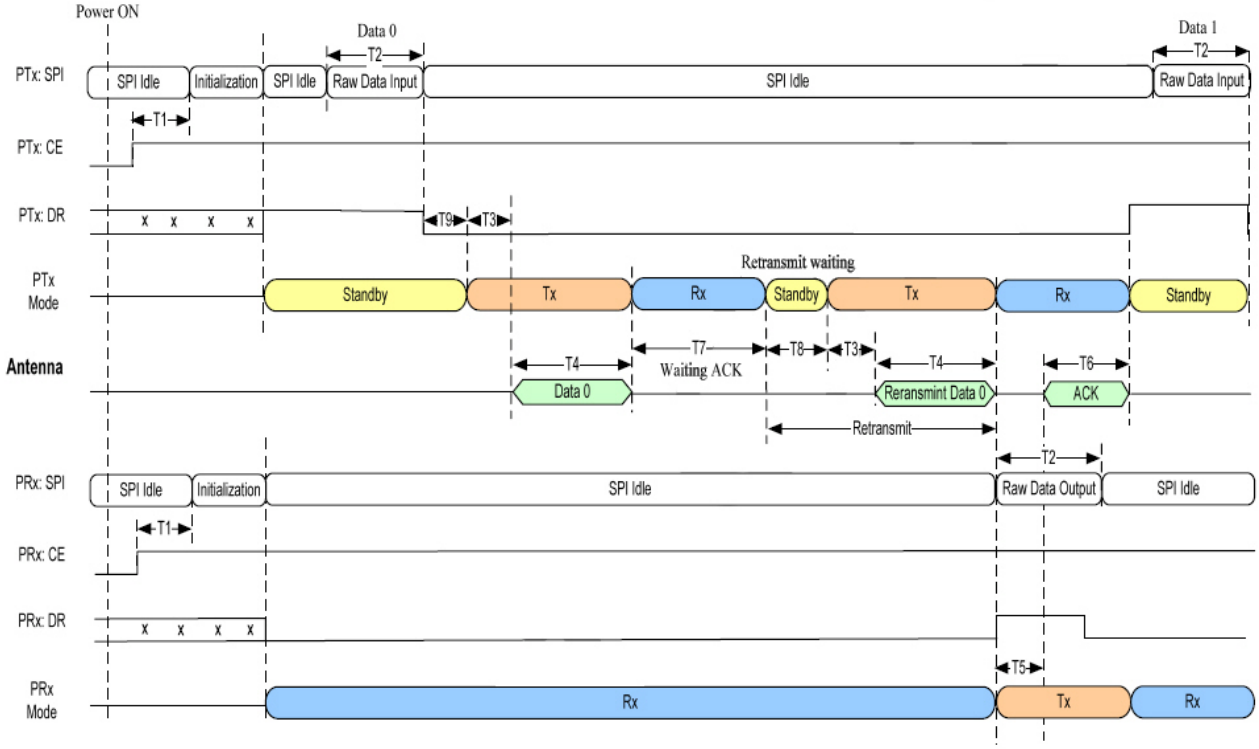


Figure 12: ACK Lost Condition for Tx/Rx Link with Auto-ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

After Data 0 is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits specified time for ACK packet (T7), if it is not in specified time slot, the PTX retransmit the Data 0. When the retransmitted packet is received by the PRX, the PRX DR is asserted and ACK is transmitted back to the PTX. When the ACK is received by the PTX, the PTX DR is asserted.

Tx/Rx Link Operation Timing Diagram with Auto ACK in Buffer Mode
ACK Lost Condition: PTx transmits Data → PTx doesn't receive ACK → Retransmit Data (Retransmit time=1) → PTx doesn't receive ACK again → Packet Loss Count + 1

Tx to Rx Operation Timing Diagram, 0x47[7:4]RETRYCNT=1

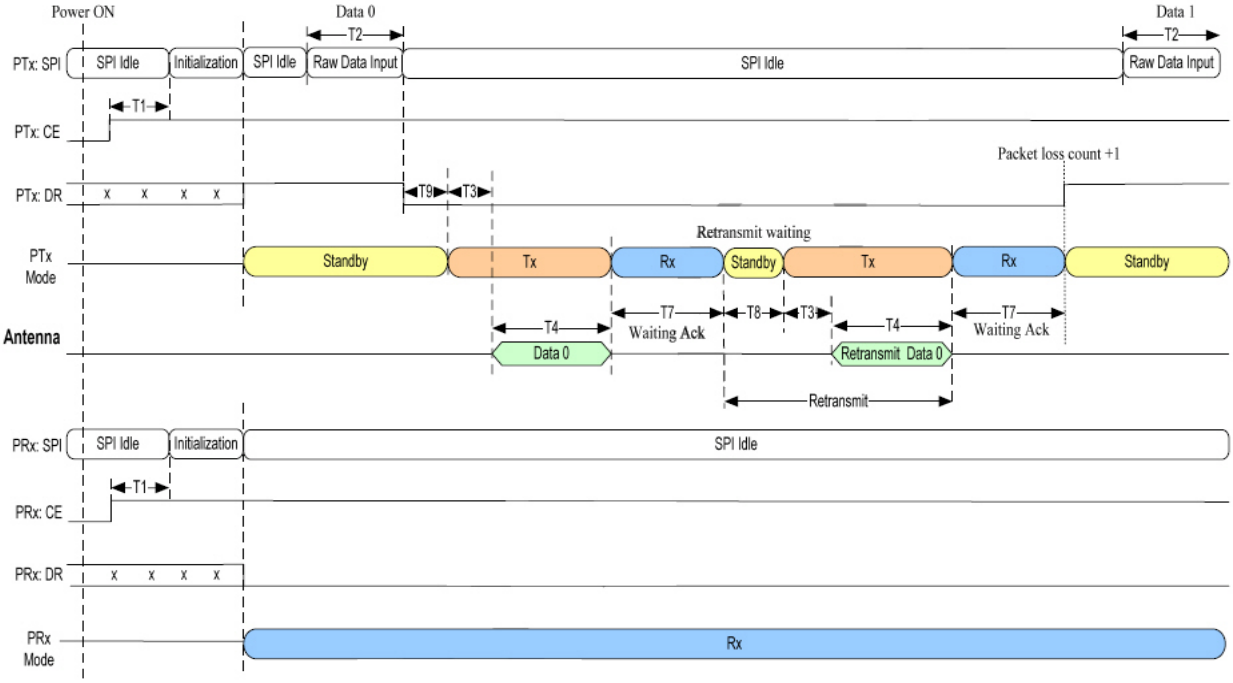


Figure 13: ACK Lost Condition for Tx/Rx Link with Auto-ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

If the PTX retransmit counter exceeds the RETRYCNT 0x47[7:4], the PTX DR is asserted and automatically add one to packet loss count (0x4F[7:3]). The payload in PTX FIFO is removed.

Tx/Rx Link Operation Timing Diagram in Direct Mode

Tx to Rx Operation Timing Diagram

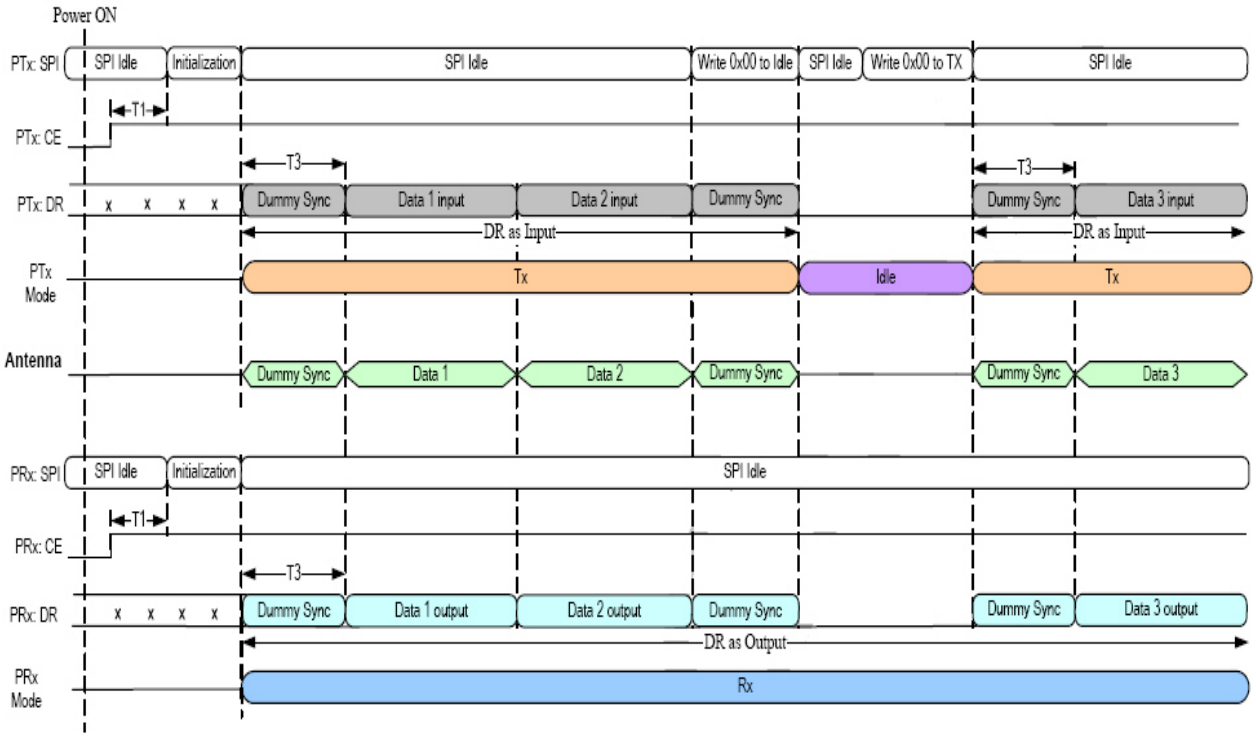


Figure 14: Tx/Rx Link Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for Rx device
Set 0x00[4:3] = 01 for Tx device

When RF blocks are active in Tx device, we need to write dummy sync from pin of DR. It can reduce the Rx receiving settling time. The figure shows the timing diagram from direct mode into idle mode, then into direct mode again.

Tx/Rx Switching Operation Timing Diagram in Direct Mode

Tx DR Mode to Rx DR Mode Timing Diagram

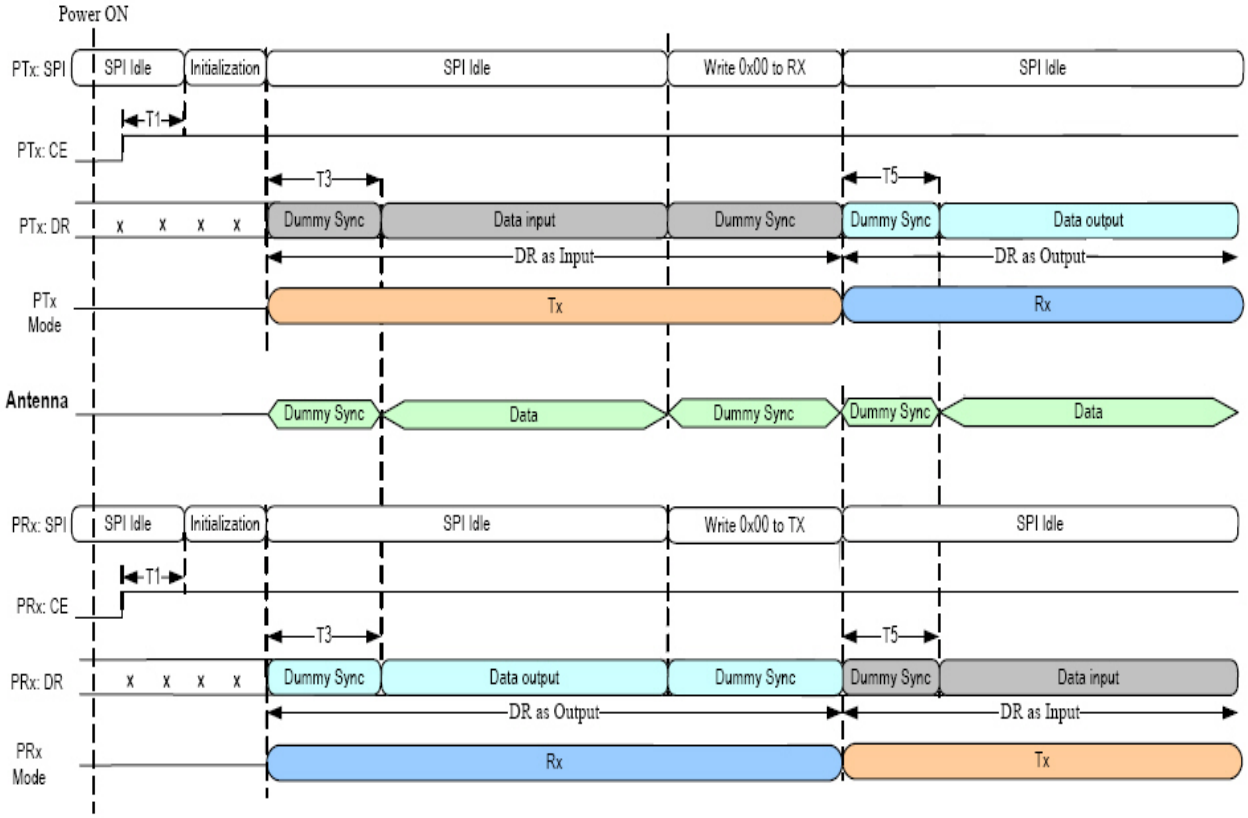


Figure 15: Tx/Rx Switching Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for Rx device
Set 0x00[4:3] = 01 for Tx device

When RF blocks are active in Tx device, we need to write dummy sync from pin of DR. It can reduce the Rx receiving settling time. The figure shows the timing diagram for Rx/Tx switching operation. If the devices change from Tx(Rx) into Rx(Tx) directly, the devices don't go into standby mode. Besides, the PLL block only takes the time T5 not T3 for PLL settling time.

Time Formula Description:
Payload Length: **n**
Data rate: **rate**
Sync 0x43 [4:0]: **s**
Address 0x42[7:6]: **a**
SCK Frequency: **SCK**
CRC Check 0x43 [6:5]: **r**
SOF: 1 byte
PID: When STARNET 0x40[7] =1, PID = 1 byte, else PID=0
Slot time 0x47 [3:0]: **SLT**
ACKTOSLOT 0x49 [7:0]: **ATS**
BACKOFFWIN 0x58 [7:0]: **BFW**

Formula Description
T1 must be over 0.8ms for Xtal and regulator settling when using external Xtal with internal oscillator. Only 200us is needed for regulator settling when system reference clock is shared with MCU
Burst Mode : T2 = (n+1) *8 /SCK Non-Burst Mode : T2 = (2*n) *8 /SCK
T3 = 120us
T4 = (s+SOF+a+n+r)*8/rate + 15us
T5 =60us
T6=(s+SOF+PID+a+r)*8/rate
T7= ATS*SLT*10us
T8= BFW*SLT*10us
T9= 10us

Table 5: Delay Times Information

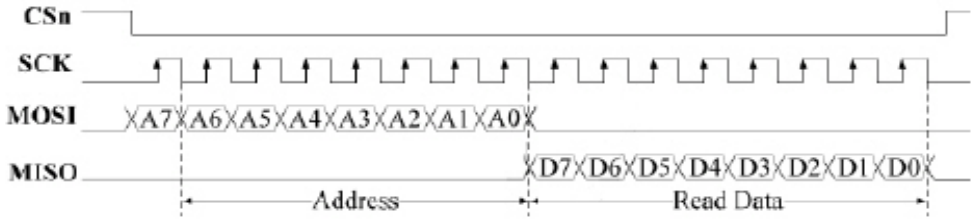
T1: Initiation setting time
T2: TX: Write data to FIFO; RX: Read data from FIFO
T3: RF delay time for transmit data. (Waiting for PLL settling)
T4: Packet Input Data Transmission Time
T5: RF delay for transmit ACK data. (Waiting for PLL settling)
T6: ACK packet Data Transmission Time
T7: ACK waiting time, must be larger then T5+T6, programmable from 10us to 32ms.
T8: Retransmit waiting time, programmable from 0 to 32ms
T9: Packet Handling Time

8. SPI Interface Timing Diagram

A. SPI interface Read / Write for Register

When A7 = 1, MCU read value from EM198850 register.
When A7 = 0, MCU write value to EM198850 register.

SPI Read A7=1



SPI Write A7=0

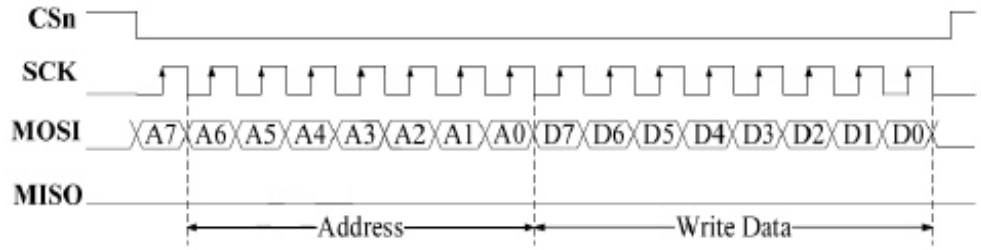
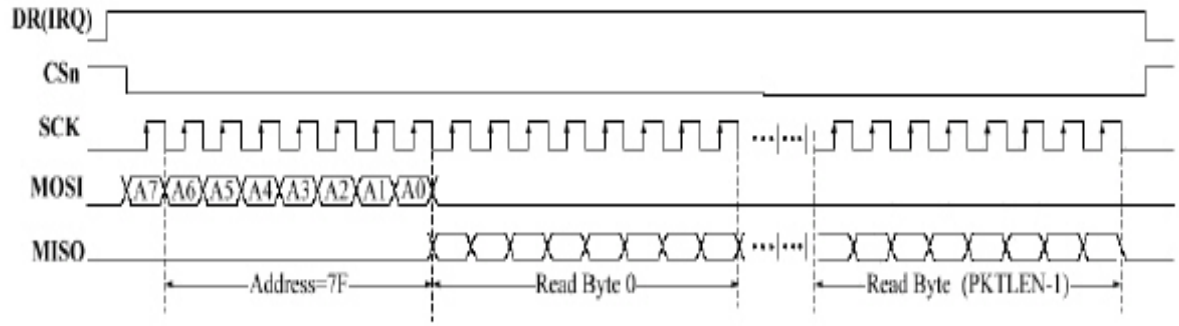


Figure 16: SPI Read/Write Register Timing Diagram

B. SPI interface Read / Write for Buffer mode

- ✓ When 0x40[6] = 1, SPI interface switch to Burst mode.
- ✓ Address = 0x7F for FIFO address

Burst Mode:
Buffer Read A7=1 (PKTCNT=1)



Buffer Write A7=0 (PKTCNT=1)

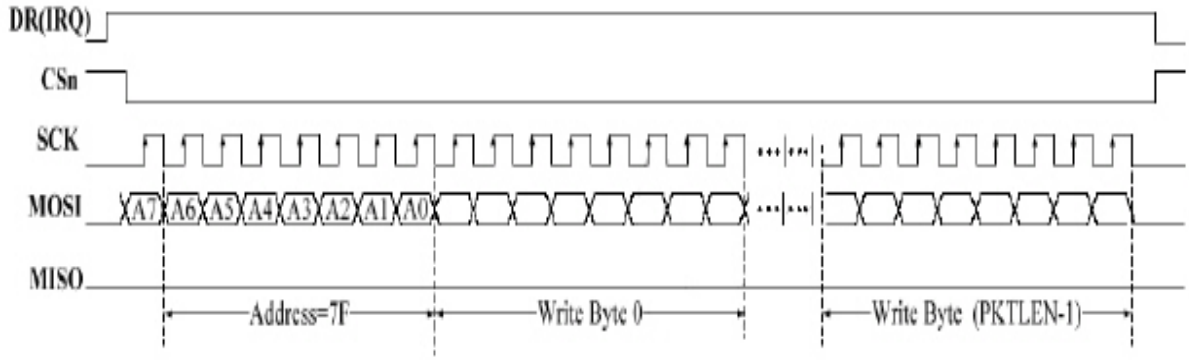
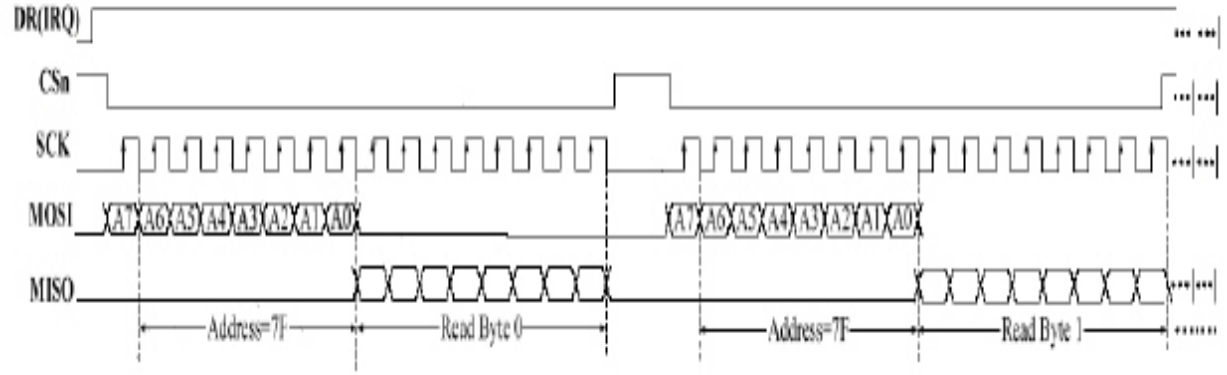


Figure 17: SPI interface switch to Burst mode when 0x40[6]=1

- ✓ When 0x40[6] = 0, SPI interface switch to Non-Burst mode.
- ✓ Address = 0x7F for FIFO address

Non-Burst Mode:
Buffer Read A7=1 (PKTCNT=1)



Buffer Write A7=0 (PKTCNT=1)

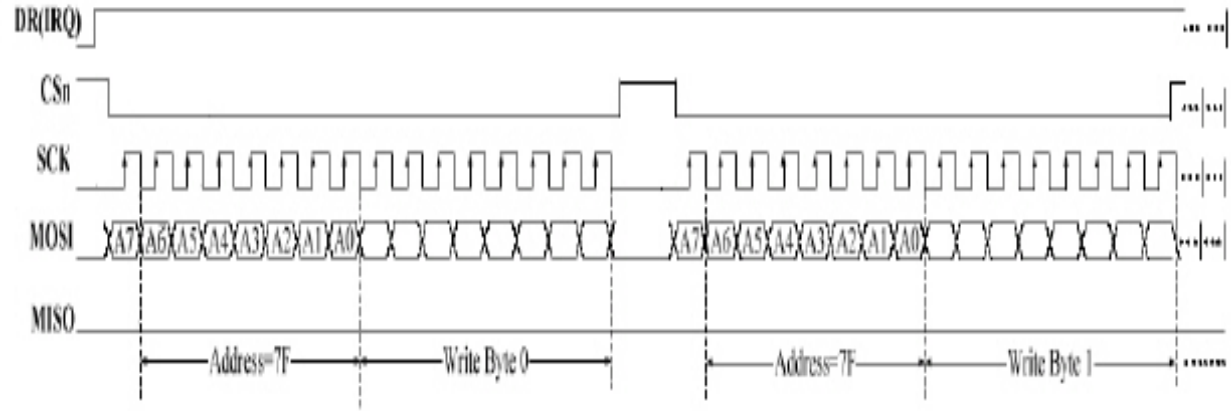


Figure 18: SPI interface switch to Non-Burst mode when 0x40[6]=0

9. SPI Programmable Function Description

- **Data Rate & Crystal Frequency Register Setting**

Data Rate	XO Freq.	R00	R01	R29	R03						R0A	R4E	R42	R46	R2D	R29	R2E	R2D	R26	R0C	R28	R4A
(Mbps)	(MHz)	5	0	5	5	4	3	2	1	0	5	[7:0]	[5:0]	[5:3]	[2:0]	[3:2]	0	5	3	5	3	[7:0]
1.6	12	1	0	1	0	0	0	1	1	0	1	0x02	01111	110	100	10	0	1	0	0	1	0x27
1	12	1	0	1	0	0	0	1	1	0	0	0x02	11000	001	010	10	1	0	1	1	0	0x3F
1.6	16	1	1	x	0	0	1	0	0	0	1	0x01	1010	110	100	10	0	1	0	0	1	0x27
1	16	1	1	x	0	0	1	0	0	0	0	0x01	10000	001	010	10	1	0	1	1	0	0x3F
1.6	24	0	1	1	0	0	1	1	0	0	1	0x02	01111	110	100	10	0	1	0	0	1	0x27
1	24	0	1	1	0	0	1	1	0	0	0	0x02	11000	001	010	10	1	0	1	1	0	0x3F

Table 6: Data Rate & Crystal Frequency Register Setting Table

According to the date rate and crystal frequency, find out the corresponding register values before write registers. When write the initial register values, set the relative register values.

- **Description of register R0x0E[7]**
  - 1: set 1 to forbid to write anyone of RF SPI registers address from 0x20 to 0x33
  - 0: set 0 to allow to write anyone of RF SPI registers address from 0x20 to 0x33
  - Example:
    If MCU needs to write register R28, because it is one of RF SPI registers from 0x20 to 0x33, MCU writes register sequence from R0E[7] = 0 → R28 → R0E[7] =1

- **Operation Mode Register Setting in Direct Mode**

Operation Mode	R0C	R28	R00	R00	R01	R44	R43	R00					R40		R41	R7F
	5	3	7	5	[3:1]	[6:0]	[4:0]	6	4	3	1	0	1	0	[7:0]	[7:0]
Tx Device in Direct Mode	0	1	1	1*b	010	0x01	0x00	0	0	1	1	1	1	0	0x80	0x00
Rx Device in Direct Mode	0	1	1	1*b	010	0x08	0x04	0	1	0	1	1	0	1	0x81	x

Table 7: Operation Mode Register Setting Table

*b: the register value of R00[5] is selected by the Table 7. It's determined by Xtal frequency.

Write Register Sequence from R0C → R0E[7]=0 → R28 → R0E[7] =1 → R00 → R00 → R01 → R44 → R43 → R00 → R40 → R41 → R7F into direct mode

- **RF Status Indication**

RF Status indication	R07[6]	R2E[5]
RSSI[5:0]	0	1
{RSSI[5:1], LD}	1	1

Table 8: RF Status Indication Table

- When set R0x07[6] = 0 & R2E[5] =1,
  - When PLL turns on, MCU needs to wait 150usec, then MCU reads R0x4B[5:0] to get the RSSI digital output value, RSSI[5:0].

- Write Register Sequence from R07 → R0E[7]=0 → R2E → R0E[7] =1

◆ When set R0x07[6] = 1 & R2E[5] =1,
- When PLL turns on, MCU needs to wait 150usec, then MCU reads R0x4B[5:1] to get the RSSI digital output value, RSSI[5:1].
- When PLL turns on, MCU needs to wait 350usec, then MCU reads R0x4B[0] to get the LD signal (PLL lock detection indication).
- Write Register Sequence from R07 → R0E[7]=0 → R2E → R0E[7] =1

● **Operation Mode Register Setting *in Normal Operation Condition***

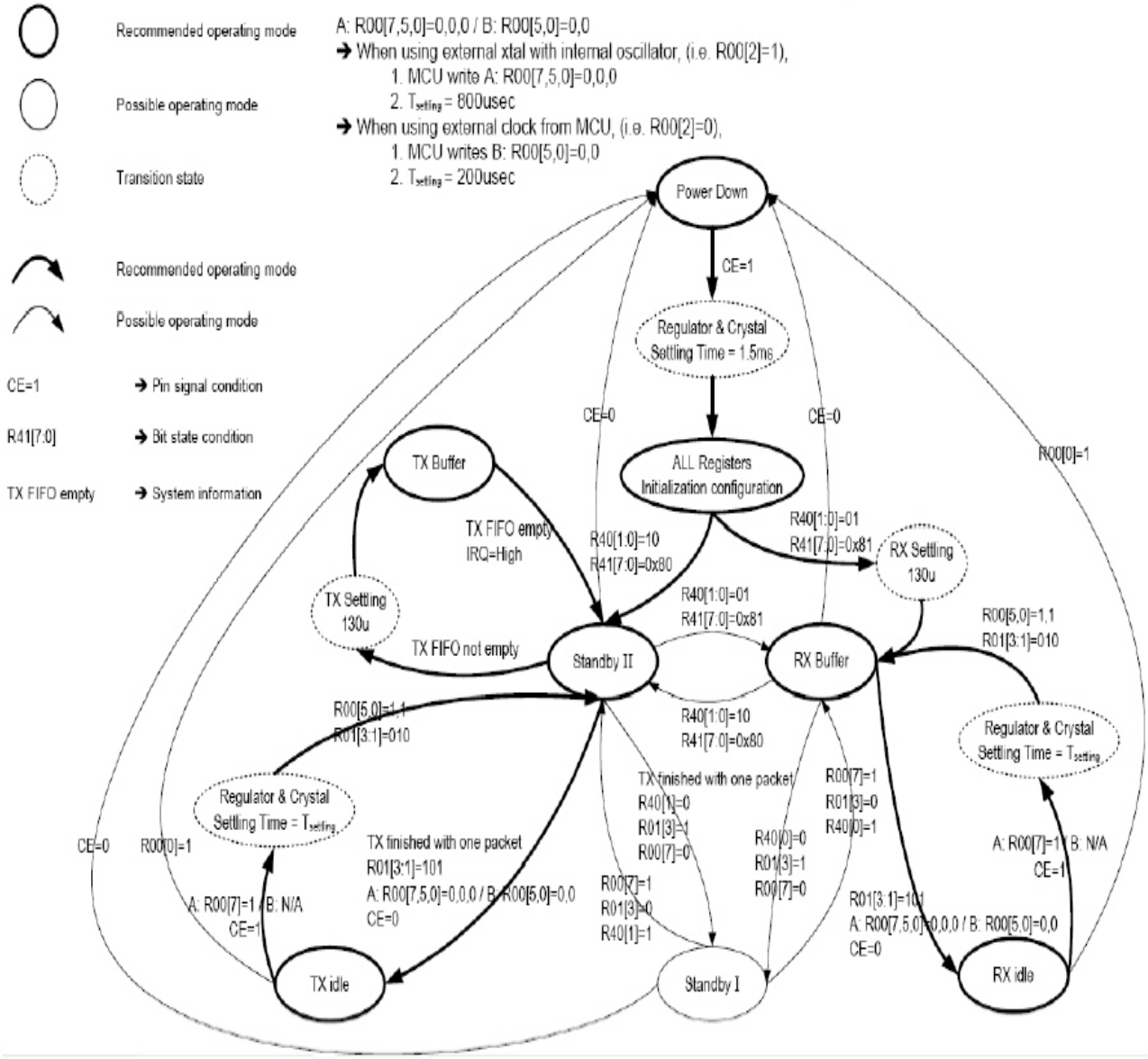


Figure 19: Operation Mode Register Setting in Normal Operation Condition

- **Channel Change in Buffer Mode:**
  - Write 0x02[6:0] as the table listed below

CH_NO	0x02[6:0]
1	0x01
2	0x02
• • •	• • •
62	0x3E
63	0x3F
• • •	• • •
80	0x50
81	0x51
82	0x52

Table 9: Channel Change Control Table

- **Frequency Deviation Control:**

0x0a[3:0]	Frequency Deviation (kHz)
0 0 1 1	200
0 1 1 1	400
1 1 0 1	500

Table 10: Frequency Deviation Setting

- **Battery Detection Level Setting**

Threshold Voltage		
0x29[1:0]	**0x26[7]=0**	**0x26[7]=1**
00	**1.9**	**1.7**
01	**2.0**	**1.8**
10	**2.1**	**1.9**
11	**2.2**	**2.0**

Table 11: Battery Detection Level Setting

  - Write Register Sequence from R0E[7]=0 → R29 → R26 → R0E[7]=1 to change the battery detection level.
  - Battery detection function is only active when CE = High.

- **RX/TX FIFO Reset Function**

When MCU writes R0x4D[0] = 1, FIFO will be reset. For RX device, because RX receiver is always active, RF blocks need 120usec settling time after FIFO reset

10. Serial Register Format of Power ON Initialization

Follow the serial register addresses showed below to initialize the EM198850 RF transceiver. The register address 0x40[7:0] and 0x41[7:0] are used to set the device into TX or RX mode.

The values showed in table are for the condition listed below:
– Date Rate = 1Mbps
– Xtal Frequency = 12MHz
– TX/RX Buffer Mode
– Package Length = 8 bytes
– Syn. Length = 4 bytes
– Disable Star Network

Register Address	Initialization Register		Description
	TX	RX	
0x4E	0x02		Value reference to Table 6
0x4D	0x01		
0x42	0x98		Value reference to Table 6
0x43	0xC4		
0x44	0x08		
0x45	0x10		
0x46	0x09		Value reference to Table 6
0x47	0x11		
0x48	0x01		
0x49	0x8A		
0x4A	0x27		Value reference to Table 6
0x4B	0x00		
0x4C	0x06		
0x50	0x00		
0x51	0x11		
0x52	0x22		
0x53	0x33		
0x54	0x44		
0x55	0x55		
0x56	0x66		
0x57	0x77		
0x58	0x08		
0x00	0xE5		Value reference to Table 6
0x01	0x84		Value reference to Table 6
0x02	0x00		
0x03	0xC6		Value reference to Table 6
0x04	0x00		
0x05	0x40		
0x06	0x5D		

0x07	0x18	
0x08	0x40	
0x09	0x18	
0x0A	0x47	Value reference to Table 6
0x0B	0x0B	
0x0C	0xE0	Value reference to Table 6
0x0D	0x4F	
0x0E	0x11	
0x0F	0x1C	
0x20	0xAD	
0x21	0x64	
0x22	0x00	
0x23	0xC3	
0x24	0xBD	
0x25	0xA2	
0x26	0x1A	Value reference to Table 6
0x27	0x09	
0x28	0x00	Value reference to Table 6
0x29	0xB8	Value reference to Table 6
0x2A	0x71	
0x2B	0x06	
0x2C	0x80	
0x2D	0x1A	Value reference to Table 6
0x2E	0x09	
0x2F	0x64	
0x30	0xC0	
0x31	0x00	
0x32	0x40	
0x33	0x3B	
0x00	0xA7	
0x32	0x4A	
0x00	0xE5	Value reference to Table 6
0x0E	0x91	
0x40	0x51	
0x41	0x81	
0x0C	0xC0	
0x02	0x80	
0x04	0x4A	
0x05	0xDA	
0x06	0xFA	
After waiting 250uS, MCU continues reading 0X4B[5:0] 5times.		
0x4A	“0x4B (Max)-4	Select maximum 0x4B value and minus 4, then write this result into 0x4A
0x05	0x40	

0x02	0x00	
0x0C	0xE0	