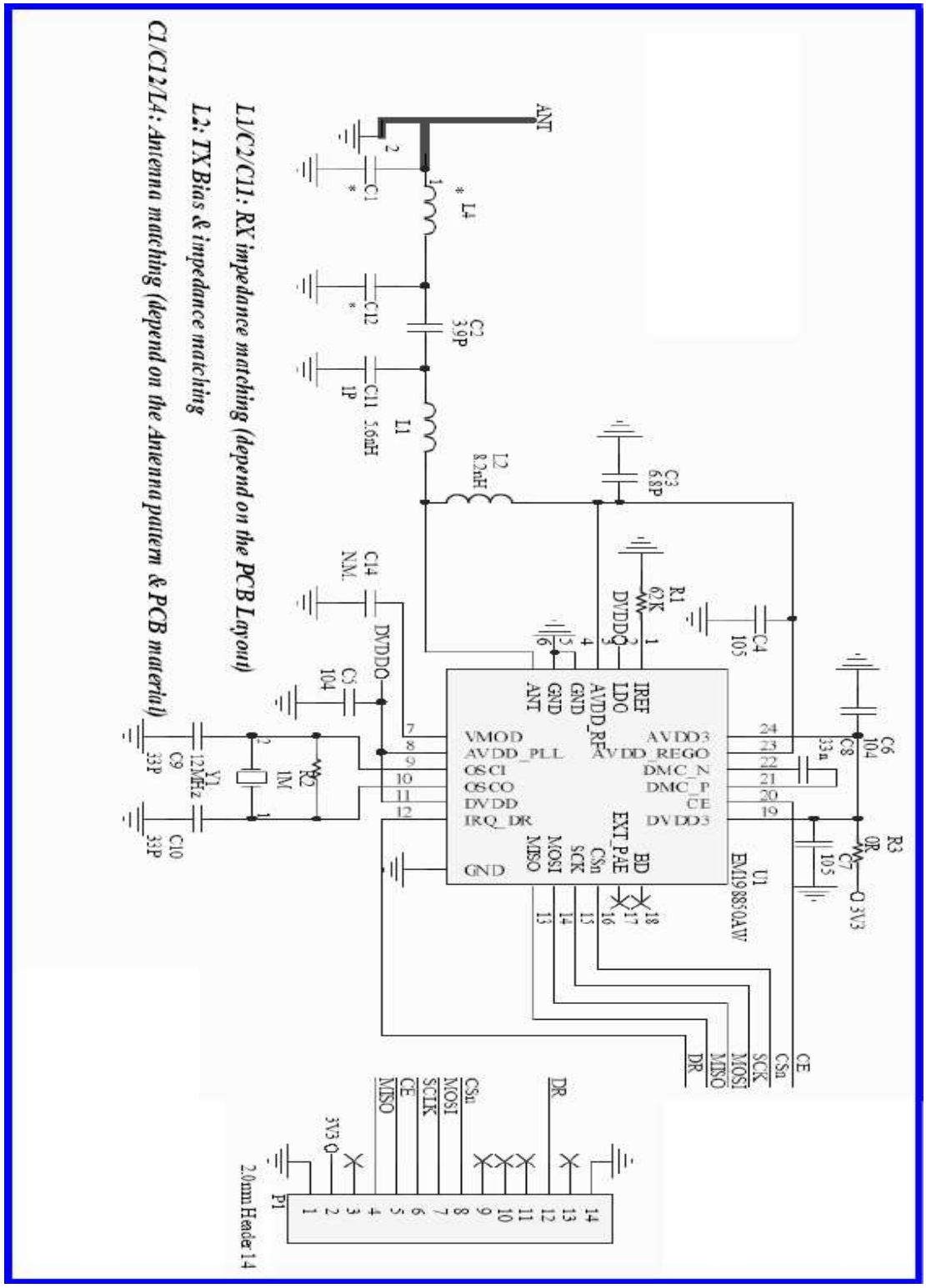
1. Module Description

Schematic & PCB Layout



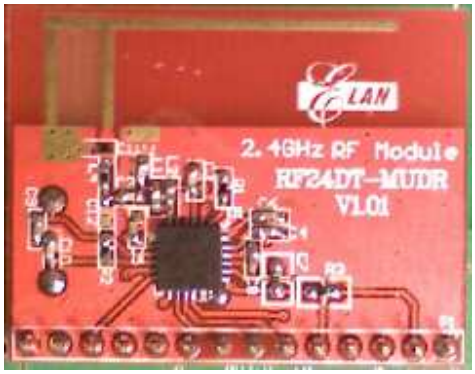


Figure 1: Module PCB Board

Pin Assignment for Connector

PIN	Description	PIN	Description
1	GND	8	SPI_CSn
2	VDD	9	NC
3	NC	10	NC
4	SPI_MISO	11	NC
5	CE	12	DR_IRQ
6	SPI_CLK	13	NC
7	SPI_MOSI	14	GND

Table 1: Module Pin out

PCB Layout Consideration

1. Standard FR4 material is used in a two-layer PCB
2. Resistor for pin 10 and pin11 must close with pin.
3. Pin6 connects to L1 with the shortest distance. L2 places close to pin3.
4. In order to secure isolation between pin3 and pin6, short pin5 and pin4 to ground.
5. RF IO's trace must use 50 ohm transmission line.
6. The trace doesn't pass through below RF_IO's path.

Description of TX/RX Link Operation Timing Diagram

The following descriptions in this section are showed the TX/RX link operation timing diagram.

- **TX/RX Link Operation Timing Diagram without Auto ACK in Buffer Mode**

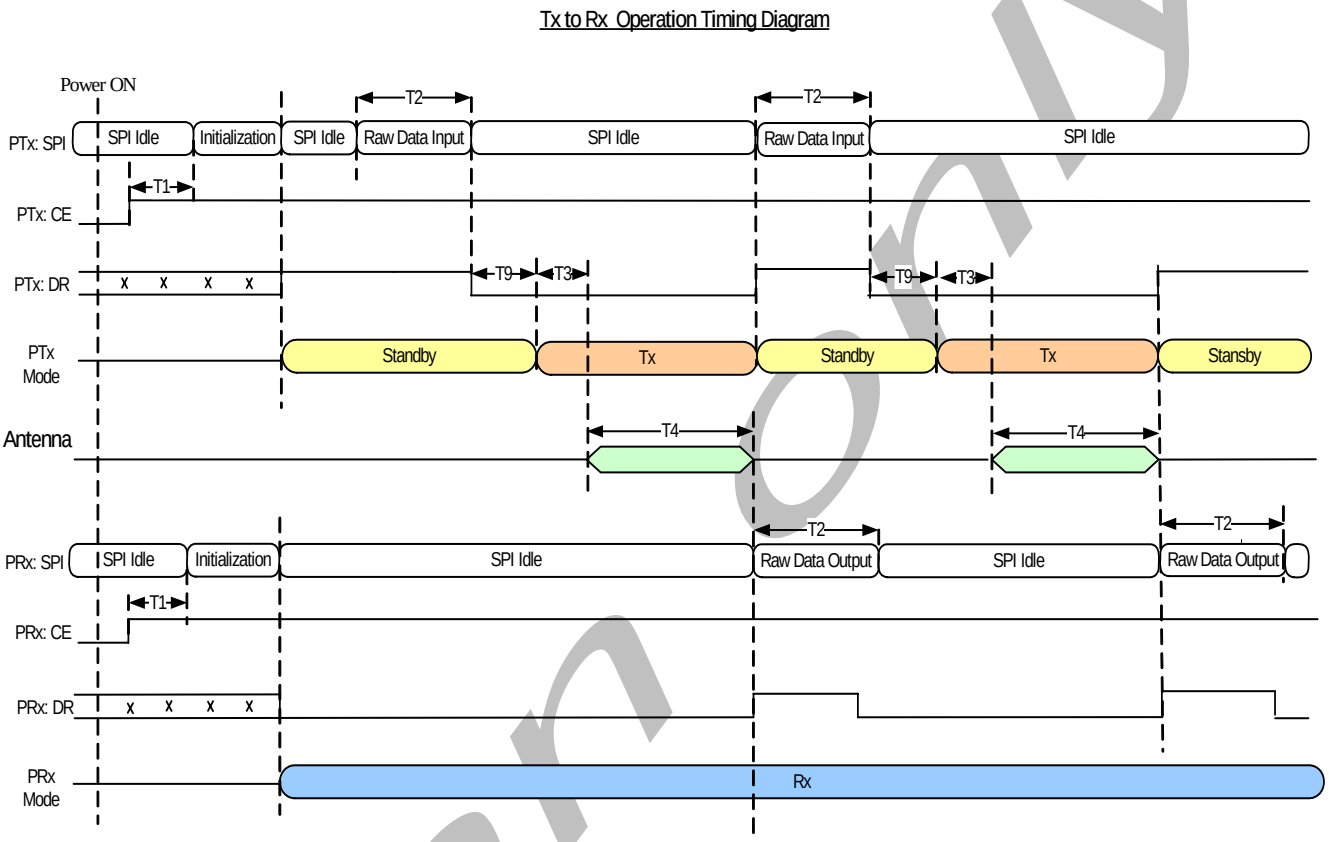


Figure 10: TX/RX Link Operation Timing Diagram without Auto ACK in Buffer Mode

Condition: Disable Auto ACK 0x40[3:2] = 00
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

The PTX DR is asserted after the packet is transmitted by the PTX.
The PRX DR is asserted after the packet is received by the PRX.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

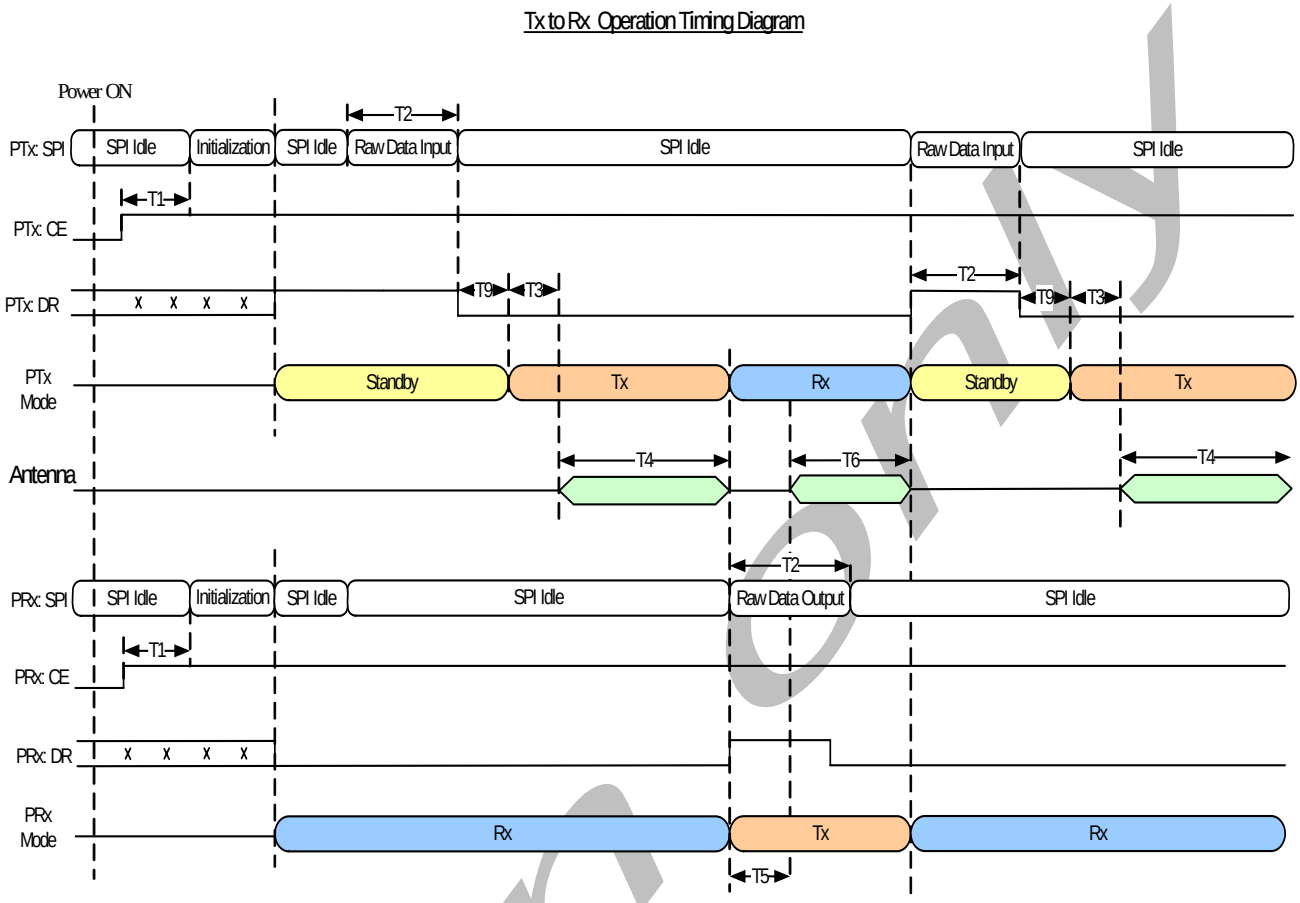


Figure 11: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

When the transmission ends the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to MCU. When the PRX device receives the packet it responds with an interrupt to MCU.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

  ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX receives ACK

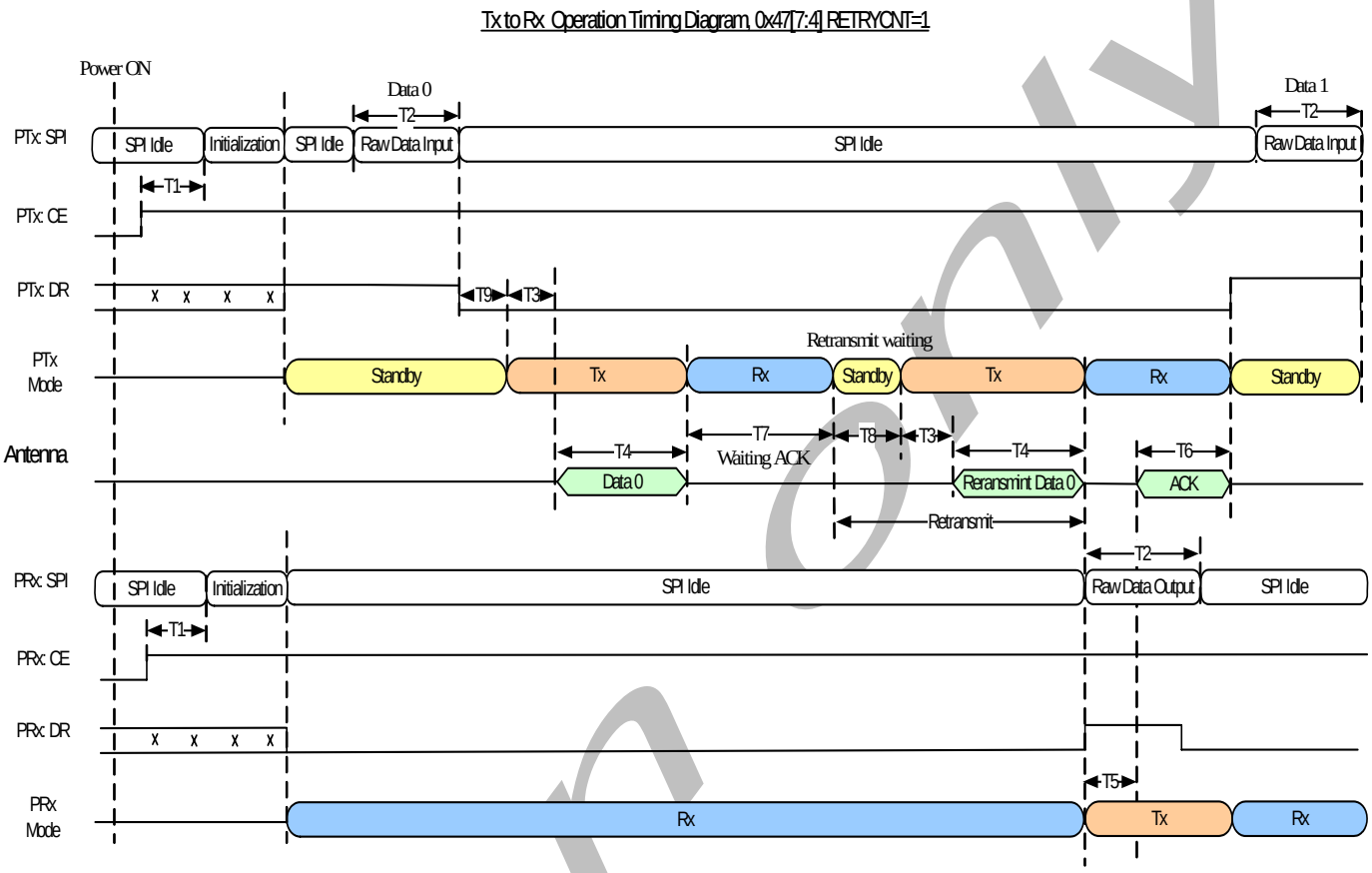


Figure 12: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

After Data 0 is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits specified time for ACK packet (T7). If it is not in specified time slot, the PTX retransmit the Data 0. When the retransmitted packet is received by the PRX, the DR of PRX is asserted and ACK is transmitted back to the PTX. When the ACK is received by the PTX, the DR of PTX is asserted.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

  ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX doesn't receive ACK again ➔ Packet Loss Count + 1

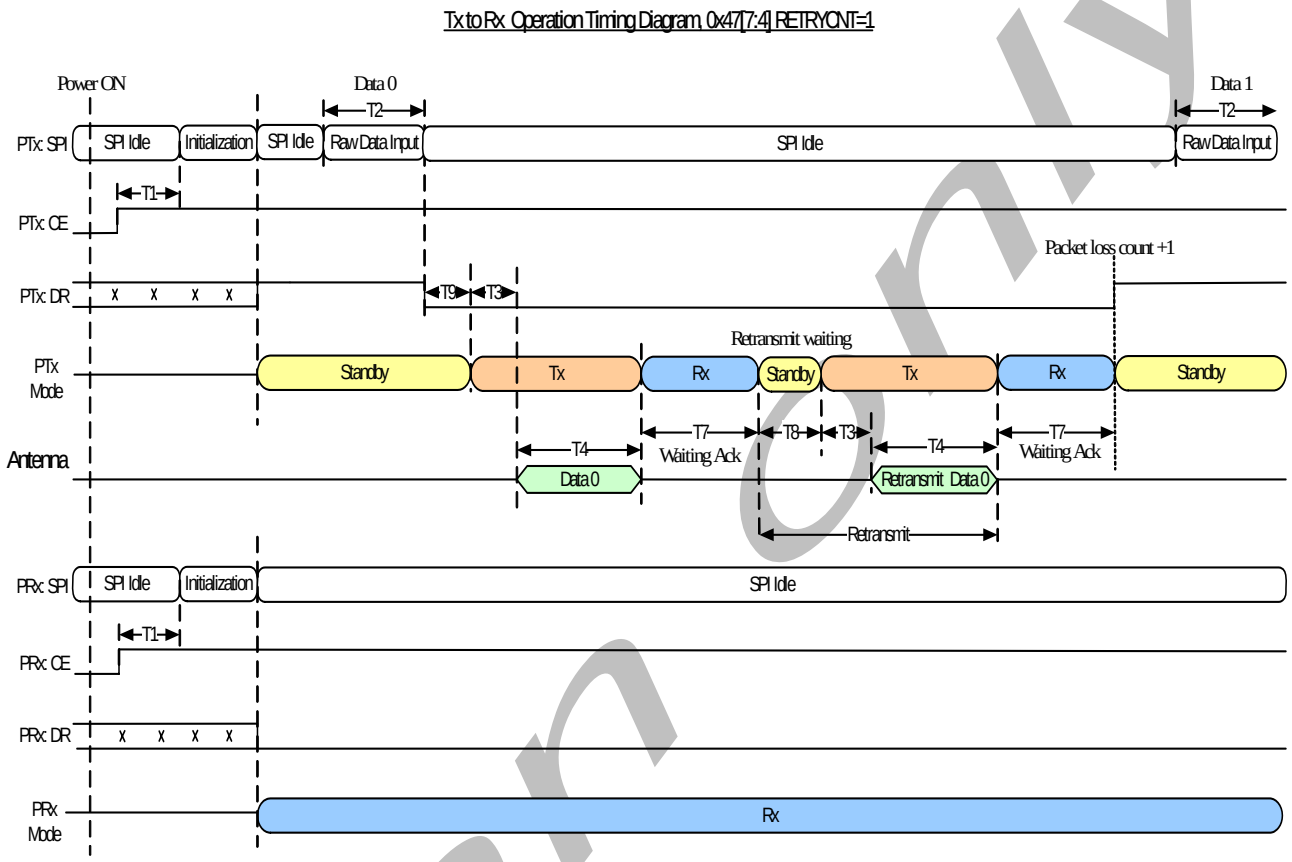


Figure 13: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

When the PTX retransmit counter exceeds the RETRYCNT 0x47[7:4], the PTX DR is asserted and automatically adds one to packet loss count (0x4F[7:3]). Then the payload in PTX FIFO will be removed.

- **TX/RX Link Operation Timing Diagram in Direct Mode**

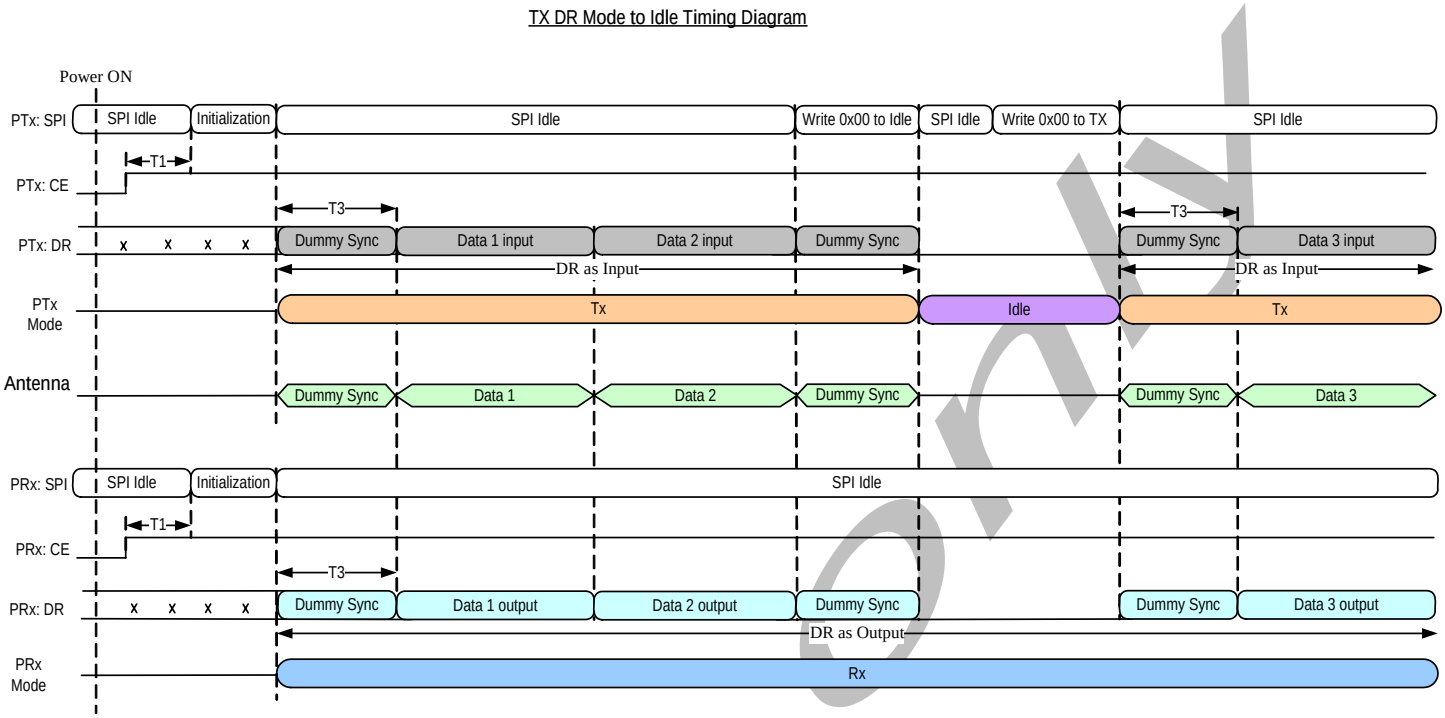


Figure 14: TX/RX Link Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, you must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. Figure 14 shows the timing diagram of operation mode change from direct mode into idle mode, then into direct mode again.

- **TX/RX Switching Operation Timing Diagram in Direct Mode**

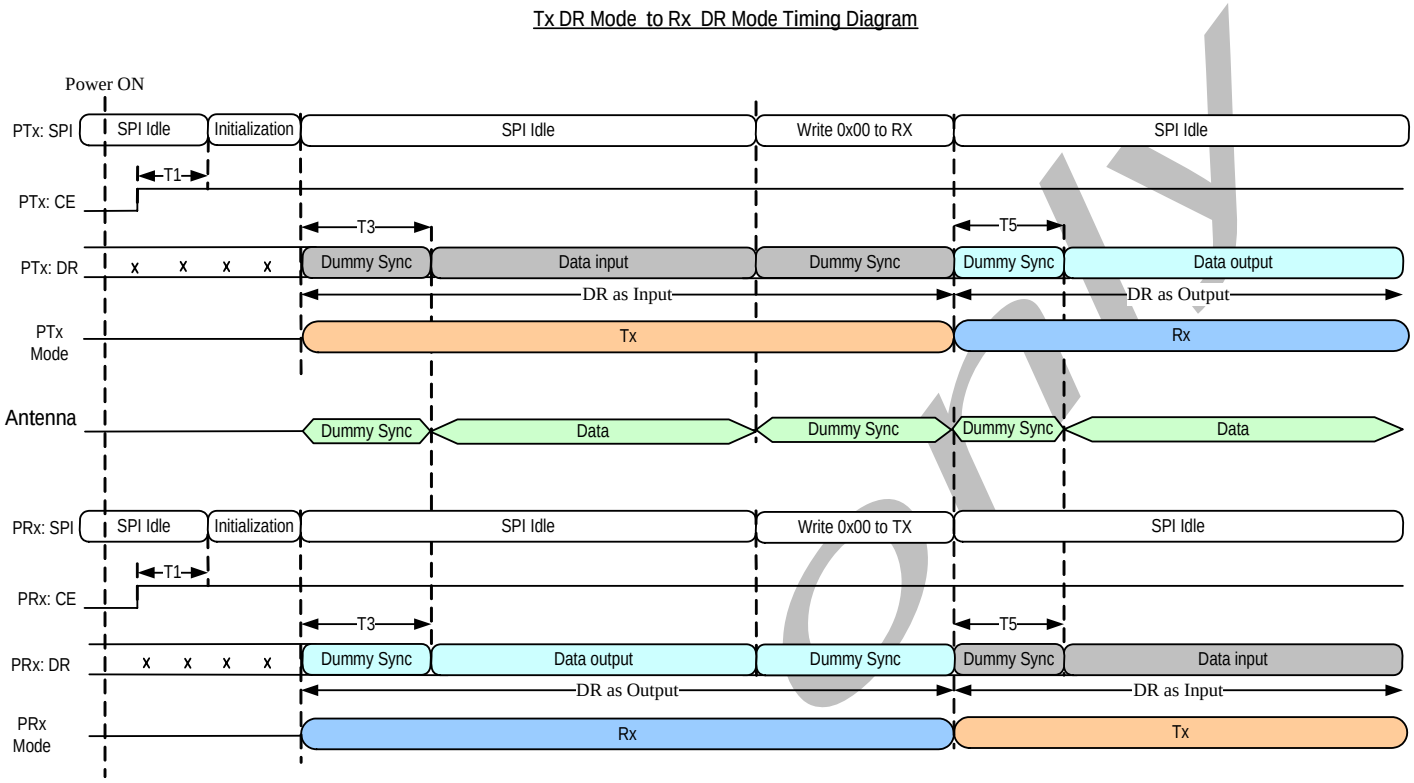


Figure 15: TX/RX Switching Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, you must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. Figure 15 shows the timing diagram for RX/TX switching operation. When the devices change from TX(RX) into RX(TX) directly, the devices don't go into standby mode. Besides, the PLL block only takes the time T5 not T3 for PLL settling time.