Serial Register Format of Power ON Initialization-C Ver.

Follow the serial register addresses showed below to initialize the EM198850AW RF transceiver. The register address 0x40[7:0] and 0x41[7:0] are used to set the device into TX or RX mode.

The values showed in table are for the condition listed below:

– Date Rate = 1Mbps

– Xtal Frequency = 12MHz

– TX/RX Buffer Mode

– Package Length = 8 bytes

– Syn. Length = 4 bytes

– Disable Star Network

Register Address	**Initialization Register**		**Description**
	TX	**RX**	
0x4E	0x02		Value reference to Table 4
0x4D	0x01		
0x42	0x98		Value reference to Table 4
0x43	0xC4		
0x44	0x08		
0x45	0x10		
0x46	0x09		Value reference to Table 4
0x47	0x11		
0x48	0x01		
0x49	0x8A		
0x4A	0x27		Value reference to Table 4
0x4B	0x00		
0x4C	0x06		
0x50	0x00		
0x51	0x11		
0x52	0x22		
0x53	0x33		
0x54	0x44		
0x55	0x55		
0x56	0x66		
0x57	0x77		
0x58	0x08		
0x00	0xE5		Value reference to Table 4
0x01	0x84		Value reference to Table 4
0x02	0x00		

0x03	0xC6	Value reference to Table 4
0x04	0x00	
0x05	0x40	
0x06	0x5D	
0x07	0x18	
0x08	0x40	
0x09	0x18	
0x0A	0x47	Value reference to Table 4
0x0B	0x0B	
0x0C	0xE0	Value reference to Table 4
0x0D	0x4F	
0x0E	0x11	
0x0F	0x1C	
0x20	0xAD	
0x21	0x64	
0x22	0x00	
0x23	0xC3	
0x24	0xBD	
0x25	0xA2	
0x26	0x1A	Value reference to Table 4
0x27	0x09	
0x28	0x00	Value reference to Table 4
0x29	0xB8	Value reference to Table 4
0x2A	0x71	
0x2B	0x06	
0x2C	0x80	
0x2D	0x1A	Value reference to Table 4
0x2E	0x09	
0x2F	0x64	
0x30	0xC0	
0x31	0x00	
0x32	0x40	
0x33	0x3B	
0x00	0xA7	
0x32	0x4A	
0x00	0xE5	Value reference to Table 4
0x0E	0x91	
0x40	0x51	
0x41	0x81	

0x0C	0xC0	
0x02	0x80	
0x04	0x4A	
0x05	0xDA	
0x06	0xFA	
After waiting 250uS, MCU continues reading 0X4B[5:0] 5times.		
0x4A	“0x4B (Max)-4	Select maximum 0x4B value and minus 4, then write this result into 0x4A
0x05	0x40	
0x02	0x00	
0x0C	0xE0	

RF Status Indication

RF Status indication	R07[6]	R2E[5]
RSSI[5:0]	0	1
{RSSI[5:1], LD}	1	1

Table 1: RF Status Indication Table

- When set R0x07[6] = 0 & R2E[5] =1, MCU read R0x4B[5:0] to get the RSSI digital output value, RSSI[5:0].
- When set R0x07[6] = 1 & R2E[5] =1, MCU read R0x4B[5:0] to get the RSSI value only at R0x4B[5:1] mapping to RSSI[5:1] and LD (PLL lock detection indication) at R0x4B[0].

Channel Change in Buffer Mode:

- Write 0x02[6:0] as the table listed below

CH_NO	0x02[6:0]
1	0x01
2	0x02
• • •	• • •
62	0x3E
63	0x3F
• • •	• • •
80	0x50
81	0x51
82	0x52

Table 2: Channel Change Control Table

Frequency Deviation Control:

0x0a[3:0]	Frequency Deviation (kHz)
0 0 1 1	200
0 1 1 1	400
1 1 0 1	500

Table 3: Frequency Deviation Setting

RX/TX FIFO Reset Function

When MCU writes R0x4D[0] = 1, FIFO will be reset. For RX device, because RX receiver is always active, RF blocks need 120usec settling time after FIFO reset.

SPI Programmable Function Description

1. Data Rate & Crystal Register Setting

Data Rate	XO Freq.	R00	R01	R29	R03						R0A	R4E	R42	R46	R2D	R29	R2E	R2D	R26	R0C	R28	R4A
(Mbps)	(MHz)	5	0	5	5	4	3	2	1	0	5	[7:0]	[5:0]	[5:3]	[2:0]	[3:2]	0	5	3	5	3	[7:0]
1.6	12	1	0	1	0	0	0	1	1	0	1	0x02	01111	110	100	10	0	1	0	0	1	0x27
1	12	1	0	1	0	0	0	1	1	0	0	0x02	11000	001	010	10	1	0	1	1	0	0x3F
1.6	16	1	1	x	0	0	1	0	0	0	1	0x01	1010	110	100	10	0	1	0	0	1	0x27
1	16	1	1	x	0	0	1	0	0	0	0	0x01	10000	001	010	10	1	0	1	1	0	0x3F
1.6	24	0	1	1	0	0	1	1	0	0	1	0x02	01111	110	100	10	0	1	0	0	1	0x27
1	24	0	1	1	0	0	1	1	0	0	0	0x02	11000	001	010	10	1	0	1	1	0	0x3F

Table 4: Data Rate & Crystal Frequency Register Setting Table

According to the date rate and crystal frequency, find out the corresponding register values before write registers. When write the initial register values, set the relative register values.

2. Description of register R0x0E[7]

- 1: set 1 to forbid to write anyone of RF SPI registers address from 0x20 to 0x33
- 0: set 0 to allow to write anyone of RF SPI registers address from 0x20 to 0x33
- Example:
  If MCU needs to write register R28, because it is one of RF SPI registers from 0x20 to 0x33, MCU writes register sequence from R0E[7] = 0 □ R28 □ R0E[7] =1

3. Operation Mode Register Setting in Direct Mode

Operation Mode	R0C	R28	R00	R00	R01	R44	R43	R00					R40		R41	R7F
	5	3	7	5	[3:1]	[6:0]	[4:0]	6	4	3	1	0	1	0	[7:0]	[7:0]
Tx Device in Direct Mode	0	1	1	1*b	010	0x01	0x00	0	0	1	1	1	1	0	0x80	0x00
Rx Device in Direct Mode	0	1	1	1*b	010	0x08	0x04	0	1	0	1	1	0	1	0x81	x

Table 5: Operation Mode Register Setting Table

*b: the register value of R00[5] is selected by the Table 7. It's determined by Xtal frequency.

Write Register Sequence from R0C → R0E[7]=0 → R28 → R0E[7] =1 → R00 → R00 → R01 → R44 → R43 → R00 → R40 → R41 → R7F into direct mode

4. Operation Mode Register Setting
in Normal Operation Condition