DATA SHEET

EM198850AW

2.4 GHz ISM Band Transceiver/Framer IC
(QFN24 4x4x0.8mm package)

Preliminary Specification
(V1.2)

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Revision History

Rev. No.	History	Issue Date	Remark
V1.0	Preliminary Specifications	19-12-2008	
V1.1	Update 1. Current consumption; channel rejection ratio 2. Operating modes timing diagram 3. Star network 4. Application circuit	20-3-2009	
V1.2	1. Registers map update	3-30-2009	

CONTENTS

2.4 GHz ISM Band Transceiver/Framer IC

1. Introduction

The EM198850AW is a CMOS integrated circuit that performs all functions from the antenna to the microcontroller for transmission and reception of a 2.4GHz digital data. This transceiver IC integrates most of the functions required for data transmission into a single integrated circuit. Additionally, the programmability implemented reduces significantly external components count, board space requirements and external adjustments.

Key Features:

- Single-chip FSK transceiver
- Auto ACK & Retransmit
- Star-Network with 6 channels
- Address and CRC computation
- 1/1.6Mbps Data Rate
- 1 ~ 64 bytes Payload Length
- 64 bytes FIFO Size
- 4-wire digital interface (SPI)
- Boost data mode
- Power supply range: 1.8 to 3.6V
- Automatic bypass internal LDO in low supply voltage
- Battery Low Supply Voltage Detector
- Support 4 power modes: Active/Standby/Idle/Power Down
- Operation range: -40 ^{0}C to +85 ^{0}C
- Standard CMOS process
- On-chip VCO, PLL and PLL Loop Filter
- On chip channel filter
- 24-pin- 4x4 QFN package with minimum RF parasitic
- Lead-free packaging

Applications

- Wireless mouse, keyboard, joystick
- Keyless entry
- Alarm and security system
- Home automation
- Surveillance
- Automotive
- Telemetry
- Industrial sensors
- Wireless data communication
- Toys

1.1 Description

The Elan EM198850AW IC is a low-cost, fully integrated CMOS radio frequency (RF) transceiver, combined with dual 64-byte buffered framer block. The RF transceiver is a self-contained, fast-hopping FSK data modem, data rate can be operated up to 1.6Mbps in buffer mode or 2Mbps in direct mode, optimised for use in the widely available 2.4 GHz ISM band. It consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator, a demodulator, modulator, and Auto-ACK protocol engine. A reduced off chip filter is realized by the low IF RX architecture, minimizing the need for external components.

The transceiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments. Typical transmit power is 0dBm and digitally controlled, low-IF receiver architecture results in sensitivity to -92dBm or better, with impressive selectivity. User can program transmitter output power, frequency channels, and protocol setup easily through a SPI interface.

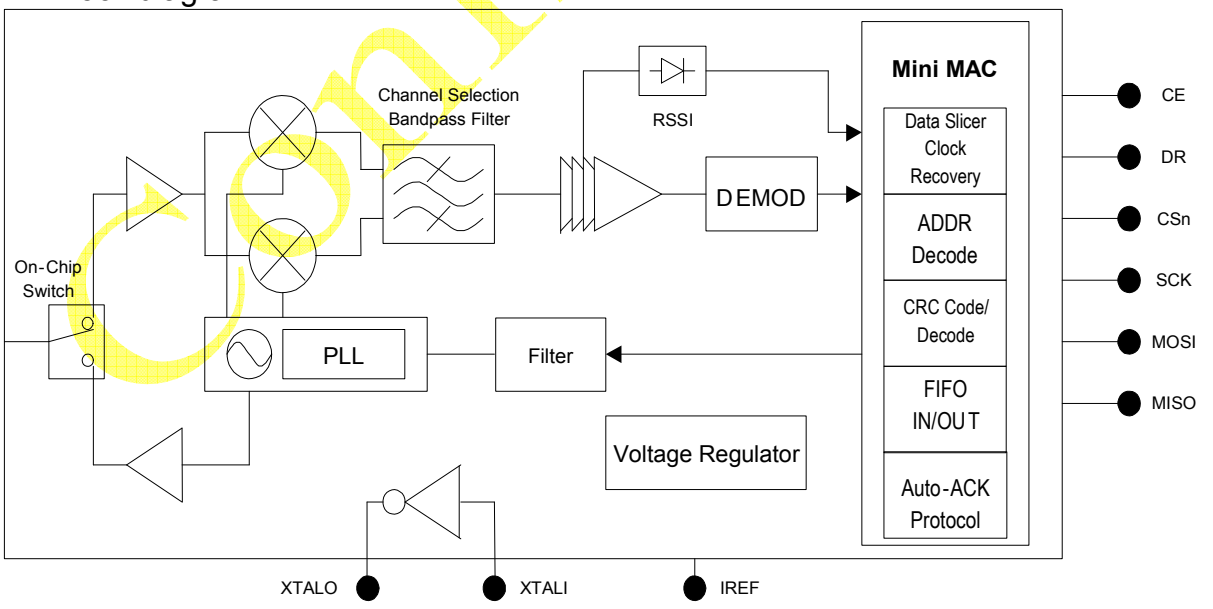
In normal application, the on-chip framer processes and stores the RF data in the background, unloading this critical timing function from the MCU. This lowers MCU speed requirements, expedites product development time, and frees the MCU for implementing additional product features.

Many configurations are possible, depending on the user's specific needs. Transmit data is easily sent over-the-air as a complete frame of data, with syncword, SOF, address, payload, and CRC. Receiving data is just the opposite, using the syncword to train the receiver clock recovery, then the address is checked, then the data is reverse formatted for receive, followed by CRC. All of this is done in hardware to ease the programming and overhead requirements of the baseband MCU.

For longer battery life, power consumption is minimized by automatic enabling of the various transmit, receive, PLL, and PA sections, depending on the instantaneous state of the chip. An idle mode is also provided for ultra low current consumption.

This product is available in 24-lead 4x4 mm JEDEC standard QFN package and Lead-free RoHS compliant, featuring an exposed pad on the bottom for best RF characteristics.

1.2 Block diagram



- Fig. 1 -

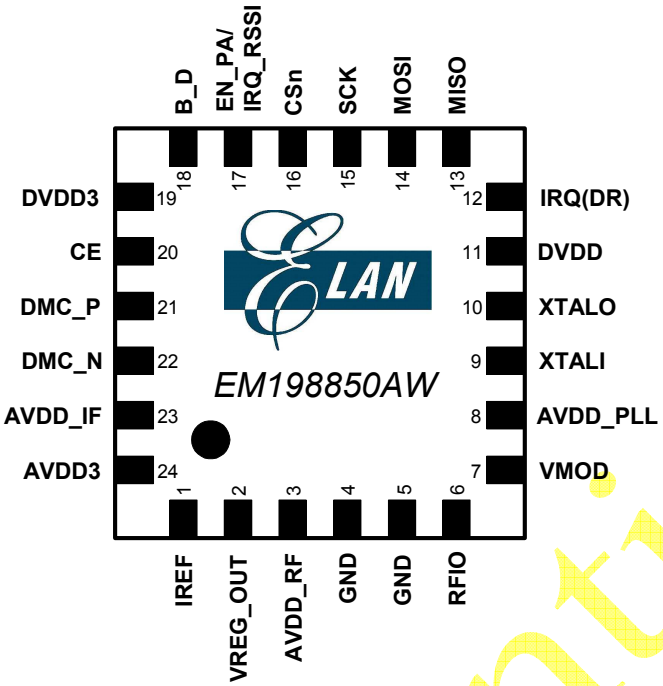
2. Pins Names and Pins Assignment

2.1 Pins names

SYMBOL	Type	PIN	DESCRIPTION
IREF	Analog Input	1	Reference resistor pin, connect to an external resistor
VREG_OUT	PWR	2	On-chip voltage regulator output
AVDD_RF	PWR	3	RF power supply
GND	GND	4	Ground connection
GND	GND	5	Ground connection
RFIO	Analog I/O	6	RF input/output
VMOD	Analog I/O	7	Connect to external capacitor for filtering
AVDD_PLL	PWR	8	PLL power supply
XTALI	Analog I/O	9	Crystal pin1
XTALO	Analog I/O	10	Crystal pin2
DVDD	PWR	11	Digital power supply
IRQ(DR)	Digital I/O	12	a. Interrupt signal in buffer mode b. Data input/data output in direct mode
MISO	Digital I/O	13	a. Master input/slave output in SPI mode b. Data output in buffer mode
MOSI	Digital I/O	14	a. Master output/slave input in SPI mode b. Data input in buffer mode
SCK	Digital I/O	15	SPI input clock
CSn	Digital I/O	16	SPI selection/programming enable
EN_PA/IRQ_RSSI	Digital I/O	17	Be configured as the two output modes: 1. To control the external PA chip 2. IRQ_RSSI output high - to indicate the MCU to read the RSSI, RSSI only valid during receiving signal - Let MCU know the channel is occupied
B_D	Digital I/O	18	Battery Low Power Detector
DVDD3	PWR	19	Digital I/O power supply
CE	Digital I/O	20	Chip enable, enable voltage regulator
DMC_P	Analog I/O	21	Demodulator analog output, connect to an external AC coupling capacitor
DMC_N	Analog I/O	22	Demodulator analog output, connect to an external AC coupling capacitor
AVDD_IF	PWR	23	RX IF power supply, voltage regulator output
AVDD3	PWR	24	Voltage regulator input power supply
GND	GND	Exposed pad	

- Table 1 –

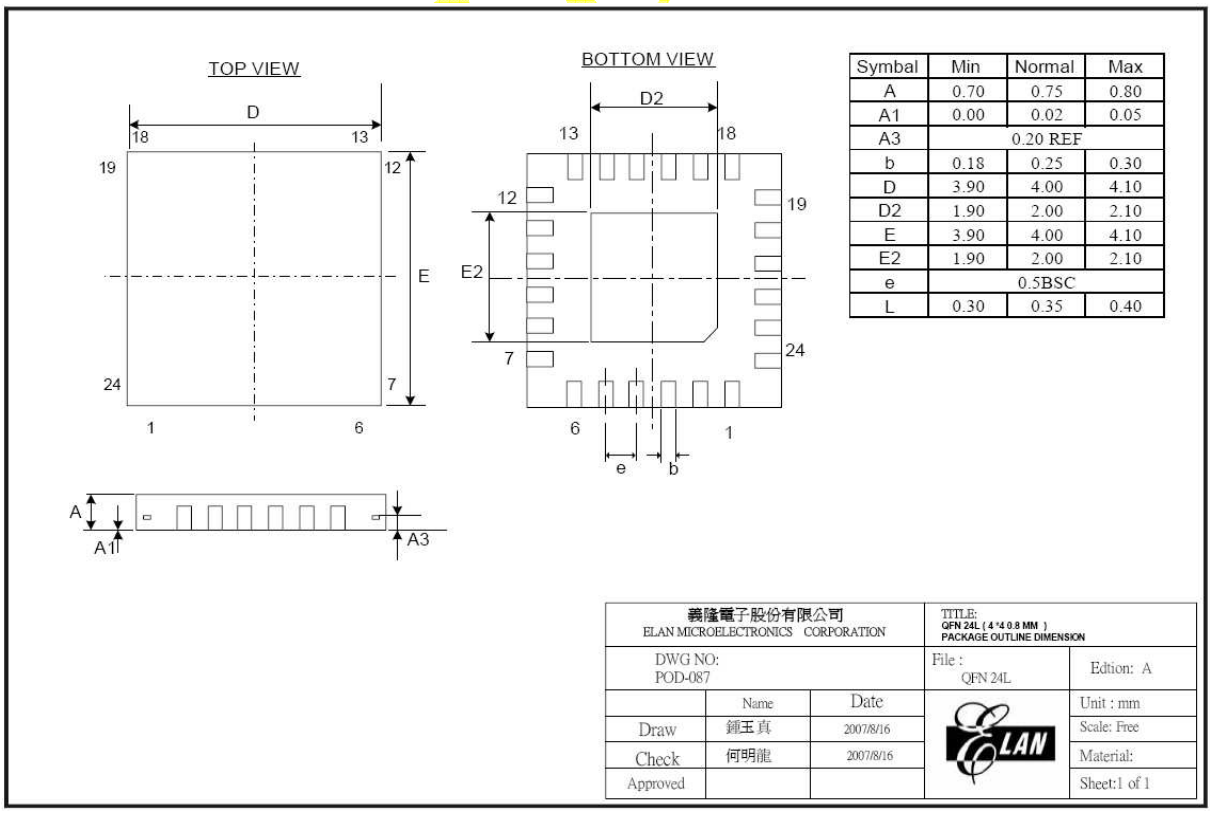
2.2 Pin assignment



- Figure 2 -

2.3 Package Outline

QFN24 Lead Exposed Pad Package, 4x4 mm Pkg.



Symbal	Min	Normal	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D	3.90	4.00	4.10
D2	1.90	2.00	2.10
E	3.90	4.00	4.10
E2	1.90	2.00	2.10
e		0.5BSC	
L	0.30	0.35	0.40

義隆電子股份有限公司
ELAN MICROELECTRONICS CORPORATION

TITLE:
QFN 24L (4 *4 0.8 MM)
PACKAGE OUTLINE DIMENSION

DWG NO: POD-087
File : QFN 24L
Edition: A

	Name	Date
Draw	鍾玉真	2007/8/16
Check	何明龍	2007/8/16
Approved		

Unit : mm
Scale: Free
Material:
Sheet:1 of 1

- Figure 3 -

2.4 Order information

Type number	Package	
	Name	Description
EM198850AW	QFN24	Plastic, quad flat package; no leads; 24 terminals; body 4 x 4 x 0.8 mm

- Table 2 -

3.Electrical Specification

3.1 Absolute Maximum Rating

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Storage Temp.	$T_{STORAGE}$	-40		+125	℃
Supply Voltage	V_S	-0.3		+3.6	VDC
Input RF Level	P_{IN}			+10	dBm
ESD protection	V_{ESD} HBM	2K			V
	MM	200			V

- Table 3 -

Note: 1.Absoute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2.These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

3. ESD of pin6 (RFIO) only can pass 1KV in HBM and 50V in MM.

3.2 Electrical Characteristics

The following specifications are guaranteed for T_A=25℃, V_{CC}=2.5DC.
Measured on EM198850AW reference board.

Parameter	Symbol	Specification			Unit	Conditions and Notes
		Min.	Typ.	Max.		
Supply Voltage						
Supply Voltage	V_{DD}	2.1	3.0	3.6	V	With internal LDO
		1.8		2.1	V	Internal circuits will sense the V_{DD} and bypass the internal LDO
Core Supply Voltage	V_{DD_CORE}	1.7	1.8	2.1	V	
Operating ambient temperature	T_{amb}	-40	25	+85	℃	
Current Consumption						
Current Consumption - TX	I_{DD_TX}		20		mA	0dBm output power
Current Consumption - RX	I_{DD_RX}		23		mA	
Standby I mode current	I_{DD_STBI}		1		mA	Xtal ON / Regulator ON
Standby II mode current	I_{DD_STBII}		2.5		mA	Xtal ON / Regulator ON
Idle mode current	I_{DD_IDLE}		100		uA	Keep registers content
Supply current in power down	I_{DD_PD}		<1		uA	
Battery low power detector	V_{TH}	1.7		2.2	V	V_{TH} config. by register, Logic High output when supply less than V_{TH}
Digital Inputs						
Logic input high	V_{IH}	0.7		3.6	V	
Logic input low	V_{IL}	V_{SS}		0.3V_{DD}	V	
Digital Outputs						
Logic output high	V_{OH}	V_{DD}-0.3		V_{DD}	V	
Logic output low	V_{OL}	V_{SS}		0.3	V	
Clock Signals						
SPI_CLK rise, fall time	T_{r_spi}			25	nS	Requirement for error-free register reading, writing.
SPI_CLK frequency range	F_{SPI}	0	10		MHz	
Overall Transceiver						
Operating Frequency Range	$F_{\_OP}$	2400		2483	MHz	
Channel Switch Time				180	uS	
T/R Switch Time				60	uS	

Standby to Transmit Data		$T_{PD/TX}$			120	uS	
Standby to Receive Data		$T_{PD/RX}$			120	uS	
Receive Section: @ BER≦0.1%							
Receiver sensitivity				-90		dBm	Buffer Mode@1Mbps ; FD=400kHz
				-85		dBm	Buffer Mode@1.6Mbps ; FD=500kHz
RX System Noise Figure				7		dB	Include on chip switch
Maximum useable signal				-20		dBm	
Min. Carrier/Interference ratio: @ BER≦0.1% ; 1Mbps							
Co-Channel Interference		$CI_{cochannel}$		11		dBc	Wanted signal at 3dB higher than Sensitivity, 2MHz channel spacing. *The interfering signal I_{N-3} will fold to 2MHz under 2MHz IF of the receiver, so it is not as good as the interfering rejection at I_{N+3}.
Adjacent Ch. Interference, 1MHz offset		CI_{N+1} CI_{N-1}		-20 -15		dBc	
Adjacent Ch. Interference, 2MHz offset		CI_{N+2} CI_{N-2}		-37 -7*		dBc	
Adjacent Ch. Interference, ≥ 3MHz offset		CI_{N+3} CI_{N-3}		-40 -30		dBc	
Out-of-Band Blocking / Desensitization		OBB_1		46		dBc	0.03 ~ 2.0 GHz (Image signal reference to image spec.)
		OBB_2		46		dBc	2.0 ~ 2.399GHz
		OBB_3		50		dBc	2.498 ~ 3.0GHz
		OBB_4		70		dBc	3 ~ 12.75 GHz
RSSI Section:							
RSSI Range				50		dB	-100dBm ~ -50dBm (6-bits)
RSSI Accuracy				+/-4		dB	
RSSI Setting Time		T_{RSSI_ON}		1		uS	
Transmit Section:							
RF Output Power		P_{AV}		0		dBm	Pout=nominal output power.
Second Harmonic				-40		dBc	Conducted to ANT pin.
Third Harmonic				-50		dBc	Conducted to ANT pin.
Frequency Deviation		$\triangle f$	160		500	kHz	One-Side Deviation
Data Rate	Buffer Mode	R_{data}		1	1.6	Mbps	
	Direct Mode	R_{data}		1	2	Mbps	
Out-of-Band Spurious Emission							
Operation		OBS_O_1			-36	dBm	30 MHz ~ 1 GHz
		OBS_O_2			-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal
		OBS_O_3			-47	dBm	1.8 GHz ~ 1.9 GHz
		OBS_O_4			-47	dBm	5.15 GHz ~ 5.3 GHz
Frequency Synthesizer Section:							
Typical PLL lock range		F_{LOCK}	2366		2516	MHz	
TX, RX Frequency Tolerance				--		ppm	Same as XTAL pins frequency tolerance.
VCO phase noise				-100		dBc/Hz	+/-1MHz offset
PLL Settling Time		T_{HOP}			120	uS	
Spurious Emissions		OBS_1		-57		dBm	30 MHz ~ 1 GHz (Standby state, Synthesizer and VCO ON.)
		OBS_2		-47		dBm	1 GHz ~ 12.75 GHz
Crystal oscillator frequency		f_{XTAL}		12/16/24		MHz	
Crystal oscillator frequency accuracy				+/-60		ppm	Need to run offset calibration if Xtal accuracy > +/-40ppm
Crystal oscillator start-up time				0.7	1	ms	

- Table 4 -

4. Modes of Operation

The EM198850AW can be configured in eight main modes of operation.

4.1 Operational modes configuration

Modes	0x40	0x41	0x0E	0x26	0x00				0x01	CE	CSn	MOSI	MISO	(IRQ)
	[1:0]	[7:0]	[7]	[0]	[7]	[6]	[5]	[0]	[3:1]	(pin)	(pin)	(pin)	(pin)	(pin)
Power Down	X	X	X	X	X	X	X	1	0	0	X	SPI_{in}	SPI_{out}	
Idle	X	X	0	1	0	1	0	0	000	0	X	SPI_{in}	SPI_{out}	
Configuration	X	X	X	X	X	X	X	1	X	1	0	SPI_{in}	SPI_{out}	
Standby I	00	X	0	1	0	1	1	1	110	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Buffered	10	0x80	1	0	1	1	1	1	110	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
Standby II	10	0x80	1	0	1	1	1	1	110	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Direct	10	0x80	1	0	1	0	1	1	110	1	1	SPI_{in}	SPI_{out}	$Data_{in}$
RX Buffered	01	0x81	1	0	1	1	1	1	110	1	1	SPI_{in}	$FIFO_{out}$	IRQ_{out}
RX Direct	01	0x81	1	0	1	0	1	1	110	1	1	SPI_{in}	SPI_{out}	$Data_{out}$

- Table 5 –

For detail register setting, refer to the state machine of operation modes on Figure 4. Please follow the register sequence order showed from up to down when you write the register setting. The symbol “x” means that don’t write the registers when you change the operation mode.

4.2 Power Down Mode

When the pin CE sets to 0 and R0x00[0] sets to 1, EM198850AW is disabled with the minimal current consumption. When entering the power down mode, the EM198850AW is not active including voltage regulators and crystal block, and the values of the all registers are clear.

4.3 Configuration Mode

When CSn=0 and CE = 1, the SPI interface may be activated to program the SPI register value.

4.4 Idle Mode

Idle mode is used to minimize average current consumption while maintaining short start up times. In this mode, the contents of all registers are maintained by internal power supply voltage. It will reduce the register initialization time on the next start up time from idle mode into buffer mode. EM198850AW is not active including voltage regulators and crystal block..

4.5 Standby I Mode

For RX or TX device, all the RF blocks and mini Mac baseband system clock will be turned off to save average current consumption. In this mode, only voltage regulators, crystal oscillator and clock buffers are active to speed up the start-up time. The configuration word content is maintained during standby I mode.

4.6 TX Buffered Mode

As a transmitter with the function of FIFO and packet handling.

4.7 Standby II Mode

When TX FIFO is empty in TX buffer mode, the TX device would stay in the standby II mode. In this mode, the regulators, crystal oscillator, clock buffers and mini Mac baseband system clock are activated. No any start-up time is need.

4.8 TX Direct Mode

As a transmitter without the function of the FIFO and packet handling.

4.9 RX Buffered Mode

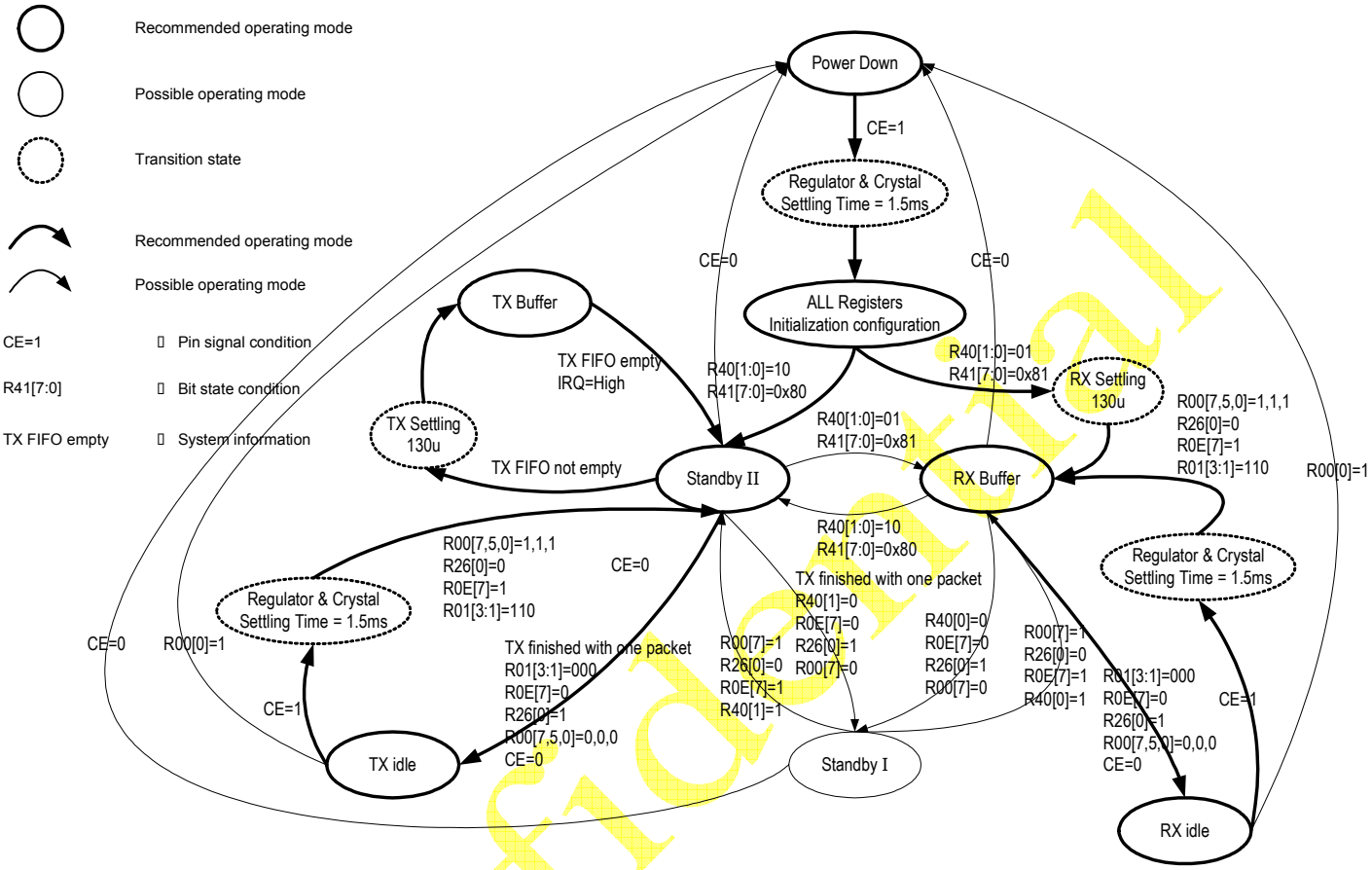
As a receiver with the function of FIFO and packet handling.

4.10 RX Direct Mode

As a receiver without the function of the FIFO and packet handling.

4.11 State Machine of Operation Modes

Figure-4 is the state machine of operation modes. The MCU can follow the register sequence to write SPI registers into the desired operation mode through digital SPI interface.



- Figure 4 -

5. Packet Handling Methods

The packet handler makes it possible to use the high data rate offered by EM198850AW without the needs of a costly, high-speed micro-controller (MCU) for data processing and clock recovery. By placing all high speed signal processing related to RF protocol on-chip,EM198850AW offers the application MCU a simple SPI compatible interface, the SPI clock(SCK) is decided by the interface-speed the MCU itself setup by allowing the digital part of the application to run at low speed, while maximizing the data rate on the RF link.

In RX Buffered Mode, IRQ notifies the MCU when a valid address and payload is received respectively. The MCU can then clock out the received payload from an EM198850AW RX FIFO.

In TX Buffered Mode, EM198850AW digital part automatically generates preamble and CRC value. This means reduced memory demand in the MCU resulting in a low cost MCU, as well as reduced software development time. EM198850AW has 64 bytes RX FIFO and 64 bytes TX FIFO. The MCU can access the FIFO at any time.

5.1 Auto-Acknowledgement (RX)

If auto acknowledgement is enabled and a valid packet with correct data pipe address and CRC is received, the RX device will enter the TX mode and send an acknowledgement packet to TX device. After the RX device has sent the acknowledgement packet to TX device, normal operation in RX device will be resumed.

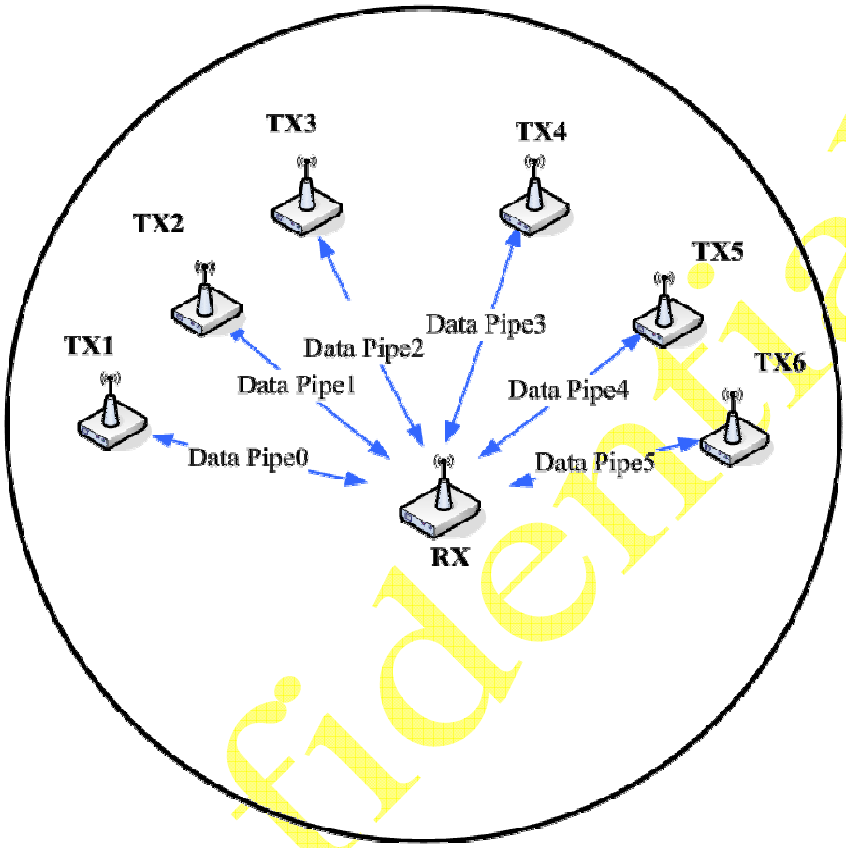
5.2. Auto Re-Transmission (TX)

An auto retransmission is available when auto acknowledgement is enabled at the TX device. It will be possible to state how many times the data in the data register will resent if data is not acknowledged. After each sending, the TX device will enter the RX mode and wait a specified time period for acknowledgement. When the ACK packet is received, the TX device will return to the normal transmit function. If there is no more unsent data in the TX FIFO, the TX device will go into the Standby mode.

If the acknowledgement is not received at the TX device, the TX device will transfer to TX mode and resend the data after a specified time period. This will continue until acknowledgement is received at the TX device or a time out occurs because of the maximum number of resending is reached.

5.3. Star Network

An EM198850AW configured as primary RX will be able to receive data through 6 different data pipes. A data pipe will have a unique address but share the same frequency channel. This means that up to 6 different EM198850AW configured as primary TX can communicate with one EM198850AW configured as RX, and the EM198850AW configured as RX will be able to distinguish between them. Data pipe 0 has a unique 16 bit configurable address. Each of data pipe 1-5 has an 8 bit unique address and shares the 8 most significant address bits.



EM198850AW in a star network Configuration

- Figure 5 -

The following settings are common to all data pipes:

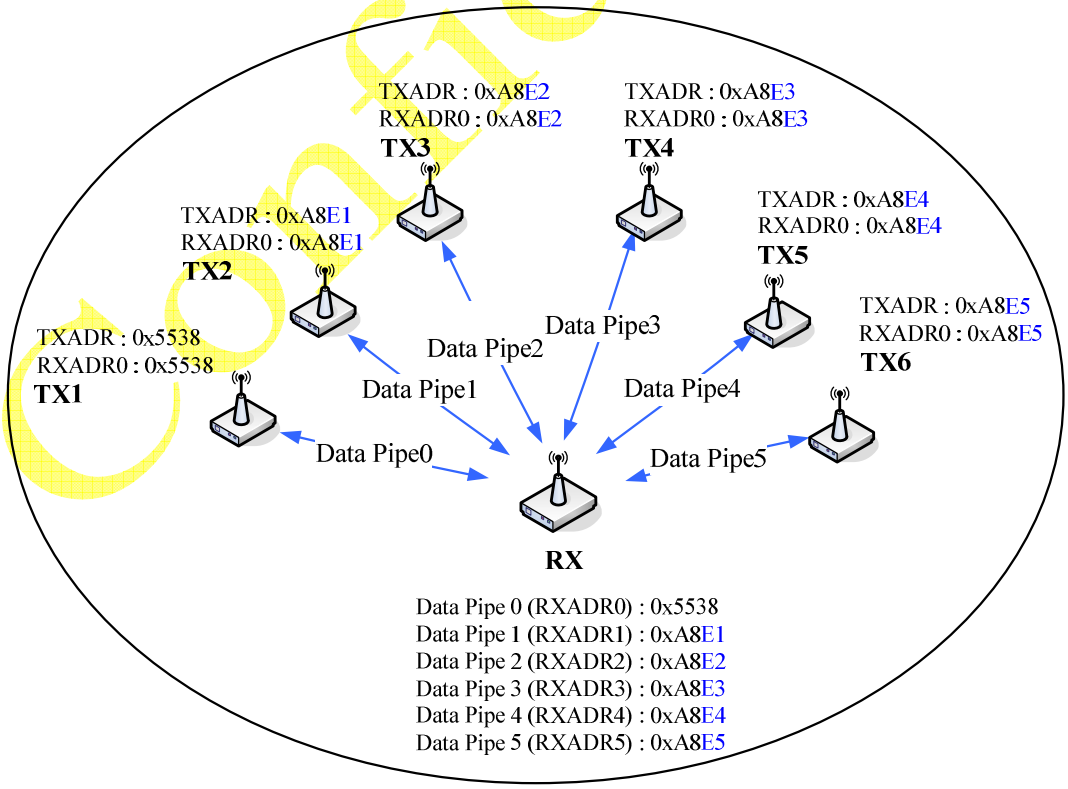
- Auto ACK enable
- STARTNET enable
- CRC encoding scheme
- TX / RX Address width
- Frequency channel
- Air data pipe
- RF data rate

The data pipes are enabled with the bits in the 0x41[5:0] register.
Each data pipe address is configured in the RXADR0 ~ RXADR5. Each data pipe can have up to 2 byte configurable address. Data pipe 0 has a unique 2 bytes address. Data pipe 1~5 shares the 8 most significant address bits. Figure 6 is an example of how data pipes 0~5 are addressed.

	When ADRBC = 2	
	Byte 1	Byte 0
Data Pipe 0 (RXADR0[15:0] = 0x51[7:0],0x50[7:0])	0x55	0x38
Data Pipe 1 (RXADR1[15:0] = 0x53[7:0],0x52[7:0])	0xA8	0xE1
Data Pipe 2 (RXADR2[15:0] = 0x53[7:0],0x54[7:0])	0xA8	0xE2
Data Pipe 3 (RXADR3[15:0] = 0x53[7:0],0x55[7:0])	0xA8	0xE3
Data Pipe 4 (RXADR4[15:0] = 0x53[7:0],0x56[7:0])	0xA8	0xE4
Data Pipe 5 (RXADR5[15:0] = 0x53[7:0],0x57[7:0])	0xA8	0xE5

Addressing Data Pipes 0~5
- Figure 6 -

The RX receives packet from more than one TX. To ensure that the ACK packet from the RX is transmitted to the correct TX, RX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. On the TX device, the TXADR must be the same as the RXADR0. On the RX device, the RXADR0~RXADR5, defined as the data pipe address, must be unique. Figure 7 is an example of data pipe addressing for the TX and RX.



- Figure 7 -

5.4 Packet Description

Data Frame Structure

sync	SOF	address	PID	payload	CRC

ACK Frame Structure

sync	SOF	address	PID	CRC

- Figure 8 -

- **Sync**: 4-12 bytes (Default 4 bytes)
- **SOF**: Start of Frame (1byte)
- **Address**: programmable byte length (1-2 byte)
- **PID**: 1 byte

  When STARNET 0x40[7] is enabled, PID is adding to frame structure.
  When STARNET 0x40[7] is disabled, PID is removing from frame structure.

  Example:

  If STARNET 0x40[7] is enabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),
  → PID= 1 byte, the available payload = 3 bytes

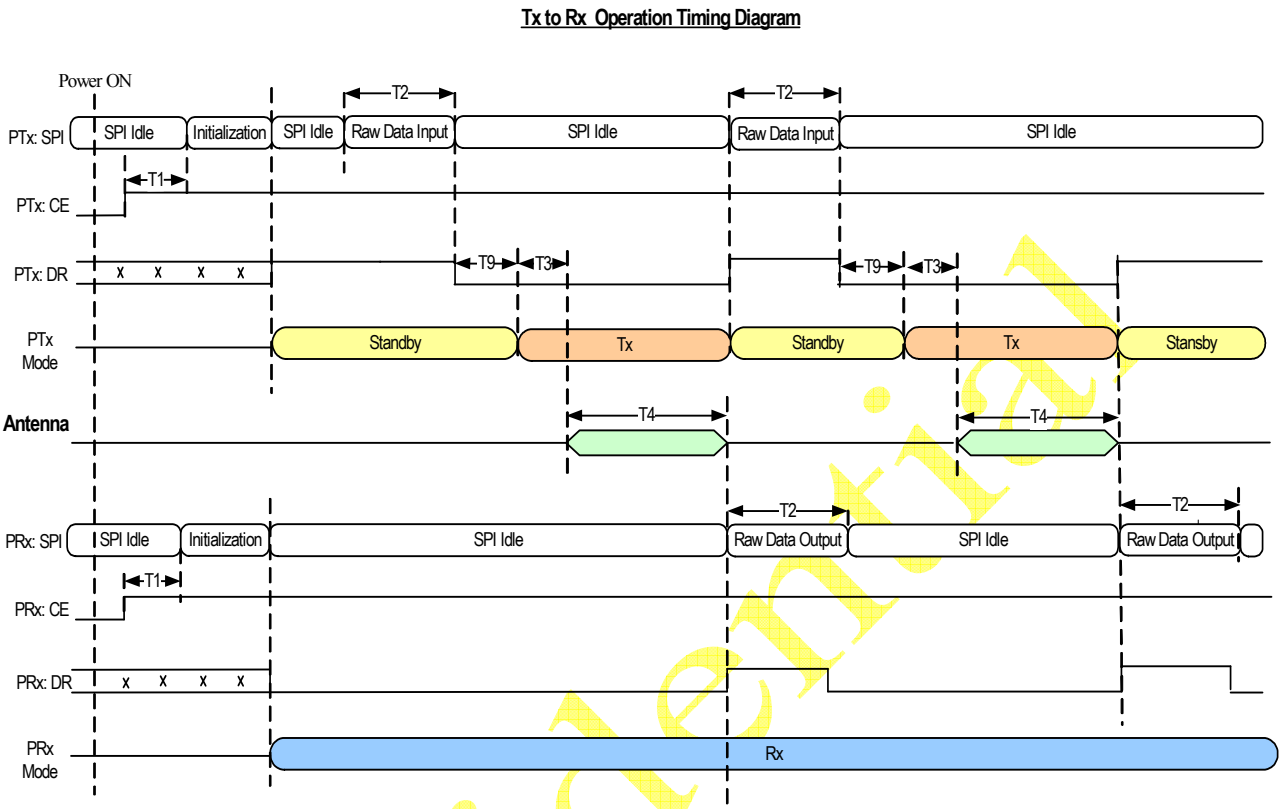
  If STARNET 0x40[7] is disabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),
  → PID= 0 byte, the available payload = 4 bytes

  - [7]: packet type, auto generate by HW
    - 1'b0 : data packet (needs ACK or not)
    - 1'b1: ACK packet
  - [6:4]: 000~101 Pipe data number, auto generate by HW
  - [3:0]: Packet sequence number, It is used by the RX device to determine if a packet is new or retransmitted. It defined by user.
- **Payload**: programmable byte length (1-64 byte)
- **CRC**: programmable length (0,1,2,4 byte)

6. Operation Timing Diagram

The following descriptions in this section are showed the TX/RX link operation timing diagram.

6.1_TX/RX Link Operation Timing Diagram without Auto ACK in Buffer Mode

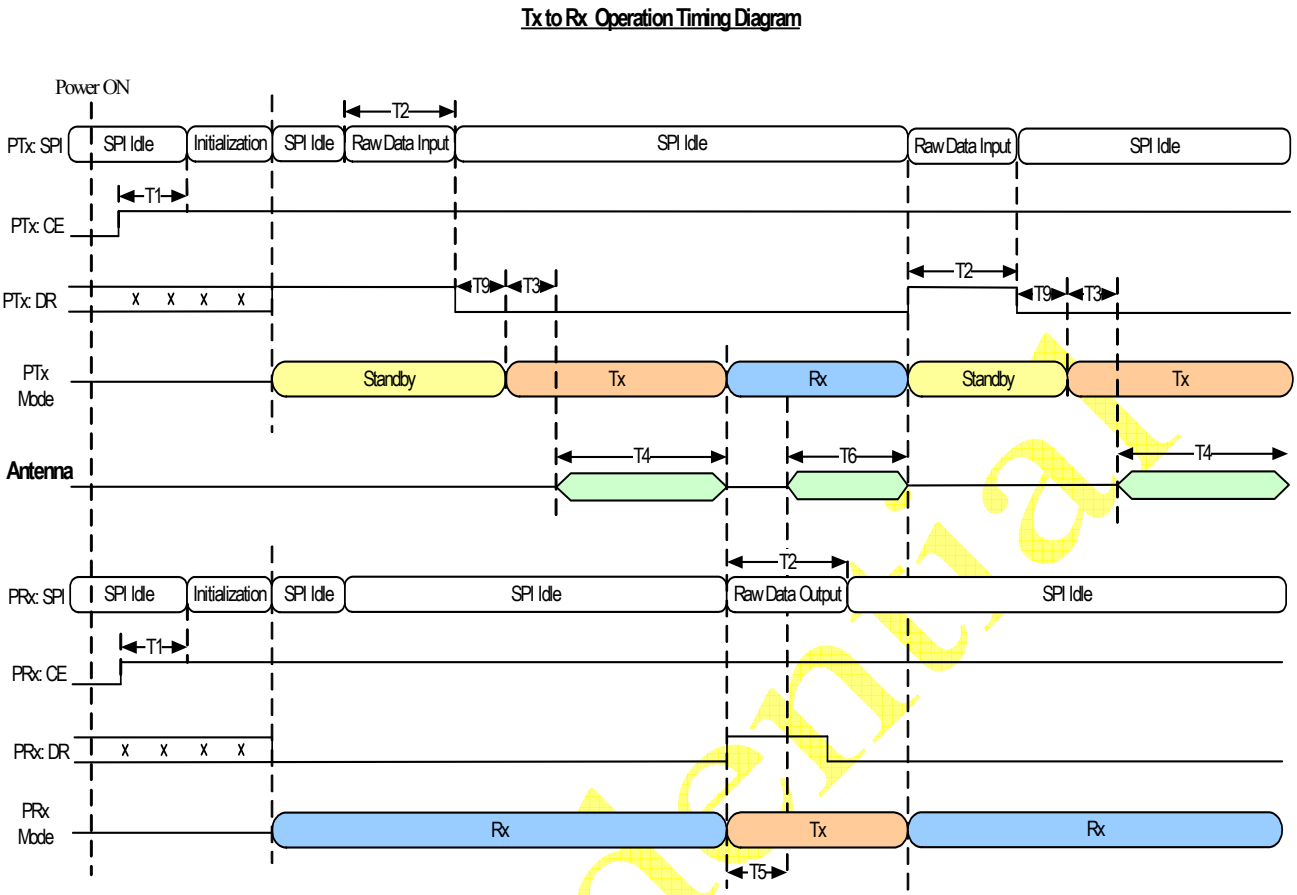


- Figure 9 –

Condition: Disable Auto ACK 0x40[3:2] = 00
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

The PTX DR is asserted after the packet is transmitted by the PTX.
The PRX DR is asserted after the packet is received by the PRX.

6.2 TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode



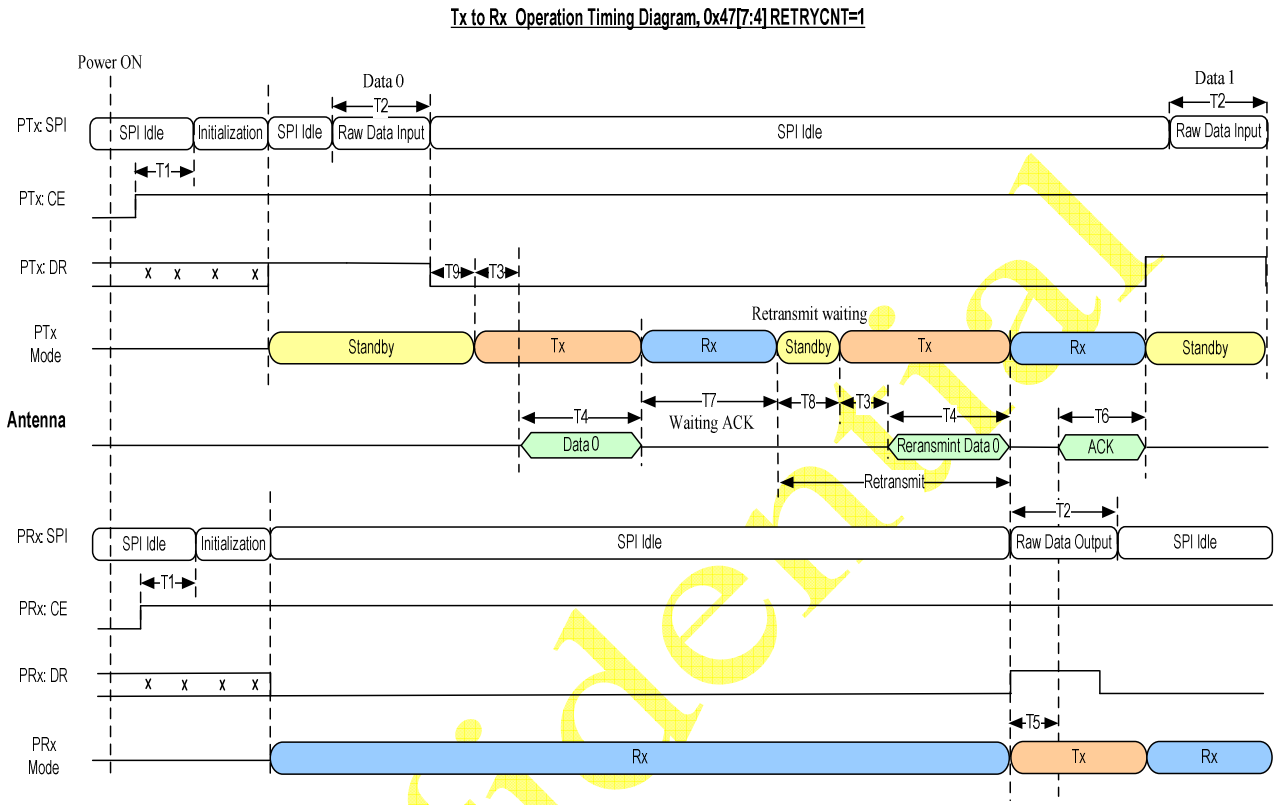
- Figure 10 -

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

When the transmission ends, the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to MCU. When the PRX device receives the packet, it responds with an interrupt to MCU.

6.3 TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX receives ACK



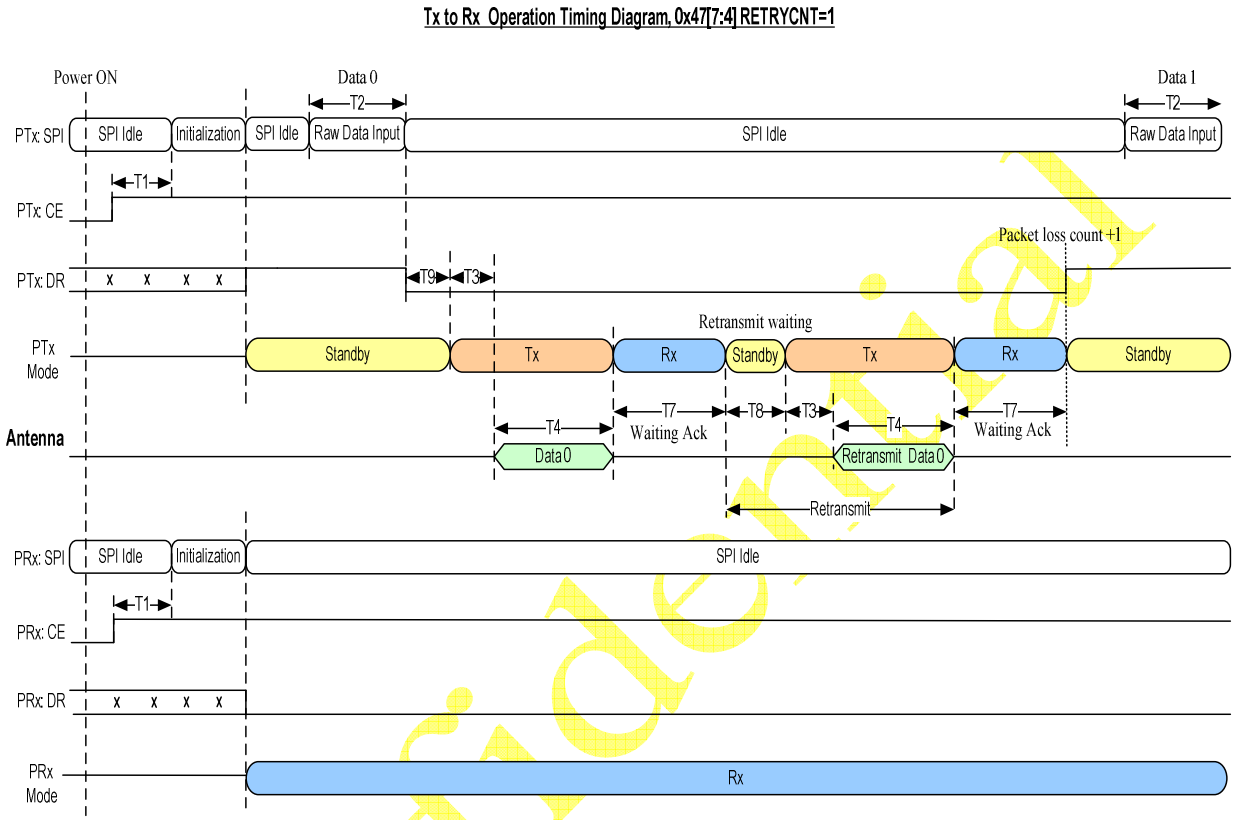
- Figure 11 -

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

After Data 0 is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits specified time for ACK packet (T7), if it is not in specified time slot, the PTX retransmit the Data 0. When the retransmitted packet is received by the PRX, the DR of PRX is asserted and ACK is transmitted back to the PTX. When the ACK is received by the PTX, the DR of PTX is asserted.

6.4 TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX doesn't receive ACK again ➔ Packet Loss Count + 1

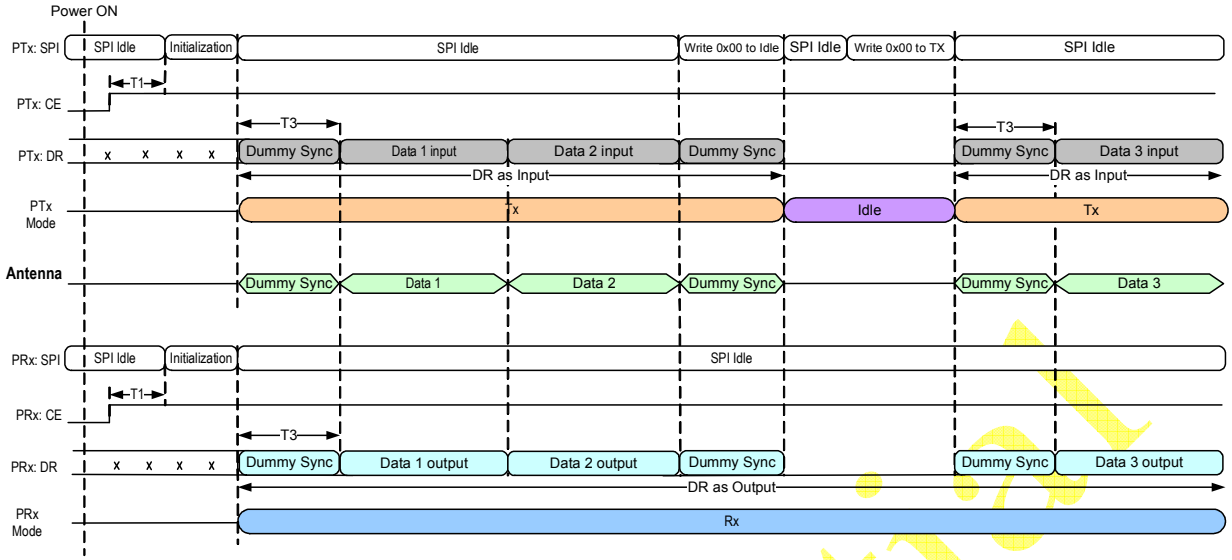


- Figure 12 -

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

When the PTX retransmit counter exceeds the RETRYCNT 0x47[7:4], the PTX DR is asserted and automatically adds one to packet loss count (0x4F[7:3]). Then the payload in PTX FIFO will be removed.

6.5 TX/RX Link Operation Timing Diagram in Direct Mode

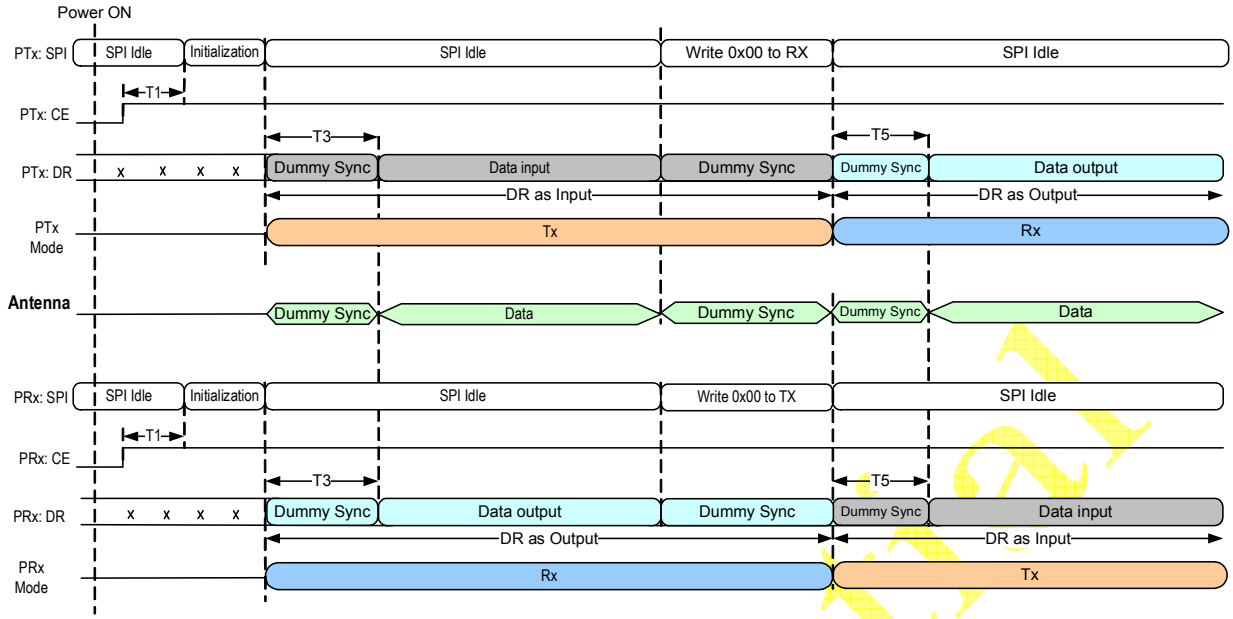


- Figure 13 -

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, user must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. Figure 13 shows the timing diagram of operation mode change from direct mode into idle mode, then into direct mode again.

6.6 TX/RX Switching Operation Timing Diagram in Direct Mode



-Figure14 -

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, user must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. The figure shows the timing diagram for RX/TX switching operation. If the devices change from TX(RX) into RX(TX) directly, the devices don't go into standby mode. Besides, the PLL block only takes the time T5 not T3 for PLL settling.

6.7 Time Formula Description:

Payload Length: **n**
Data rate: **rate**
Sync 0x43 [4:0]: **s**
Address 0x42[7:6]: **a**
SCK Frequency: **SCK**
CRC Check 0x43 [6:5]: **r**
SOF: 1 byte
PID: When STARNET 0x40[7] =1, PID = 1 byte, else PID=0
Slot time 0x47 [3:0]: **SLT**
ACKTOSLOT 0x49 [7:0]: **ATS**
BACKOFFWIN 0x58 [7:0]: **BFW**

Delay Times Information

Formula Description
● **T1 must be over 1ms for Xtal and regulator settling.** ● **Only 500us is needed for regulator settling when system reference clock is shared with MCU**
Burst Mode : T2 = (n+1) *8 /SCK **Non-Burst Mode : T2 = (2*n) *8 /SCK**
T3 = 120us
T4 = (s+SOF+a+n+r)*8/rate
T5 = 60us
T6= (s+SOF+PID+a+r)*8/rate
T7= ATS*SLT*10us
T8= BFW*SLT*10us
T9= 10us

- Table 6 -

T1: Initiation setting time
T2: TX: Write data to FIFO; RX: Read data from FIFO
T3: RF delay time for transmit data. (Waiting for PLL settling)
T4: Packet Input Data Transmission Time
T5: RF delay for transmit ACK data. (Waiting for PLL settling)
T6: ACK packet Data Transmission Time
T7: ACK waiting time, must be larger then T5+T6, programmable from 10us to 32ms.
T8: Retransmit waiting time, programmable from 0 to 32ms
T9: Packet Handling Time

6.8 FIFO and PKTCNT

A 64bytes FIFO size is available on EM198850AW. The PKTCNT (0x45[7:4]) define the number of payloads can be stored in FIFO.

In TX Mode, the pin DR will keep high until the number of payload in FIFO reach the PKTCNT. For example: Set payload length 4 bytes (PKTLEN[6:0]=4) and PKTCNT = 4. When the data in FIFO reach to 16 bytes, the DR will pull low to indicate the MCU that no more data is allowed to input.

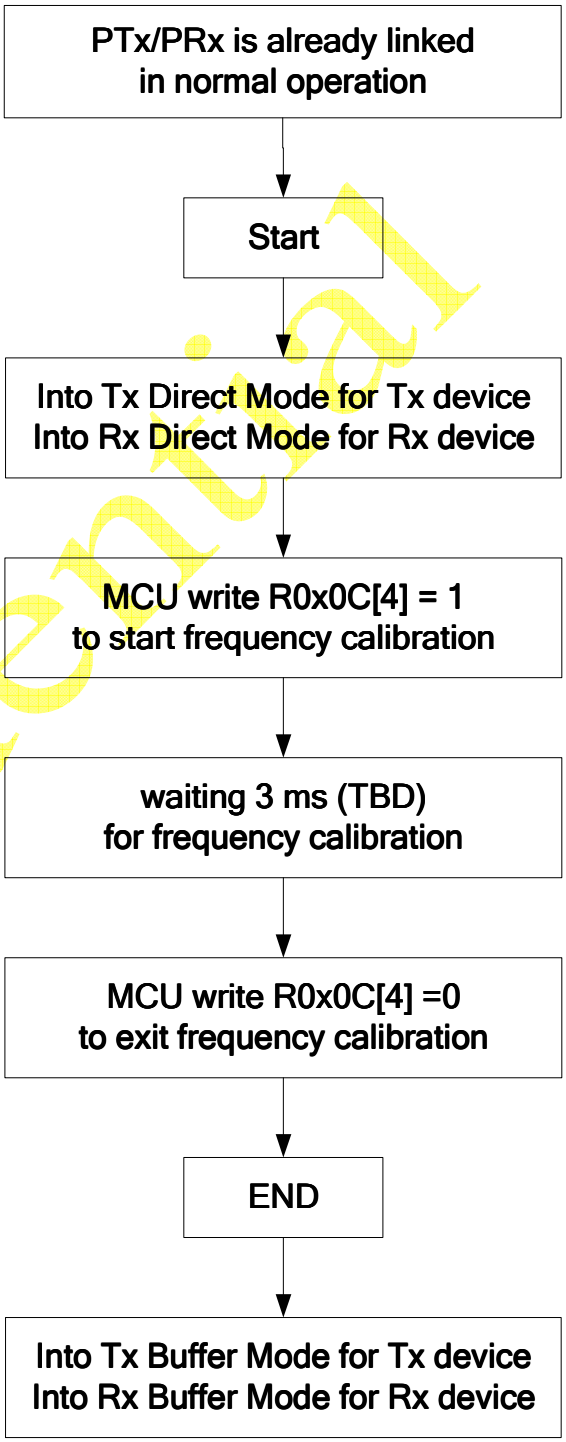
In RX Mode, PKTCNT also define the maximum number of payload in FIFO, when the RX FIFO is full, number of payload equal to PKTCNT but it can be less than 64 bytes, the receiver will be turned off to save power. The receiver will turn on immediately after MCU read out the FIFO data.

7. Xtal Frequency Offset Calibration

When the EM198850AW uses the external Xtal with internal oscillator to create the system clock, the EM198850AW provide the auto frequency timing engine to fine tune the Xtal frequency.

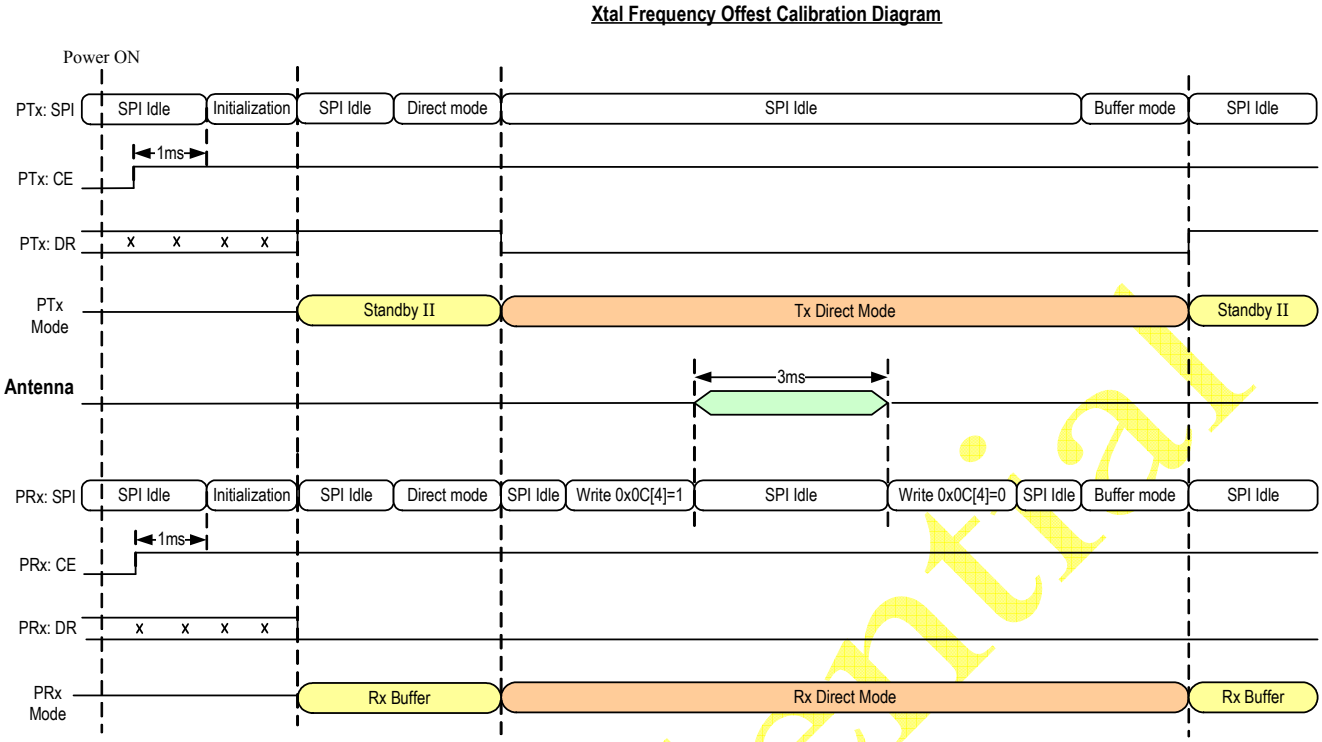
- Calibration Flow

1. **Start**
2. **Set registers into Direct Mode**
3. **For RX device, write R0x0C[4]=1 to start frequency calibration. For TX device, it outputs a single carrier as reference frequency for RX device.**
4. **Wait 3 msec for the timing of frequency calibration (TBD)**
5. **For RX device, write R0x0c[4]=0 to finish the calibration flow**
6. **End**
7. **Recover to the normal operation mode**



- Figure 15 -

Xtal Frequency Offset Calibration Timing Diagram



- Figure 16 -

Note: When the devices go into POWER DOWN mode, all the calibration result will be refreshed.

7.1 EM198850AW sharing crystal with a MCU

When using a MCU to drive the crystal reference pin XTALO of the EM198850AW transceiver, some rules must be followed. When MCU drives the EM198850AW clock input pin, XTALO, the requirement of load capacitance C_L is set by the MCU only. The frequency accuracy of +/-60ppm is still required to get a functional radio link. The input signal should not have amplitudes exceeding any rail voltage, but any DC voltage within this is OK. To achieve low current consumption and also good SNR ratio when using an external clock from MCU, it is recommended to use an input signal larger than 0.4 V_{-peak}. When clocked externally, XTALO is the input pin, and XTALI is not used. XTALI can be left as an open pin.

8. 4-wire SPI interface - Digital Interface to control chip parameter

All configuration of EM198850AW is defined by values in some configuration registers. All these register are writable via the SPI interface.

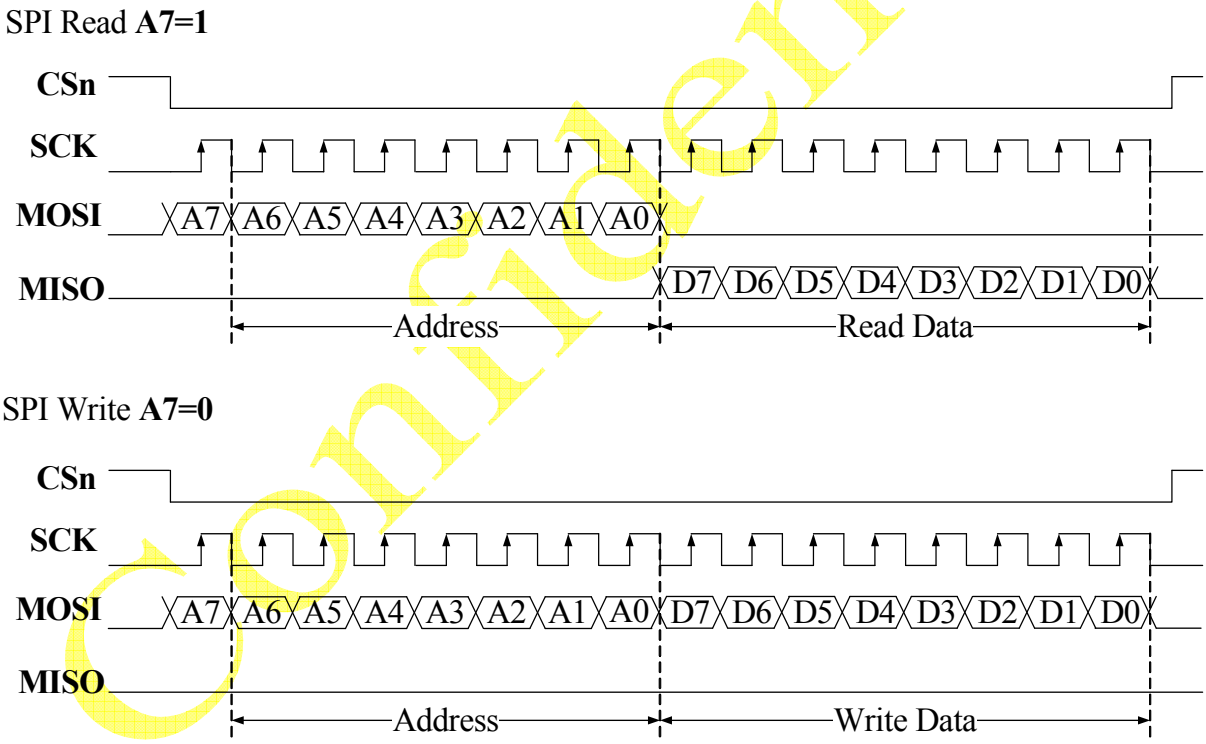
The data are loaded into the shift register and sent to micro-controller on the rising edge of the clock SCK and latched on the falling edge of the CSn signal. When the CSn pin is high, the data stored in the shift register is retained even if a SCK is applied. When the CSn pin is low the data can be rewritten and resent. Inputs timing of the SCK, CSn, MOSI and MISO are shown in the Figure 18.

SPI Timing

Chip Select: CSn
Input Clock: SCK
Input Data: MOSI
Output Signal: MISO

- SPI interface Read / Write for Register

When A7 = 1, MCU read value from EM198850AW register.
When A7 = 0, MCU write value to EM198850AW register.



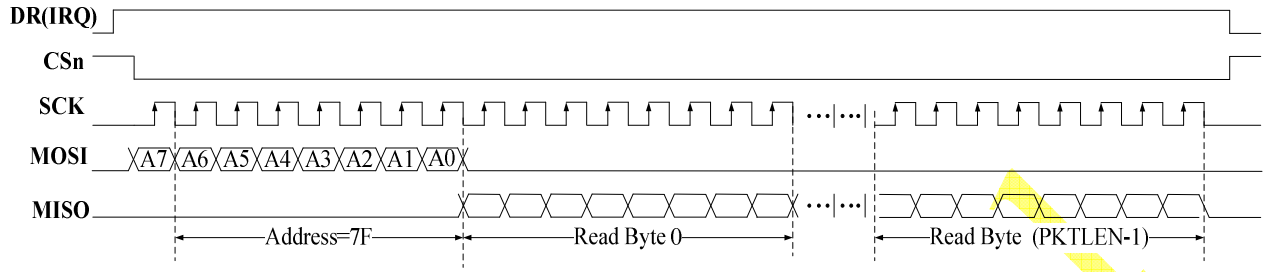
- Figure 17 -

- SPI interface Read / Write for Buffer mode

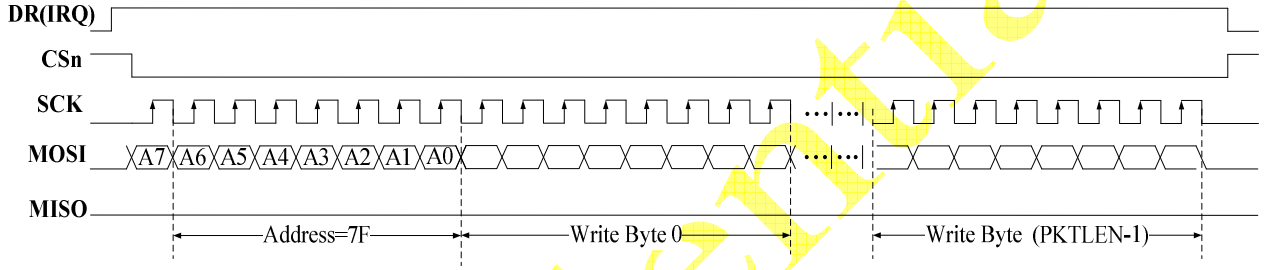
✓ **When 0x40[6] = 1, SPI interface switch to Burst mode.**

Burst Mode:

Buffer Read **A7=1** (PKTCNT=1)



Buffer Write **A7=0** (PKTCNT=1)

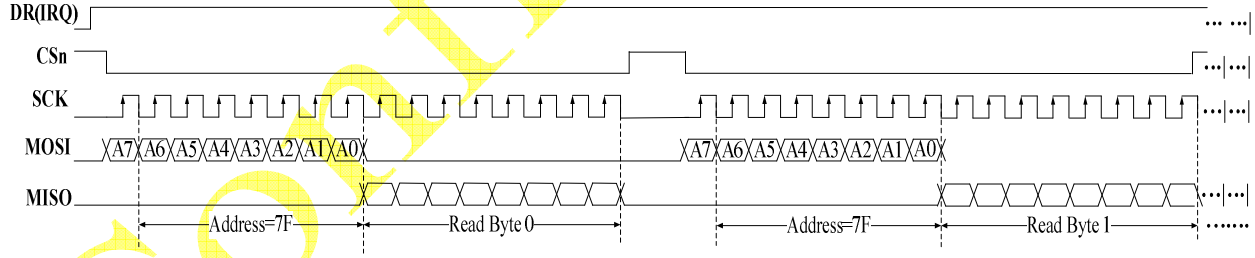


- Figure 18 -

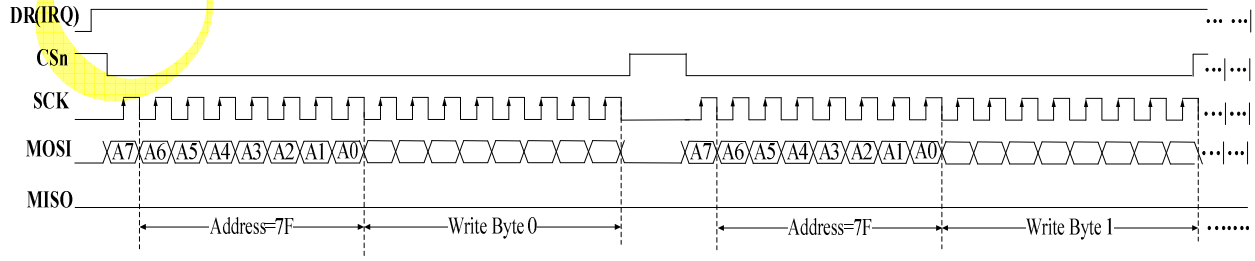
✓ **When 0x40[6] = 0, SPI interface switch to Non-Burst mode.**

Non-Burst Mode:

Buffer Read **A7=1** (PKTCNT=1)



Buffer Write **A7=0** (PKTCNT=1)



- Figure 19 -

Parameter	Min.	Max.	Unit
Data to SCK Setup	**3**		**nS**
SCK to Data Hold	**3**		**nS**
SCK Frequency	**0**	**10**	**MHz**

- Table 7 -

9. RF Transceiver Registers Map

9.1 Configuration Registers for RF Transceiver

	D7	D6	D5	D4	D3	D2	D1	D0
0x00	EN_CLK	H_Buf_L_DR	EN_24M	DR_EN_RX	DR_EN_TX	EN_XO	DR_EN_PLL	nENFun_idle
0x01	PA_AAC	TX_PWR[2:0]			nEN_XO_2uA	nEN_Ictrl_XO[1]	EN_Ictrl_XO[0]	Sel_16_12
0x02	CH_AutoMan	CH_NO						
0x03	FIX_KXO	EN_75M	CntR[5:0]					
0x04	CntB[7:0]							
0x05	EnFun_ManTrigAFC	EN_AFC_Code	Manual_EN_AFC	CntA[4:0]				
0x06	PA3_WC[2:0]			PA2_WC[1:0]		PA1_WC[1:0]		D2S_Gain
0x07	EN_BB_TM		EN_AAC_TM	VCO_AFC_Resol[1:0]		VCO_AFC_3W[2:0]		
0x08	TXDC_SW_3w	EN_RXEN_Delay	SC_CH[5:0]					
0x09	Delay_RXEN[2:0]			EN_TXMOD	SEL_I_V	SEL_VB[2:0]		
0x0a	Delay_XO[2]	EN_SignalDet	EN_3M_IF	EN_TXDC_LPF	SEL_MOD_RES_Offset	SEL_MOD_RES[2:0]		
0x0b	Delay_TXDC[1:0]		CHP_SW_3w	Delay_CHP_SW[3:0]				EN_PLL_FAST
0x0c	SD_EN_DutyDelta	SD_EN_FreqDelta	Sel_SD	EN_KXO	KXO_spi[3:0]			
0x0d	SD_DutyDelta[1:0]		SD_FreqDelta[1:0]		SD_RangeH[1:0]		SD_Range	SD_Noise
0x0e	Low_wRFSPI	EN_PAONdelay	EN_Stop1M_D[1:0]		EN_PAON_D[3:0]			
0x0f	Delay_XO[1:0]		I_PA3_UP	I_PA3_DN	I_PA2_UP	I_PA2_DN	I_PA1_UP	I_PA1_DN
0x20	FE_PTAT	MIX_Ilo	MIX_BS[3:0]			LNA_BS[3:0]		
0x21	FILT_PTAT_CTR[1:0]		CLM_G[2:0]			CLM_SW[2:0]		
0x22	SLICE_Nb[3:0]				SLICE_Pb[3:0]			
0x23	EN_PTAT_Buf_RXMx	Ictrl_Buf_RXMx[2:0]			EN_PTAT_Div2	Ictrl_Div2[2:0]		
0x24	EN_PTAT_Buf_D2S	Ictrl_Buf_D2S[2:0]			EN_PTAT_Buf_IQComb	Ictrl_Buf_IQ_Comb[2:0]		
0x25	Vctrl_VCO_CAL[1:0]		Ictrl_VCO[2:0]			EN_PTAT_Pre	Ictrl_Pre[1:0]	
0x26	bat_det_win	PD_sel_10p	SLICE_G[3]	L_bypassSavePower	EN_700K	Ictrl_CHP_UP<4>	EN_CLK_STOP	EN_SavePower
0x27	Ictrl_CHP_UP[3:0]				Ictrl_CHP_DN[3:0]			
0x28	TS_dig_pllbw	TS_dig_RXdelay	TS_dig_KXO32	TS_dig_KXO10			H_macPD_L_enPD	Manual_EN_PLL
0x29	EN_TSO_LDPA	EN_TSO_SD	nEN12_EN24	EN_75M_toKXO	vf_reg_ctrl[1:0]		bat_det_level[1:0]	
0x2a	PA3_BIT[3:0]				PA2_BIT[3:0]			
0x2b	Ictrl_PAPD[3:0]				PA1_BIT[3:0]			
0x2c	EN_PA_PTAT	SLICE_G[0]	DCLevel_BIT[1:0]		CP_WIN	PD_GC_BIT[2:0]		
0x2d	EN_BPF_bypass	ENB_SL_PD	SLICE_G[1]	EN_LDout_TS	EN_FILT_AUTO	FILT_AUTO_BW[2:0]		
0x2e	DLL_PVT_OPT	EN_Vf_TS	EN_LD	EN_Vk_TS	BY_PTAT	BY_BG	EN_CtrlRXOut_bySD	SLICE_G[2]
0x2f	EN_Vf_B_TS	TS_Id_EnPA	REG1_RB[2:0]			BGR_RB[2:0]		
0x30	Sel_LNA_Gain	EN_Internal_LPF	EN_TM_PLL_VT	TSO_PA[2:0]			EN_TN_DLL	DLL_VT_IO
0x31	SW_TSIO_LPF	SW_TSIO_BPF	EN_TSO_DLL_FILT	EN_TSO_PA_PLL	EN_TSO_RSSI	EN_TSIO_LPF	EN_TSIO_BPF	EN_TSIO_BS
0x32	Syn_En_Delay[3:0]				En_Syn_PFD	En_Chp_Vt_initial	EN_LD_TS	EN_TSIO_DIG
0x33	EN_TSO_EN_VCO	EN_TSO_Vref_PD	Sel_SDOUT_Issig	Sel_EN_Fast	nEN_DLLPVT	EN_NoAFC_swCH	EN_Bat_out	En_Fun_1Mstop

- Table 8 –

Address from 0x00 to 0x0F

Address (Hex)	Register Name	Bit	Default Value	Type	Description
0x00	Register Name	Bit	default	W	Description
	EN_CLK	7	1		Enable Digital Circuits System Clock
	H_Buf_L_DR	6	1		1: Buffer mode operation 0: Direct mode operation
	nEN_24M	5	1		Set 0 when 24MHz reference clock is used
	DR_EN_RX	4	0		Enable RX in DR mode
	DR_EN_TX	3	0		Enable TX in DR mode
	EN_XO	2	1		Enable Crystal Buffer
	DR_EN_PLL	1	0		Enable PLL in DR mode
	nENFun_idle	0	1		Set 0 to enable idle mode
0x01	Register Name	Bit	default	W	Description
	PA_AAC	7	1		Enable PA Auto Amplitude Control function (PA AAC)
	TX_PWR[2:0]	6:4	000		TX output power selection in Test mode
	nEN_XO_2uA	3	1		Crystal buffer bias current, default 110.
	nEN_Ictrl_XO[1]	2	1		
	EN_Ictrl_XO[0]	1	0		
	Sel_16_12	0	0		Reference clock settling 1: 16MHz 0: 12MHz
0x02	Register Name	Bit	default	W	Description
	CH_AutoMan	7	0		Switch manual / look up table program RF channel. Look up table: set by CH_NO 0: Auto lookup table approach 1: Manual control via registers R0x04 & R0x05 (for test only)
	CH_NO	6:0	0		Channel frequency setting (RF Frequency) Data Rate = 1Mbps CH_NO / TX (Fc) / RX (Fc-2MHz) 'h00 / 2400MHz / 2398MHz 'h01 / 2401MHz / 2399MHz 'h53 / 2483MHz / 2481MHz (RF Frequency) Data Rate = 1.6Mbps CH_NO / TX (Fc) / RX (Fc-3MHz) 'h00 / 2401MHz / 2398MHz 'h01 / 2402MHz / 2399MHz 'h53 / 2484MHz / 2481MHz
0x03	Register Name	Bit	default	W	Description
	FIX_KXO	7	1		After crystal calibration, set to High.
	EN_75M	6	1		Enable 75M reference clock function
	CntR[5:0]	5:0	000110		Ref. Clock / CntR[5:0] 12MHz / 000110 16MHz / 001000 24MHz / 001100
0x04	Register Name	Bit	default	W	Description
	CntB[7:0]	7:0	0		B counter of PLL
0x05	Register Name	Bit	default	W	Description
	EnFun_ManTrigAFC	7	0		Manual trigger AFC (for test only)
	EN_AFC_Code	6	1		Enable AFC
	Manual_EN_AFC	5	0		Manual enable AFC (for test only)
	CntA[4:0]	4:0	0		A counter of PLL
0x06	Register Name	Bit	default	W	Description
	PA3_WC[2:0]	7:5	010		PA3 Gain Control (for test only) Increase gain refer to 010 PA3_WC[2:0] / Increase Gain 0 0 1 / -5dB 0 1 0 / 0dB
	PA2_WC[1:0]	4:3	11		PA2 Gain Control (for test only) Increase gain is refer to 10 PA2_WC[1:0] / Increase Gain 0 1 / -10dB 1 0 / 0dB
	PA1_WC[1:0]	2:1	10		PA1 Gain Control (for test only) Increase gain is refer to 10 PA1_WC[1:0] / Increase Gain 0 1 / -10dB 1 0 / 0dB

	D2S_Gain	0	1		D2S Gain control 2.5dB/step
0x07	Register Name	Bit	default	W	Description
	EN_BB_TM	7	0		BB Test Mode Enable (for test only) 1: Test mode
	EN_RF_TM	6	0		RF Test Mode Enable (for test only)
	EN_AAC_TM	5	1		PA ACC auto-calibrated control 1: manual control PA power 0: PA output power auto calibration
	VCO_AFC_Resol[1:0]	4:3	11		VCO AFC resolution control (Fixed)
	VCO_AFC_3W[2:0]	2:0	000		VCO AFC curve manual selection when 0x05[5]=1 (for test only)
0x08	Register Name	Bit	default	W	Description
	TXDC_SW_3W	7	0		Manual control TX LPF corner (for test only)
	EN_RXEN_Delay	6	1		In Receiver Mode, disable the RX chain to save current during PLL un-locked
	SC_CH[5:0]	5:0	0		VCO capacitor array for fast settling (Fixed)
0x09	Register Name	Bit	default	W	Description
	Delay_RXEN[2:0]	7:5	000		RX chain off time control (Check with 0x08[6]) Off Time=20us*(1+Delay_RXEN[2:0]) Default = 100uS (Fixed)
	EN_TXMOD	4	1		Enable the frequency deviation tuning (Tuning by 0x0a[2:0])
	SEL_I_V	3	1		Switch ADC input from RSSI or Vtune of VCO (SEL_I_V) 1: RSSI 0: Vtune of VCO (for test only)
	SEL_VB[2:0]	2:0	000		Selection ADC Full range Voltage SEL_B[2:0] (Fixed)
0x0a	Register Name	Bit	default	W	Description
	Delay_XO[2]	7	0		Crystal settling wait time during frequency calibration (Fixed)
	EN_SignalDet	6	1		Enable Signal Detection Circuits (For test only)
	EN_3M_IF	5	0		When 1.6Mbps Mode, set High to change the receiver IF. Default 0 for 1Mbps Mode.
	EN_TXDC_LPF	4	0		Transmitter data compensation filter enable. (Fixed)
	SEL_MOD_RES_Offset	3	0		MSB of Frequency Deviation control.
	SEL_MOD_RES[2:0]	2:0	111		Transmitter Frequency Deviation Control 0x0a[3:0] / Frequency Deviation (kHz) 0011 / 200 0111 / 400 1101 / 500
0x0b	Register Name	Bit	default	W	Description
	Delay_TXDC[1:0]	7:6	00		Check with 0x0a[4], compensation filter settling time control (Fixed)
	CHP_SW_3w	5	0		Charge Pump Current Control Mode (for test only)
	Delay_CHP_SW[3:0]	4:1	0101		Charge Pump bias current (Fixed)
	EN_PLL_Fast	0	1		Enable PLL fast settling option
0x0c	Register Name	Bit	default	W	Description
	SD_EN_DutyDelta	7	1		RX Signal detection option. (Fixed)
	SD_EN_FreqDelta	6	1		
	Sel_SD	5	1		
	EN_KXO	4	0		Enable crystal Frequency calibration function
	KXO_spi[3:0]	3:0	0000		Crystal Frequency calibration resolution control (Fixed) 1000: CL=12p 1111: CL=27p 0000: CL=16p
0x0d	Register Name	Bit	default	W	Description
	SD_DutyDelta[1:0]	7:6	01		RX Signal detection options. (Fixed)
	SD_FreqDelta[1:0]	5:4	00		
	SD_RangeH[1:0]	3:2	11		
	SD_Range	1	1		
	SD_Noise	0	1		
0x0e	Register Name	Bit	default	W	Description
	Low_wRFSPI	7	1		Set 0 to write RF SPI registers
	EN_PAONdelay	6	0		Enable the time delay between PLL ON and PA ON (for test only)
	EN_Stop1M_D[1:0]	5:4	01		Clock gating delay for internal circuit's system clock. (Fixed)
	EN_PAON_D[3:0]	3:0	0001		Check with 0x0e[6], setting the delay time (for test only)
0x0f	Register Name	Bit	default	W	Description
	Delay_XO[1:0]	7:6	00		Crystal settling wait time during frequency calibration (Fixed)
	I_PA3_UP	5	0		PA gain control options. (Fixed)
	I_PA3_DN	4	1		
	I_PA2_UP	3	1		
	I_PA2_DN	2	0		
	I_PA1_UP	1	1		

	I_PA1_DN	0	1		

- Table 9 -

Address 0x20 to 0x33

Address (Hex)	Register Name	Bit	Default Value	Type	Description
0x20	Register Name	Bit	default	W	Description
	FE_PTAT	7	1		Front-End PTAT enable (Fixed)
	Mix_BS	6	0		RX Mixer bias control (Fixed)
	MIX_BS[2:0]	5:3	101		RX Mixer bias control (Fixed)
	LNA_BS[2:0]	2:0	101		RX LNA bias control (Fixed)
0x21	Register Name	Bit	default	W	Description
	FILT_PTAT_CTRL[1:0]	7:6	01		Filter PTAT Control Default: 01
	CLM_G[2:0]	5:3	100		RX buffer High/Low gain mode control (Fixed)
	CLM_SW[2:0]	2:0	100		RX buffer High/Low output swing control (Fixed)
0x22	Register Name	Bit	default	W	Description
	SLICE_Nb[3:0]	7:4	0		RX Slicer Common DC control (Fixed)
	SLICE_Pb[3:0]	3:0	0		
0x23	Register Name	Bit	default	W	Description
	EN_PTAT_Buf_RXMx	7	1		Enable PTAT option for RX Mixer 1: with PTAT 0: without PTAT
	Ictrl_Buf_RXMx[2:0]	6:4	100		RX Mixer bias control (Fixed)
	EN_PTAT_Div2	3	0		Enable PTAT option for divide by 2
	Ictrl_Div2[2:0]	2:0	011		Divide by 2 bias control (Fixed)
0x24	Register Name	Bit	default	W	Description
	EN_PTAT_Buf_D2S	7	1		Enable PTAT option for RF D2S buffer
	Ictrl_Buf_D2S[2:0]	6:4	011		RF D2S buffer bais control (Fixed)
	EN_PTAT_Buf_IQComb	3	1		Enable PTAT option for IQ combiner buffer
	Ictrl_Buf_IQ_Comb[2:0]	2:0	101		IQ combiner buffer bias control (Fixed)
0x25	Register Name	Bit	default	W	Description
	Vctrl_VCO_CAL[1:0]	7:6	10		VCO AFC 's control voltage selection (Fixed)
	Ictrl_VCO[2:0]	5:3	100		VCO bias control (Fixed)
	EN_PTAT_Pre	2	0		Enable PTAT option for Prescaler
	Ictrl_Pre[1:0]	1:0	10		Prescaler bias control (Fixed)
0x26	Register Name	Bit	default	W	Description
	bat_det_win	7	0		Windows selection for battery detection, check with 0x29[1:0]
	PD_sel_10p	6	0		Capacitor selection for RX demodulator (Fixed)
	SLICE_G[3]	5	0		Demodulator Buffer Gain (Fixed)
	L_bypassSavePower	4	1		Set Low to bypass Save Power function (for test only)
	EN_700K	3	1		RX IF LPF bandwidth selection 1: for 1Mbps 0: for 1.6Mbps
	Ictrl_CHP_UP[4]	2	0		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
	EN_CLK_STOP	1	1		Enable clock gating in test mode(for test only)
	EN_SavePower	0	0		
0x27	Register Name	Bit	default	W	Description
	Ictrl_CHP_UP[3:0]	7:4	0000		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
	Ictrl_CHP_DN[3:0]	3:0	1001		Decrease Charge Pump Bias Current, Ictrl_CHP_DN[3:0] (Fixed)
0x28	Register Name	Bit	default	W	Description
	TS_dig_pllbw	7	0		Digital output selection in test mode (for test only)
	TS_dig_RXdelay	6	0		
	TS_dig_KXO32	5	0		
	TS_dig_KXO10	4	0		
	TS_dig_SCK	3	0		
	TS_dig_dro	2	0		
	H_macPD_L_enPD	1	0		RX demodulator Mode Selection 1: DR mode 0: Buffer mode
	Manual_EN_PLL	0	0		Manual enable PLL (for test only)
0x29	Register Name	Bit	default	W	Description
	EN_TSO_LDPA	7	0		Set LD & EN_PA to ATP in test mode
	EN_TSO_SD	6	0		Set signal detection output to ATP in test mode
	nEN12_EN24	5	1		System Reference Clock Selection 1: 24MHz 0: 12MHz / 16MHz
	EN_75M_toKXO	4	1		Enable clock gating option for frequency calibration
	Vf_reg_ctrl[1:0]	3:2	10		Set filter calibration output voltage to ATP in test mode

	bat_det_level[1:0]	1:0	00		Selection of Battery detection level Threshold Voltage 0x29[1:0] / 0x26[7]=0 / 0x26[7]=1 00 / 1.9 / 1.7 01 / 2.0 / 1.8 10 / 2.1 / 1.9 11 / 2.2 / 2.0
0x2a	Register Name	Bit	default	W	Description
	PA3_BIT[3:0]	7:4	0111		TX PA3 Bias current control (Fixed)
	PA2_BIT[3:0]	3:0	1000		TX PA2 Bias current control (Fixed)
0x2b	Register Name	Bit	default	W	Description
	Ictrl_PAPD[3:0]	7:4	0000		TX PA AAC bias current control (Fixed)
	PA1_BIT[3:0]	3:0	0000		TX PA1 Bias current control (Fixed)
0x2c	Register Name	Bit	default	W	Description
	EN_PA_PTAT	7	1		TX PA1 PTAT enable 1: enable PTAT bias
	SLICE_G[0]	6	0		Demodulator gain control (Fixed)
	DCLevel_BIT[1:0]	5:4	01		TX PA AAC reference level selection (Fixed)
	CP_WIN	3	0		TX PA AAC comparator windows selection (Fixed)
	PD_GC_BIT[2:0]	2:0	010		TX PA AAC comparator reference voltage selection (Fixed)
0x2d	Register Name	Bit	default	W	Description
	EN_BPF_PASS	7	0		RX BPF Bypass enable (for test only) 0: normal operation 1: Bypass BPF(no BPF filtering)
	ENB_SL_PD	6	0		Disable Demodulator 1: Disable 0: Enable
	SLICE_G[1]	5	0		Demodulator gain control (Fixed)
	EN_LDout_TS	4	0		Set LD to ATP in test mode
	EN_FILT_AUTO	3	1		AUTO / Manual Filter calibration loop 1: Filter bandwidth auto calibration 0: Manual settling for filter bandwidth (for test only)
	FILT_AUTO_BW	2:0	010		Filter Bandwidth settling for Filter Calibration loop
0x2e	Register Name	Bit	default	W	Description
	DEM_PVT_OPT	7	0		Demodulator reset control
	EN_Vf_TS	6	0		Set Filter Vtune to ATP in test mode
	EN_LD	5	0		Enable PLL Lock detection function
	EN_Vf_TS	4	0		Enable Filter Vtune Test Output
	BY_PTAT	3	0		Bypass PTAT
	BY_BG	2	0		Bypass Bandgap
	EN_CtrlRXOut_bySD	1	1		RX data output notch function 1: Notch the data output when no RF signal input 0: Continues to output RX data
	SLICE_G[2]	0	1		Demodulator gain control (Fixed)
0x2f	Register Name	Bit	default	W	Description
	EN_Vf_B_TS	7	0		Set filter Vf to ATP in test mode
	TS_ld_EnPA	6	0		Enable Test Output for LD & EN_PA (for test only)
	REG1_RB[2:0]	5:3	100		Regulator A output voltage selection (for PLL and Digital)
	BGR_RB[2:0]	2:0	100		Regulator B output voltage selection (for RF & IF)
0x30	Register Name	Bit	default	W	Description
	Sel_LNA_Gain	7	1		To Enhance the LNA Gain 0: Default 1: Enhance LNA Gain
	EN_Internal_LPF	6	1		Enable Internal PLL Loop Filter 0: External PLL loop filter 1: On-Chip PLL loop filter
	EN_TM_PLL_VT	5	0		Enable internal PLL tuning voltage to out-of-chip. (for test only)
	TSO_PA[2:0]	4:2	000		PA biasing voltage selection for test only
	EN_TM_DEM	1	0		Demodulator test mode enable 0: normal operation 1: test mode
	DEM_VT_IO	0	0		Demodulator reference voltage tracking (when R0x30[1]=1, for test only)
0x31	Register Name	Bit	default	W	Description
	SW_TSIO_LPF	7	0		Test Mode Setting (for test only)
	SW_TSIO_BPF	6	0		
	EN_TSO_DEM_FILT	5	0		
	EN_TSO_PA_PLL	4	0		
	EN_TSO_RSSI	3	0		
	EN_TSIO_LPF	2	0		
	EN_TSIO_BPF	1	0		
	EN_TSIO_BS	0	0		
0x32	Register Name	Bit	default	W	Description

	Syn_En_Delay[3:0]	7:4	0100		Time selection for PLL synchronization (Fixed)
	En_Syn_PFD	3	1		PLL synchronization function enable to speed up the PLL settling (Fixed)
	En_Chp_Vt_initial	2	0		Set High to give initial voltage for PLL (Fixed)
	EN_LD_TS	1	0		Set EN_PA to ATP in test model
	EN_TSIO_DIG	0	0		Baseband Test signal IO (when R0x07[7]=1) ATP1: digital output ATP2: digital input
0x33	Register Name	Bit	default	W	Description
	EN_TSO_EN_VCO	7	0		For test only, 1: Set EN_VCO to ATP in test mode 0: Set EN_PA to ATP in test mode
	EN_TSO_Vref_PD	6	0		For test only, 1: Set peak detection reference voltage of PA AAC to ATP in test mode 0: Set PLL locking voltage to ATP in test mode
	Sel_SDOUT_Issig	5	1		Signal detection output selection. 1: SDOUT (default) 0: Issig (for test only)
	Sel_EN_Fast	4	1		To enable the demodulator reset option.
	nEN_DEMPVT	3	1		Demodulator Reset control signal source. Valid when R0x33[3]=1 (for test only) 1: initialization by EN_Fast 0: initialization by EN_DEM
	EN_NoAFC_swCH	2	0		Set High means don't go into AFC when channel switch
	EN_Bat_out	1	0		Battery detection function enable
	En_fun_1Mstop	0	1		Enable the clock gating for PA AAC loop (Fixed)

- Table 10 -

Note: PTAT (Proportional to Absolute Temperature). The circuits bias current proportional to the temperature.

User only can change the configuration registers which highlight with gray background.

9.2 Configuration Registers for Mini MAC

	D7	D6	D5	D4	D3	D2	D1	D0
0x40	STARNET	BURSTMD	PLLOPT	BAKOFFOPT	AUTOACK	NEEDACK	TXDEV	RXDEV
0x41	RXOPT		RXEN5	RXEN4	RXEN3	RXEN2	RXEN1	RXEN0
0x42	ADRBC[1:0]		BRATEC[5:0]					
0x43	PADOPT	CRCLEN[1:0]	SYNCBC[4:0]					
0x44		PKTLEN[6:0]						
0x45	PKTCNT[3:0]							
0x46			TDTXOPT[2:0]			TDPLLOPT[2:0]		
0x47	RETRYCNT[3:0]				SLOTLEN[3:0]			
0x48	INIBACKOFF[7:0]							
0x49	ACKTOSLOT[7:0]							
0x4a			RSSITH[5:0]					
0x4b			RF_RSSI[5:0]					
0x4c					TD_PLLRT[3:0]			
0x4d								SWRST
0x4e							CLKMODE[1:0]	
0x4f	PACKET LOST COUNT[7:0]							
0x50	TXADR[7:0] or RXADR0[7:0]							
0x51	TXADR[15:8] or RXADR0[15:8]							
0x52	RXADR1[7:0]							
0x53	RXADR1[15:8]							
0x54	RXADR2[7:0]							
0x55	RXADR3[7:0]							
0x56	RXADR4[7:0]							
0x57	RXADR5[7:0]							
0x58	BACKOFFWIN[7:0]							

- Table 11 -

Address 0x40 to 0x58

Address (Hex)	Register Name	Bit	Default Value	Type	Description
0x40	Register Name	Bit	default	W/R	Description
	STARNET	7	0		1: there will be a PID byte in Frame structure, and PID byte in TX/RX buffer payload(packet). 0: no PID byte in frame structure, no PID byte in TX/RX buffer payload (packet).
	BURSTMD	6	1		1: SPI master should assert PKTLEN+1 bytes cycles for a complete packet buffer access. The PKTLEN length data succeed with 1 bytes address 0: SPI master will assert 2 cycles PKTLEN times for a complete packet buffer access. 1 bytes address + 1 bytes data in PKTLEN cycles times
	PLLOPT	5	0		when set, TX/RX dev won't wait TDPLLOPT time for normal EN_TX/EN_RX assertion
	BACKOFFOPT	4	1		when 1, during TX Back off window, TXDev's RF will stay in Idle mode. When 0, will stay in RX mode.
	AUTOACK	3	1		valid under RXDEV, RXDEV will auto transmit ACK packet after receiving address hit packet (RXADR0-RXADR5)
	NEEDACK	2	1		valid under TXDEV, TX complete interrupt will be set after receiving ACK from a transmitted packet
	TXDEV	1	0		set current device as a transmitter device, only valid when RXDEV=0
	RXDEV	0	0		set current device as a receiver device, only valid when TXDEV=0
0x41	Register Name	Bit	default	W/R	Description
	RXOPT	7	1		When 1 fixed, chip timing. When 0 dynamic modify chip timing according to zero crossing position.
		6	0		
	RXEN5	5	0		enable receiving packet with RXADR5 address
	RXEN4	4	0		enable receiving packet with RXADR4 address
	RXEN3	3	0		enable receiving packet with RXADR3 address
	RXEN2	2	0		enable receiving packet with RXADR2 address
	RXEN1	1	0		enable receiving packet with RXADR1 address
	RXEN0	0	0		enable receiving packet with RXADR0 address
0x42	Register Name	Bit	default	W/R	Description
	ADRBC[1:0]	7:6	10		address byte counts in each TX/RX frame valid value1-2.
	BRATEC[5:0]	5:0	011000		bit rate counter When CLKMODE=2'b01 (system runs at 16MHz) 6'd16: 1Mbps 6'd10: 1.6Mbps

					When CLKMDOE=2'b10 (system runs at 24MHz) 6'd24: 1Mbps 6'd15: 1.6Mbps
0x43	Register Name	Bit	default	W/R	Description
	PADOPT	7	1		When 1, HW will auto pad one after successively 4 zeros or pad zero after successively 4 ones. Otherwise, after successive 8 zeros or ones
	CRCOPT[1:0]	6:5	10		CRC option 2'h0: no CRC in each TX/RX frame 2'h1: 1 byte CRC in each TX/RX frame with polynomial : x8+x4+x3+x2+1 2'h2: 2 bytes CRC in each TX/RX frame with polynomial : x16+x15+x2+1 2'h3: 4 bytes CRC in each TX/RX frame with polynomial : x32+x26+x23+x22 +x16+x12+x11+x10+x8+x7+x5+x4+x2+x+1
	SYNCBC[4:0]	4:0	00100		sync word length in byte unit. If SYNCBC=10, there will be 10 bytes 8'haa sync pattern in each TX/RX frame
0x44	Register Name	Bit	default	W/R	Description
		7	0		
	PKTLEN[6:0]	6:0	1000		Payload length, excludes ADR and CRC, but *includes PID in star network*.
0x45	Register Name	Bit	default	W/R	Description
	PKTCNT[3:0]	7:4	0111		Max packet counts in buffer. There are PKTCNT packets could be stored in the TX/RX buffer. Make sure PKTLEN * PKTCNT <= 64. (buffer length).
		3:0	0000		
0x46	Register Name	Bit	default	W/R	Description
		7:6	00		
	TDTXOPT	5:3	001		Time delay for TX amplifier. TX device will wait 10+ 5*TDTXOPT (us) for TX amplifier
	TDPLLOPT	2:0	001		Time delay for PLL enable. TX/RX device will wait 100+20*TDPLLOPT (us) for PLL stable.
0x47	Register Name	Bit	default	W/R	Description
	RETRYCNT[3:0]	7:4	0001		TX retry count, valid only when NEEDACK=1. TX device will transmit RETRYCNT+1 times before transmission retry time out. When RETRYCNT=0, the TX device will transmit the packet only once.
	SLOTLEN[3:0]	3:0	0001		In unit 10us, when SLOTLEN=2, which means a slot time is 20us
0x48	Register Name	Bit	default	W/R	Description
	INIBACKOFF[7:0]	7:0	1		in slot unit, TX device will check the channel clearance for INIBACKOFF slots, before transmitting the packet at the first time
0x49	Register Name	Bit	default	W/R	Description
	ACKTOSLOT[7:0]	7:0	10001010		Ack packet response time out length in slot unit. If slot=20us, when ACKTOSLOT[7:0]=10, which means ACK time out when no valid ACK packet received within 200us after transmitting a packet (which needs ack)
0x4a	Register Name	Bit	default	W/R	Description
		7:6	00		
	RSSITH[5:0]	5:0	100111		When mini MAC input RSSI[5:0] larger than RSSITH, which indicates channel occupied (CA=1). If don't want to check the channel clearance, just set RSSITH=63
0x4b	Register Name	Bit	default	R	Description
		7:6			
	RF_RSSI[5:0]	5:0	0		Read only, RF RSSI output
0x4c	Register Name	Bit	default	W/R	Description
		7:4			
	TD_PLLRT	3:0	0110		in unit 10us
0x4d	Register Name	Bit	default	W/R	Description
		7:1			
	SWRST	0	1		1: reset whole system and all configuration except CLKMODE
0x4e	Register Name	Bit	default	W/R	Description
		7:2			
	CLKMODE[1:0]	1:0	10		System Reference Clock 01: 16MHz 10: 24MHz
0x4f	Register Name	Bit	default	W/R	Description
	Packet lost count	7:3	00000		R/W. update by HW. SW write 0 to clear. When lost packet larger than 31, will saturate lost packet count to 31
		2:0			
0x50	Register Name	Bit	default	W/R	Description
	TXADR[7:0]	7:0	0		valid when ADRBC=1-2, when ADRBC=1, TXADR={TXADR[7:0]}
0x51	Register Name	Bit	default	W/R	Description
	TXADR[15:8]	7:0	0		valid when ADRBC=2,when ADRBC=2,

					TXADR={TXADR[15:8],TXADR[7:0]};
0x52	Register Name	Bit	default	W/R	Description
	RXADR1[7:0]	7:0	0		valid when ADRBC=1-2, when ADRBC=1, RXADR1={RXADR1[7:0]}
0x53	Register Name	Bit	default	W/R	Description
	RXADR1[15:8]	7:0	0		valid when ADRBC=2,when ADRBC=2, RXADR1={RXADR1[15:8],RXADR1[7:0]};
0x54	Register Name	Bit	default	W/R	Description
	RXADR2[7:0]	7:0	0		valid when ADRBC=1-2, when ADRBC=1, RXADR2={RXADR2[7:0]}; when ADRBC=2, RXADR2={RXADR1[15:8],RXADR2[7:0]};
0x55	Register Name	Bit	default	W/R	Description
	RXADR3[7:0]	7:0	0		RXADR3[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR3={RXADR3[7:0]}; when ADRBC=2 RXADR3={RXADR1[15:8],RXADR3[7:0]};
0x56	Register Name	Bit	default	W/R	Description
	RXADR4[7:0]	7:0	0		RXADR4[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR4={RXADR4[7:0]}; when ADRBC=2 RXADR4={RXADR1[15:8],RXADR4[7:0]};
0x57	Register Name	Bit	default	W/R	Description
	RXADR5[7:0]	7:0	0		RXADR5[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR5={RXADR5[7:0]}; when ADRBC=2 RXADR5={RXADR1[15:8],RXADR5[7:0]};
0x58	Register Name	Bit	default	W/R	Description
	BACKOFFWIN[7:0]	7:0	0		in slot unit, TX device will check the channel clearance for BACKOFFWIN slots, before transmitting the packet at the retry sequence.

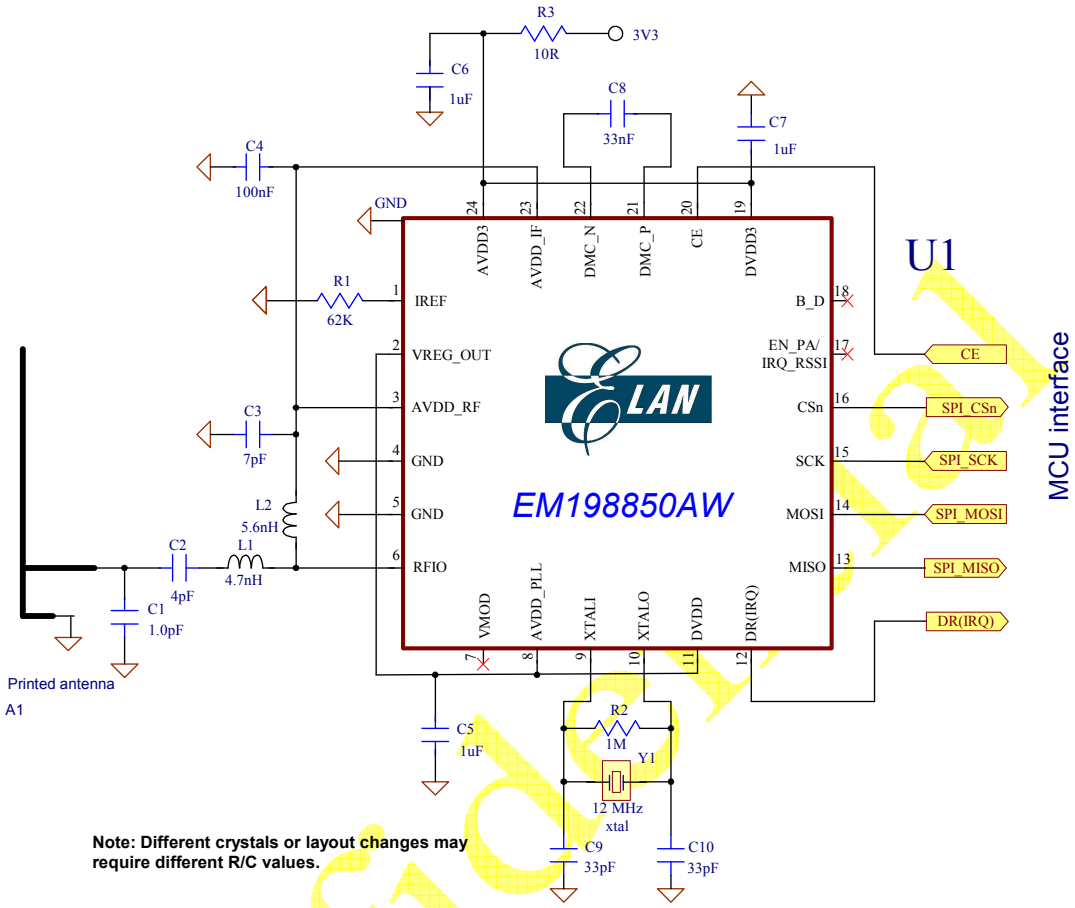
- Table 12 -

Note: User only can change the configuration registers which highlight with gray background.

For the latest register value recommendations, please contact Elan Microelectronics technical group.

10. Application Circuit

Typical Application



- Figure 20 -

BOM list

Comment	Description	Designator	Quantity	Footprint
1pF	Capacitor	C1	1	
4pF	Capacitor	C2	1	SMD-0603
7pF	Capacitor	C3	1	SMD-0603
33pF	Capacitor	C9 C10	2	
33nF	Capacitor	C8	1	
100nF	Capacitor	C4	1	SMD-0603
1.0uF	Capacitor	C5 C6 C7	3	SMD-0603
4.7nH	Inductor	L1	1	
5.6nH	Inductor	L2	1	
10 ohm	Resistor	R3	1	SMD-0603
62k	Resistor	R1	1	SMD-0603
1M	Resistor	R2	1	SMD-0603
12MHz	Crystal	Y1	1	OSC 5x3.2
EM198850AW	IC	U1	1	QFN 24 4x4

- Table 13 -

PCB layout

Top layer **Bottom layer**

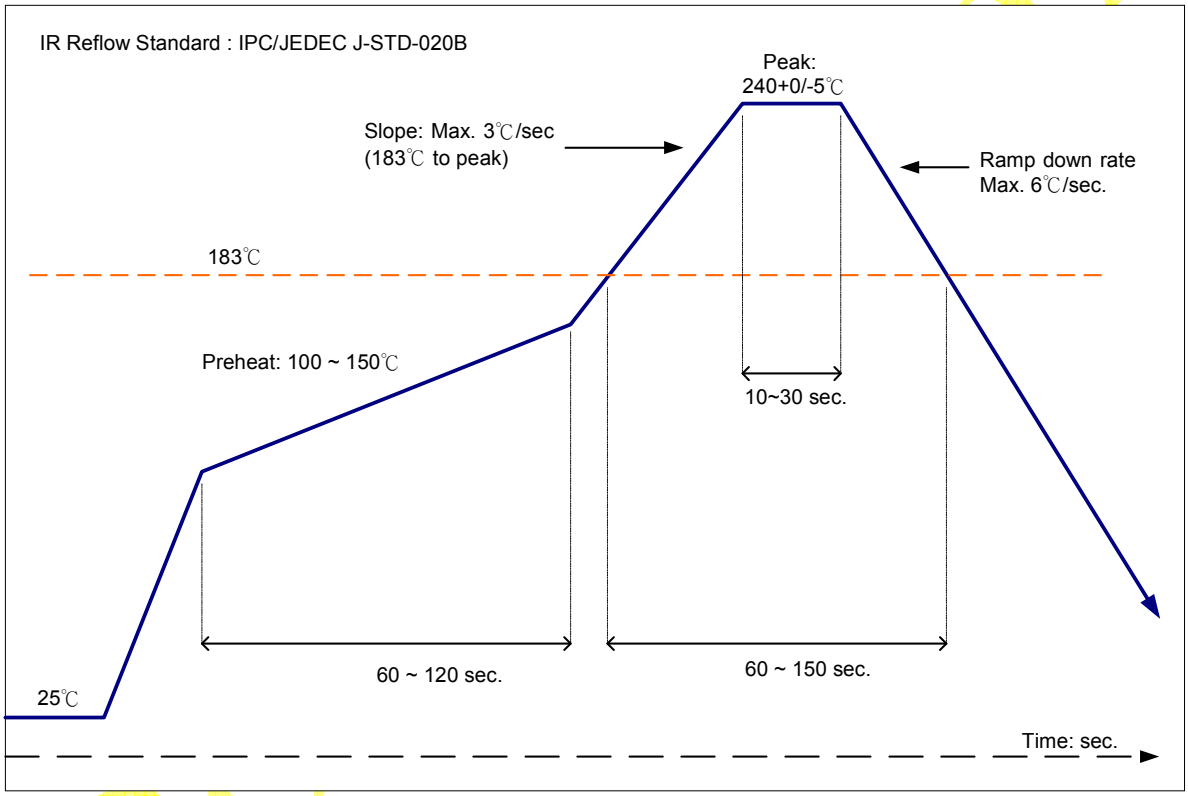
- Figure 21 -

11. SOLDERING

Reflow soldering requires paste to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for reflowing, throughput times vary between 100 and 300 seconds depending on heating method.

Recommendation: Follow IPC/JEDEC J-STD-020B

Condition: Average ramp-up rate (183℃ to peak): 3℃/sec. max.
Preheat: 100 ~ 150℃ 60 ~ 120 sec.
Temperature maintained above 183℃: 60 ~ 150sec.
Time within 5℃ of actual peak temperature: 10 ~ 30sec.
Peak temperature: 240+0/-5℃
Ramp-down rate: 6℃/sec. max.
Time 25℃ to peak temperature: 6 minutes max.
Cycle interval: 5 minutes



- Figure 22 -

DATA SHEET STATUS

Data Sheet Status	Product Status	Definitions
Objective specification	Development	This data sheet contains data from the objective specification for product development. Elan Microelectronics reserves the right to change the specification in any manner without notice.
Preliminary specification	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Elan Microelectronics reserves the right to change the specification without notice in order to improve the design and supply the best possible product.
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