1. Configuration Registers for RF Transceiver

1.1. Register Table of Address 0x00 to 0x33

User only can change the configuration registers which highlight with gray background.

	D7	D6	D5	D4	D3	D2	D1	D0
0x00	1	H_Buf_L_DR	nEN_24M	DR_EN_RX	DR_EN_TX	EN_XO	DR_EN_PLL	nENFun_idle
0x01	1	0	0	0	0	1	0	Sel_16_12
0x02	0	CH_NO						
0x03	1	1	CntR[5:0]					
0x04	0	0	0	0	0	0	0	0
0x05	0	1	0	0	0	0	0	0
0x06	0	1	0	1	1	1	0	1
0x07	0	0	0	1	1	0	0	0
0x08	0	1	0	0	0	0	0	0
0x09	0	0	0	1	1	0	0	0
0x0a	0	1	EN_3M_IF	0	SEL_MOD_RES[3:0]			
0x0b	0	0	0	0	1	0	1	1
0x0c	1	1	1	EN_KXO	KXO_spi[3:0]			
0x0d	0	1	0	0	1	1	1	1
0x0e	1	0	0	1	0	0	0	1
0x0f	0	0	0	1	1	1	0	0
0x20	1	0	1	0	1	1	0	1
0x21	0	1	1	0	0	1	0	0
0x22	0	0	0	0	0	0	0	0
0x23	1	1	0	0	0	0	1	1
0x24	1	0	1	1	1	1	0	1
0x25	1	0	1	0	0	0	1	0
0x26	bat_det_win	0	0	1	EN_700K	0	1	0
0x27	0	0	0	0	1	0	0	1
0x28	0	0	0	0	0	0	0	0
0x29	1	0	nEN12_EN24	1	1	0	bat_det_level[1:0]	
0x2a	0	1	1	1	0	0	0	1
0x2b	0	0	0	0	0	1	1	0
0x2c	1	0	0	0	0	0	0	0
0x2d	0	0	0	1	1	0	1	0
0x2e	0	0	0	0	0	0	1	1

0x2f	0	1	1	0	0	1	0	0
0x30	1	1	0	0	0	0	0	0
0x31	0	0	0	0	0	0	0	0
0x32	0	1	0	0	1	0	1	0
0x33	0	0	1	1	1	0	1	1

Table 1: Configuration Registers for RF Transceiver

1.2. Function Description of Address 0x00 to 0x33

1.2.1. RF Operation Mode Setting / Testing Function Setting

Address	Register Name	Bit	Default	Type	Description
0x00	**Register Name**	**Bit**	**default**	**W**	**Description**
	H_Buf_L_DR	6	1		1: Buffer mode operation 0: Direct mode operation
	nEN_24M	5	1		1: when the other reference clock is used 0: when 24MHz reference clock is used
	DR_EN_RX	4	0		1: Enable RX in DR mode 0: Disable RX in DR mode
	DR_EN_TX	3	0		1: Enable TX in DR mode 0: Disable TX in DR mode
	DR_EN_PLL	1	0		1: Enable PLL in DR mode 0: Disable PLL in DR mode
	nENFun_idle	0	1		1: Disable idle mode 0: Enable idle mode
0x01	**Register Name**	**Bit**	**default**	**W**	**Description**
	Sel_16_12	0	0		Reference clock settling 1: 16MHz 0: 12MHz
0x07	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_BB_TM	7	0		1: Enable BB Test mode for test only 0: Disable BB Test mode for test only
0x28	**Register Name**	**Bit**	**default**	**W**	**Description**
	TS_dig_pllbw	7	0		Digital output selection in test mode (for test only)
	TS_dig_rxdelay	6	0		
	TS_dig_KXO32	5	0		
	TS_dig_KXO10	4	0		
	Reversed	2	0		
	Manual_EN_PLL	0	0		Manual enable PLL for test only
0x29	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TSO_LDPA	7	1		1: Set LD & EN_PA to ATP in test mode
	EN_TSO_SD	6	0		1: Set signal detection output to ATP in test mode
	nEN12_EN24	5	1		System Reference Clock Selection 1: 24MHz 0: 12MHz / 16MHz
0x2d	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_LDout_TS	4	1		Set LD to ATP in test mode
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_Vf_TS	6	0		Set Filter Vtune to ATP in test mode
	EN_Vf_TS	4	0		Enable filter Vtune test output in test mode
0x2f	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_Vf_B_TS	7	0		Set filter Vf to ATP in test mode
	TS_ld_EnPA	6	1		Enable Test Output for LD & EN_PA for test only
0x30	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TM_PLL_VT	5	0		Enable internal PLL tuning voltage to out-of-chip for test only
	TSO_PA[2:0]	4:2	000		PA biasing voltage selection for test only
	EN_TM_DEM	1	0		Demodulator test mode enable 0: normal operation 1: test mode
	DEM_VT_IO	0	0		Demodulator reference voltage tracking (when R0x30[1]=1, for test only)
0x31	**Register Name**	**Bit**	**default**	**W**	**Description**

	SW_TSIO_LPF	7	0		Test Mode Setting for test only
	SW_TSIO_BPF	6	0		Test Mode Setting for test only
	EN_TSO_DEM_FILT	5	0		Test Mode Setting for test only
	EN_TSO_PA_PLL	4	0		Test Mode Setting for test only
	EN_TSO_RSSI	3	0		Test Mode Setting for test only
	EN_TSIO_LPF	2	0		Test Mode Setting for test only
	EN_TSIO_BPF	1	0		Test Mode Setting for test only
	EN_TSIO_BS	0	0		Test Mode Setting for test only
0x32	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_LD_TS	1	1		1: Set EN_PA to ATP in test model
	EN_TSIO_DIG	0	0		Baseband Test signal IO (when R0x07[7]=1) ATP1: digital output ATP2: digital input
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TSO_EN_VCO	7	0		For test only, 1: Set EN_VCO to ATP in test mode 0: Set EN_PA to ATP in test mode
	EN_TSO_Vref_PD	6	0		For test only, 1: Set peak detection reference voltage of PA AAC to ATP in test mode 0: Set PLL locking voltage to ATP in test mode

Table 2: RF Operation Mode Setting / Testing Function Setting

1.2.2. RF Bandgap / Regulator / PTAT / Battery Detection Setting

Address	**Register Name**	**Bit**	**Default**	**Type**	**Description**
0x26	**Register Name**	**Bit**	**default**	**W**	**Description**
	bat_det_win	7	0		Windows selection for battery detection, check with 0x29[1:0]
	L_bypassSavePower	4	1		Set Low to bypass Save Power function for test only
	EN_CLK_STOP	1	1		Enable clock gating in test mode for test only
	Reversed	0	0		
0x29	**Register Name**	**Bit**	**default**	**W**	**Description**
	bat_det_level[1:0]	1:0	00		Selection of Battery detection level Threshold Voltage 0x29[1:0] / 0x26[7]=0 / 0x26[7]=1 00 / 1.9 / 1.7 01 / 2.0 / 1.8 10 / 2.1 / 1.9 11 / 2.2 / 2.0
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	BY_PTAT	3	0		Bypass PTAT for test only
	BY_BG	2	0		Bypass Bandgap for test only
0x2f	**Register Name**	**Bit**	**default**	**W**	**Description**
	REG1_RB[2:0]	5:3	100		Regulator A output voltage selection for PLL and Digital
	BGR_RB[2:0]	2:0	100		Regulator B output voltage selection for RF & IF
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_Bat_out	1	1		Battery detection function enable

Table 3: RF Bandgap / Regulator / PTAT / Battery Detection Setting

1.2.3. RF Clock / Crystal Setting

Address	**Register Name**	**Bit**	**Default**	**Type**	**Description**
0x00	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_CLK	7	1		1: Enable Digital Circuits System Clock 0: Disable Digital Circuits System Clock
	EN_XO	2	1		1: Enable Crystal Buffer 0: Disable Crystal Buffer
0x01	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_SavePower	3	0		Enable clock gating in test mode for test only
	nEN_Ictrl_XO[1]	2	1		Crystal buffer bias current, {R0x0b[7],R0x01[2:1]} default 010.
	EN_Ictrl_XO[0]	1	0		
0x03	**Register Name**	**Bit**	**default**	**W**	**Description**
	Reserved	7	1		
	EN_75M	6	1		Enable 75M reference clock function
0x0a	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_XO[2]	7	0		Crystal settling wait time during frequency calibration

0x0c	Register Name	Bit	default	W	Description
	EN_KXO	4	0		1: Start crystal frequency calibration 0: Disable crystal frequency calibration
	KXO_spi[3:0]	3:0	0000		Crystal Loading Capacitor Selection 0000: CL=27p
0x0f	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_XO[1:0]	7:6	00		Crystal settling wait time during frequency calibration

Table 4: RF Clock / Crystal Setting

1.2.4. RF Digital Function Setting

Address	Register Name	Bit	Default	Type	Description
0x08	**Register Name**	**Bit**	**default**	**W**	**Description**
	TxDC_SW_3W	7	0		Manual control TX LPF corner for test only
	EN_RxEN_Delay	6	1		1: Enable the function which delays to enable RX RF to save current during PLL un-locked in Rx mode.
0x09	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_RxEN[2:0]	7:5	000		RX chain off time control (Check with 0x08[6]) Off Time=20us*(1+Delay_RxEN[2:0])
0x0b	**Register Name**	**Bit**	**default**	**W**	**Description**
	nEN_XO_2uA	7	0		Crystal buffer bias current, {R0x0b[7],R0x01[2:1]} default 010.
	Delay_TxDC[0]	6	0		Check with 0x0a[4], compensation filter settling time control
	CHP_SW_3w	5	0		Charge Pump Current Control Mode for test only
	Delay_CHP_SW[3:0]	4:1	0101		Charge Pump bias current control
	EN_PLL_Fast	0	1		1: Enable PLL fast settling option
0x0e	**Register Name**	**Bit**	**default**	**W**	**Description**
	Low_wRFSPI	7	1		1: Set 1 to forbid to write RF SPI registers, 0x20 to 0x33 0: Set 0 to allow to write RF SPI registers, 0x20 to 0x33
	EN_PAONdelay	6	0		1: Enable the time delay between PLL ON and PA ON for test only
	EN_Stop1M_D[1:0]	5:4	01		Clock gating delay for internal circuit's system clock.
	EN_PAON_D[3:0]	3:0	0001		Check with 0x0e[6], setting the delay time for test only
0x29	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_75M_toKXO	4	1		1: Enable clock gating option for frequency calibration
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	En_fun_1Mstop	0	1		Enable the clock gating for PA AAC loop (Fixed)

Table 5: RF Digital Function Setting

1.2.5. PLL Block Setting

Address	Register Name	Bit	Default	Type	Description
0x23	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PTAT_Buf_RxMx	7	1		Enable PTAT option for RX Mixer 1: with PTAT 0: without PTAT
	Ictrl_Buf_RxMx[2:0]	6:4	100		RX Mixer bias control (Fixed)
	EN_PTAT_Div2	3	0		Enable PTAT option for divide by 2 1: with PTAT 0: without PTAT
	Ictrl_Div2[2:0]	2:0	011		Divide by 2 bias control (Fixed)
0x24	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PTAT_Buf_D2S	7	1		Enable PTAT option for RF D2S buffer 1: with PTAT 0: without PTAT
	Ictrl_Buf_D2S[2:0]	6:4	011		RF D2S buffer bais control (Fixed)
	EN_PTAT_Buf_IQComb	3	1		Enable PTAT option for IQ combiner buffer 1: with PTAT 0: without PTAT
	Ictrl_Buf_IQ_Comb[2:0]	2:0	101		IQ combiner buffer bias control (Fixed)
0x25	**Register Name**	**Bit**	**default**	**W**	**Description**
	Ictrl_VCO[2:0]	5:3	100		VCO bias control (Fixed)
	EN_PTAT_Pre	2	0		Enable PTAT option for Prescaler 1: with PTAT 0: without PTAT
	Ictrl_Pre[1:0]	1:0	10		Prescaler bias control (Fixed)
0x26	**Register Name**	**Bit**	**default**	**W**	**Description**
	Ictrl_CHP_UP[4]	2	0		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
0x27	**Register Name**	**Bit**	**default**	**W**	**Description**

	Ictrl_CHP_UP[3:0]	7:4	0000		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
	Ictrl_CHP_DN[3:0]	3:0	1001		Decrease Charge Pump Bias Current, Ictrl_CHP_DN[3:0] (Fixed)
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_LD	5	0		1: Enable PLL lock detection function 0: Disable PLL lock detection function
0x30	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_Internal_LPF	6	1		Enable Internal PLL Loop Filter 0: External PLL loop filter for test only 1: On-Chip PLL loop filter
0x32	**Register Name**	**Bit**	**default**	**W**	**Description**
	Syn_En_Delay[3:0]	7:4	0100		Time selection for PLL synchronization (Fixed)
	En_Syn_PFD	3	1		1: Enable PLL synchronization function to speed up the PLL settling
	En_Chp_Vt_initial	2	0		1: give initial voltage for PLL

Table 6: PLL Block Setting

1.2.6. Channel and AFC Setting

<table>
<tr><th>Address</th><th>Register Name</th><th>Bit</th><th>Default</th><th>Type</th><th>Description</th></tr>
<tr><td>0x02</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>CH_AutoMan</td><td>7</td><td>0</td><td></td><td>Switch manual / look up table program RF channel.
Look up table: set by CH_NO
0: Auto lookup table approach
1: Manual control via registers R0x04 & R0x05 (for test only)</td></tr>
<tr><td></td><td>CH_NO</td><td>6:0</td><td>0000000</td><td></td><td>Channel frequency setting
(RF Frequency)
<table>
<tr><th colspan="3">Data Rate = 1Mbps</th></tr>
<tr><td>CH_NO</td><td>TX
(Fc)</td><td>RX
(Fc-2MHz)</td></tr>
<tr><td>‘h00</td><td>2400MHz</td><td>2398MHz</td></tr>
<tr><td>‘h01</td><td>2401MHz</td><td>2399MHz</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>‘h53</td><td>2483MHz</td><td>2481MHz</td></tr>
</table>
(RF Frequency)
<table>
<tr><th colspan="3">Data Rate = 1.6Mbps</th></tr>
<tr><td>CH_NO</td><td>TX
(Fc)</td><td>RX
(Fc-3MHz)</td></tr>
<tr><td>‘h00</td><td>2401MHz</td><td>2398MHz</td></tr>
<tr><td>‘h01</td><td>2402MHz</td><td>2399MHz</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>‘h53</td><td>2484MHz</td><td>2481MHz</td></tr>
</table></td></tr>
<tr><td>0x03</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>CntR[5:0]</td><td>5:0</td><td>000110</td><td></td><td>
<table>
<tr><th>Ref. Clock</th><th>CntR[5:0]</th></tr>
<tr><td>12MHz</td><td>000110</td></tr>
<tr><td>16MHz</td><td>001000</td></tr>
<tr><td>24MHz</td><td>001100</td></tr>
</table></td></tr>
<tr><td>0x04</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>CntB[7:0]</td><td>7:0</td><td>00000000</td><td></td><td>B counter of PLL for test mode</td></tr>
<tr><td>0x05</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>EnFun_ManTrigAFC</td><td>7</td><td>0</td><td></td><td>Manual trigger AFC for test only</td></tr>
<tr><td></td><td>EN_AFC_Code</td><td>6</td><td>1</td><td></td><td>Enable AFC</td></tr>
<tr><td></td><td>Manual_EN_AFC</td><td>5</td><td>0</td><td></td><td>Manual enable AFC for test only</td></tr>
<tr><td></td><td>CntA[4:0]</td><td>4:0</td><td>00000</td><td></td><td>A counter of PLL for test mode</td></tr>
<tr><td>0x07</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>VCO_AFC_Resol[1:0]</td><td>4:3</td><td>11</td><td></td><td>VCO AFC resolution control</td></tr>
<tr><td></td><td>VCO_AFC_3W[2:0]</td><td>2:0</td><td>000</td><td></td><td>VCO AFC curve manual selection when 0x05[5]=1 for test only</td></tr>
<tr><td>0x08</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>SC_CH[5:0]</td><td>5:0</td><td>000000</td><td></td><td>VCO capacitor array for fast settling</td></tr>
<tr><td>0x25</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>Vctrl_VCO_CAL[1:0]</td><td>7:6</td><td>10</td><td></td><td>VCO AFC ‘s control voltage selection (Fixed)</td></tr>
<tr><td>0x33</td><td>Register Name</td><td>Bit</td><td>default</td><td>W</td><td>Description</td></tr>
<tr><td></td><td>EN_NoAFC_swCH</td><td>2</td><td>0</td><td></td><td>Set High means don’t go into AFC when channel switch</td></tr>
</table>

Table 7: Channel and AFC Setting

1.2.7. RX Demodulator Setting

Address	Register Name	Bit	Default	Type	Description
0x09	**Register Name**	**Bit**	**default**	**W**	**Description**
	SEL_I_V	3	1		Switch ADC input from RSSI or Vtune of VCO (SEL_I_V) 1: RSSI 0: Vtune of VCO for test only
	SEL_VB[2:0]	2:0	000		Selection ADC Full range Voltage SEL_B[2:0] for test only
0x0a	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_SignalDet	6	1		1: Enable Signal Detection Circuits for test only
0x0c	**Register Name**	**Bit**	**default**	**W**	**Description**
	SD_EN_DutyDelta	7	1		RX Signal detection option.
	SD_EN_FreqDelta	6	1		
	Sel_SD	5	1		
0x0d	**Register Name**	**Bit**	**default**	**W**	**Description**
	SD_DutyDelta[1:0]	7:6	01		RX Signal detection options. (Fixed)
	SD_FreqDelta[1:0]	5:4	00		
	SD_RangeH[1:0]	3:2	11		
	SD_Range	1	1		
	SD_Noise	0	1		
0x28	**Register Name**	**Bit**	**default**	**W**	**Description**
	PDEN_HR_LSD	3	0		RX Data Controlled by RSSI or Signal Detect Function 1: by RSSI 0: by Signal Detect Function
	H_macPD_L_enPD	1	0		RX demodulator Mode Selection
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_CtrlRxOut_bySD	1	1		RX data output notch function 1: Notch the data output when no RF signal input 0: Continues to output RX data
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	DataEN_HR_LSD	5	1		Signal detection output selection. 1: controlled by RSSI (default) 0: controlled by Signal Detect Function (for test only)

Table 8: RX Demodulator Setting

1.2.8. RX Block Setting

Address	Register Name	Bit	Default	Type	Description
0x07	**Register Name**	**Bit**	**default**	**W**	**Description**
	LRSSI_HLD	6	0		RF Status Indication (as R2E[5] = 1) 1: Read R0x4B[0] to get LD signal 0: Read R0x4B[0] to get RSSI[0]
0x0a	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_3M_IF	5	0		1: IF = 3MHz for 1.6Mbps data rate 0: IF = 2MHz for 1Mbps data rate
0x20	**Register Name**	**Bit**	**default**	**W**	**Description**
	FE_PTAT	7	1		Enable PTAT option for Front-End 1: with PTAT 0: without PTAT
	Reversed	6	0		
	MIX_BS[3:0]	5:3	101		RX Mixer bias control (Fixed)
	LNA_BS[3:0]	2:0	101		RX LNA bias control (Fixed)
0x21	**Register Name**	**Bit**	**default**	**W**	**Description**
	FILT_PTAT_CTRL[1:0]	7:6	01		Filter PTAT Control. Default: 01
	CLM_G[2:0]	5:3	100		RX buffer High/Low gain mode control (Fixed)
	CLM_SW[2:0]	2:0	100		RX buffer High/Low output swing control (Fixed)
0x22	**Register Name**	**Bit**	**default**	**W**	**Description**
	SLICE_Nb[3:0]	7:4	0000		RX Slicer Common DC control (Fixed)
	SLICE_Pb[3:0]	3:0	0000		
0x26	**Register Name**	**Bit**	**default**	**W**	**Description**
	PD_sel_10p	6	0		Capacitor selection for RX demodulator (Fixed)
	SLICE_G[3]	5	0		Demodulator Buffer Gain (Fixed)
	EN_700K	3	1		RX IF LPF bandwidth selection 1: for 1Mbps data rate 0: for 1.6Mbps data rate
0x29	**Register Name**	**Bit**	**default**	**W**	**Description**
	Vf_reg_ctrl[1:0]	3:2	10		Set filter calibration output voltage to ATP in test mode
0x2c	**Register Name**	**Bit**	**default**	**W**	**Description**
	SLICE_G[0]	6	0		Demodulator gain control (Fixed)
0x2d	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_BPF_PASS	7	0		0: normal operation

					1: Bypass Rx BPF for test only
	ENB_SL_PD	6	0		1: Disable Demodulator for test only 0: Normal operation
	SLICE_G[1]	5	0		Demodulator gain control (Fixed)
	EN_FILT_AUTO	3	1		AUTO / Manual Filter calibration loop 1: Filter bandwidth auto calibration 0: Manual settling for filter bandwidth for test only
	FILT_AUTO_BW	2:0	010		Filter Bandwidth settling for Filter Calibration loop
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	DEM_PVT_OPT	7	0		Demodulator reset control in test mode
	SLICE_G[2]	0	1		Demodulator gain control (Fixed)
0x30	**Register Name**	**Bit**	**default**	**W**	**Description**
	Sel_LNA_Gain	7	1		To Enhance the LNA Gain 0: Default 1: Enhance LNA Gain
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	Sel_EN_Fast	4	1		To enable the demodulator reset option.
	nEN_DEMPVT	3	1		Demodulator Reset control signal source. Valid when R0x33[3]=1 (for test only) 1: initialization by EN_Fast 0: initialization by EN_DEM

Table 9: RX Block Setting

1.2.9. TX Block Setting

Address	Register Name	Bit	Default	Type	Description
0x01	**Register Name**	**Bit**	**default**	**W**	**Description**
	PA_AAC	7	1		Toggle PA Auto Amplitude Control function
	TX_PWR[2:0]	6:4	000		TX output power selection in Test mode. Default = 000 (0dBm)
0x06	**Register Name**	**Bit**	**default**	**W**	**Description**
	PA3_WC[2:0]	7:5	010		PA3 Gain Control. Please refer to the application note in detail.
	PA2_WC[1:0]	4:3	11		PA2 Gain Control. Please refer to the application note in detail.
	PA1_WC[1:0]	2:1	10		PA1 Gain Control. Please refer to the application note in detail.
	D2S_Gain	0	1		D2S Gain control. Please refer to the application note in detail.
0x07	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_AAC_TM	5	0		Enable PA AAC auto-calibrated control 1: Enable PA output power auto calibration.
0x09	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TxMOD	4	1		1: Enable the frequency deviation tuning (Tuning by 0x0a[2:0])
0x0a	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TxDC_LPF	4	0		1: Enable transmitter data compensation filter
	SEL_MOD_RES[3:0]	3:0	0111		Transmitter Frequency Deviation Control 0x0a[3:0] / Frequency Deviation (kHz) 0 0 1 1 / 200 0 1 1 1 / 400 1 1 0 1 / 500
0x0f	**Register Name**	**Bit**	**default**	**W**	**Description**
	I_PA_UPDN[5:0]	5:0	011100		PA gain control options.
0x2a	**Register Name**	**Bit**	**default**	**W**	**Description**
	PA3_BIT[3:0]	7:4	0111		TX PA3 Bias current control (Fixed)
	PA2_BIT[3:0]	3:0	0001		TX PA2 Bias current control (Fixed)
0x2b	**Register Name**	**Bit**	**default**	**W**	**Description**
	Ictrl_PAPD[3:0]	7:4	0000		TX PA AAC bias current control (Fixed)
	PA1_BIT[3:0]	3:0	0110		TX PA1 Bias current control (Fixed)
0x2c	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PA_PTAT	7	1		Enable PTAT option for TX PA1 1: with PTAT 0: without PTAT
	DCLevel_BIT[1:0]	5:4	00		TX PA AAC reference level selection (Fixed)
	CP_WIN	3	0		TX PA AAC comparator windows selection (Fixed)
	PD_GC_BIT[2:0]	2:0	000		TX PA AAC comparator reference voltage selection (Fixed)

Table 10: TX Block Setting

Note: PTAT (Proportional to Absolute Temperature): The bias currents of the circuits are proportional

to the temperature

2. Configuration Registers for Mini MAC

2.1. Register Table of Address 0x40 to 0x58

User only can change the configuration registers which highlight with gray background.

	D7	D6	D5	D4	D3	D2	D1	D0
0x40	STARNET	BURSTMD	0	1	AUTOACK	NEEDACK	TXDEV	RXDEV
0x41	1	0	RXEN5	RXEN4	RXEN3	RXEN2	RXEN1	RXEN0
0x42	ADRBC[1:0]		BRATEC[5:0]					
0x43	1	CRCLEN[1:0]		SYNCBC[4:0]				
0x44	0	PKTLEN[6:0]						
0x45	PKTCNT[3:0]				0	0	0	0
0x46	0	0	TDTXOPT[2:0]			TDPLLOPT[2:0]		
0x47	RETRYCNT[3:0]				SLOTLEN[3:0]			
0x48	0	0	0	0	0	0	0	1
0x49	ACKTOSLOT[7:0]							
0x4a	0	0	RSSITH[5:0]					
0x4b	0	0	RF_RSSI[5:0]					
0x4c	0	0	0	0	TD_PLLRT[3:0]			
0x4d	0	0	0	0	0	0	0	SWRST
0x4e	0	0	0	0	0	0	CLKMODE[1:0]	
0x4f	PACKET LOST COUNT[7:3]					0	0	0
0x50	TXADR[7:0] or RXADR0[7:0]							
0x51	TXADR[15:8] or RXADR0[15:8]							
0x52	RXADR1[7:0]							
0x53	RXADR1[15:8]							
0x54	RXADR2[7:0]							
0x55	RXADR3[7:0]							
0x56	RXADR4[7:0]							
0x57	RXADR5[7:0]							
0x58	BACKOFFWIN[7:0]							

Table 11: Configuration Registers for Mini MAC

2.2. Function Description of Address 0x40 to 0x58

2.2.1. System Setting

Address	Register Name	Bit	Default	Type	Description
0x40	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	STARNET	7	0		1: there will be a PID in frame structure, and this 1 byte PID will be in MSB of TX/RX buffer payload(packet). For detail information, please refer to the section of Packet Description. 0: no PID byte in frame structure, no PID byte in TX/RX buffer payload (packet).
	BURSTMD	6	1		For the detail description, please refer to the section of SPI interface read/write FIFO for buffer mode. 1: SPI master should assert PKTLEN+1 bytes cycles for a complete packet buffer access. The PKTLEN length data succeed with 1 bytes address 0: SPI master will assert 2 cycles PKTLEN times for a complete packet buffer access. 1 bytes address + 1 bytes data in PKTLEN cycles times
	PLLOPT	5	0		1: TX/RX dev won't wait TDPLLOPT time for normal EN_TX/EN_RX assertion 0: TX/RX dev will wait TDPLLOPT time for normal EN_TX/EN_RX assertion
	BACKOFFOPT	4	1		1: as during TX Back off window, TX device's RF will stay in Idle mode. 0: otherwise, it will stay in RX mode.
	AUTOACK	3	1		1: only valid under RXDEV, RXDEV will transmit ACK packet after receiving address hit packet automatically (RXADR0-RXADR5) 0: Disable Auto ACK function
	NEEDACK	2	1		1: only valid under TXDEV, TX complete interrupt will be set after receiving ACK from a transmitted packet 0: Disable the function
	TXDEV	1	1		1: set current device as a transmitter device, only valid when RXDEV=0
	RXDEV	0	0		1: set current device as a receiver device, only valid when TXDEV=0
0x41	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXOPT	7	1		1: chip timing. 0: dynamic modify chip timing according to zero crossing position.
	Reserved	6	0		
	RXEN5	5	0		1: enable receiving packet with RXADR5 address
	RXEN4	4	0		1: enable receiving packet with RXADR4 address
	RXEN3	3	0		1: enable receiving packet with RXADR3 address
	RXEN2	2	0		1: enable receiving packet with RXADR2 address
	RXEN1	1	0		1: enable receiving packet with RXADR1 address
	RXEN0	0	0		1: enable receiving packet with RXADR0 address

Table 12: System Setting

2.2.2. Frame Format Setting

Address	Register Name	Bit	Default	Type	Description
0x42	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	ADRBC[1:0]	7:6	10		address byte counts in each TX/RX frame valid value1-2.
	BRATEC[5:0]	5:0	011000		bit rate counter When CLKMODE=2'b01 (system runs at 16MHz) 6'd16: 1Mbps 6'd10: 1.6Mbps When CLKMDOE=2'b10 (system runs at 24MHz) 6'd24: 1Mbps 6'd15: 1.6Mbps
0x43	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	PADOPT	7	1		1: HW will auto pad one after successively 4 zeros or pad zero after successively 4 ones. 0: otherwise, after successive 8 zeros or ones
	CRCOPT[1:0]	6:5	10		CRC option 00: no CRC in each TX/RX frame 01: 1 byte CRC in each TX/RX frame with polynomial : x8+x4+x3+x2+1 10: 2 bytes CRC in each TX/RX frame with polynomial : x16+x15+x2+1 11: 4 bytes CRC in each TX/RX frame with polynomial : x32+x26+x23+x22 +x16+x12+x11+x10+x8+x7+x5+x4+x2+x+1
	SYNCBC[4:0]	4:0	00100		sync word length in byte unit. If SYNCBC=10, there will be 8 bytes 8'haa sync pattern (8'b10101010) in each TX/RX frame

0x44	Register Name	Bit	default	W/R	Description
	Reserved	7	0		
	PKTLEN[6:0]	6:0	0001000		Payload length, excludes ADR and CRC, but *includes PID in star network*.
0x45	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	PKTCNT[3:0]	7:4	0001		Max packet counts in buffer. There are PKTCNT packets could be stored in the TX/RX buffer. Make sure PKTLEN * PKTCNT <= 64. (buffer length).
	Reserved	3:0	0000		

Table 13: Frame Format Setting

2.2.3. RF Signal Control Setting

Address	Register Name	Bit	Default	Type	Description
0x46	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:6	00		
	TDTXOPT	5:3	001		Time delay for TX amplifier. TX device will wait 10+5*TDTXOPT (us) for TX amplifier stable.
	TDPLLOPT	2:0	001		Time Delay for PLL enable TX/RX device will wait 100+ 20*TDPLLOPT (us) for PLL stable
0x4c	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:4	0000		
	TD_PLLRT	3:0	0110		in unit 10us

Table 14: RF Signal Control Setting

2.2.4. CSMA CA Setting

Address	Register Name	Bit	Default	Type	Description
0x47	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RETRYCNT[3:0]	7:4	0001		TX retry count, valid only when NEEDACK=1. TX device will transmit RETRYCNT+1 times before transmission retry time out. When RETRYCNT=0, the TX device will transmit the packet only once.
	SLOTLEN[3:0]	3:0	0001		In unit 10us, when SLOTLEN=2, which means a slot time is 20us
0x48	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	INIBACKOFF[7:0]	7:0	00000001		in slot unit, TX device will check the channel clearance for INIBACKOFF slots, before transmitting the packet at the first time
0x49	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	ACKTOSLOT[7:0]	7:0	10001010		Ack packet response time out length in slot unit. If slot=20us, when ACKTOSLOT[7:0]=10, which means ACK time out when no valid ACK packet received within 200us after transmitting a packet (which needs ack)
0x4a	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:6	00		
	RSSITH[5:0]	5:0	100111		When mini MAC input RSSI[5:0] larger than RSSITH, which indicates channel occupied (CA=1). If don't want to check the channel clearance, just set RSSITH=63

Table 15: CSMA CA Setting

2.2.5. RF SPI Interface Setting

Address	Register Name	Bit	Default	Type	Description
0x4b	**Register Name**	**Bit**	**default**	**R**	**Description**
	Reserved	7:6	00		
	RF_RSSI[5:0]	5:0			Read only, RF RSSI output
0x4d	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:1	0000000		
	SWRST	0	1		1: reset whole system and all configuration except CLKMODE
0x4e	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:2	000000		
	CLKMODE[1:0]	1:0	10		System Reference Clock 01: 16MHz 10: 24MHz
0x4f	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Packet lost count	7:3	00000		R/W. update by HW. SW write 0 to clear. When lost packet larger than

					31, will saturate lost packet count to 31
	Reserved	2:0	000		

Table 16: RF SPI Interface Setting

2.2.6. TX/RX Address 0/1 Setting

Address	Register Name	Bit	Default	Type	Description
0x50	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	TXADR[7:0]	7:0	00000000		valid when ADRBC=1-2, when ADRBC=1, TXADR={TXADR[7:0]}
0x51	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	TXADR[15:8]	7:0	00010001		valid when ADRBC=2,when ADRBC=2, TXADR={TXADR[15:8],TXADR[7:0]};
0x52	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR1[7:0]	7:0	00100010		valid when ADRBC=1-2, when ADRBC=1, RXADR1={RXADR1[7:0]}
0x53	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR1[15:8]	7:0	00110011		valid when ADRBC=2,when ADRBC=2, RXADR1={RXADR1[15:8],RXADR1[7:0]};

Table 17: TX/RX Address 0/1 Setting

2.2.7. RX Address 2/3/4/5 Setting

Address	Register Name	Bit	Default	Type	Description
0x54	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR2[7:0]	7:0	01000100		valid when ADRBC=1-2, when ADRBC=1, RXADR2={RXADR2[7:0]}; when ADRBC=2, RXADR2={RXADR1[15:8],RXADR2[7:0]};
0x55	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR3[7:0]	7:0	01010101		RXADR3[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR3={RXADR3[7:0]}; when ADRBC=2 RXADR3={RXADR1[15:8],RXADR3[7:0]};
0x56	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR4[7:0]	7:0	01100110		RXADR4[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR4={RXADR4[7:0]}; when ADRBC=2 RXADR4={RXADR1[15:8],RXADR4[7:0]};
0x57	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR5[7:0]	7:0	01110111		RXADR5[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR5={RXADR5[7:0]}; when ADRBC=2 RXADR5={RXADR1[15:8],RXADR5[7:0]};

Table 18: RX Address 2/3/4/5 Setting

2.2.8. BACKOFFWIN Setting

Address	Register Name	Bit	Default	Type	Description
0x58	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	BACKOFFWIN[7:0]	7:0	00001000		in slot unit, TX device will check the channel clearance for BACKOFFWIN slots, before transmitting the packet at the retry sequence.

Table 19: BACKOFFWIN setting

3. Power ON Initialization Procedure

3.1. The Procedure of the state of “All Registers Initialization Configuration”

The Figure will be shown the procedure of the all registers initialization configuration. First, initialize the all registers. Then, do the RX RSSI calibration.

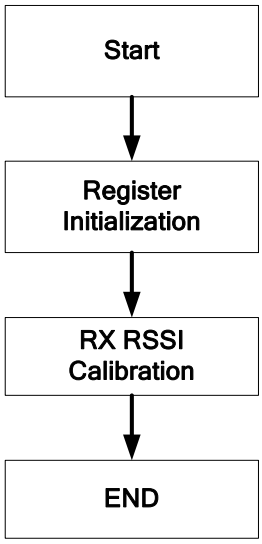
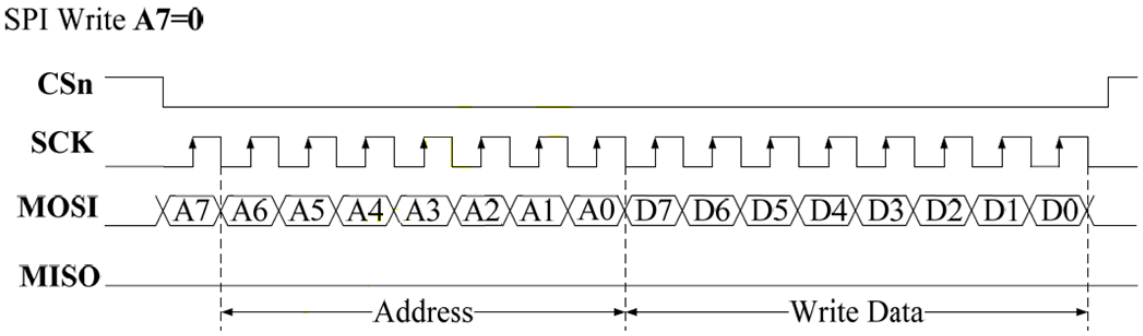


Figure 1: The state machine of the all registers initialization configuration

3.2. SPI Timing Description



Example: Write Address:4E ,Data 02 ➔ 4E02
A7,A6,A5,A4,A3,A2,A1,A0=01001110
D7,D6,D5,D4,D3,D2,D1,D0=00000010

Note: The maximum SCK Clock is given 10MHz.

3.3. The Contents of the state of “Register Initialization”

The contents listed below are the registers initialization procedure in sequence.

4E02 → 4D01 → 4298 → 43C4 → 4408 → 4510 → 4609 → 4711 → 4801 → 498A → 4A27 → 4B00 → 4C06 → 5000 → 5111 → 5222 → 5333 → 5444 → 5555 → 5666 → 5777 → 5808 → 00E5 → 0184 → 0200 → 03C6 → 0400 → 0540 → 065D → 0718 → 0840 → 0918 → 0A47 → 0B0B → 0CE0 → 0D4F → 0E11 → 0F1C → 20AD → 2164 → 2200 → 23C3 → 24BD → 25A2 → 261A → 2709 → 2800 → 29B8 → 2A71 → 2B06 → 2C80 → 2D1A → 2E03 → 2F64 → 30C0 → 3100 → 3240 → 333B → 00A7 → 324A → 00E5 → 0E91

3.4. The Contents of the state of “RX RSSI Calibration”

The contents listed below are the RX RSSI Calibration procedure in sequence.

4051 → 4181 → 0CC0 → 0280 →044A →05DA →05FA → MCU delay 250usec
→ MCU continues reading 0x4B 5 times → MCU selects the maximal 0x4B value and minus 4[*7].
Then, MCU writes the result into 0x4A → 0540 → 0200 → 0CE0

* 1: As data rate = 1Mbps, minus 4. As data rate = 1.6Mbps, minus 6.

3.5. The initialization Contents for the system condition

The register contents are for the system condition listed below:

- Data Rate = 1Mbps
- Crystal Frequency = 12MHz
- TX/RX Buffer Mode
- Package Length = 8 bytes
- Syn. Length = 4 bytes
- Disable Star Network
- Disable Auto-ACK & Auto Re-Transmission

4. Programmable Function Description

4.1. Data Rate & Ref. Clock Register Setting

Data Rate	Clock.	R00	R01	R29	R03	R0A	R26	R42	R4A	R4E
(Mbps)	(MHz)	[5]	[0]	[5]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]	[7:0]
1.6	12	1	0	1	0xC6	0x4D	0x12	0x8F	0x27	0x02
1	12	1	0	1	0xC6	0x47	0x1A	0x98	0x3F	0x02
1.6	16	1	1	x	0xC8	0x4D	0x12	0x8A	0x27	0x01
1	16	1	1	x	0xC8	0x47	0x1A	0x90	0x3F	0x01
1.6	24	0	1	1	0xCC	0x4D	0x12	0x8F	0x27	0x02
1	24	0	1	1	0xCC	0x47	0x1A	0x98	0x3F	0x02

Table 20: Data Rate & Crystal Frequency Register Setting

According to the specification of date rate and reference clock, find out the corresponding register values before write registers. When write the initial register values, set the relative register values. For example: if data rate = 1Mbps & reference clock = 12MHz, the initial content of register 0x03 will be written 0xC6. If data rate = 1.6Mbps & reference clock = 24MHz, the initial content of register 0x03 will be written 0xCC.

4.2. Description of Register 0x0E[7]

- 0x0E[7]=1: set 1 to forbid to write anyone of RF SPI registers address from 0x20 to 0x33
- 0x0E[7]=0: set 0 to allow to write anyone of RF SPI registers address from 0x20 to 0x33

Example:

If MCU needs to write register R28, because it is one of RF SPI registers from 0x20 to 0x33, MCU writes register sequence from 0E11 → content of register 0x28 → 0E91

4.3. RF Channel Setting

CH_No.	0x02[7:0]
0	0x00
1	0x01
2	0x02
⋮	⋮
62	0x3E
63	0x3F
⋮	⋮
81	0x51
82	0x52
83	0x53

Table 21: RF Channel Setting

4.4. RX/TX FIFO Reset Function

When MCU writes 4D01 through 4-wire SPI, TX/RX FIFO will be reset. For RX device, because RX receiver is always active, RF blocks need 120usec settling time after FIFO reset.