MU2400 / MU2401

2.4GHZ Low Data Rate RF Transceiver

Data Sheet

DATA SHEET

Version 1.4.0

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MuChip Corp. Ltd

MU2400/MU2401 – 2.4GHz Low Data Rate RF Transceiver

General Description

The MU2400 is a single-chip FSK low data rate RF transceiver for the world wide 2.4 – 2.5GHz ISM band. The data rate of the MU2400 can be operated up to 1.6Mbps in buffer mode. The MU2400 uses the standard CMOS process to offer a complete FSK RF transceiver solution with small size, low power consumption, minimum external parts and high reliability.

The MU2400 consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator, a demodulator, modulator, and Auto-ACK protocol engine. A reduced off chip filter is realized by the low-IF RX architecture. MU2400 is programmable for transmitter output power, frequency channels, and protocol setup easily through a SPI interface.

Except the RFIO, all the features of the MU2401 are the same as the MU2400. The MU2400 integrates the RF switch on chip, but the MU2401 removes this switch for the applications with external PA.

Features

- Single-chip FSK transceiver
- Auto-ACK & retransmit
- Star-Network with 6 channels
- Address and CRC computation
- 1/1.6Mbps data rate
- 1 ~ 64 bytes payload length
- 64 bytes FIFO size
- 4-wire digital interface (SPI)
- Power supply range: 1.8 to 3.6V
- Battery low supply voltage detector
- Support 4 power modes: Active/Standby/Idle/Power Down
- Operation range: -40 ^{o}C to +85 ^{o}C
- Standard CMOS process
- 24-pin 4x4 QFN package
- On-chip VCO, PLL and PLL loop filter
- On chip channel filter

Applications

- Wireless mouse, keyboard, joystick
- Keyless entry
- Alarm and security system
- Home automation
- Surveillance
- Automotive
- Telemetry
- Industrial sensors
- Wireless data communication
- Toys

Pin Assignment of MU2400

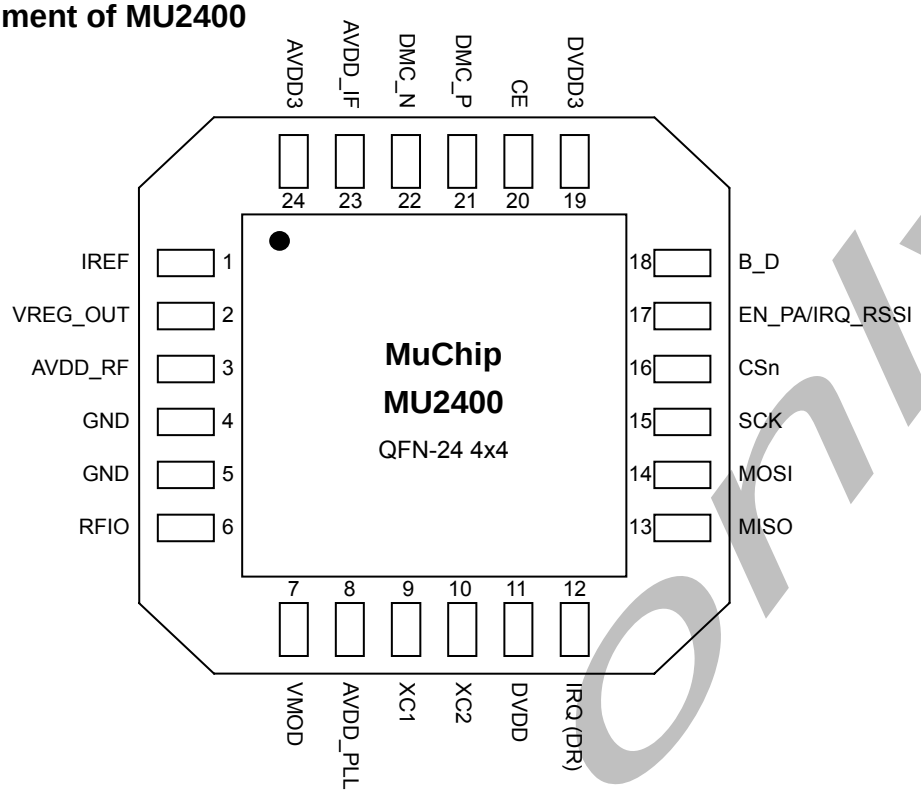


Figure 1: Pin Assignment of MU2400

Block Diagram of MU2400

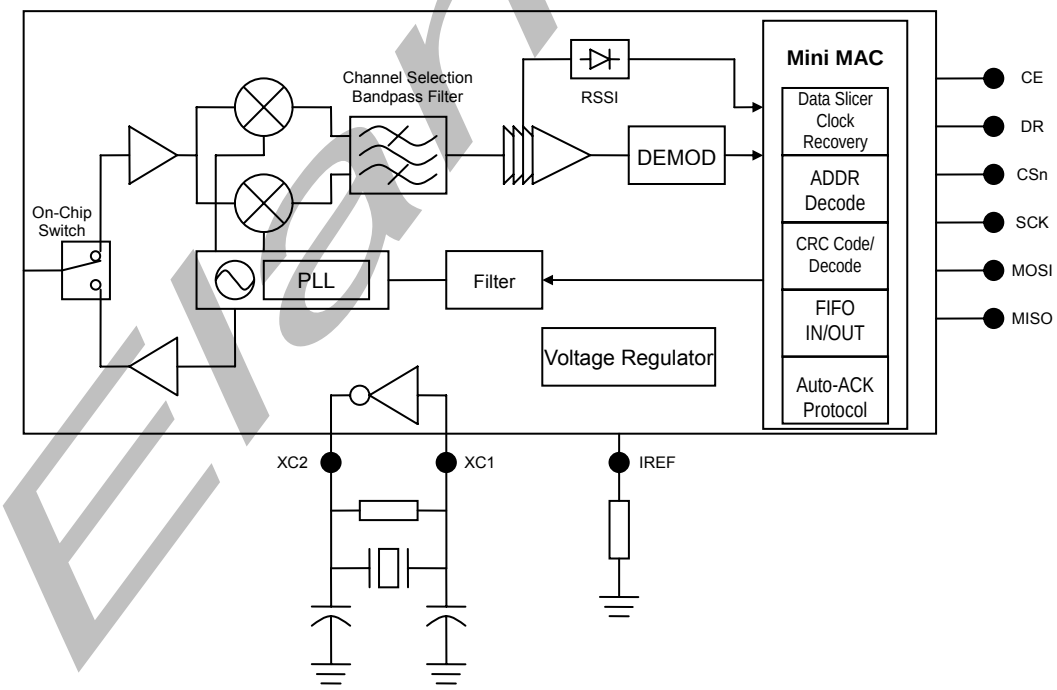


Figure 2: Block Diagram of MU2400

Pin Assignment of MU2401

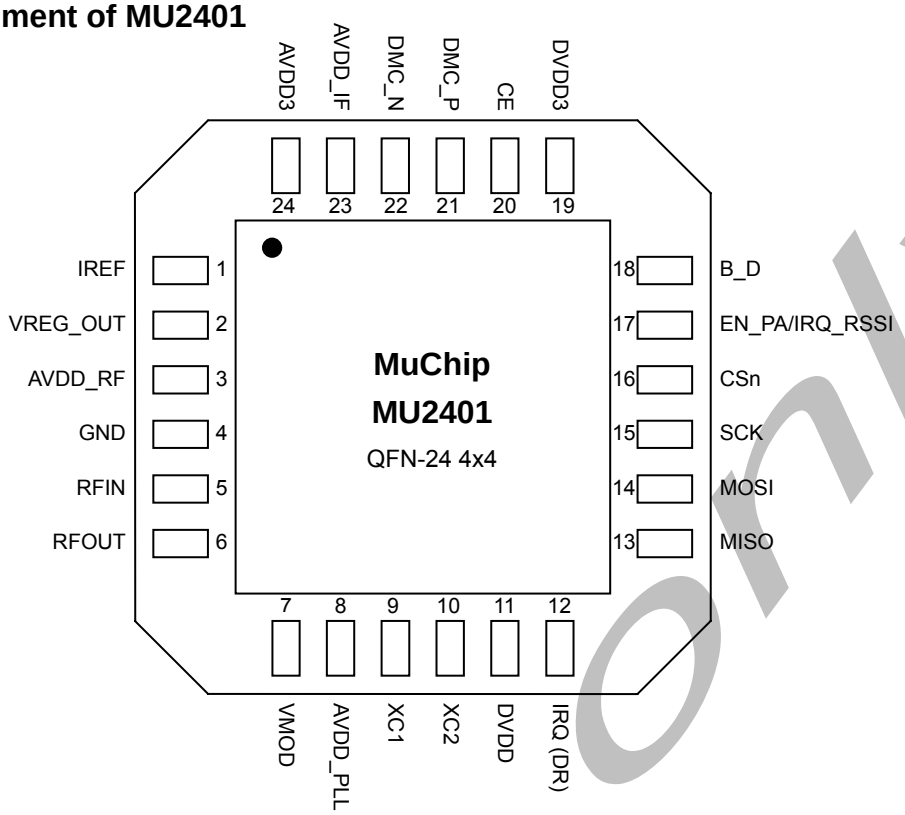


Figure 3: Pin Assignment of MU2401

Block Diagram of MU2401

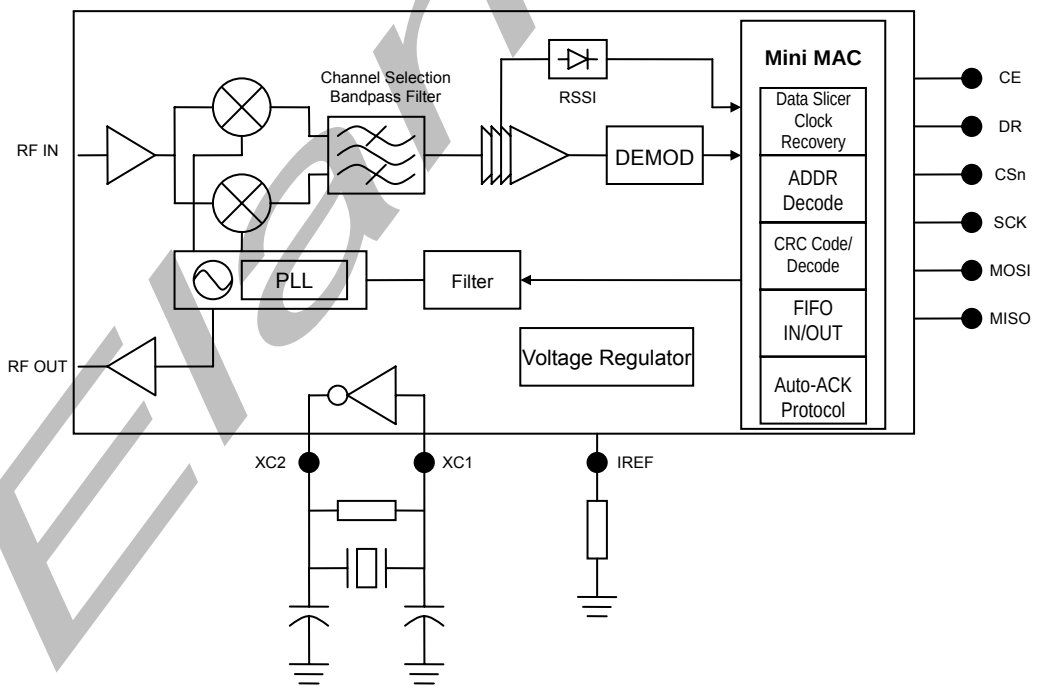


Figure 4: Block Diagram of MU2401

Pin Description:

Pin	Name	Type	Description
1	IREF	Analog Input	Reference resistor pin, connect to an external resistor
2	VREG_OUT	Power	On-chip voltage regulator output
3	AVDD_RF	Power	RF power supply
4	GND	Ground	Connect to PCB ground
5	GND/RFIN	Ground /Analog Input	Be configured as the two pin definitions: a. GND: GND in MU2400. b. RFIN: RF Input in MU2401
6	RFIO/RFOUT	Analog I/O /Analog Output	Be configured as the two pin definitions: a. RFIO: RF input/output in MU2400. b. RFOUT: RF Output in MU2401
7	VMOD	Analog I/O	Connect to external capacitor for filtering
8	AVDD_PLL	Power	PLL power supply
9	XC1	Analog I/O	Crystal pin1 for external crystal
10	XC2	Analog I/O	Be configured as the two pin definitions: a. Crystal pin2 for external crystal b. For external clock signal, it's the input pin of external clock
11	DVDD	Power	Digital power supply
12	IRQ(DR)	Digital I/O	Be configured as the two operation modes: a. IRQ: Interrupt signal in buffer mode b. DR: data input/data output in direct mode
13	MISO	Digital Output	Be configured as the two operation modes: a. master input/slave output in SPI mode b. data output in buffer mode
14	MOSI	Digital Input	Be configured as the two operation modes: a. master output/slave input in SPI mode b. data input in buffer mode
15	SCK	Digital Input	SPI input clock
16	CSn	Digital Input	SPI selection / programming enable
17	EN_PA/ IRQ_RSSI	Digital Output	Be configured as the two output modes: 1. EN_PA: To control the external PA chip 2. IRQ_RSSI outputs high – To indicate the MCU to read the RSSI digital registers,

			RSSI is only valid during receiving signal. – Let MCU know the channel is occupied.
18	B_D	Digital Output	Battery Low Power Detector
19	DVDD3	Power	Digital I/O power supply
20	CE	Digital Input	Chip enable, enable voltage regulator
21	DMC_P	Analog Output	Demodulator analog output, connecting to an external AC coupling capacitor
22	DMC_N	Analog Input	Demodulator analog input, connecting to an external AC coupling capacitor
23	AVDD_IF	Power	RX IF power supply, voltage regulator output
24	AVDD3	Power	Voltage regulator input power supply

Table 1: Pin Function Description of MU2400/MU2401

Electrical Specification

Absolute Maximum Rating

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_S		-0.3		3.6	V
Input RF level	P_{RF}				+10	dBm
Storage Temperature	$T_{Storage}$		-40		125	°C
ESD protection	V_{ESD}	HBM MM	2K*[1] 200			V

Table 2: MU2400/MU2401 Absolute Maximum Rating

*1: ESD of pin4/pin5 (RF IO) only can pass 1KV in HBM and 50V in MM

Electrical Characteristics (@ VDD=+3.0V, T_{amb}=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Overall						
Supply Voltage	V_{DD}	With internal LDO	2.1	3.0	3.6	V
Threshold Voltage to bypass internal LDO		Internal circuits will sense V_{DD} and bypass the internal LDO	1.8		2.1	V
Core Supply Voltage	V_{DD_CORE}		1.7	1.8	2.1	V
Operating ambient temperature	T_{amb}		-40	25	85	°C
Digital Input Pin						
HIGH level input voltage	V_{DINH}		0.7V		3.6	V
LOW level input voltage	V_{DINL}		VSS		0.3VDD	V
Digital Output Pin						
HIGH level output voltage (Iout=-1mA)	V_{DOUTH}		VDD-0.3		VDD	V
LOW level output voltage (Iout=1mA)	V_{DOUTL}		VSS		0.3	V
General RF Conditions						
RF frequency range	f_{RF}		2400		2483	MHz
TX supply current	I_{VDD_TX}	0dBm output power		20		mA
RX supply current	I_{VDD_RX}			23		mA
Standby I supply current	I_{VDD_STBI}	Xtal ON, Regulator ON		1.5		mA

Standby II supply current	I_{VDD_STBII}	Xtal ON, Regulator ON		3.7		mA
Idle Mode	I_{VDD_IDLE}	Keep registers content		30		uA
Supply current in power down	I_{VDD_PD}			<1		uA
Battery Low Power Detector	V_{TH}	Output logic high when V_{DD} is less than V_{TH}	1.7		2.2	V
Receive Section						
RX Sensitivity (BER<10^{-3}) Buffer Mode@1Mbps @1.6Mbps		 FD=400kHz FD=500kHz		 -90 -85		 dBm dBm
RX System Noise Figure		Include on chip switch		7		dB
Saturation (maximum input)		BER<10^{-3}		-20		dBm
Co-channel rejection	C/I_{CO}	BER<10^{-3} @1Mbps *2		11		dBc
1st Adjacent channel rejection	C/I_{N+1} C/I_{N-1}	wanted signal at 3dB higher than Sensitivity		-20 -15		dBc
2nd Adjacent channel rejection	C/I_{N+2} C/I_{N-2}	2MHz channel spacing		-37 -7*3		dBc
3rd Adjacent channel rejection	C/I_{N+3} C/I_{N-3}			-40 -30		dBc
Image channel rejection	C/I_{img}			-7		dBc
Blocking / Desensitization 0.03 - 2.0 GHz 2.0 - 2.399 GHz 2.498 - 3.0 GHz 3 - 12.75 GHz		Image signal reference to image spec.		 46 46 50 70		 dBc dBc dBc dBc
Spurious Emission 30M - 1 GHz 1 - 12.75 GHz				 -57 -47		 dBm dBm
RSSI Section						
RSSI Range		The range is -100dBm ~ -50dBm (6-bits)		50		dB
RSSI Accuracy				±4		dB
RSSI Settling Time	T_{RSSI_ON}			1		µs
Transmit Section						
Transmit data rate @Buffer Mode @Direct Mode	R_{data}			 1 1	 1.6 2	 Mbps Mbps

Frequency Deviation Range (FD)	Δf	One-Sided Deviation	160		500	±kHz
RF Output Power Mode	P_{TX}			0		dBm
				-6		
Harmonics 2nd order harmonic 3rd order harmonic		BW=100kHz		 -40 -50		 dBc dBc
Spurious Emission 30 - 1000MHz 1 - 12.75 GHz 1.8 - 1.9 GHz 5.15 - 5.3 GHz		BW=100kHz			 -36 -30 -47 -47	 dBm dBm dBm dBm
Optimum load impedance				TBD		
Freq. Synthesizer Section						
Crystal oscillator frequency	f_{XTAL}		12/16/24			MHz
Crystal oscillator frequency accuracy requirement				±60*4		ppm
Crystal oscillator start-up time				0.6	0.8	ms
VCO phase noise		±1MHz offset		-100		dBc/Hz
Channel switch time					180	μs
Standby mode to transmit data	$T_{PD/TX}$				130	μs
Standby mode to receive data	$T_{PD/RX}$				130	μs
T/R Switch Time					60	us
Idle mode to Tx standby II/Rx buffer mode	$T_{settling}$	When using external Xtal with internal oscillator		600	800	us
	$T_{settling}$	When using external clock from MCU		120	200	us

Table 3: MU2400/MU2401 RF Electrical Characteristics

*2: The interfering signal is a modulated signal with PRBS9, data rate and frequency deviation equal to MU2400.
*3: The interfering signal I_{N-3} will fold to 2MHz under 2MHz IF of the receiver, so it is not as good as the interfering rejection at I_{N+3}
*4: Need to run Xtal frequency offset calibration if Crystal accuracy > ±40ppm

Mode of Operation

Operation Mode	0x40	0x41	0x00			0x01	CE	CSn	MOSI	MISO	IRQ
	[1:0]	[7:0]	[7]	[6]	[0]	[3:1]	(pin)	(pin)	(pin)	(pin)	(pin)
Power Down	x	x	x	x	1	x	0	x	SPI_{in}	SPI_{out}	
Idle	x	x	0[*5]	0	0	101	0	x	SPI_{in}	SPI_{out}	
Configuration	x	x	1	1	1	010	1	0	SPI_{in}	SPI_{out}	
Standby I	00	x	0	1	1	110	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Buffered	10	0x80	1	1	1	010	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
Standby II	10	0x80	1	1	1	010	1	1	$FIFO_{in}$	SPI_{out}	IRQ_{out}
TX Direct	10	0x80	1	0	1	010	1	1	SPI_{in}	SPI_{out}	$Data_{in}$
RX Buffered	01	0x81	1	1	1	010	1	1	SPI_{in}	$FIFO_{out}$	IRQ_{out}
RX Direct	01	0x81	1	0	1	010	1	1	SPI_{in}	SPI_{out}	$Data_{out}$

Table 4: MU2400/MU2401 Mode of Operation

*5: When using external xtal with internal oscillator, (i.e. R00[2]=1), MCU write 0. When using external clock from MCU, (i.e. R00[2]=0), register R00[7] don't care..

For detail register setting, refer to the state machine of operation modes on Figure 5. Please follow the register sequence order showed from up to down when you write the register setting. The symbol "x" means that don't write the registers when you change the operation mode.

Configuration

When CSn=0 and CE = 1, the SPI interface may be activated to program the SPI register value. For the detail timing diagram, you can refer to the Figure 17 ~ Figure 19.

Power Down Mode

When the pin CE sets to 0 and 0x00[0] sets to 1, the MU2400 is disabled with the minimal current consumption. When entering the power down mode, MU2400 is not active including voltage regulators and crystal block, and the values of all registers are clear.

Idle

Idle mode is used to minimize average current consumption while maintaining short start up times. In this mode, the contents of all registers are maintained by internal power supply voltage. It will reduce the register initialization time on the next start up time from idle mode into buffer mode. MU2400 is not active including

voltage regulators and crystal block.

Standby I

For RX or TX device, all the RF blocks and mini Mac baseband system clock will be turned off to save average current consumption. In this mode, only voltage regulators, crystal oscillator and clock buffers are active to speed up the start-up time. The configuration word content is maintained during standby I mode.

TX Buffered Mode (BUF)

As a transmitter with the function of FIFO and packet handling

Standby II

When TX FIFO is empty in TX buffer mode, the TX device would stay in the standby II mode. In this mode, the regulators, crystal oscillator, clock buffers and mini Mac baseband system clock are activated. No any start-up time is need.

TX Direct Mode (DR)

As a transmitter without the function of the FIFO and packet handling

RX Buffered Mode (BUF)

As a receiver with the function of FIFO and packet handling

RX Direct Mode (DR)

As a receiver without the function of the FIFO and packet handling

State Machine of Operation Modes

The Figure is the state machine of operation modes. The MCU can follow the register sequence to write SPI registers into the desired operation mode through digital SPI interface.

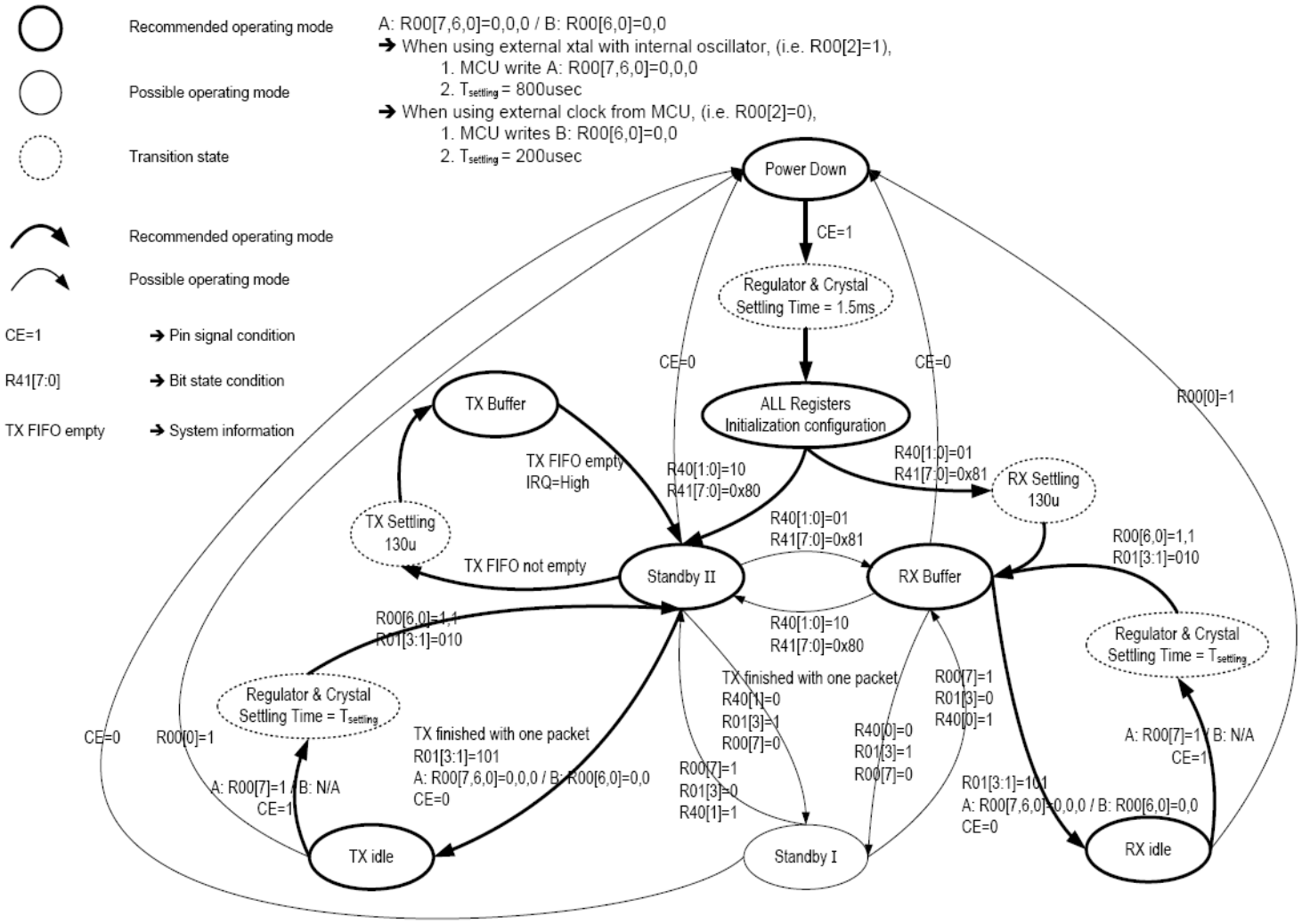


Figure 5: State Machine of Operation Modes

Packet Handling Methods

The packet handler makes it possible to use the high data rate offered by MU2400 without the need of a costly, high-speed microcontroller (MCU) for data processing and clock recovery. By placing all high speed signal processing related to RF protocol on-chip. MU2400 can offer the application microcontroller a simple SPI compatible interface, and the SPI input clock, SCK, will be determined by the interface-speed microcontroller itself setup by allowing the digital part of the application to run at the lower speed while operating at the maximal data rate, i.e. 1.6Mbps .

In RX Buffered Mode, IRQ notifies the MCU when a valid address and payload is received respectively. The MCU can then clock out the received payload from an MU2400 RX FIFO.

In TX Buffered Mode, MU2400 digital part automatically generates preamble value and CRC value. All together, this means reduced memory demand in the MCU resulting in a low cost MCU, as well as reduced software development time. MU2400 has 64 bytes RX FIFO and 64 bytes TX FIFO. The MCU can access the FIFO at any time.

Auto-Acknowledgement (RX)

If auto acknowledgement is enabled and a valid packet with correct data pipe address and CRC is received, the RX device will enter the TX mode and send an acknowledgement packet to TX device. After the RX device has sent the acknowledgement packet to TX device, normal operation in RX device will be resumed.

Auto Re-Transmission (TX)

An auto retransmission is available when auto acknowledgement is enabled. It is used at the TX device. It will be to state how many times the data in the data register will resend if data is not acknowledged. After each sending, the TX device will enter the RX mode and wait a specified time period for acknowledgement. When the ACK packet is received, the TX device will return to the normal transmit function. If there is no more unsent data in the TX FIFO, the TX device will go into the Standby mode.

If the acknowledgement is not received in the TX device, the TX device will transfer to TX mode and resend the data after a specified time period. This will continue until acknowledgement is received in the TX device or a time out occurs because of the maximum number of resending is reached.

Star Network

An MU2400 configured as primary RX will be able to receive data through 6 different data pipes. A data pipe will have a unique address but share the same frequency channel. This means that up to 6 different MU2400 configured as primary TX can communicate with one MU2400 configured as RX, and the MU2400 configured as RX will be able to distinguish between them. Only one data pipe can receive a packet at a time.

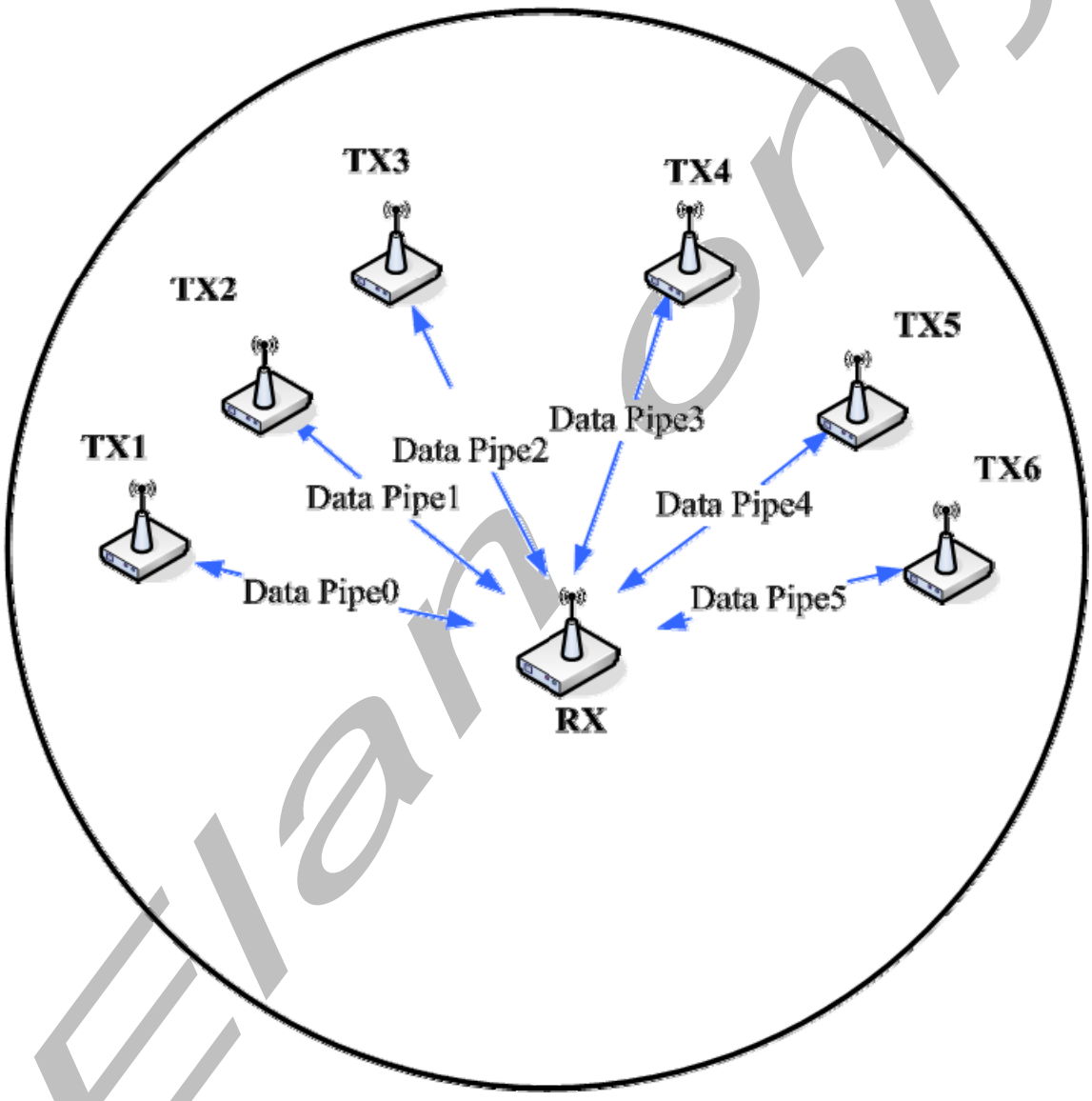


Figure 6: Star Network Configuration

The following settings are common to all data pipes:

- Auto ACK enable
- STARTNET enable
- CRC encoding scheme
- TX / RX Address width
- Frequency channel
- Air data pipe
- RF data rate

The data pipes are enabled with the bits in the 0x41[5:0] register.

Each data pipe address is configured in the RXADR0 ~ RXADR5. Each data pipe can have up to 2 byte configurable address. Data pipe 0 has a unique 2 byte address. Data pipe 1~5 shares the 8 most significant address bits. Figure 5. is an example of how data pipes 0~5 are addressed.

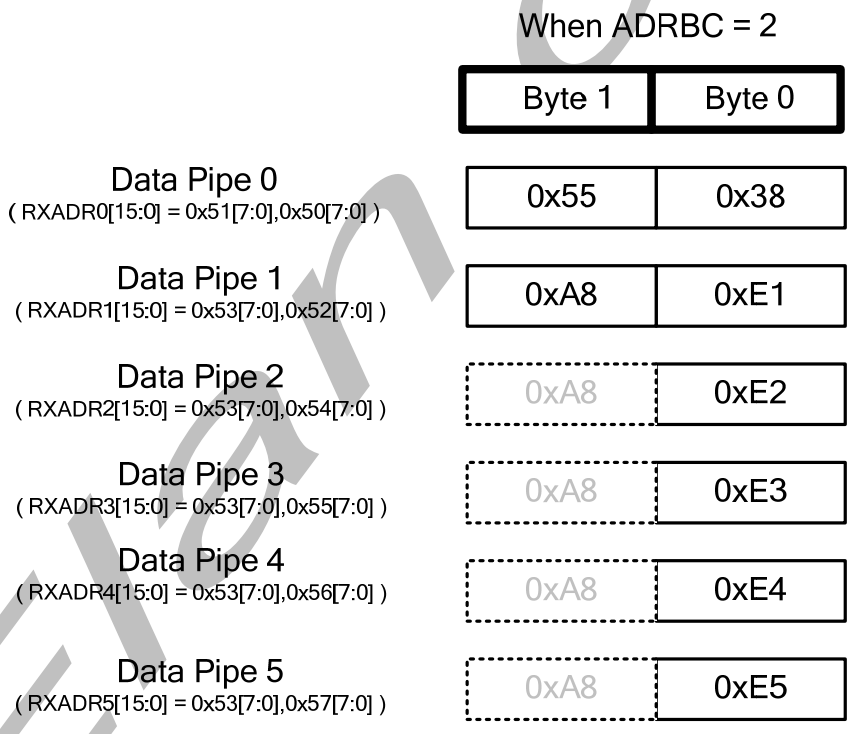


Figure 7: Addressing Data Pipes 0~5

The RX receives packet from more than one TX. To ensure that the ACK packet from the RX is transmitted to the correct TX, the RX takes the data pipe address where it received the packet and use it as the TX address when transmitting the ACK packet. On the TX device, the TXADR must be the same as the RXADR0. On the RX device, the RXADR0~RXADR5, defined as the data pipe address, must be unique. Figure 6. is an example of data pipe addressing for the TX and RX.

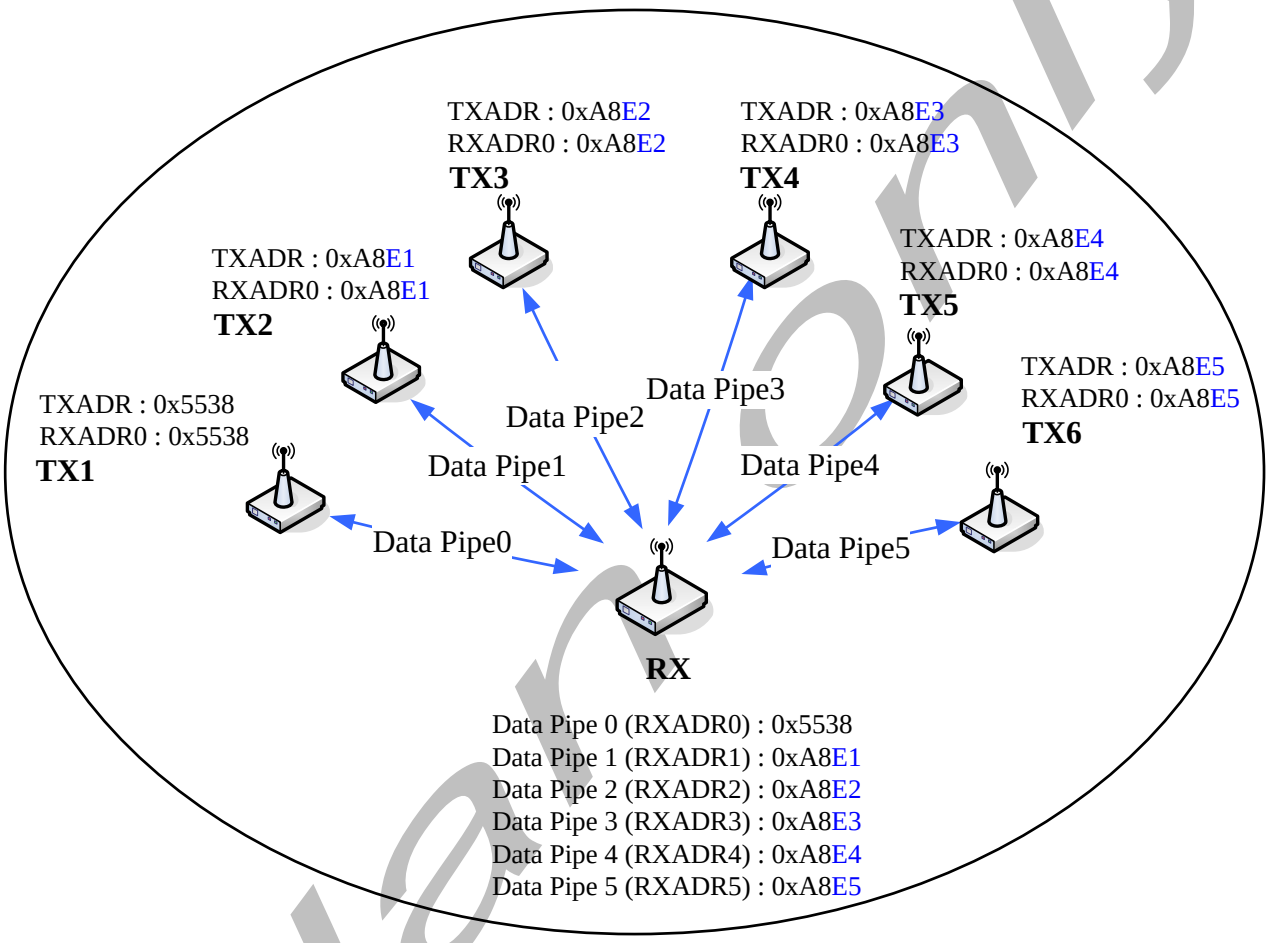


Figure 8: Example of data pipe addressing

Packet Description

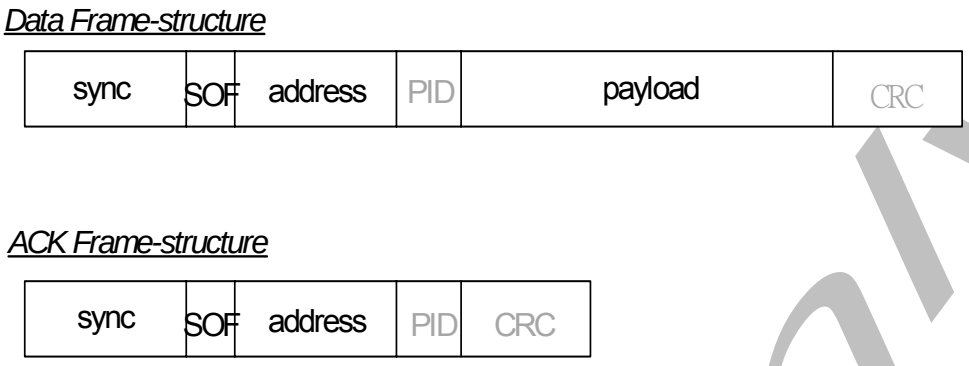


Figure 9: Package Description

- **Sync: 4**-12 bytes (Default 4 bytes)
- **SOF:** Start of Frame (1byte)
- **Address:** Programmable byte length (1-2 Byte)
- **PID:** 1 byte

  When STARNET 0x40[7] is enabled, PID is adding to frame structure.

  When STARNET 0x40[7] is disabled, PID is removing from frame structure.

  Example:

  If STARNET 0x40[7] is enabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),

  → PID= 1 byte, the available payload = 3 bytes

  If STARNET 0x40[7] is disabled and set payload length 4 bytes (PKTLEN 0x44[6:0] = 4),

  → PID= 0 byte, the available payload = 4 bytes

  - [7]: Packet type, auto generate by HW
    - 1'b0 : Data packet (needs ACK or not)
    - 1'b1: ACK packet
  - [6:4]: 000~101 Pipe data number, auto generate by HW
  - [3:0]: Packet sequence number, It is used by the RX device to determine if a packet is new or retransmitted. It defined by user.
- **Payload:** Programmable byte length (1-64 Byte)
- **CRC:** Programmable length(0,1,2,4 Byte)

Description of TX/RX Link Operation Timing Diagram

The following descriptions in this section are showed the TX/RX link operation timing diagram.

- **TX/RX Link Operation Timing Diagram without Auto ACK in Buffer Mode**

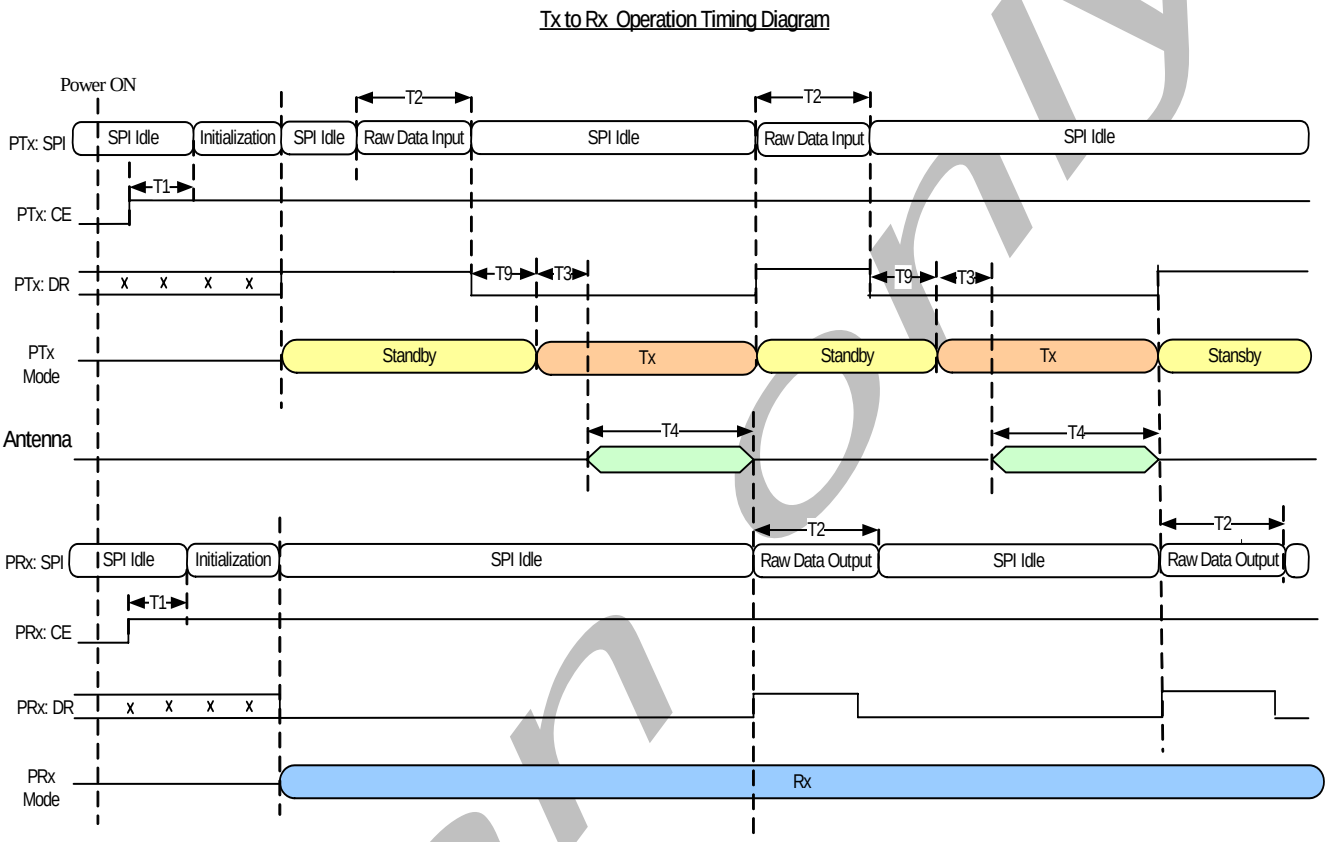


Figure 10: TX/RX Link Operation Timing Diagram without Auto ACK in Buffer Mode

Condition: Disable Auto ACK 0x40[3:2] = 00
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

The PTX DR is asserted after the packet is transmitted by the PTX.
The PRX DR is asserted after the packet is received by the PRX.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

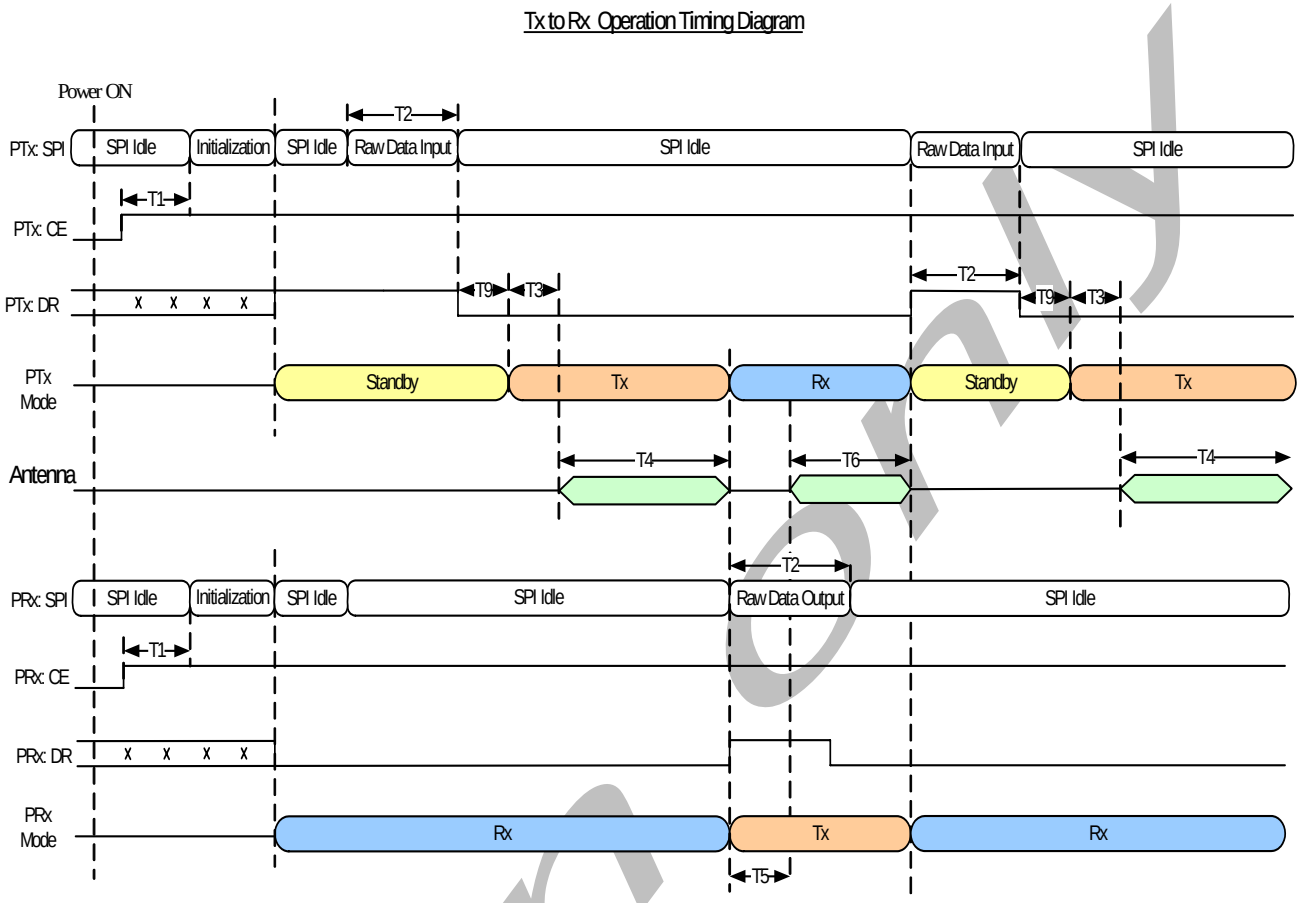


Figure 11: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001

When the transmission ends the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to MCU. When the PRX device receives the packet it responds with an interrupt to MCU.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

  ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX receives ACK

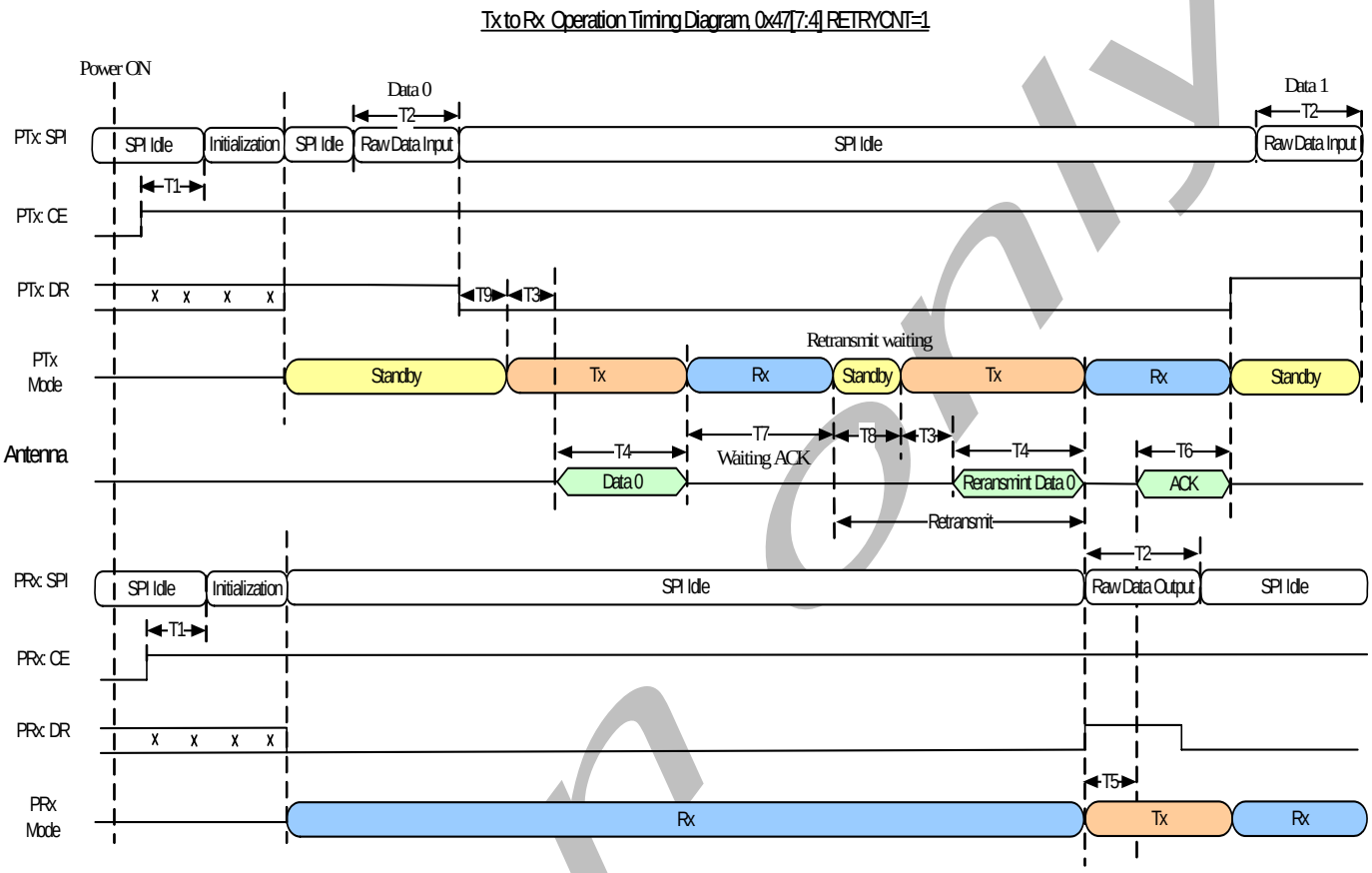


Figure 12: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

After Data 0 is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits specified time for ACK packet (T7). If it is not in specified time slot, the PTX retransmit the Data 0. When the retransmitted packet is received by the PRX, the DR of PRX is asserted and ACK is transmitted back to the PTX. When the ACK is received by the PTX, the DR of PTX is asserted.

- **TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode**

  ACK Lost Condition: PTX transmits Data ➔ PTX doesn't receive ACK ➔ Retransmit Data (Retransmit time=1) ➔ PTX doesn't receive ACK again ➔ Packet Loss Count + 1

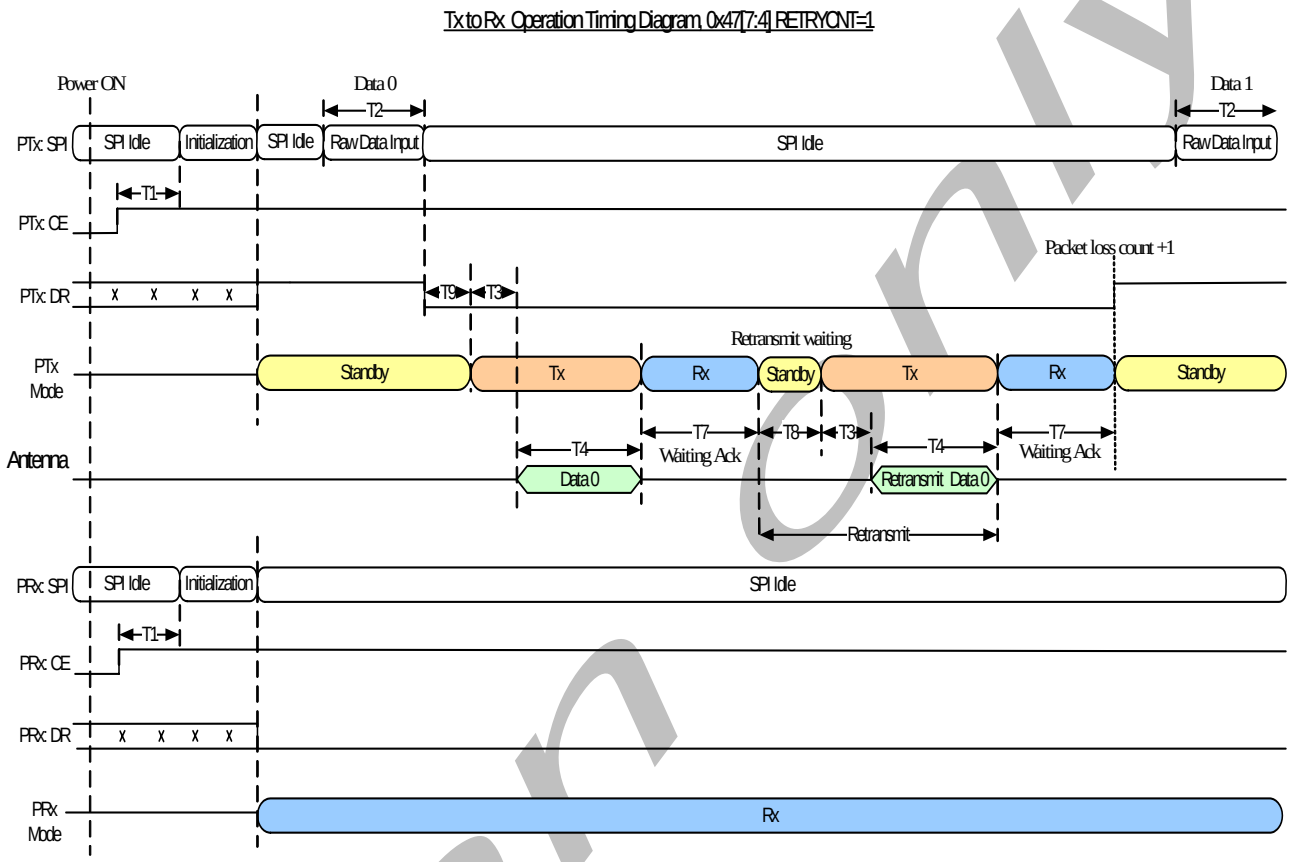


Figure 13: TX/RX Link Operation Timing Diagram with Auto ACK in Buffer Mode

Condition: Enable Auto ACK 0x40[3:2] = 11
PKTCNT 0x45[7:4] = 0001
Enable RXEN0 0x41[5:0] = 000001
RETRYCNT 0x47[7:4] = 0001

When the PTX retransmit counter exceeds the RETRYCNT 0x47[7:4], the PTX DR is asserted and automatically adds one to packet loss count (0x4F[7:3]). Then the payload in PTX FIFO will be removed.

- **TX/RX Link Operation Timing Diagram in Direct Mode**

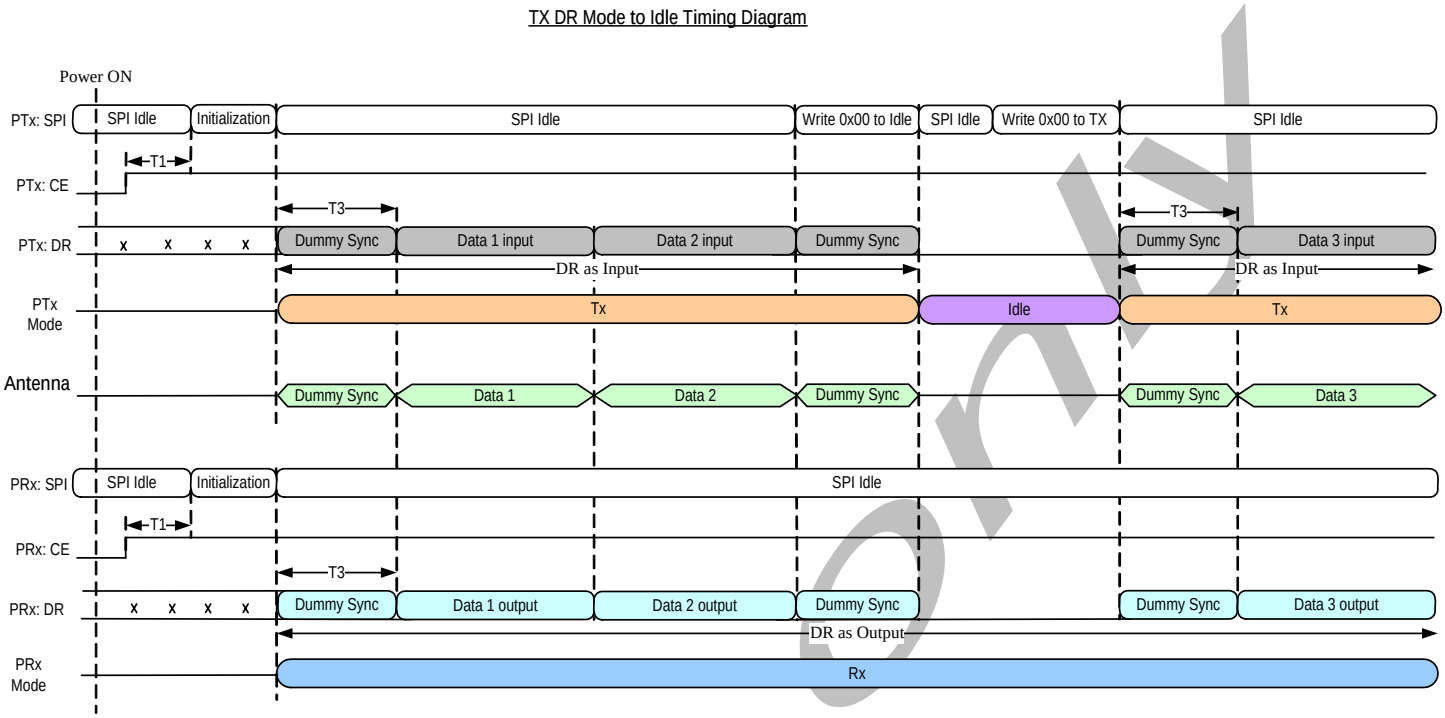


Figure 14: TX/RX Link Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, you must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. Figure 14 shows the timing diagram of operation mode change from direct mode into idle mode, then into direct mode again.

- **TX/RX Switching Operation Timing Diagram in Direct Mode**

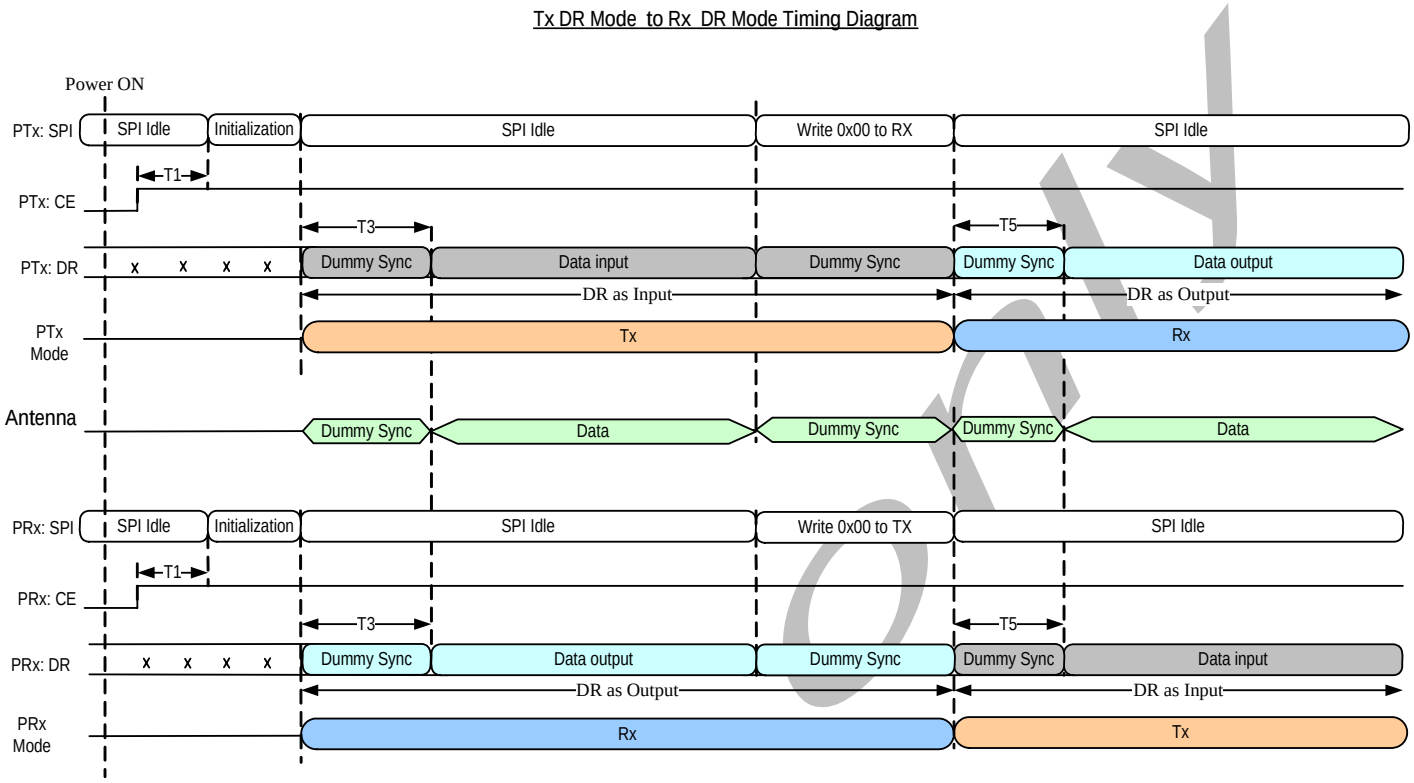


Figure 15: TX/RX Switching Operation Timing Diagram in Direct Mode

Condition: Set 0x00[6] = 0, 0x00[1] = 1
Set 0x00[4:3] = 10 for RX device
Set 0x00[4:3] = 01 for TX device

When RF blocks are active in TX device, you must be to write dummy sync from pin of DR. It can reduce the RX receiving settling time. Figure 15 shows the timing diagram for RX/TX switching operation. When the devices change from TX(RX) into RX(TX) directly, the devices don't go into standby mode. Besides, the PLL block only takes the time T5 not T3 for PLL settling time.

Time Formula Description:

Payload Length: **n**
Data rate: **rate**
Sync 0x43 [4:0]: **s**
Address 0x42[7:6]: **a**
SCK Frequency: **SCK**
CRC Check 0x43 [6:5]: **r**
SOF: 1 byte
PID: When STARNET 0x40[7] =1, PID = 1 byte, else PID=0
Slot time 0x47 [3:0]: **SLT**
ACKTOSLOT 0x49 [7:0]: **ATS**
BACKOFFWIN 0x58 [7:0]: **BFW**

Formula Description
T1 must be over 0.8ms for Xtal and regulator settling when using external Xtal with internal oscillator. Only 200us is needed for regulator settling when system reference clock is shared with MCU
Burst Mode : T2 = (n+1) *8 /SCK Non-Burst Mode : T2 = (2*n) *8 /SCK
T3 = 120us
T4 = (s+SOF+a+n+r)*8/rate
T5 =60us
T6=(s+SOF+PID+a+r)*8/rate
T7= ATS*SLT*10us
T8= BFW*SLT*10us
T9= 10us

Table 5: Delay Times Information

T1: Initiation setting time
T2: TX: Write data to FIFO; RX: Read data from FIFO
T3: RF delay time for transmit data. (Waiting for PLL settling)
T4: Packet Input Data Transmission Time
T5: RF delay for transmit ACK data. (Waiting for PLL settling)
T6: ACK packet Data Transmission Time
T7: ACK waiting time, must be larger then T5+T6, programmable from 10us to 32ms.
T8: Retransmit waiting time, programmable from 0 to 32ms
T9: Packet Handling Time

FIFO and PKTCNT

A 64bytes FIFO size is available on MU2400. The PKTCNT (0x45[7:4]) define the number of payloads can be stored in FIFO.

In TX Mode, the pin DR will keep high until the number of payload in FIFO reach the PDKCNT. For example: Set payload length 4 bytes (PKTLEN[6:0]=4) and PKTCNT = 4. When the data in FIFO reach to 16 bytes, the DR will pull low to indicate the MCU that no more data is allowed to input.

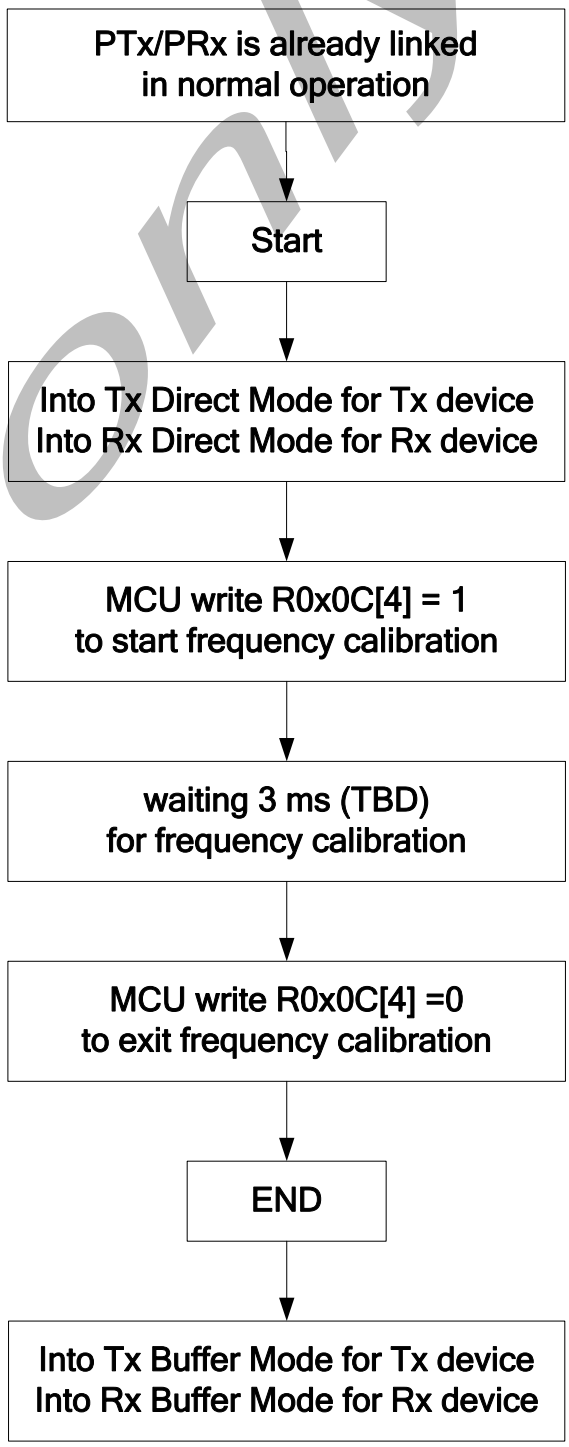
In RX Mode, PKTCNT also define the maximum number of payload in FIFO, when the RX FIFO is full, number of payload equal to PKTCNT but it can be less than 64 bytes, the receiver will be turned off to save power. The receiver will turn on immediately after MCU read out the FIFO data.

Xtal Frequency Offset Calibration

When the external Xtal with internal oscillator is used to create the system clock, the MU2400 provides the auto frequency tuning engine to fine tune the Xtal frequency.

Calibration Flow

1. Start
2. Set registers into Direct Mode
3. For RX device, write R0x0C[4]=1 to start frequency calibration. For TX device, it outputs a single carrier as reference frequency for RX device
4. Waiting 3 msec for the timing of frequency calibration (TBD)
5. For RX device, write R0x0c[4]=0 to finish the calibration flow
6. End
7. Recover to the normal operation mode



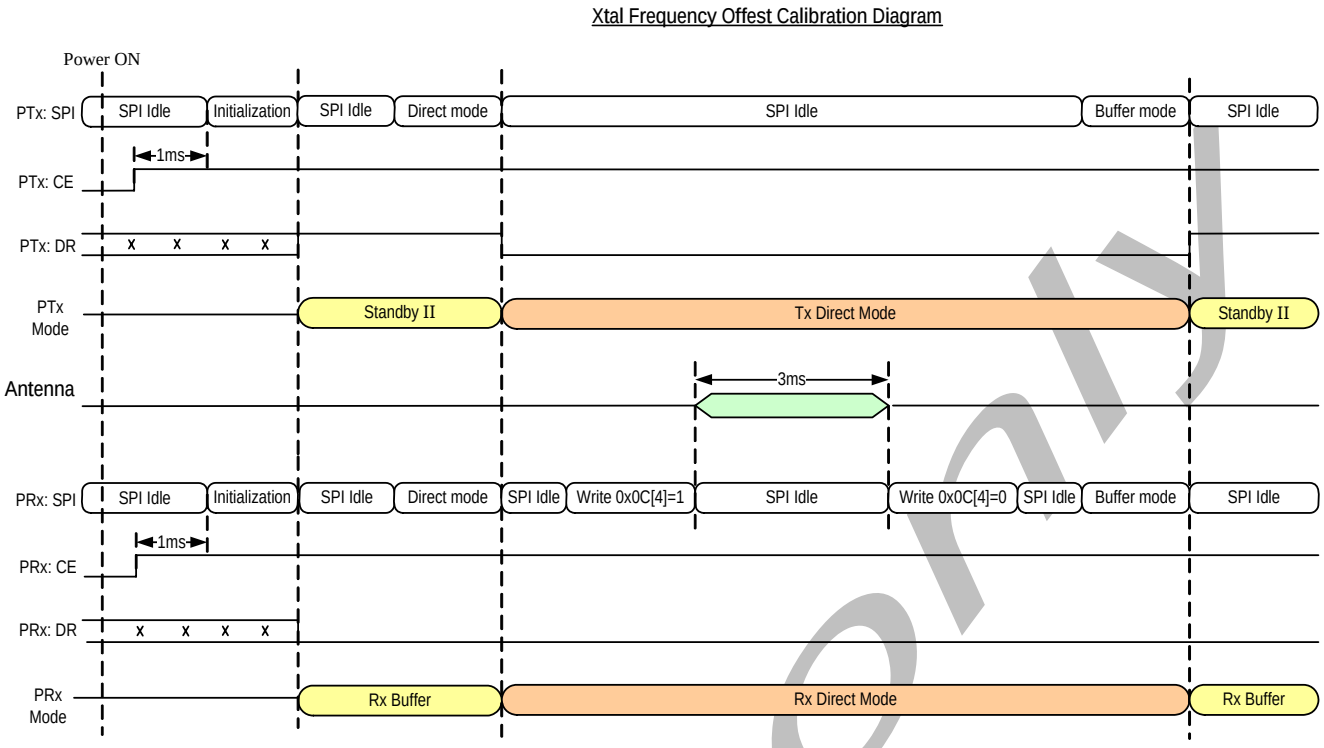


Figure 16: Xtal Frequency Offset Calibration Timing Diagram

Note: When the devices go into POWER DOWN mode, all the calibration result will be refreshed

MU2400/MU2401 sharing crystal with a MCU

When using a MCU to drive the crystal reference pin XC2 of the MU2400 transceiver, some rules must be followed. First, the register R0x00[2] is set to Low. When MCU drives the MU2400 clock input pin, XC2, the requirement of load capacitance C_L is set by the MCU only. The frequency accuracy of +/-60ppm is still required to get a functional radio link. The input signal should not have amplitudes exceeding any rail voltage, but any DC voltage within this is OK. To achieve low current consumption and also good SNR ratio when using an external clock from MCU, it is recommended to use an input signal larger than 0.4 V_{-peak}. When clocked externally, XC2 is the input pin, and XC1 is not used. XC1 can be left as an open pin.

4-Wire SPI interface - Digital Interface to control chip parameter

All configuration of MU2400 is defined by values in some configuration registers. All these register are writable via the SPI interface.

SPI Timing

Chip Select: CSn
Input Clock: SCK
Input Data: MOSI
Output Signal: MISO

- **SPI interface Read / Write Register Value for Register Setting**

  When A7 = 1, MCU read value from MU2400 register.

  When A7 = 0, MCU write value to MU2400 register.

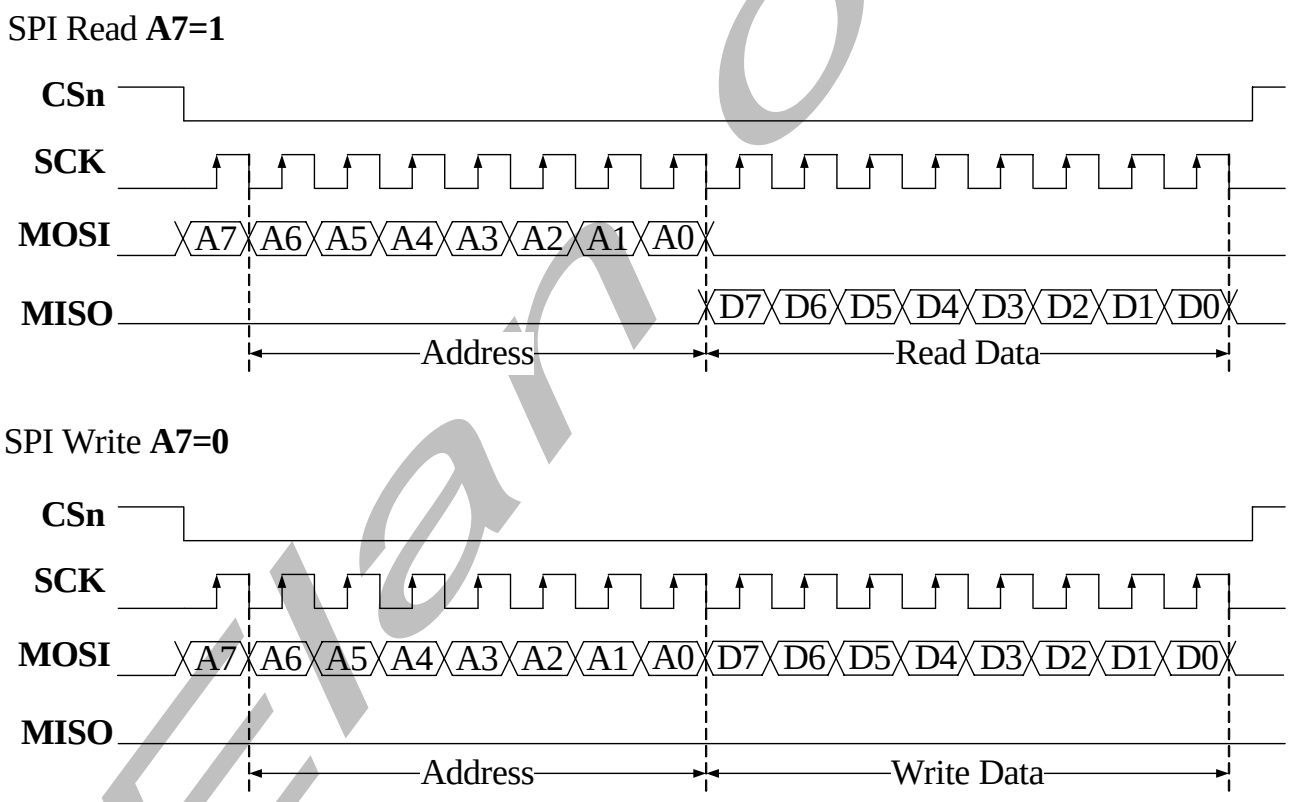


Figure 17: SPI Read/Write Register Timing Diagram

- **SPI interface Read / Write FIFO Data for Buffer mode**
  - ✓ When 0x40[6] = 1, SPI interface switch to Burst mode.
  - ✓ Address = 0x7F for FIFO address

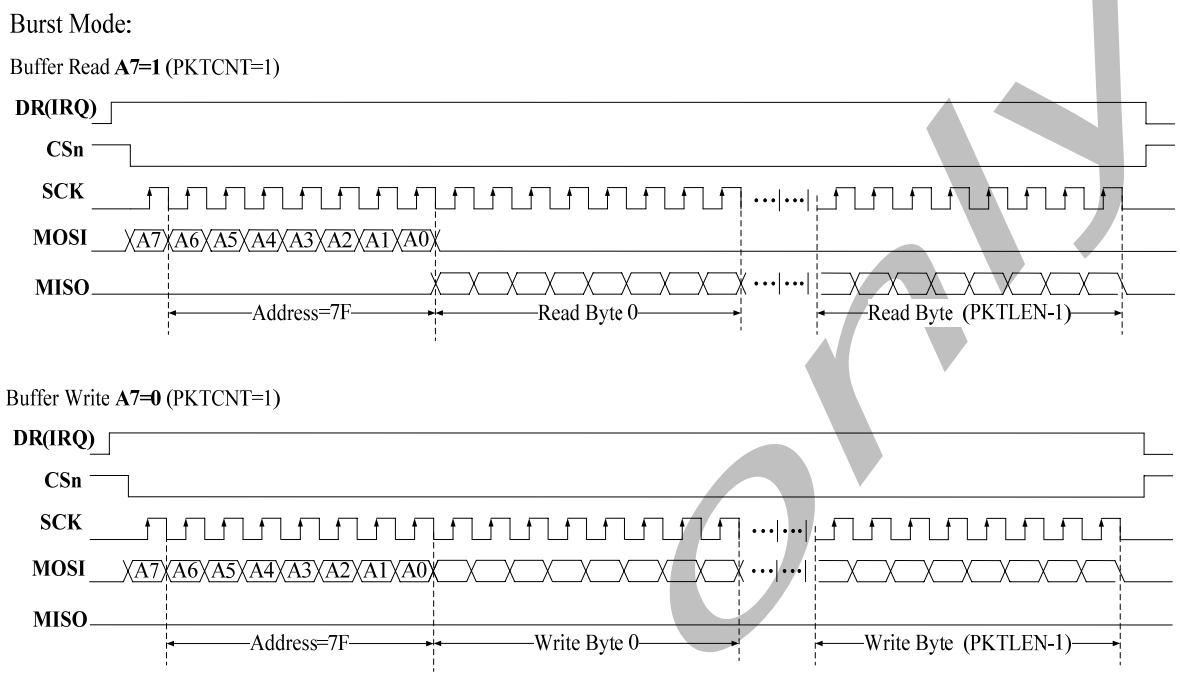


Figure 18: SPI interface switch to Burst mode when 0x40[6]=1

- ✓ When 0x40[6] = 0, SPI interface switch to Non-Burst mode.
- ✓ Address = 0x7F for FIFO address

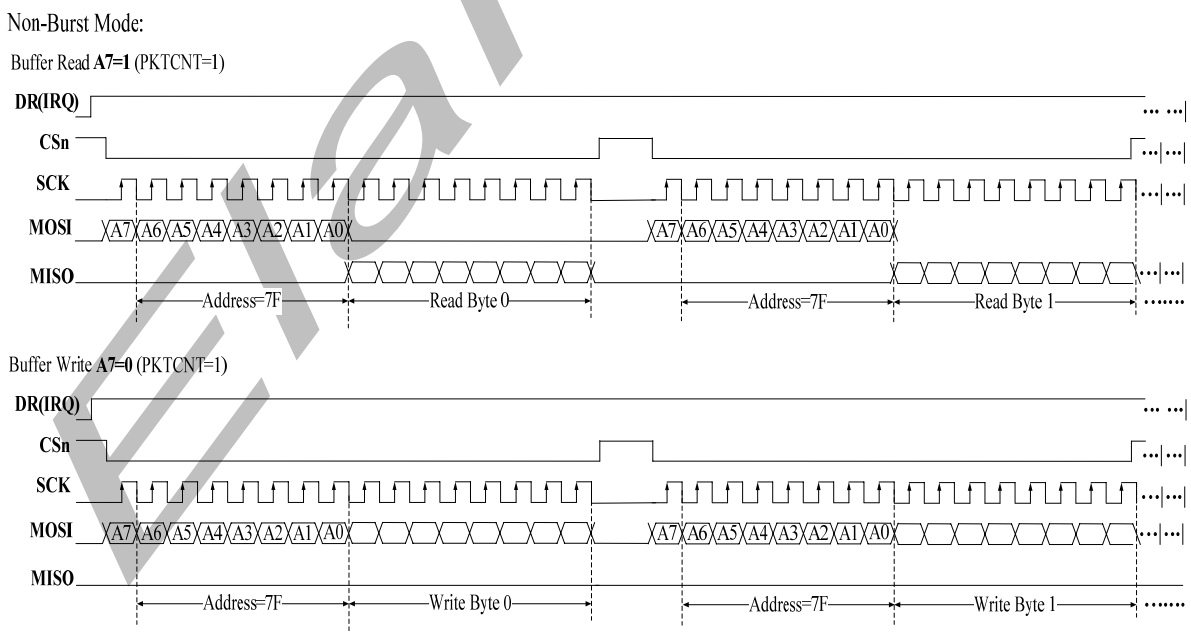


Figure 19: SPI interface switch to Non-Burst mode when 0x40[6]=0

Configuration Registers for RF Transceiver

User only can change the configuration registers which highlight with gray background.

	D7	D6	D5	D4	D3	D2	D1	D0
0x00	1	H_Buf_L_DR	nEN_24M	DR_EN_RX	DR_EN_TX	EN_XO	DR_EN_PLL	nENFun_idle
0x01	1	0	0	0	0	1	0	Sel_16_12
0x02	0	CH_NO						
0x03	1	1	CntR[5:0]					
0x04	0	0	0	0	0	0	0	0
0x05	0	1	0	0	0	0	0	0
0x06	PA3_WC[2:0]			PA2_WC[1:0]		PA1_WC[1:0]		D2S_Gain
0x07	0	0	1	1	1	0	0	0
0x08	0	1	0	0	0	0	0	0
0x09	0	0	0	1	1	0	0	0
0x0a	0	1	EN_3M_IF	0	SEL_MOD_RES[3:0]			
0x0b	0	0	0	0	1	0	1	1
0x0c	1	1	1	EN_KXO	KXO_spi[3:0]			
0x0d	0	1	0	0	1	1	1	1
0x0e	1	0	0	1	0	0	0	1
0x0f	0	0	0	1	1	0	0	0
0x20	1	0	1	0	1	1	0	1
0x21	0	1	1	0	0	1	0	0
0x22	0	0	0	0	0	0	0	0
0x23	1	1	0	0	0	0	1	1
0x24	1	0	1	1	1	1	0	1
0x25	1	0	1	0	0	0	1	0
0x26	bat_det_win	0	0	1	EN_700K	0	1	0
0x27	0	0	0	0	1	0	0	1
0x28	0	0	0	0	0	0	0	0
0x29	1	0	nEN12_EN24	1	1	0	bat_det_level[1:0]	
0x2a	0	0	1	1	0	0	1	1
0x2b	0	0	0	0	0	1	0	1
0x2c	1	0	0	1	0	0	1	0
0x2d	0	0	0	1	1	0	1	0
0x2e	0	0	0	0	0	0	1	1

0x2f	0	1	1	0	0	1	0	0
0x30	1	1	0	0	0	0	0	0
0x31	0	0	0	0	0	0	0	0
0x32	0	1	0	0	1	0	1	0
0x33	0	0	0	1	1	0	1	1

Table 6: Configuration Registers for RF Transceiver

Address from 0x00 to 0x0E

Address	Register Name	Bit	Default	Type	Description
0x00	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_CLK	7	1		1: Enable Digital Circuits System Clock 0: Disable Digital Circuits System Clock
	H_Buf_L_DR	6	1		1: Buffer mode operation 0: Direct mode operation
	nEN_24M	5	1		1: when the other reference clock is used 0: when 24MHz reference clock is used
	DR_EN_RX	4	0		1: Enable RX in DR mode 0: Disable RX in DR mode
	DR_EN_TX	3	0		1: Enable TX in DR mode 0: Disable TX in DR mode
	EN_XO	2	1		1: Enable Crystal Buffer 0: Disable Crystal Buffer
	DR_EN_PLL	1	0		1: Enable PLL in DR mode 0: Disable PLL in DR mode
	nENFun_idle	0	1		1: Disable idle mode 0: Enable idle mode
0x01	**Register Name**	**Bit**	**default**	**W**	**Description**
	PA_AAC	7	1		Toggle PA Auto Amplitude Control function
	TX_PWR[2:0]	6:4	000		TX output power selection in Test mode
	EN_SavePower	3	0		Enable clock gating in test mode for test only
	nEN_Ictrl_XO[1]	2	1		Crystal buffer bias current, {R0x0b[7],R0x01[2:1]} default 010.
	EN_Ictrl_XO[0]	1	0		
	Sel_16_12	0	0		Reference clock settling 1: 16MHz 0: 12MHz
0x02	**Register Name**	**Bit**	**default**	**W**	**Description**
	CH_AutoMan	7	0		Switch manual / look up table program RF channel. Look up table: set by CH_NO 0: Auto lookup table approach 1: Manual control via registers R0x04 & R0x05 (for test only)
	CH_NO	6:0	0000000		Channel frequency setting (RF Frequency) Data Rate = 1Mbps CH_NO / TX (Fc) / RX (Fc-2MHz) 'h00 / 2400MHz / 2398MHz 'h01 / 2401MHz / 2399MHz 'h53 / 2483MHz / 2481MHz (RF Frequency) Data Rate = 1.6Mbps CH_NO / TX (Fc) / RX (Fc-3MHz) 'h00 / 2401MHz / 2398MHz 'h01 / 2402MHz / 2399MHz 'h53 / 2484MHz / 2481MHz
0x03	**Register Name**	**Bit**	**default**	**W**	**Description**
	Reserved	7	1		
	EN_75M	6	1		Enable 75M reference clock function

	CntR[5:0]	5:0	000110		Ref. Clock / CntR[5:0] 12MHz / 000110 16MHz / 001000 24MHz / 001100
0x04	**Register Name**	**Bit**	**default**	**W**	**Description**
	CntB[7:0]	7:0	00000000		B counter of PLL for test mode
0x05	**Register Name**	**Bit**	**default**	**W**	**Description**
	EnFun_ManTrigAFC	7	0		Manual trigger AFC for test only
	EN_AFC_Code	6	1		Enable AFC
	Manual_EN_AFC	5	0		Manual enable AFC for test only
	CntA[4:0]	4:0	00000		A counter of PLL for test mode
0x06	**Register Name**	**Bit**	**default**	**W**	**Description**
	PA3_WC[2:0]	7:5	010		PA3 Gain Control. Please refer to the application note in detail.
	PA2_WC[1:0]	4:3	11		PA2 Gain Control. Please refer to the application note in detail.
	PA1_WC[1:0]	2:1	10		PA1 Gain Control. Please refer to the application note in detail.
	D2S_Gain	0	1		D2S Gain control. Please refer to the application note in detail.
0x07	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_BB_TM	7	0		1: Enable BB Test mode for test only 0: Disable BB Test mode for test only
	Reserved	6	0		
	EN_AAC_TM	5	1		Enable PA AAC auto-calibrated control 1: Enable PA output power auto calibration.
	VCO_AFC_Resol[1:0]	4:3	11		VCO AFC resolution control
	VCO_AFC_3W[2:0]	2:0	000		VCO AFC curve manual selection when 0x05[5]=1 for test only
0x08	**Register Name**	**Bit**	**default**	**W**	**Description**
	TxDC_SW_3W	7	0		Manual control TX LPF corner for test only
	EN_RxEN_Delay	6	1		1: Enable the function which delays to enable RX RF to save current during PLL un-locked in Rx mode.
	SC_CH[5:0]	5:0	000000		VCO capacitor array for fast settling
0x09	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_RxEN[2:0]	7:5	000		RX chain off time control (Check with 0x08[6]) Off Time=20us*(1+Delay_RxEN[2:0])
	EN_TxMOD	4	1		1: Enable the frequency deviation tuning (Tuning by 0x0a[2:0])
	SEL_I_V	3	1		Switch ADC input from RSSI or Vtune of VCO (SEL_I_V) 1: RSSI 0: Vtune of VCO for test only
	SEL_VB[2:0]	2:0	000		Selection ADC Full range Voltage SEL_B[2:0] for test only
0x0a	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_XO[2]	7	0		Crystal settling wait time during frequency calibration
	EN_SignalDet	6	1		1: Enable Signal Detection Circuits for test only
	EN_3M_IF	5	0		1: IF = 3MHz for 1.6Mbps data rate 0: IF = 2MHz for 1Mbps data rate
	EN_TxDC_LPF	4	0		1: Enable transmitter data compensation filter
	SEL_MOD_RES[3:0]	3:0	0111		Transmitter Frequency Deviation Control 0x0a[3:0] / Frequency Deviation (kHz) 0 0 1 1 / 200 0 1 1 1 / 400 1 1 0 1 / 500
0x0b	**Register Name**	**Bit**	**default**	**W**	**Description**
	nEN_XO_2uA	7	0		Crystal buffer bias current, {R0x0b[7],R0x01[2:1]} default 010.
	Delay_TxDC[0]	6	0		Check with 0x0a[4], compensation filter settling time control
	CHP_SW_3w	5	0		Charge Pump Current Control Mode for test only
	Delay_CHP_SW[3:0]	4:1	0101		Charge Pump bias current control
	EN_PLL_Fast	0	1		1: Enable PLL fast settling option
0x0c	**Register Name**	**Bit**	**default**	**W**	**Description**
	SD_EN_DutyDelta	7	1		RX Signal detection option.
	SD_EN_FreqDelta	6	1		
	Sel_SD	5	1		
	EN_KXO	4	0		1: Start crystal frequency calibration 0: Disable crystal frequency calibration
	KXO_spi[3:0]	3:0	0000		Crystal Loading Capacitor Selection 0000: CL=27p
0x0d	**Register Name**	**Bit**	**default**	**W**	**Description**
	SD_DutyDelta[1:0]	7:6	01		RX Signal detection options. (Fixed)
	SD_FreqDelta[1:0]	5:4	00		
	SD_RangeH[1:0]	3:2	11		
	SD_Range	1	1		
	SD_Noise	0	1		

0x0e	Register Name	Bit	default	W	Description
	Low_wRFSPI	7	1		1: Set 1 to forbid to write RF SPI registers, 0x20 to 0x33 0: Set 0 to allow to write RF SPI registers, 0x20 to 0x33
	EN_PAONdelay	6	0		1: Enable the time delay between PLL ON and PA ON for test only
	EN_Stop1M_D[1:0]	5:4	01		Clock gating delay for internal circuit's system clock.
	EN_PAON_D[3:0]	3:0	0001		Check with 0x0e[6], setting the delay time for test only
0x0f	**Register Name**	**Bit**	**default**	**W**	**Description**
	Delay_XO[1:0]	7:6	00		Crystal settling wait time during frequency calibration
	I_PA_UPDN[5:0]	5:0	011000		PA gain control options.

Table 7: Register Function Description for address from 0x00 to 0x0E

Address 0x20 to 0x33.

Address	Register Name	Bit	Default	Type	Description
0x20	**Register Name**	**Bit**	**default**	**W**	**Description**
	FE_PTAT	7	1		Enable PTAT option for Front-End 1: with PTAT 0: without PTAT
	Mix_BS	6	0		RX Mixer bias control (Fixed)
	MIX_BS[3:0]	5:3	101		RX Mixer bias control (Fixed)
	LNA_BS[3:0]	2:0	101		RX LNA bias control (Fixed)
0x21	**Register Name**	**Bit**	**default**	**W**	**Description**
	FILT_PTAT_CTRL[1:0]	7:6	01		Filter PTAT Control. Default: 01
	CLM_G[2:0]	5:3	100		RX buffer High/Low gain mode control (Fixed)
	CLM_SW[2:0]	2:0	100		RX buffer High/Low output swing control (Fixed)
0x22	**Register Name**	**Bit**	**default**	**W**	**Description**
	SLICE_Nb[3:0]	7:4	0000		RX Slicer Common DC control (Fixed)
	SLICE_Pb[3:0]	3:0	0000		
0x23	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PTAT_Buf_RxMx	7	1		Enable PTAT option for RX Mixer 1: with PTAT 0: without PTAT
	Ictrl_Buf_RxMx[2:0]	6:4	100		RX Mixer bias control (Fixed)
	EN_PTAT_Div2	3	0		Enable PTAT option for divide by 2 1: with PTAT 0: without PTAT
	Ictrl_Div2[2:0]	2:0	011		Divide by 2 bias control (Fixed)
0x24	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PTAT_Buf_D2S	7	1		Enable PTAT option for RF D2S buffer 1: with PTAT 0: without PTAT
	Ictrl_Buf_D2S[2:0]	6:4	011		RF D2S buffer bais control (Fixed)
	EN_PTAT_Buf_IQComb	3	1		Enable PTAT option for IQ combiner buffer 1: with PTAT 0: without PTAT
	Ictrl_Buf_IQ_Comb[2:0]	2:0	101		IQ combiner buffer bias control (Fixed)
0x25	**Register Name**	**Bit**	**default**	**W**	**Description**
	Vctrl_VCO_CAL[1:0]	7:6	10		VCO AFC 's control voltage selection (Fixed)
	Ictrl_VCO[2:0]	5:3	100		VCO bias control (Fixed)
	EN_PTAT_Pre	2	0		Enable PTAT option for Prescaler 1: with PTAT 0: without PTAT
	Ictrl_Pre[1:0]	1:0	10		Prescaler bias control (Fixed)
0x26	**Register Name**	**Bit**	**default**	**W**	**Description**
	bat_det_win	7	0		Windows selection for battery detection, check with 0x29[1:0]
	PD_sel_10p	6	0		Capacitor selection for RX demodulator (Fixed)
	SLICE_G[3]	5	0		Demodulator Buffer Gain (Fixed)
	L_bypassSavePower	4	1		Set Low to bypass Save Power function for test only
	EN_700K	3	1		RX IF LPF bandwidth selection 1: for 1Mbps data rate 0: for 1.6Mbps data rate
	Ictrl_CHP_UP[4]	2	0		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
	EN_CLK_STOP	1	1		Enable clock gating in test mode for test only
	Reversed	0	0		
0x27	**Register Name**	**Bit**	**default**	**W**	**Description**
	Ictrl_CHP_UP[3:0]	7:4	0000		Increase Charge Pump Bias Current, Ictrl_CHP_UP[4:0] (Fixed)
	Ictrl_CHP_DN[3:0]	3:0	1001		Decrease Charge Pump Bias Current, Ictrl_CHP_DN[3:0] (Fixed)

0x28	Register Name	Bit	default	W	Description
	TS_dig_pllbw	7	0		Digital output selection in test mode (for test only)
	TS_dig_rxdelay	6	0		
	TS_dig_KXO32	5	0		
	TS_dig_KXO10	4	0		
	Reversed	3	0		
	Reversed	2	0		
	H_macPD_L_enPD	1	0		RX demodulator Mode Selection
	Manual_EN_PLL	0	0		Manual enable PLL for test only
0x29	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TSO_LDPA	7	1		1: Set LD & EN_PA to ATP in test mode
	EN_TSO_SD	6	0		1: Set signal detection output to ATP in test mode
	nEN12_EN24	5	1		System Reference Clock Selection 1: 24MHz 0: 12MHz / 16MHz
	EN_75M_toKXO	4	1		1: Enable clock gating option for frequency calibration
	Vf_reg_ctrl[1:0]	3:2	10		Set filter calibration output voltage to ATP in test mode
	bat_det_level[1:0]	1:0	00		Selection of Battery detection level

Threshold Voltage		
0x29[1:0]	0x26[7]=0	0x26[7]=1
00	1.9	1.7
01	2.0	1.8
10	2.1	1.9
11	2.2	2.0

0x2a	Register Name	Bit	default	W	Description
	PA3_BIT[3:0]	7:4	0011		TX PA3 Bias current control (Fixed)
	PA2_BIT[3:0]	3:0	0011		TX PA2 Bias current control (Fixed)
0x2b	**Register Name**	**Bit**	**default**	**W**	**Description**
	Ictrl_PAPD[3:0]	7:4	0000		TX PA AAC bias current control (Fixed)
	PA1_BIT[3:0]	3:0	0101		TX PA1 Bias current control (Fixed)
0x2c	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_PA_PTAT	7	1		Enable PTAT option for TX PA1 1: with PTAT 0: without PTAT
	SLICE_G[0]	6	0		Demodulator gain control (Fixed)
	DCLevel_BIT[1:0]	5:4	01		TX PA AAC reference level selection (Fixed)
	CP_WIN	3	0		TX PA AAC comparator windows selection (Fixed)
	PD_GC_BIT[2:0]	2:0	010		TX PA AAC comparator reference voltage selection (Fixed)
0x2d	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_BPF_PASS	7	0		0: normal operation 1: Bypass Rx BPF for test only
	ENB_SL_PD	6	0		1: Disable Demodulator for test only 0: Normal operation
	SLICE_G[1]	5	0		Demodulator gain control (Fixed)
	EN_LDout_TS	4	1		Set LD to ATP in test mode
	EN_FILT_AUTO	3	1		AUTO / Manual Filter calibration loop 1: Filter bandwidth auto calibration 0: Manual settling for filter bandwidth for test only
	FILT_AUTO_BW	2:0	010		Filter Bandwidth settling for Filter Calibration loop
0x2e	**Register Name**	**Bit**	**default**	**W**	**Description**
	DEM_PVT_OPT	7	0		Demodulator reset control in test mode
	EN_Vf_TS	6	0		Set Filter Vtune to ATP in test mode
	EN_LD	5	0		1: Enable PLL lock detection function 0: Disable PLL lock detection function
	EN_Vf_TS	4	0		Enable filter Vtune test output in test mode
	BY_PTAT	3	0		Bypass PTAT for test only
	BY_BG	2	0		Bypass Bandgap for test only
	EN_CtrlRxOut_bySD	1	1		RX data output notch function 1: Notch the data output when no RF signal input 0: Continues to output RX data
	SLICE_G[2]	0	1		Demodulator gain control (Fixed)
0x2f	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_Vf_B_TS	7	0		Set filter Vf to ATP in test mode
	TS_Id_EnPA	6	1		Enable Test Output for LD & EN_PA for test only
	REG1_RB[2:0]	5:3	100		Regulator A output voltage selection for PLL and Digital
	BGR_RB[2:0]	2:0	100		Regulator B output voltage selection for RF & IF
0x30	**Register Name**	**Bit**	**default**	**W**	**Description**
	Sel_LNA_Gain	7	1		To Enhance the LNA Gain

					0: Default 1: Enhance LNA Gain
	EN_Internal_LPF	6	1		Enable Internal PLL Loop Filter 0: External PLL loop filter for test only 1: On-Chip PLL loop filter
	EN_TM_PLL_VT	5	0		Enable internal PLL tuning voltage to out-of-chip for test only
	TSO_PA[2:0]	4:2	000		PA biasing voltage selection for test only
	EN_TM_DEM	1	0		Demodulator test mode enable 0: normal operation 1: test mode
	DEM_VT_IO	0	0		Demodulator reference voltage tracking (when R0x30[1]=1, for test only)
0x31	**Register Name**	**Bit**	**default**	**W**	**Description**
	SW_TSIO_LPF	7	0		Test Mode Setting for test only
	SW_TSIO_BPF	6	0		
	EN_TSO_DEM_FILT	5	0		
	EN_TSO_PA_PLL	4	0		
	EN_TSO_RSSI	3	0		
	EN_TSIO_LPF	2	0		
	EN_TSIO_BPF	1	0		
	EN_TSIO_BS	0	0		
0x32	**Register Name**	**Bit**	**default**	**W**	**Description**
	Syn_En_Delay[3:0]	7:4	0100		Time selection for PLL synchronization (Fixed)
	En_Syn_PFD	3	1		1: Enable PLL synchronization function to speed up the PLL settling
	En_Chp_Vt_initial	2	0		1: give initial voltage for PLL
	EN_LD_TS	1	1		1: Set EN_PA to ATP in test model
	EN_TSIO_DIG	0	0		Baseband Test signal IO (when R0x07[7]=1) ATP1: digital output ATP2: digital input
0x33	**Register Name**	**Bit**	**default**	**W**	**Description**
	EN_TSO_EN_VCO	7	0		For test only, 1: Set EN_VCO to ATP in test mode 0: Set EN_PA to ATP in test mode
	EN_TSO_Vref_PD	6	0		For test only, 1: Set peak detection reference voltage of PA AAC to ATP in test mode 0: Set PLL locking voltage to ATP in test mode
	Sel_SDOUT_Issig	5	0		Signal detection output selection. 1: SDOUT (default) 0: Issig (for test only)
	Sel_EN_Fast	4	1		To enable the demodulator reset option.
	nEN_DEMPVT	3	1		Demodulator Reset control signal source. Valid when R0x33[3]=1 (for test only) 1: initialization by EN_Fast 0: initialization by EN_DEM
	EN_NoAFC_swCH	2	0		Set High means don't go into AFC when channel switch
	EN_Bat_out	1	1		Battery detection function enable
	En_fun_1Mstop	0	1		Enable the clock gating for PA AAC loop (Fixed)

Table 8: Register Function Description for address from 0x20 to 0x33

Note: PTAT (Proportional to Absolute Temperature): The bias currents of the circuits are proportional to the temperature

Configuration Registers for Mini MAC

User only can change the configuration registers which highlight with gray background.

	D7	D6	D5	D4	D3	D2	D1	D0
0x40	STARNET	BURSTMD	0	1	AUTOACK	NEEDACK	TXDEV	RXDEV
0x41	1	0	RXEN5	RXEN4	RXEN3	RXEN2	RXEN1	RXEN0
0x42	ADRBC[1:0]		BRATEC[5:0]					
0x43	1	CRCLEN[1:0]		SYNCBC[4:0]				
0x44	0	PKTLEN[6:0]						
0x45	PKTCNT[3:0]				0	0	0	0
0x46	0	0	TDTXOPT[2:0]		TDPLLOPT[2:0]			
0x47	RETRYCNT[3:0]				SLOTLEN[3:0]			
0x48	0	0	0	0	0	0	0	1
0x49	ACKTOSLOT[7:0]							
0x4a	0	0	RSSITH[5:0]					
0x4b	0	0	RF_RSSI[5:0]					
0x4c	0	0	0	0	TD_PLLRT[3:0]			
0x4d	0	0	0	0	0	0	0	SWRST
0x4e	0	0	0	0	0	0	CLKMODE[1:0]	
0x4f	PACKET LOST COUNT[7:3]					0	0	0
0x50	TXADR[7:0] or RXADR0[7:0]							
0x51	TXADR[15:8] or RXADR0[15:8]							
0x52	RXADR1[7:0]							
0x53	RXADR1[15:8]							
0x54	RXADR2[7:0]							
0x55	RXADR3[7:0]							
0x56	RXADR4[7:0]							
0x57	RXADR5[7:0]							
0x58	BACKOFFWIN[7:0]							

Table 9: Configuration Registers for Mini MAC

Address 0x40 to 0x58

Address	Register Name	Bit	Default	Type	Description
0x40	Register Name	Bit	default	W/R	Description
	STARNET	7	0		1: there will be a PID in frame structure, and this 1 byte PID will be in MSB of TX/RX buffer payload(packet). For detail information, please refer to the section of Packet Description. 0: no PID byte in frame structure, no PID byte in TX/RX buffer payload (packet).

	BURSTMD	6	1		For the detail description, please refer to the section of SPI interface read/write FIFO for buffer mode. 1: SPI master should assert PKTLEN+1 bytes cycles for a complete packet buffer access. The PKTLEN length data succeed with 1 bytes address 0: SPI master will assert 2 cycles PKTLEN times for a complete packet buffer access. 1 bytes address + 1 bytes data in PKTLEN cycles times
	PLLOPT	5	0		1: TX/RX dev won't wait TDPLLOPT time for normal EN_TX/EN_RX assertion 0: TX/RX dev will wait TDPLLOPT time for normal EN_TX/EN_RX assertion
	BACKOFFOPT	4	1		1: as during TX Back off window, TX device's RF will stay in Idle mode. 0: otherwise, it will stay in RX mode.
	AUTOACK	3	1		1: only valid under RXDEV, RXDEV will transmit ACK packet after receiving address hit packet automatically (RXADR0-RXADR5) 0: Disable Auto ACK function
	NEEDACK	2	1		1: only valid under TXDEV, TX complete interrupt will be set after receiving ACK from a transmitted packet 0: Disable the function
	TXDEV	1	1		1: set current device as a transmitter device, only valid when RXDEV=0
	RXDEV	0	0		1: set current device as a receiver device, only valid when TXDEV=0
0x41	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXOPT	7	1		1: chip timing. 0: dynamic modify chip timing according to zero crossing position.
	Reserved	6	0		
	RXEN5	5	0		1: enable receiving packet with RXADR5 address
	RXEN4	4	0		1: enable receiving packet with RXADR4 address
	RXEN3	3	0		1: enable receiving packet with RXADR3 address
	RXEN2	2	0		1: enable receiving packet with RXADR2 address
	RXEN1	1	0		1: enable receiving packet with RXADR1 address
	RXEN0	0	0		1: enable receiving packet with RXADR0 address
0x42	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	ADRBC[1:0]	7:6	10		address byte counts in each TX/RX frame valid value1-2.
	BRATEC[5:0]	5:0	011000		bit rate counter When CLKMODE=2'b01 (system runs at 16MHz) 6'd16: 1Mbps 6'd10: 1.6Mbps When CLKMDOE=2'b10 (system runs at 24MHz) 6'd24: 1Mbps 6'd15: 1.6Mbps
0x43	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	PADOPT	7	1		1: HW will auto pad one after successively 4 zeros or pad zero after successively 4 ones. 0: otherwise, after successive 8 zeros or ones
	CRCOPT[1:0]	6:5	10		CRC option 00: no CRC in each TX/RX frame 01: 1 byte CRC in each TX/RX frame with polynomial : x8+x4+x3+x2+1 10: 2 bytes CRC in each TX/RX frame with polynomial : x16+x15+x2+1 11: 4 bytes CRC in each TX/RX frame with polynomial : x32+x26+x23+x22 +x16+x12+x11+x10+x8+x7+x5+x4+x2+x+1
	SYNCBC[4:0]	4:0	00100		sync word length in byte unit. If SYNCBC=10, there will be 8 bytes 8'haa sync pattern (8'b10101010) in each TX/RX frame
0x44	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7	0		
	PKTLEN[6:0]	6:0	0001000		Payload length, excludes ADR and CRC, but *includes PID in star network*.
0x45	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	PKTCNT[3:0]	7:4	0001		Max packet counts in buffer. There are PKTCNT packets could be stored in the TX/RX buffer. Make sure PKTLEN * PKTCNT <= 64. (buffer length).
	Reserved	3:0	0000		
0x46	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:6	00		
	TDTXOPT	5:3	001		Time delay for TX amplifier. TX device will wait 10+5*TDTXOPT (us) for TX amplifier stable.
	TDPLLOPT	2:0	001		Time Delay for PLL enable TX/RX device will wait 100+ 20*TDPLLOPT (us) for PLL stable
0x47	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RETRYCNT[3:0]	7:4	0001		TX retry count, valid only when NEEDACK=1. TX device will transmit

					RETRYCNT+1 times before transmission retry time out. When RETRYCNT=0, the TX device will transmit the packet only once.
	SLOTLEN[3:0]	3:0	0001		In unit 10us, when SLOTLEN=2, which means a slot time is 20us
0x48	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	INIBACKOFF[7:0]	7:0	00000001		in slot unit, TX device will check the channel clearance for INIBACKOFF slots, before transmitting the packet at the first time
0x49	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	ACKTOSLOT[7:0]	7:0	10001010		Ack packet response time out length in slot unit. If slot=20us, when ACKTOSLOT[7:0]=10, which means ACK time out when no valid ACK packet received within 200us after transmitting a packet (which needs ack)
0x4a	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:6	00		
	RSSITH[5:0]	5:0	100111		When mini MAC input RSSI[5:0] larger than RSSITH, which indicates channel occupied (CA=1). If don't want to check the channel clearance, just set RSSITH=63
0x4b	**Register Name**	**Bit**	**default**	**R**	**Description**
	Reserved	7:6	00		
	RF_RSSI[5:0]	5:0			Read only, RF RSSI output
0x4c	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:4	0000		
	TD_PLLRT	3:0	0110		in unit 10us
0x4d	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:1	0000000		
	SWRST	0	1		1: reset whole system and all configuration except CLKMODE
0x4e	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Reserved	7:2	000000		
	CLKMODE[1:0]	1:0	10		System Reference Clock 01: 16MHz 10: 24MHz
0x4f	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	Packet lost count	7:3	00000		R/W. update by HW. SW write 0 to clear. When lost packet larger than 31, will saturate lost packet count to 31
	Reserved	2:0	000		
0x50	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	TXADR[7:0]	7:0	00000000		valid when ADRBC=1-2, when ADRBC=1, TXADR={TXADR[7:0]}
0x51	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	TXADR[15:8]	7:0	00010001		valid when ADRBC=2,when ADRBC=2, TXADR={TXADR[15:8],TXADR[7:0]};
0x52	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR1[7:0]	7:0	00100010		valid when ADRBC=1-2, when ADRBC=1, RXADR1={RXADR1[7:0]}
0x53	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR1[15:8]	7:0	00110011		valid when ADRBC=2,when ADRBC=2, RXADR1={RXADR1[15:8],RXADR1[7:0]};
0x54	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR2[7:0]	7:0	01000100		valid when ADRBC=1-2, when ADRBC=1, RXADR2={RXADR2[7:0]}; when ADRBC=2, RXADR2={RXADR1[15:8],RXADR2[7:0]};
0x55	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR3[7:0]	7:0	01010101		RXADR3[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR3={RXADR3[7:0]}; when ADRBC=2 RXADR3={RXADR1[15:8],RXADR3[7:0]};
0x56	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR4[7:0]	7:0	01100110		RXADR4[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR4={RXADR4[7:0]}; when ADRBC=2 RXADR4={RXADR1[15:8],RXADR4[7:0]};
0x57	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	RXADR5[7:0]	7:0	01110111		RXADR5[7:0]: valid when ADRBC=1-2, when ADRBC=1, RXADR5={RXADR5[7:0]}; when ADRBC=2 RXADR5={RXADR1[15:8],RXADR5[7:0]};
0x58	**Register Name**	**Bit**	**default**	**W/R**	**Description**
	BACKOFFWIN[7:0]	7:0	00001000		in slot unit, TX device will check the channel clearance for BACKOFFWIN slots, before transmitting the packet at the retry sequence.

Table 10: Register Function Description for address from 0x40 to 0x58

Application Diagram (MU2400)

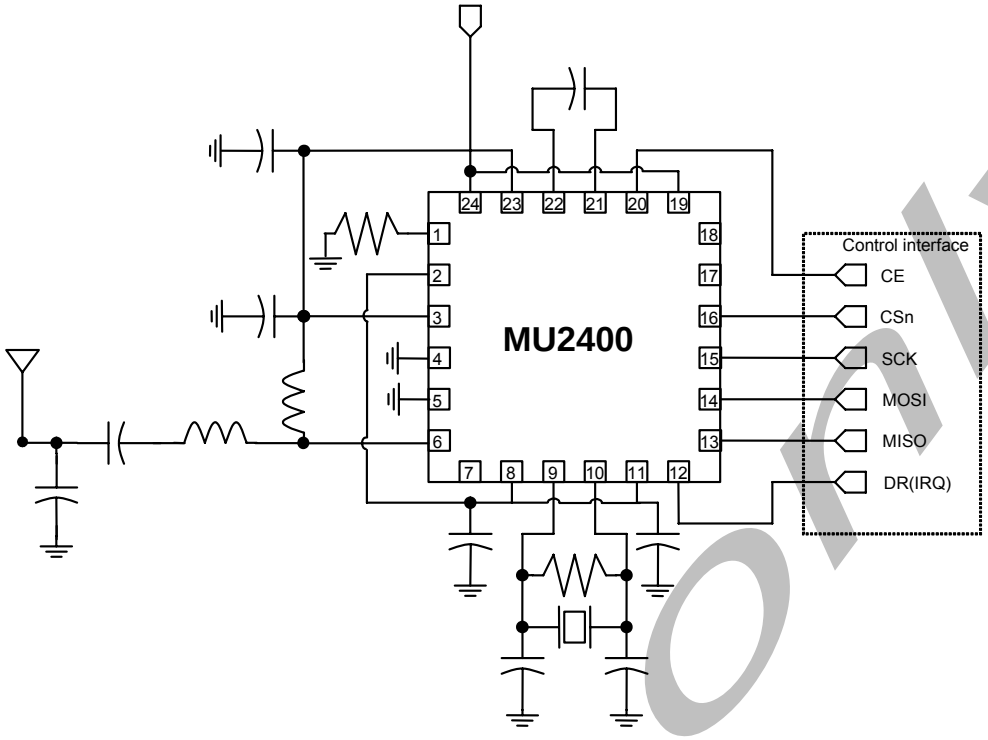


Figure 20: Application Diagram of MU2400

Application Diagram (MU2401)

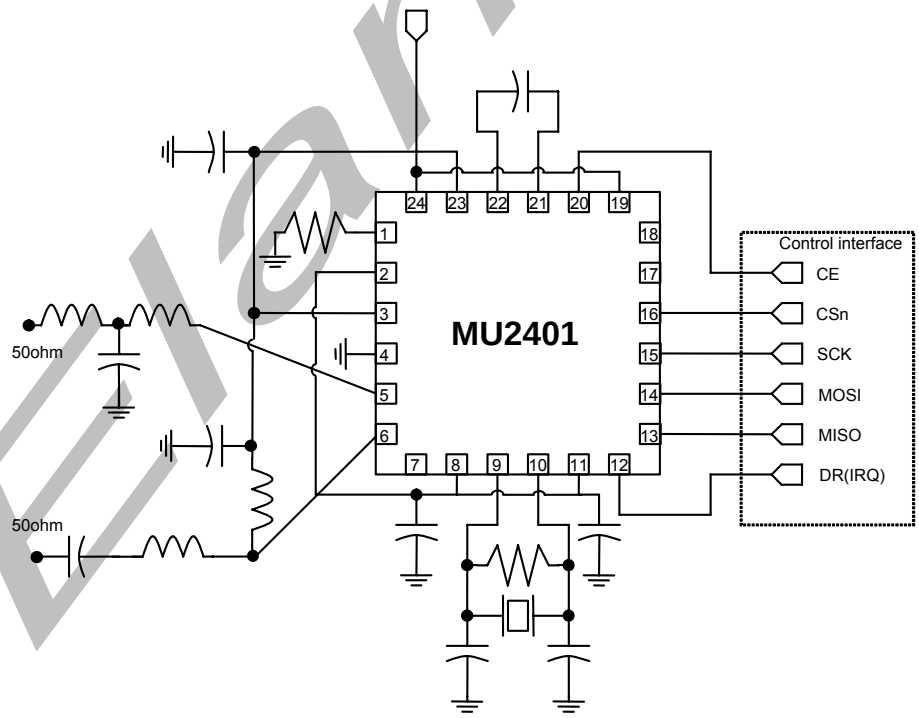
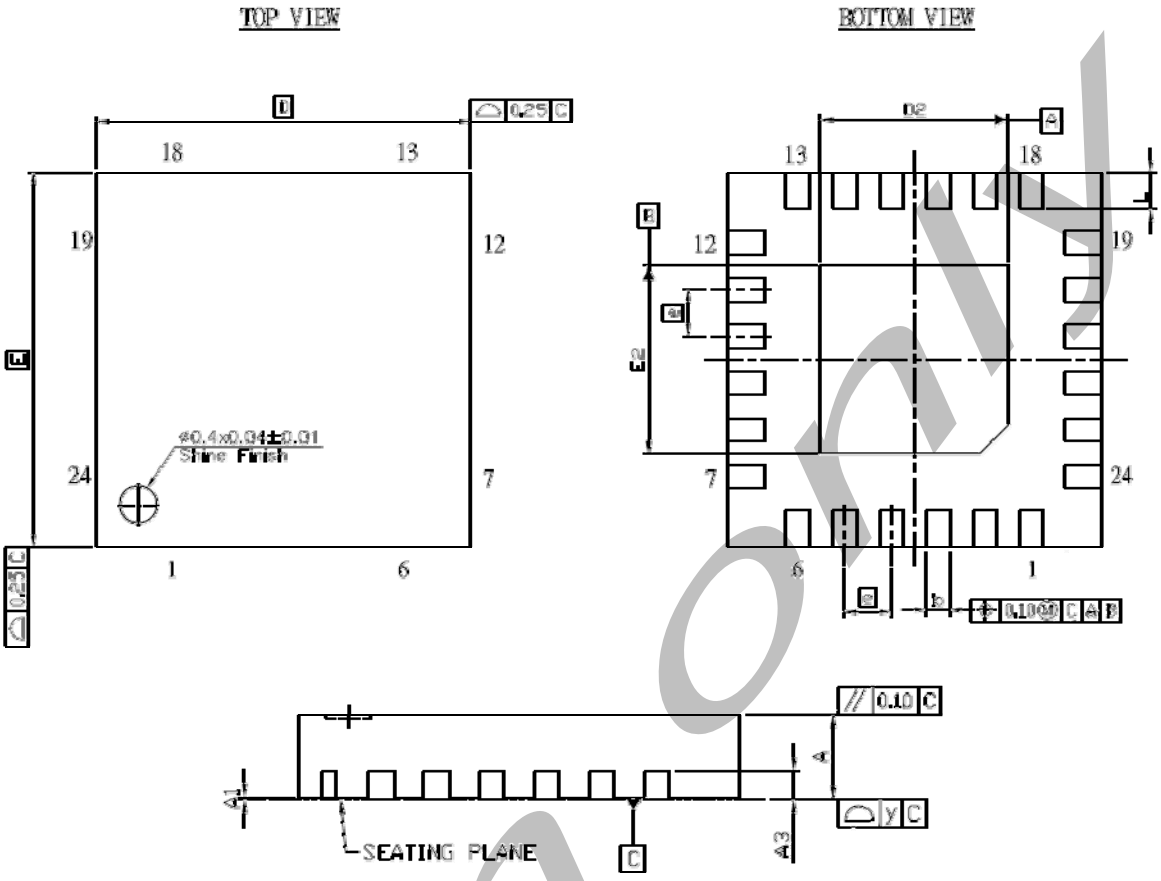


Figure 21: Application Diagram of MU2401

MU2400/MU2401 Pin Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	27.6	29.5	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	0.203 REF			8 REF		
b	0.18	0.25	0.30	7.09	9.84	11.81
D	3.90	4.00	4.10	153.5	157.5	161.4
D2	1.90	2.00	2.10	74.8	78.7	82.7
E	3.90	4.00	4.10	153.5	157.5	161.4
E2	1.90	2.00	2.10	74.8	78.7	82.7
e	0.50 BSC			19.69 BSC		
L	0.30	0.40	0.50	11.8	15.7	19.7
y	0.08			3.15		

Figure 22: Pin Package of MU2400/MU2401