Yuehao Li

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EDUCATION

University of California, Santa Cruz, CA **Sep. 2018 - May. 2022**
Bachelor of Science, Computer Engineering, Digital Hardware
GPA: 3.72/4.0
Honors: Dean's List (19, 20 Spring, 20 Fall, 21 Winter, 21 Spring, 22 Spring)
Related Courses: Computer Architecture; Analog Electronics; Logic Design with Verilog; Embedded System Design; VLSI Design; Data Structures and Algorithms; Object-oriented Programming; Signals and Systems

WORK EXPERIENCE

Cuddly LLC, Software Engineer Intern **Nov. 2022-Present**
- Responsible for onboarding developer tools used to create iOS and Android app features, database queries to fulfill data retrieval for rendering App Content, and scripting to ingest data into our database for testing, etc.

RESEARCH & PROJECT

CSE123A&B Capstone Project: Automatic Blinds **Jan. 2022-Jun. 2022**
Skills: Embedded System - Arduino, Analog Circuit Design, CAD, Swift, C, Oscilloscope
- An add-on to blinds that can be used rotating the rod based on user's input, and our design features a motor, a microcontroller, light sensors and an App.
- Mainly responsible for assembling circuits on breadboards, testing photo-resistors and 3D printing.

CSE111 Multi-Server, Multi-threaded Password Cracker **Jun. 2022**
Skills: C++, Object-oriented Programming, Parallel & Distributed Computing, TCP, UDP
- The password cracker will use 4 servers with 96 core CPUs to crack a hash code and finish in 1 second.
- UDP & TCP protocols used to transfer information and sync all cores between servers.

CSE125 Prime Tester **Jun. 2022**
Skills: Verilog, Vivado, FPGA, Xilinx Artix 7, Finite-state machine, C
- A prime number checker module that takes an input number and check if it is prime.
- Integrate this module into the prime_checker IP (AXI4-lite) to verify functionality.
- Optimized the whole system by stop counting until $\sqrt{n}$, which optimized it 100X faster.

CSE122 SRAM Design **Jan. 2022**
Skills: Sky130, VLSI, SPICE, Ngspice, Layout Versus Schematic (LVS), IRSIM
- Use Sky130A CAD to implement the layout of an SRAM bit cell that can be used in an array.
- Build a 3*3 SRAM array based on the SRAM bit cell.
- Test the CAD-designed chip circuit with simulation software.

CSE121 Embedded Distance Meter **Dec. 2021**
Skills: PSoC6, Embedded C, UART, I2C, FIFO, Circuit Design
- Built an ultrasonic distance meter which consists of a device that transmits ultrasonic pulses (at 40 kHz) and a receiver that detects echoes.
- UART protocol to communicate between two devices, FIFO to ensure data transmitted correctly under different frequencies, I2C protocol to display results on a LED display, low pass filter to debounce.

CSE100 Bidirectional Gate People Counter **Nov. 2020**
Skills: Artix-7 FPGA, Vivado, Verilog
- A traveller volume counter that counts the total number of person pass the gate.
- Two sensors placed on either side of the gate to distinguish between people entering and exiting the area.

CSE185E CPU Structure Architecture and Future **Dec.2021**
Skills: LaTeX
- Discussed the CPU structure, packaging, internal logic, manufacturing and future development.

ACTIVITIES & LEADERSHIP EXPERIENCE

Reader, CSE120 Computer Architecture **Sept. 2021–Jun. 2022**
Tutor, CSE100 Logic Design (Verilog) **Sept. 2021–Apr. 2022**

SKILLS

- **Technical Skills:** Software Engineering, Algorithms, Data Structures, Relational Databases, Hardware
- **Technology**: Python; Java; C; C++; Matlab; MIPS; Verilog; VLSI; Linux & Unix; Microsoft Office