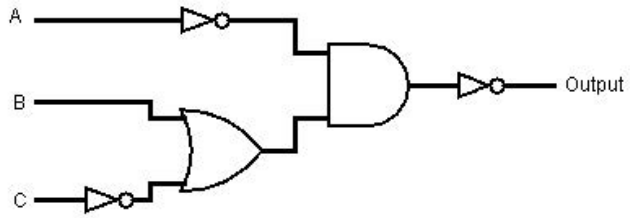
Computer Architecture Homework 4

Spring 2019, March

1 Synchronous Finite State Digital Machine Systems

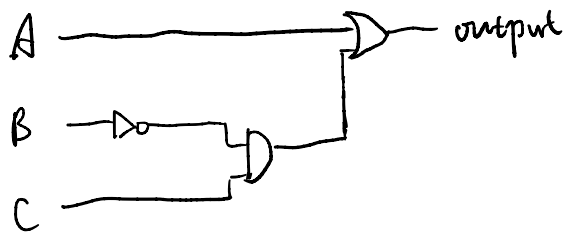
a. The circuit shown below can be simplified. Write a Boolean expression that represents the function of the simplified circuit using the minimum number of AND, OR, and NOT gate.



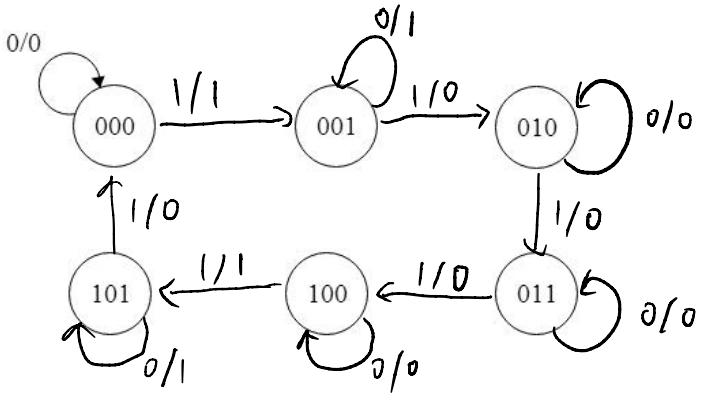
$$\overline{\bar{A}(B+\bar{C})} = A + \overline{(B+\bar{C})}$$

$$= A + \bar{B}C$$

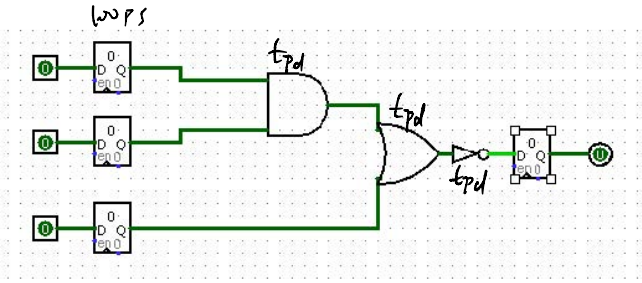
Simplified Circuit:



b. Consider the finite state machine below which has 6 states and a single input that can take on the value of 0 and 1. The finite state machine should output 1 IF AND ONLY IF 6 + sum of all the input values is not divisible by 2 or 3. One transition has been provided; complete the remainder of the diagram. (Hint: If the sum of the inputs is a multiple of 6, then we have 6 + sum of the inputs = 6n for some n. As 6n is divisible by 2, 6n cannot be prime.)



c. Consider the following circuit. Assume registers have a CLK to Q time of 60ps, a setup time of 40ps, and a hold time of 30ps. Assuming that all gates have the same propagation delay, what is the maximum propagation delay each individual gate could have to achieve a clock rate of 1 GHz.



Suppose the maximum propagation delay is t_{pd}

The register delay is Setup + C-to-Q = 0.1×10^{-9} s

$f($ register delay + $3t_{pd}$ $) = 1 \times 10^9$

$0.1 \times 10^{-9} + 3t_{pd} = 1 \times 10^9$

$\Rightarrow t_{pd} = 0.3 \times 10^{-9}$ s = 300 ps

2 Boolean Logic

1. Simplify each Boolean expression to one of the following ten expressions:
$0, 1, A, B, AB, A+B, \overline{A}\ \overline{B}, \overline{A}+\overline{B}, A\overline{B}, \overline{A}B$
Each answer may be used as many times as necessary.

a. $A(A+\overline{A})+B$

$= A\overline{A} + A\overline{A} + B = A + 0 + B = A + B$

b. $(A+B)(\overline{A}+B)\overline{B}$

$= [(A+B)\overline{A} + (A+B)B]\,\overline{B} = [B\overline{A} + AB + B]\,\overline{B} = [B\overline{A} + (A+1)B]\,\overline{B}$

$= [B(\overline{A}+1)]\,\overline{B} = 0$

c. $\overline{\overline{A}+\overline{B}}$

$= (\overline{\overline{A}})(\overline{\overline{B}}) = AB$

2. Simplify the following expression step by step (as simple as possible):

a. Standard: $(A+B)(A+\overline{B})C$

$= (AA + A\overline{B} + BA)C = (A + A(\overline{B}+B))C = (A+A)C = AC$

b. Grouping & Extra Terms: $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}\,\overline{C} + ABC + A\overline{B}C$

$= (\overline{A}+A)\overline{B}\,\overline{C} + (\overline{A}B + AB)\overline{C} + (AB + A\overline{B})C$

$= \overline{B}\,\overline{C} + B\overline{C} + AC = \overline{C} + AC = \overline{C} + A$

c. DeMorgan's: $\overline{A(\overline{B}\,\overline{C}+BC)}$

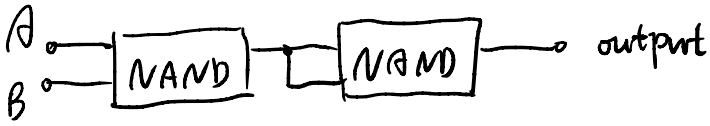
$= \overline{A} + \overline{(\overline{B}\overline{C} + BC)} = \overline{A} + (\overline{\overline{B}\overline{C}})\,\overline{(BC)}$

$= \overline{A} + (B+C)(\overline{B}+\overline{C}) = \overline{A} + B\overline{B} + B\overline{C} + C\overline{B} + C\overline{C} = \overline{A} + B\overline{C} + C\overline{B}$

3 Logic Gates

a. Create a NOT gate using only NAND gates.

b. Create an AND gate using only NAND gates. (Hint: use a)



c. Create an OR gate using only NAND gates.

d. Create a NOR gate using only NAND gates. (Hint: use a & c)