Name(Pinyin): Yuehao Wang
Email(Prefix): wangyh3

Computer Architecture Homework 6

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Instructions:

Homework 6 is due in May. 6, covers the content of caches and float-points, please refer to the lecture slides. You can print it out and write on it, and scan it into a pdf, or you can take photos or write Latex if you want, just remember: you must create a **PDF** and upload to the **Gradescope**, please assign the questions properly on Gradescope, otherwise you will lose 25% of points.

Tell us your feeling after finish it. Thank you!

Question Set 1. Direct Mapped Cache

[30 points] In a 16-bit byte-addresses machine, the clock frequency is 3GHz. We have a cache with properties as follows:

1. Cache size is 64 Bytes;
2. Block size is 4 Bytes;
3. Cache hit time is 2 cycles;
4. Cache miss penalty is 100 cycles;

1-A. What the width of each field of following address bit assignment:

TAG: 10	Set index: 4	Block offset: 2

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

The number of cache lines = 64 / 4 = 16

Set index = $\log_2 16 = 4$

Block offset = $\log_2 4 = 2$

TAG size = 16 - 4 - 2 = 10

1-B. We will access the data of addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.)

Addresses (serially access)	Tag/Index	Hit, Compulsory or Replace
0x0000	0 / 0	Compulsory
0x0004	0 / 1	Compulsory
0x0008	0 / 2	Compulsory
0x000c	0 / 3	Compulsory
0x1000	64 / 0	replace
0x1004	64 / 1	replace
0x1008	64 / 2	replace
0x100c	64 / 3	replace
0x0000	0 / 0	replace
0x0004	0 / 1	replace

1-C. Calculations. (Step-by-step, worth 50% pts)
1-C-i: Miss rate: (4 pt.)

100 %

1-C-ii: AMAT (ns): (3 pt.)

AMAT = miss rate x miss penalty + hit time = 34 ns

1-C-iii: AMAT if we don't have this cache (ns): (3 pt.)

AMAT' = miss rate x miss penalty = 33.33 ns

Question Set 2. Two-Way Set Associative Cache

From QS 1. We change the block size to 8 Bytes and implemented a two-way set associative cache. The parameters are shown as follows:

1. Cache size is 64 Bytes;
2. 16-bit byte-addresses machine;
3. Block size is 2 words;

2-A. What is the width of each field of following address bit assignment? :

TAG: 11	Set index: 2	Block offset: 3

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

Cache lines = 64/8 = 8 Block offset = $\log_2 8 = 3$

Set index = $\log_2(8/2) = 2$ TAG = 16 − 2 − 3 = 11

2-B. We will access the data of the addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.)

Addresses (serially access)	Tag/Index	Hit, Compulsory or Replace
0x0000	0/0	compulsory
0x0004	0/0	hit
0x0008	0/1	compulsory
0x000c	0/1	hit
0x1000	128/0	compulsory
0x1004	128/0	hit
0x0000	0/0	hit
0x0100	8/0	replace
0x0000	0/0	replace
0x1004	128/0	replace

2-C. Calculations.
2-C-i. Miss rate: (5 pt.)

$\frac{6}{10} = 60\%$

2-C-ii. Assume the new cache miss time is 200 cycles and hit time is 3 cycles. Calculate the AMAT in ns. Round to the nearest tenth. (5 pt.)

$AMAT = (200 \cdot 60\% + 3) \cdot \frac{1}{3} ns = 41 ns$

Question Set 3. Floating Point Numbers

We consider the IEEE 32-bit floating point representation except with a 7-bit exponent (bias of 63) and a denorm implicit exponent of -62.
3-A. Convert `-95.2` to that form. In hexadecimal.

$-95.2 = -1.4875 \times 2^6$

exponent: $63 + 6 = 69 = 1000101_2$

$0.4875 = 0.0111\,1100\,1100\,1100\ldots_2$

$\Rightarrow$ 0XC57CCCCC

3-B. Convert `0x4a23a000` into a floating point number, specify infinities as `+inf` and `-inf`, and not a number as `NaN`.

$2^{11} \times (1 + (2^{-3} + 2^{-7} + 2^{-8} + 2^{-9} + 2^{-11})) = 2333$

3-C. What is the smallest non-infinite positive integer it CANNOT represent? (an integer is `XX.0000`). Please explain why.

With the increasement of exponent, only even integer can be represented

$1.\underbrace{11\ldots1}_{24\text{ bits}}{}_2 \times 2^{24} = \underbrace{11\ldots1}_{25\text{ bits}}$ ⇒ answer is $2^{25}+1$

3-D. What's the smallest positive value it can represent that is not a denorm? Leave your answer as a power of 2. Please explain why.

Without denorm, the smallest positive value is

$1 \times (1 + 0.00\ldots) \times 2^{1-\text{bias}} = 2^{-62}$

3-E. What's the smallest positive value it can represent? Leave your answer as a power of 2. Please explain why.

With denorm, the smallest positive value is

0	00000000	00000000-------------1
		24 bits

which is

$1 \times (0 + 2 \times 10^{-24}) \times 2^{-62} = 2^{-86}$