同济大学计算机系

数字逻辑课程实验报告

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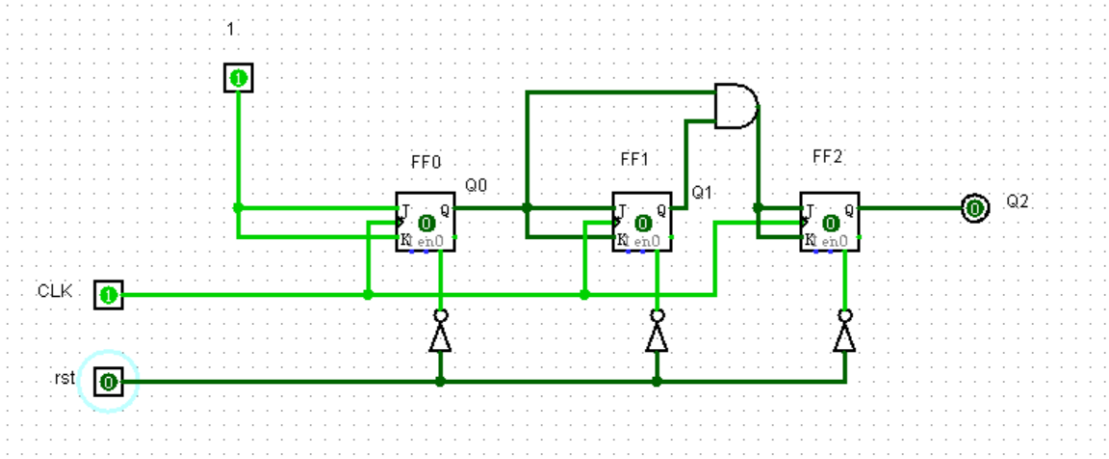
一、实验内容

实验介绍：

模 8 计数器实验： 使用 logisim 验证模 8 计数器电路逻辑，使用 Verilog 语言实现计数器的建模并设计。进行下板验证时输出到七位数码管中，利用分频器控制时钟频率观察数码管输出

二、硬件逻辑图



三、模块建模

6.7_1

```
module JK_FF(
    input CLK,
    input J,
    input K,
    input RST_n,
    output reg Q1,
    output reg Q2
    );
    always @(negedge RST_n or posedge CLK)
    begin
    if(~RST_n)
    begin
    Q1=1'b0;
    Q2=~Q1;
    end
```

```
        else    if((J==1'b0&&K==1'b1)||(J==1'b1&&K==1'b0))
                begin
                Q1=J;
                Q2=K;
                end
        else if(J==1'b0&&K==1'b0)
                ;
        else if(J==1'b1&&K==1'b1)
                begin
                Q1=~Q1;
                Q2=~Q2;
                end
        begin
        end
        end
endmodule

module display7(
        input [3:0] iData,
        output [6:0] oData
        );
        reg [6:0] oData_t;
        always @(*)
        begin
        case(iData)
                4'b0000: oData_t=7'b1000000;
                4'b0001: oData_t=7'b1111001;
                4'b0010: oData_t=7'b0100100;
                4'b0011: oData_t=7'b0110000;
                4'b0100: oData_t=7'b0011001;
                4'b0101: oData_t=7'b0010010;
                4'b0110: oData_t=7'b0000010;
                4'b0111: oData_t=7'b1111000;
                4'b1000: oData_t=7'b0000000;
                4'b1001: oData_t=7'b0010000;
                default:;
        endcase
        end
        assign oData = oData_t;
endmodule

module Divider(
        input I_CLK,
        input rst,
```

```
    output reg O_CLK = 0
    );
    parameter times = 100_000_000;
    reg [30:0]cnt = 0;
    always @(posedge I_CLK)
    begin
    if (rst)
    begin
        O_CLK = 0;
        cnt = 0;
    end
    else
    begin
        if (cnt == times/2-1)
        begin
            O_CLK = ~O_CLK;
            cnt = 0;
        end
        else
        cnt = cnt + 1;
    end
    end
endmodule

module Counter8(
    input CLK,
    input rst_n,
    output [2:0] oQ,
    output [6:0] oDisplay
    );
    wire O_CLK;
    Divider dr(CLK, 1'b0, O_CLK);
    JK_FF FF0(O_CLK, 1'b1, 1'b1, rst_n, oQ[0]);
    JK_FF FF1(O_CLK, oQ[0], oQ[0], rst_n, oQ[1]);
    JK_FF FF2(O_CLK, oQ[1]&oQ[0], oQ[1]&oQ[0], rst_n, oQ[2]);
    wire [3:0]iData={1'b0,oQ};
    display7 dis7( iData,oDisplay);
endmodule
```

6.7_2

```
module Divider(
    input I_CLK,
    input rst,
    output reg O_CLK
```

```
    );
    parameter times = 20;
    time cnt = 0;
    always @(posedge I_CLK)
    begin
    if (rst)
    begin
        O_CLK = 0;
        cnt = 0;
    end
    else
    begin
        if (cnt == times)
        begin
            O_CLK = ~O_CLK;
            cnt = 0;
        end
        cnt = cnt + 1;
    end
    end
    always @(negedge I_CLK)
    begin
        if (cnt == times)
        begin
            O_CLK = ~O_CLK;
            cnt = 0;
        end
        cnt = cnt + 1;
    end
endmodule
```

四、测试模块建模

6.7_1

```
module Counter8_tb();
reg I_CLK,rst_n;
wire [2:0] oQ;
wire [6:0] oDisplay;
Counter8 c8(I_CLK,rst_n,oQ,oDisplay);
initial
begin
```

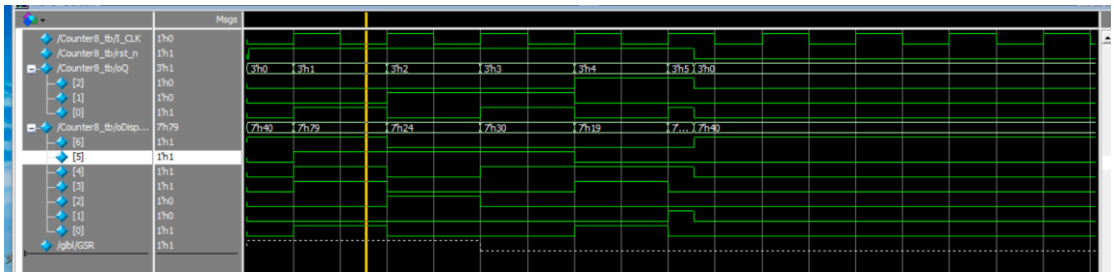
```
I_CLK<=0;
rst_n<=0;
#1 rst_n<=1;
#190 rst_n<=0;
end
always
# 20 I_CLK<=~I_CLK;
endmodule
```

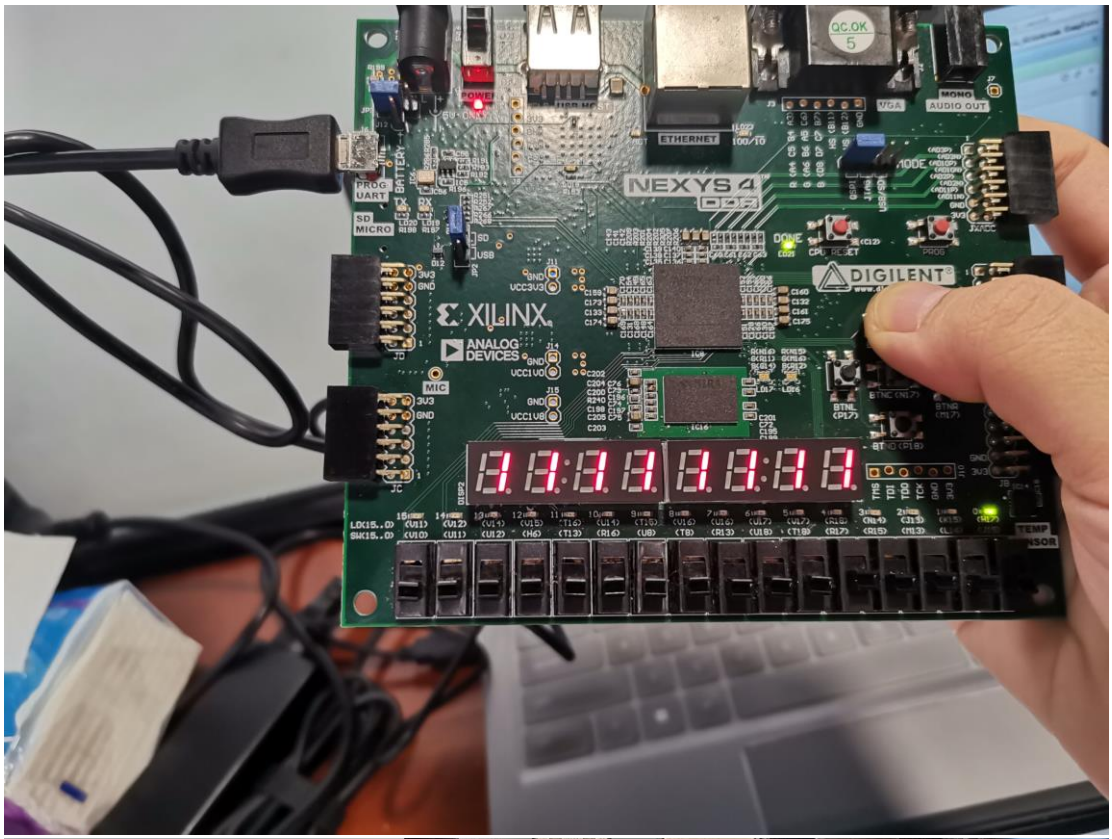
6.7_2

```
module Divider_tb();
reg I_CLK,rst;
wire O_CLK;
Divider di(I_CLK,rst,O_CLK);
initial
begin
rst<=1;
I_CLK<=0;
# 6 rst<=0;
# 390 rst<=1;
end
always
#5 I_CLK=~I_CLK;
endmodule
```

五、实验结果

6.7_1

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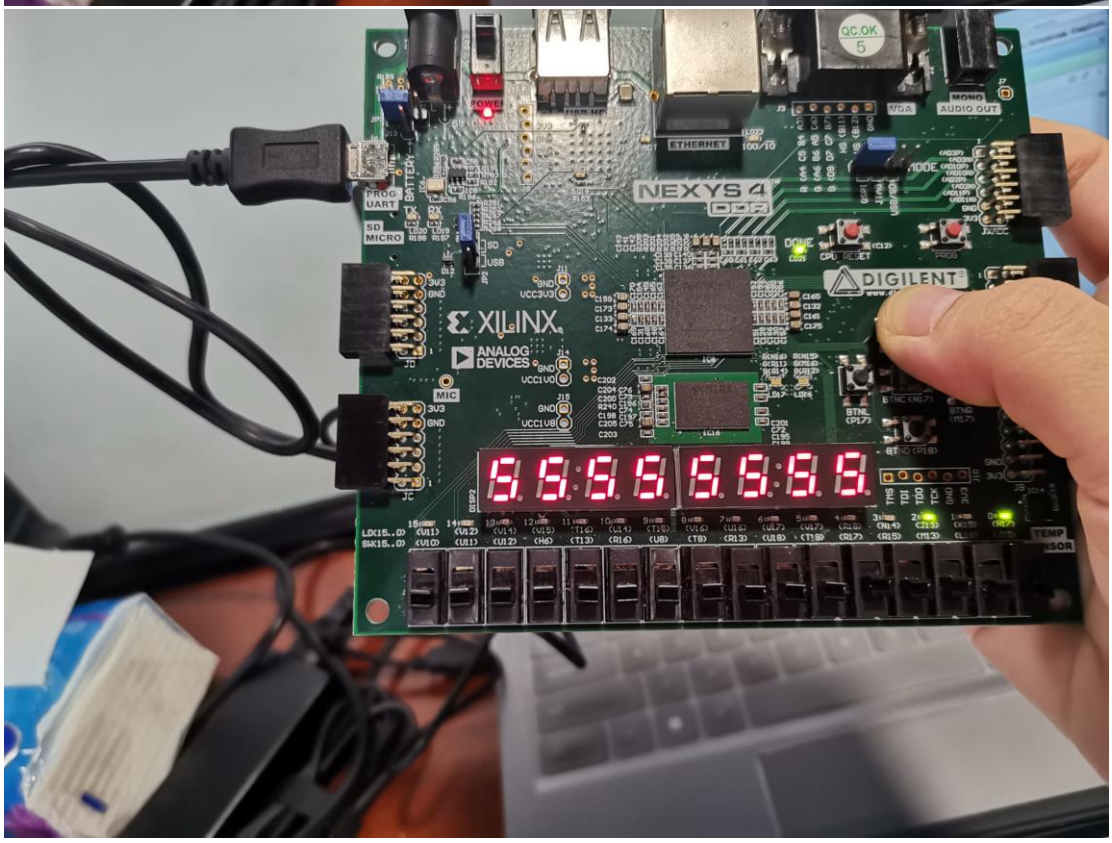
XILINX
ANALOG DEVICES
ETHERNET
VGA
AUDIO OUT
PROG UART
SD MICRO
MIC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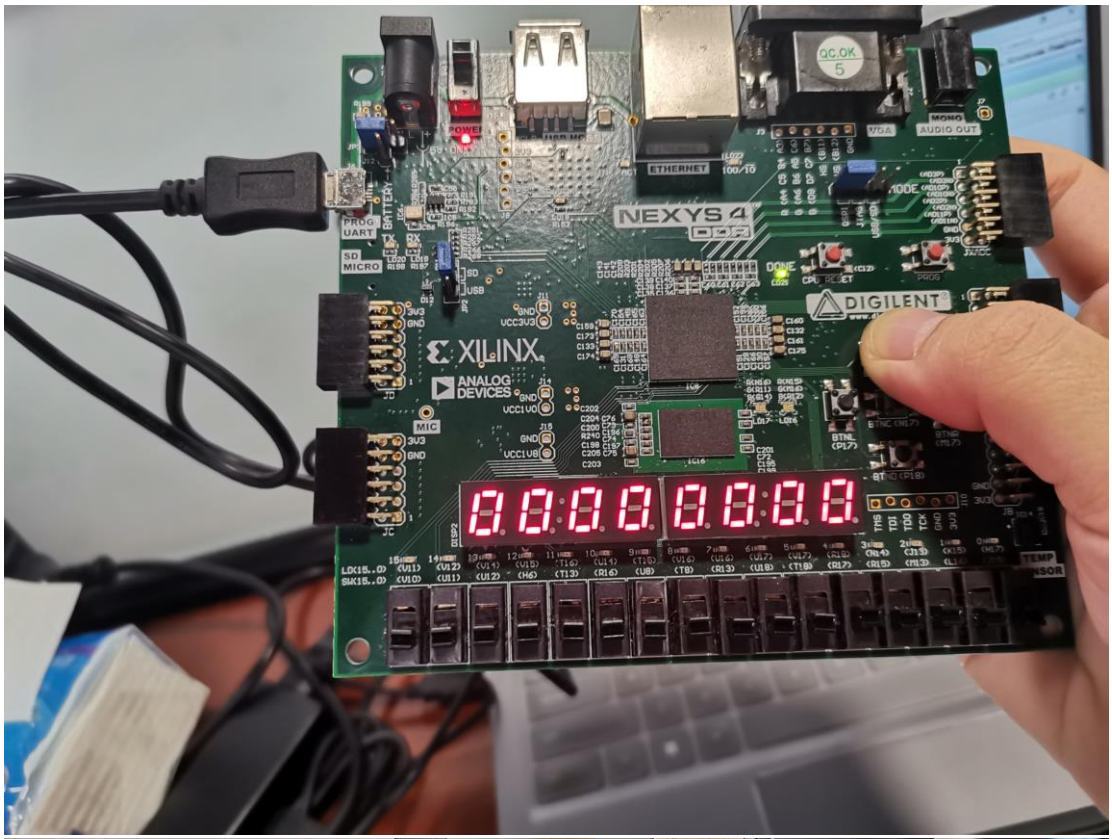
ETHERNET
VGA
AUDIO OUT
PROG UART
SD MICRO
MIC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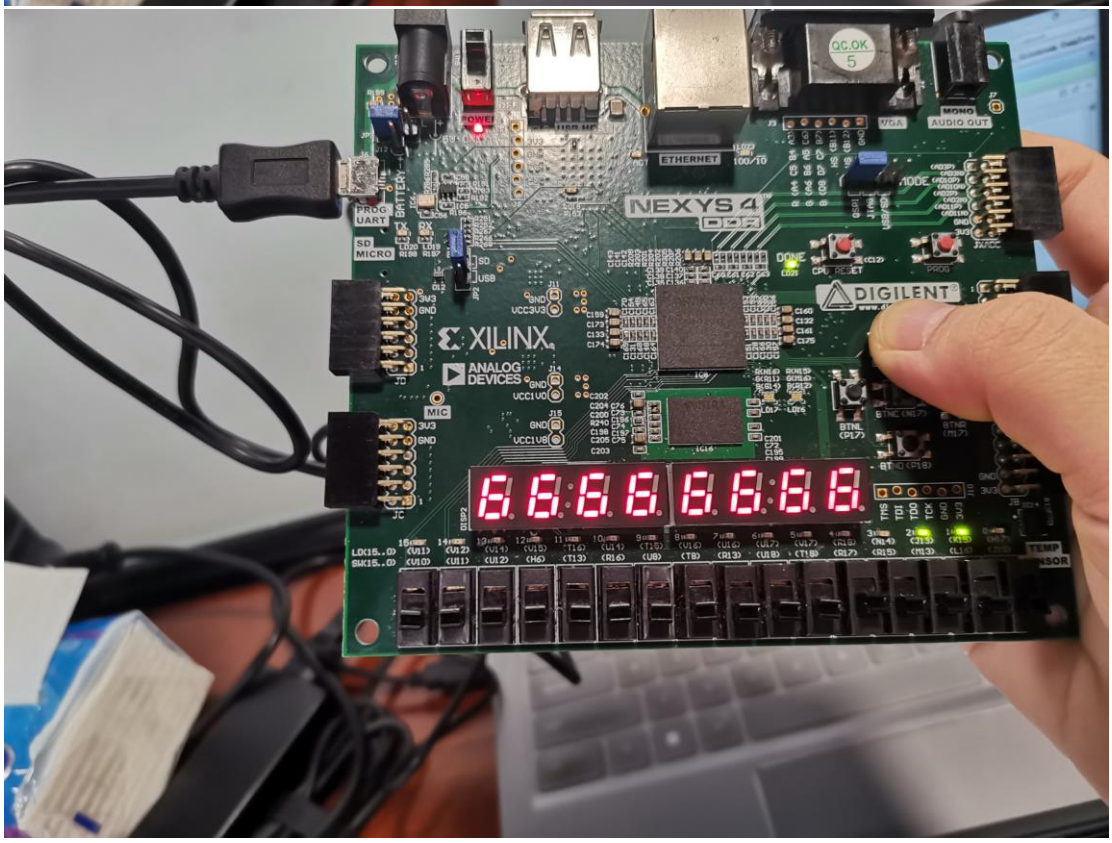
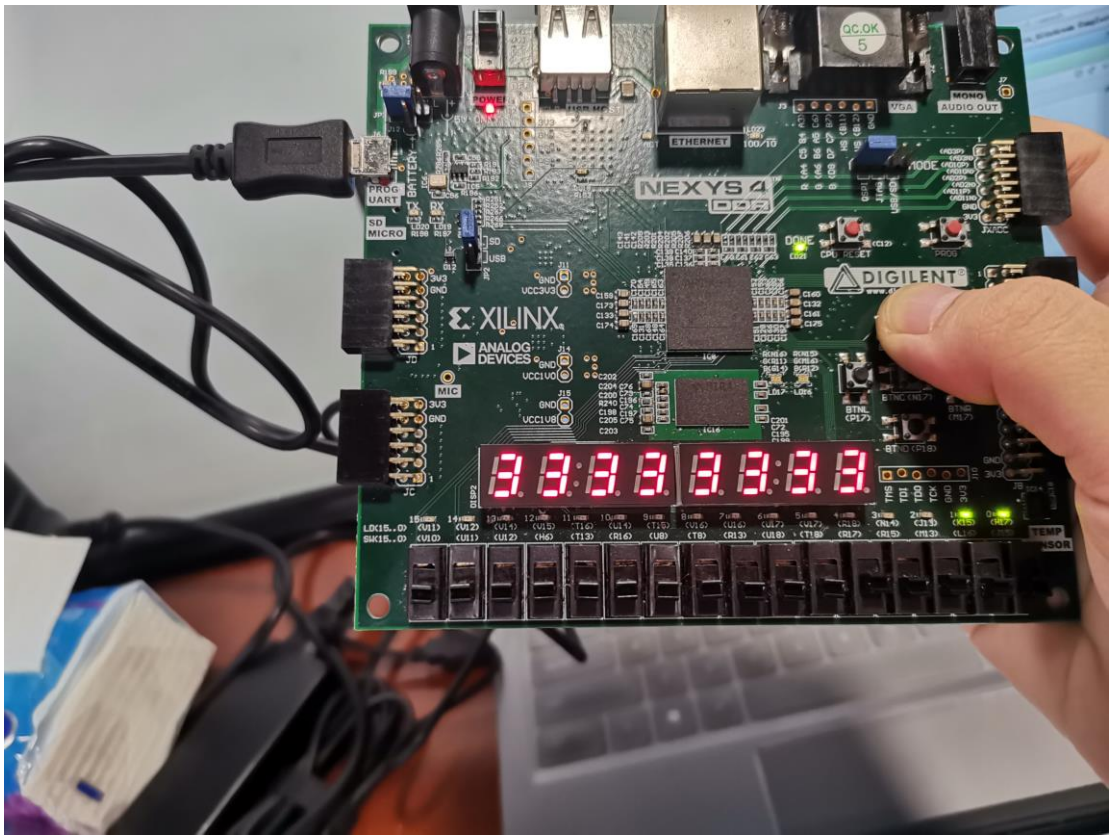
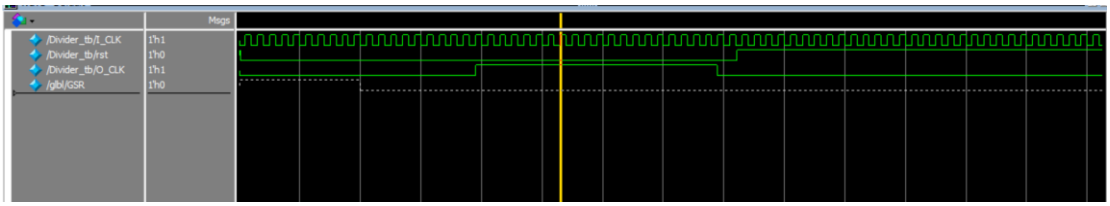
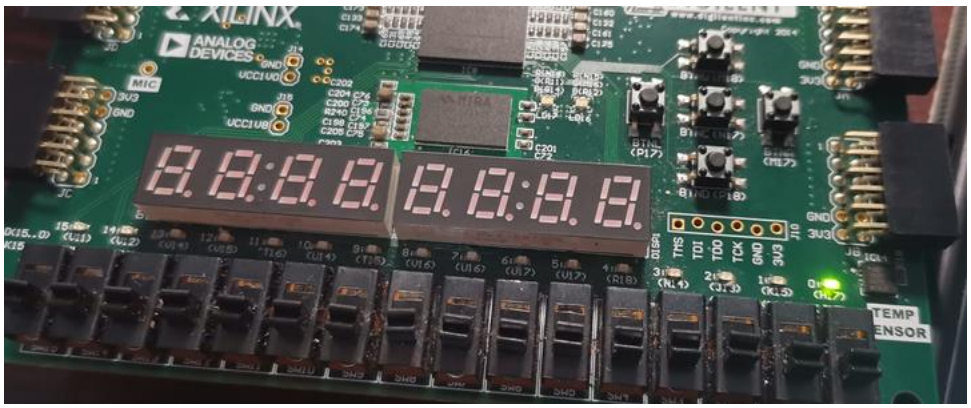
DDR
XILINX
ANALOG DEVICES
DIGILENT
ETHERNET
AUDIO OUT
QC.OK
5

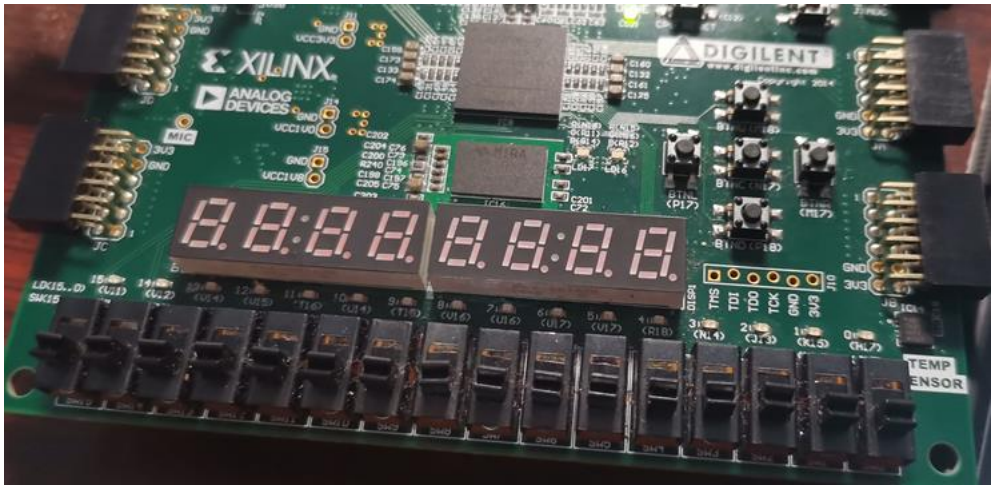

NEXYS 4
DDR
XILINX
ANALOG DEVICES
DIGILENT
ETHERNET
AUDIO OUT
QC.OK
5

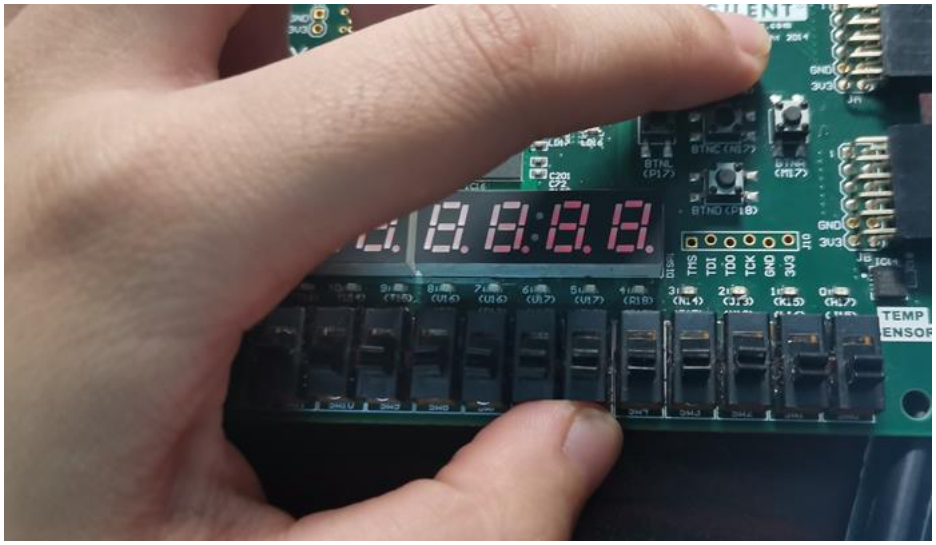

NEXYS 4
DDR
XILINX
ANALOG DEVICES
DIGILENT
ETHERNET
VGA
MONO AUDIO OUT
PROG UART
SD MICRO
MIC
TEMP SENSOR

6.7_2


Msgs
/Divider_tb/I_CLK
/Divider_tb/rst
/Divider_tb/O_CLK
/glbl/GSR


XILINX
ANALOG DEVICES
MIC
TEMP SENSOR


XILINX
ANALOG DEVICES
DIGILENT
MIC
TEMP SENSOR


TEMP SENSOR