同济大学计算机系

数字逻辑课程实验报告

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一、实验内容

在本次实验中，我们将练习使用 Verilog HDL 语言，并采用三种不同的描述方式设 计基本门电路，实现数据扩展。

6.1_1---6.1_3: 基本门电路实验

a） 结构型描述

b） 数据流型描述

c） 行为描述

6.1_4: 三态门实验

6.1_5: 数据扩展实验

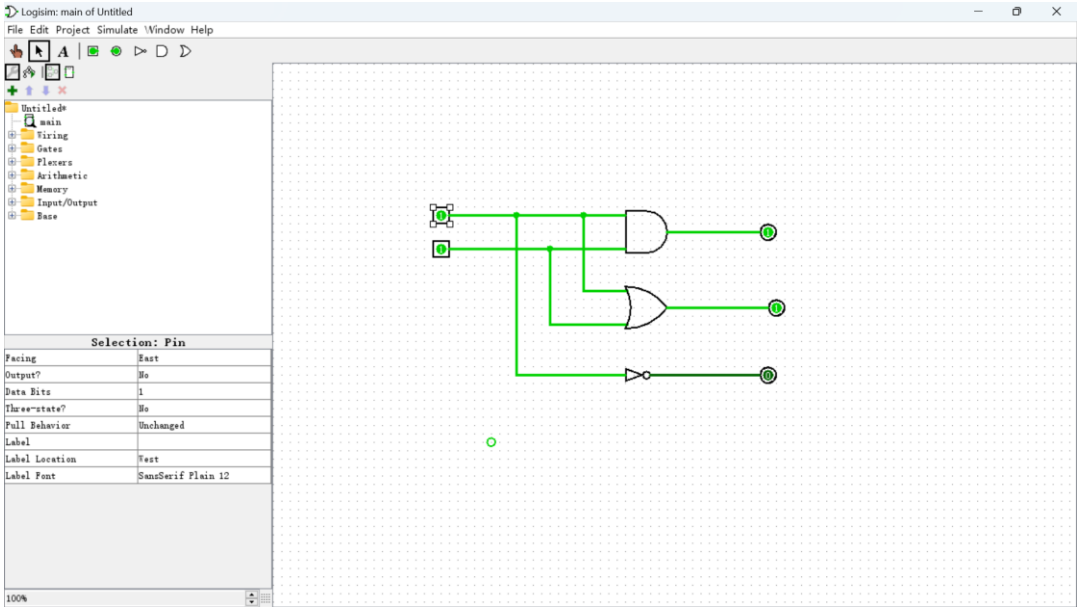
二、硬件逻辑图

（实验步骤中要求用 logisim 画图的实验，在该部分给出 logisim 原理图，否则该部分在实验报告中不用写）

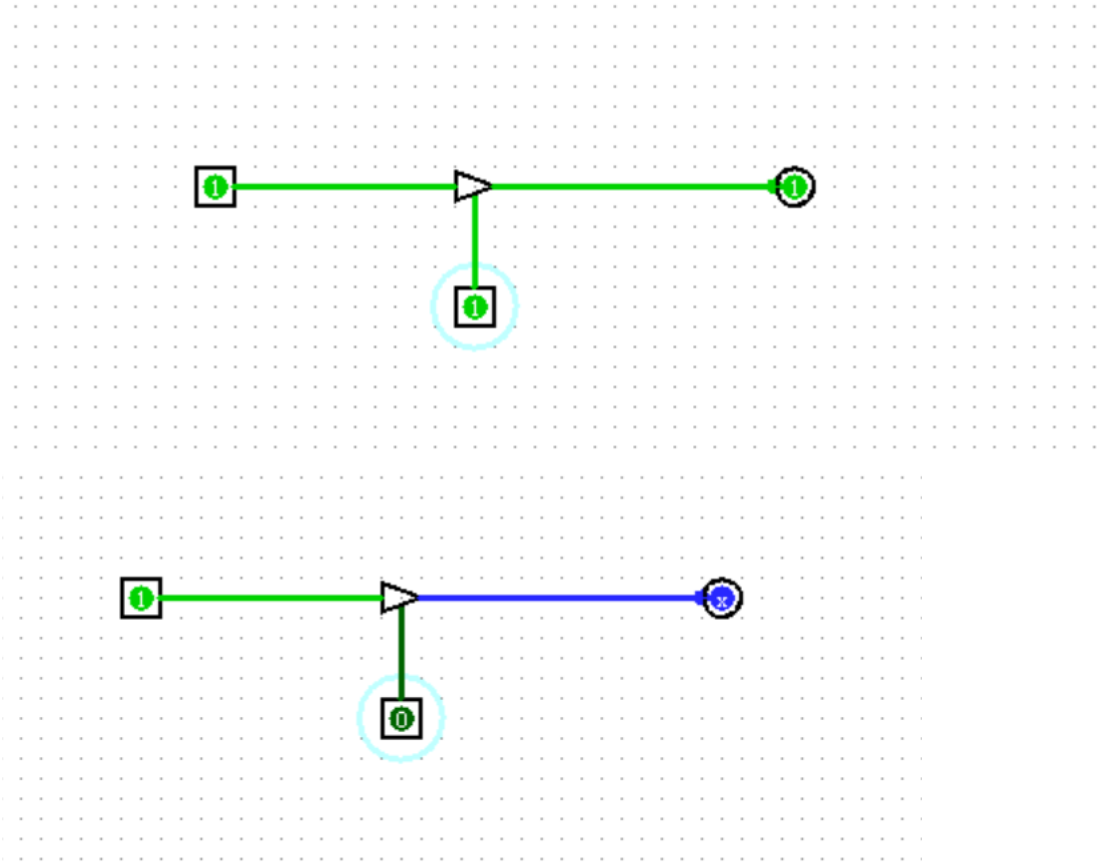
三、模块建模

（该部分要求对实验中建模的所有模块进行功能描述，并列出各模块建模的 verilog 代码）

6.1_1-----6.1_3



6.1_4



四、测试模块建模

（要求列写各建模模块的 test bench 模块代码）

6.1_1---6.1_3

```
`timescale 1ns / 1ns
module logic_gates_tb();
        reg iA;
        reg iB;
        wire oAnd;
        wire oOr;
        wire oNot;

        initial
        begin
           iA=0;
           # 40 iA=1;
           # 40 iA=0;
           # 40 iA=1;
           # 40 iA=0;
        end
```

```
        initial
        begin
           iB=0;
           # 40 iB=0;
           # 40 iB=1;
           # 40 iB=1;
           # 40 iB=0;
        end
        logic_gates_1
        logic_gates_inst(
              .iA(iA),
              .iB(iB),
              .oAnd(oAnd),
              .oOr(oOr),
              .oNot(oNot)
              );
Endmodule
```

6.1_4

```
`timescale 1ns / 1ps
module three_state_gates_tb;
  reg iA;
  reg iEna;
  wire oTriState;
three_state_gates uut (
.iA(iA),
.iEna(iEna),
.oTri(oTriState)
);
initial
begin
iA = 0;
#40 iA = 1;
  #40 iA = 0;
  #40 iA = 1;
end
initial
begin
  iEna = 1;
  #20 iEna = 0;
  #40 iEna= 1;
  #20 iEna = 0;
end
endmodule
```

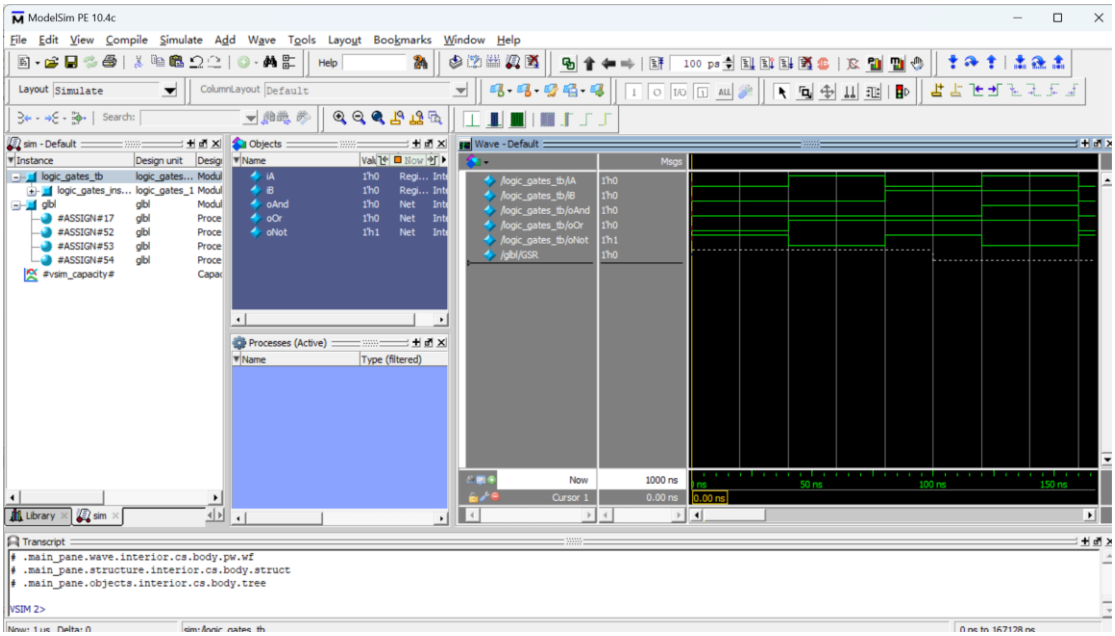
6.1_5

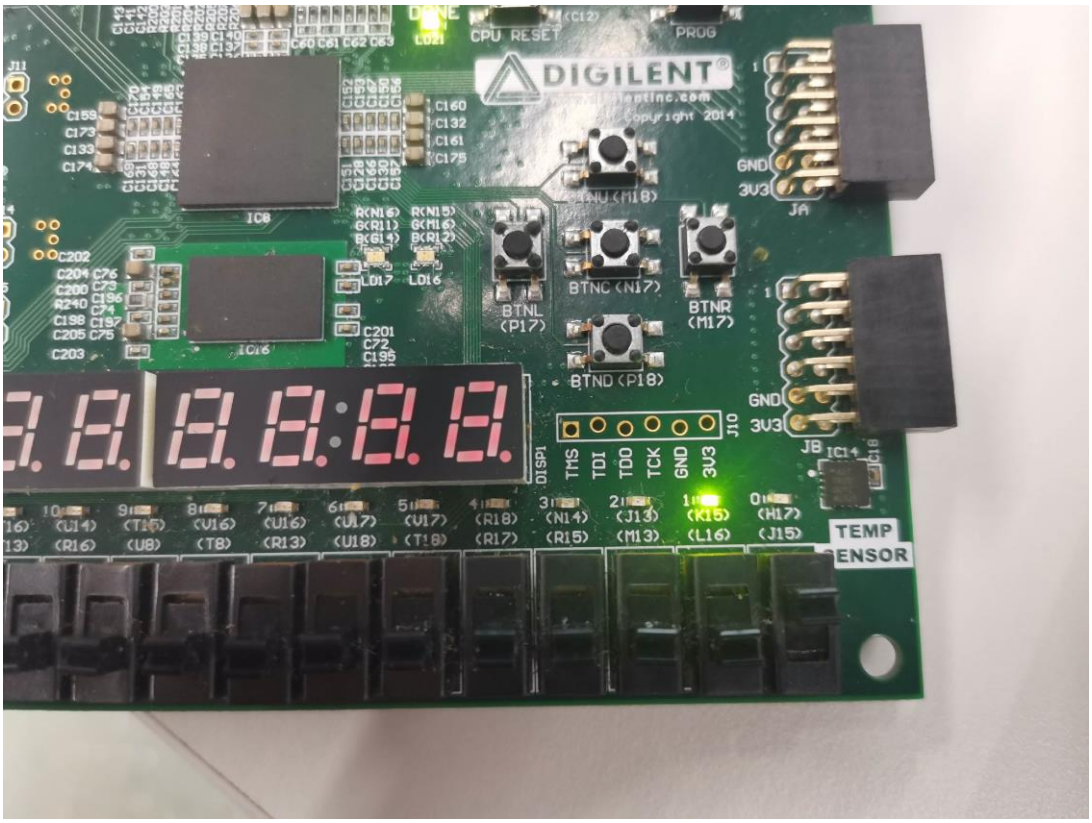
```
`timescale 1ns / 1ps
module extend_tb;
reg [15:0] a;
  reg sext;
wire [31:0] b;
// Instantiate the Unit Under Test (UUT)
extend uut (.a(a),.sext(sext),.b(b));
initial
begin
// Initialize Inputs
a = 0;
sext = 0;
// Wait 100 ns for global reset to finish
#100;
// Add stimulus here
sext = 1;
a = 16'h0000;
#100;
sext = 0;
a = 16'h8000;
#100;
sext = 1;
a = 16'h8000;
#100;
sext = 0;
a = 16'hffff;
#100;
sext = 1;
a = 16'hffff;
#100;
end
endmodule
```

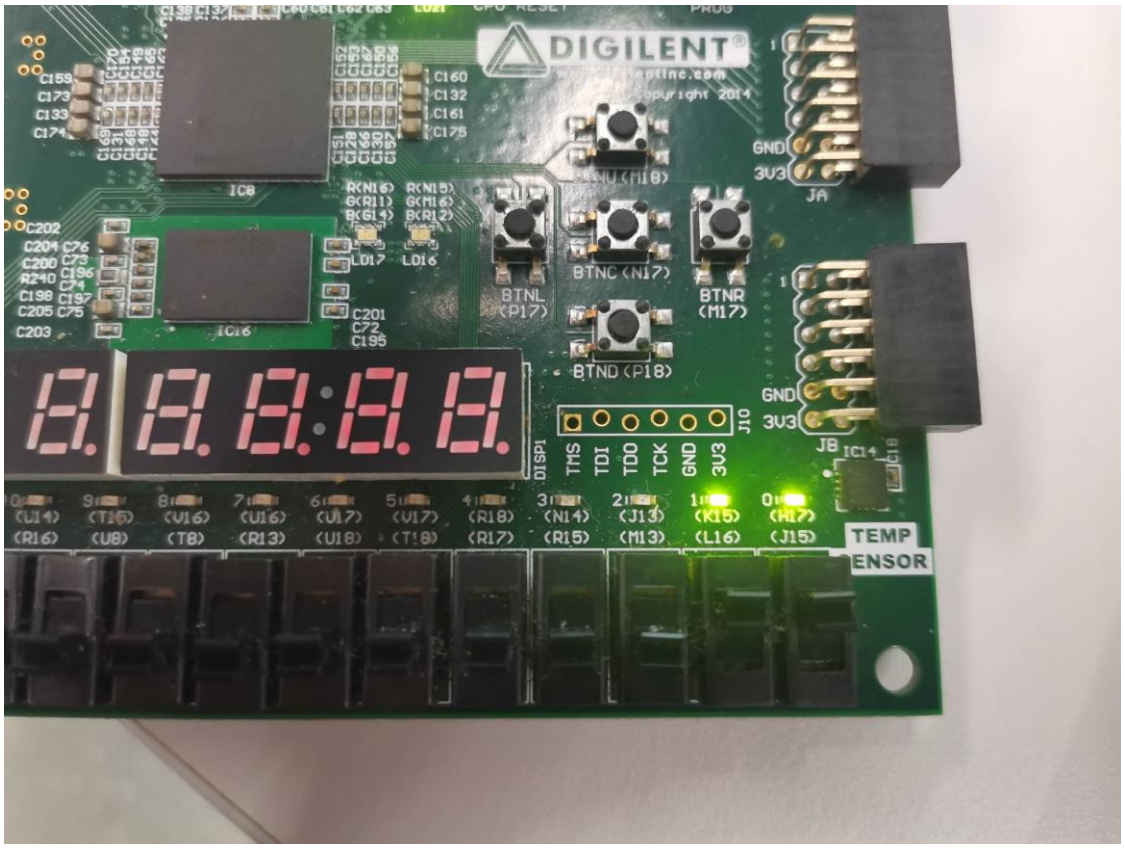
五、实验结果

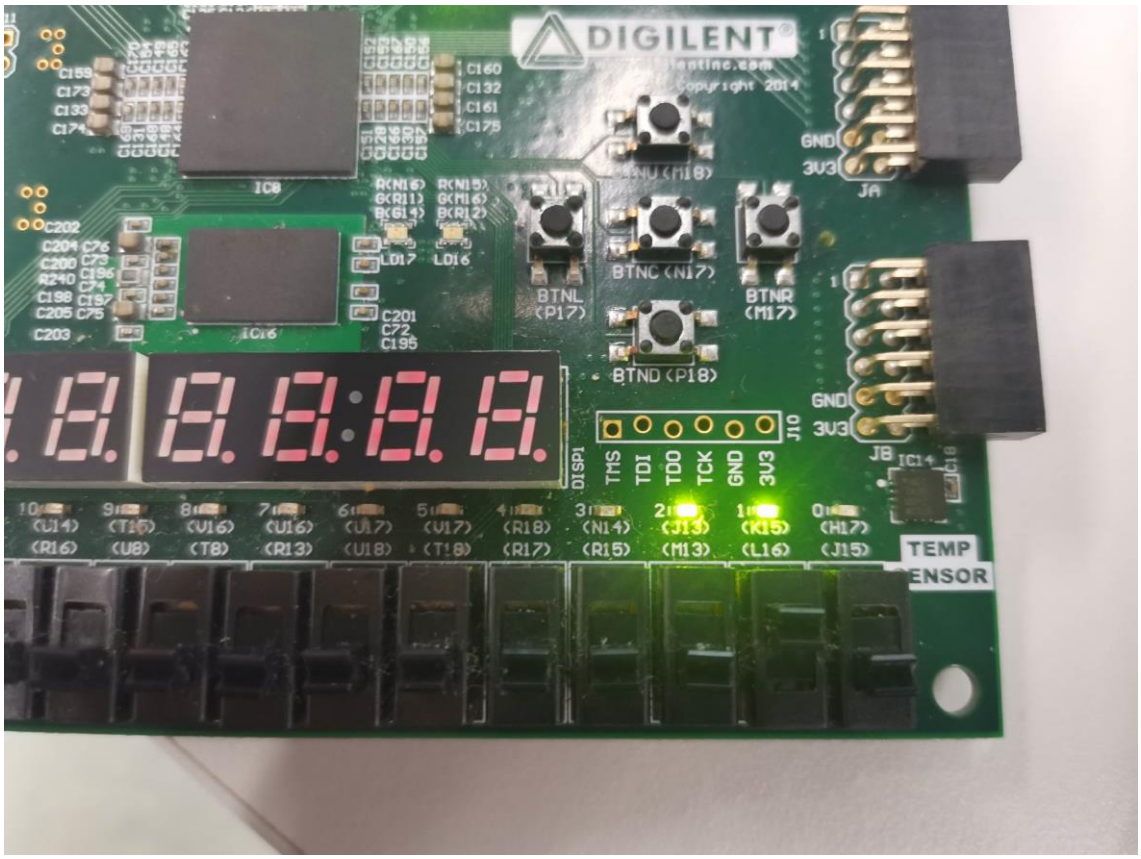
（该部分可截图说明，要求 logisim 逻辑验证图、modelsim 仿真波形图、以及下板后的实验结果贴图（实验步骤中没有下板要求的实验，不需要下板贴图））

6.1_1

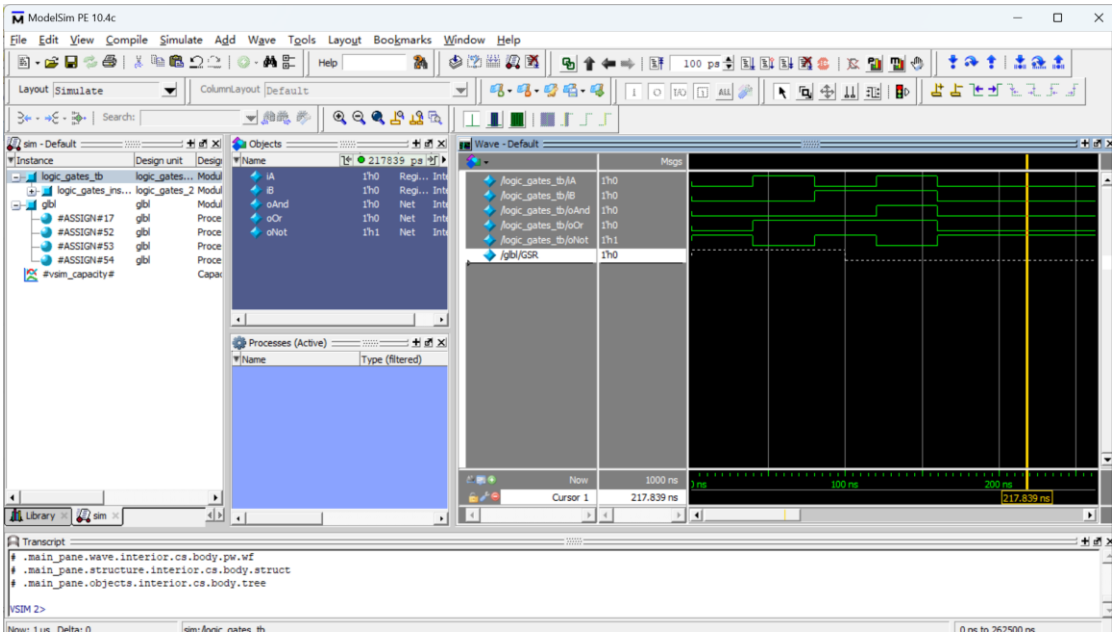

ModelSim PE 10.4c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>


DIGILENT
CPU RESET
PROG
BTNU (M18)
BTNL (P17)
BTNC (N17)
BTNR (M17)
BTND (P18)
JA
JB
GND
3V3
TEMP SENSOR


DIGILENT
BTNL (P17)
BTNC (N17)
BTNR (M17)
BTND (P18)
JA
JB
TEMP
ENSOR

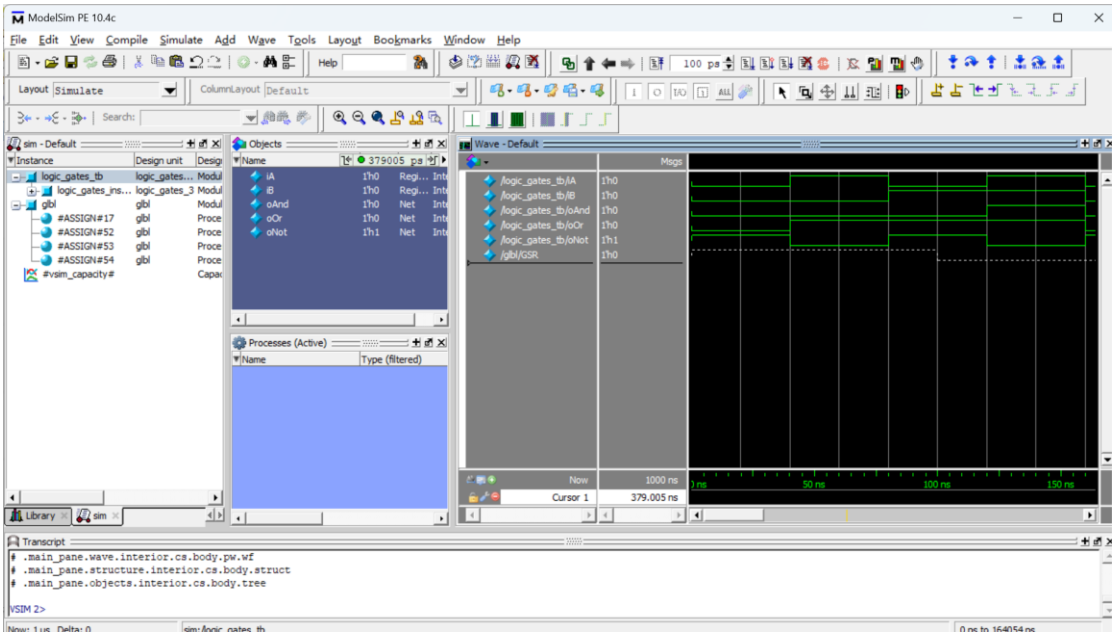

DIGILENT
BTNL (P17)
BTNC (N17)
BTNR (M17)
BTND (P18)
JA
JB
TEMP
ENSOR

6.1_2


ModelSim PE 10.4c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>

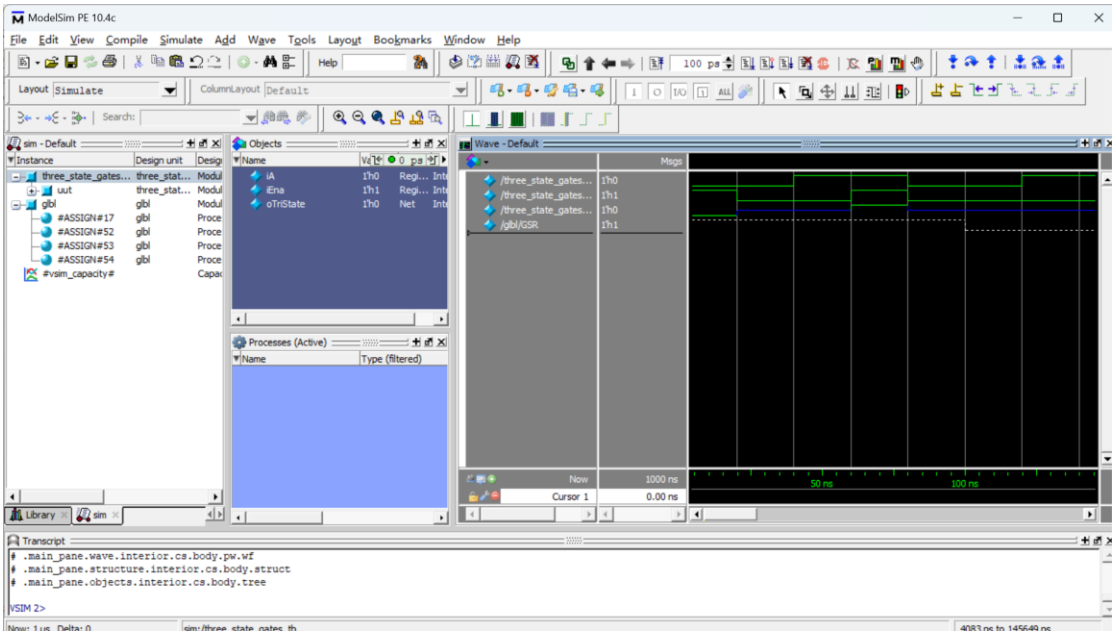
同上

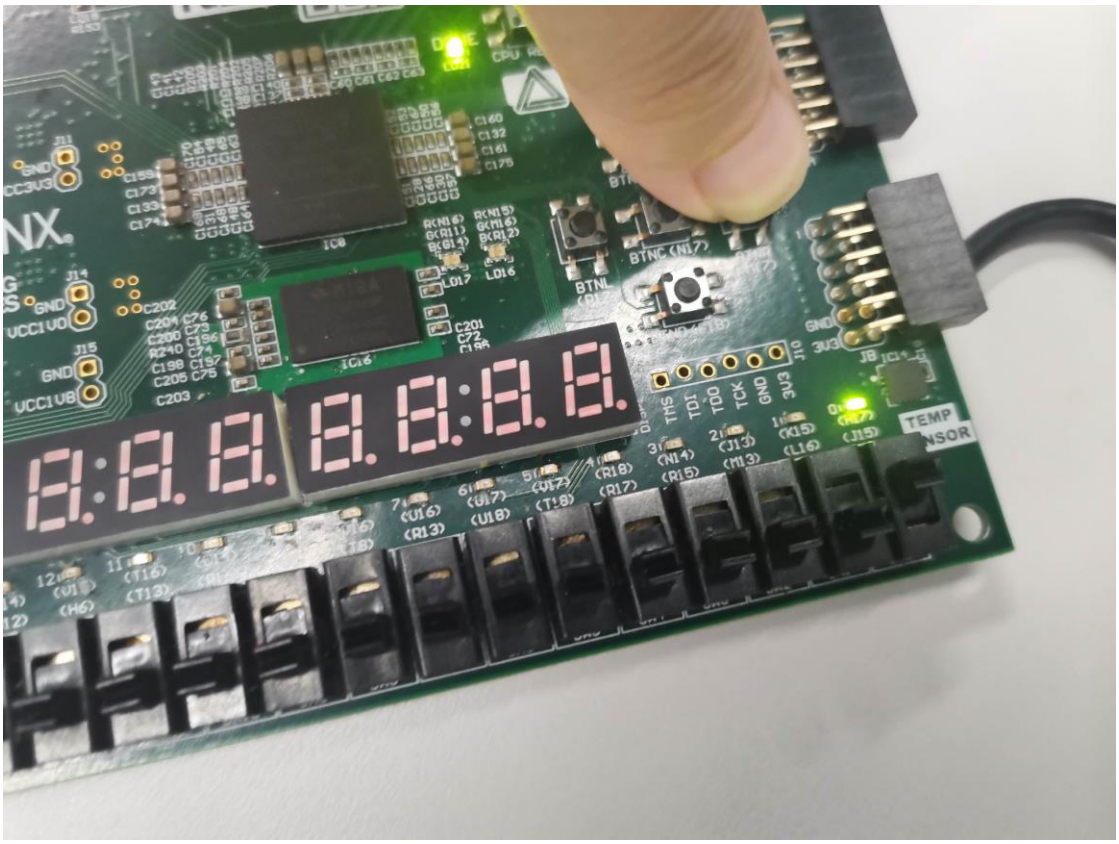
6.1_3

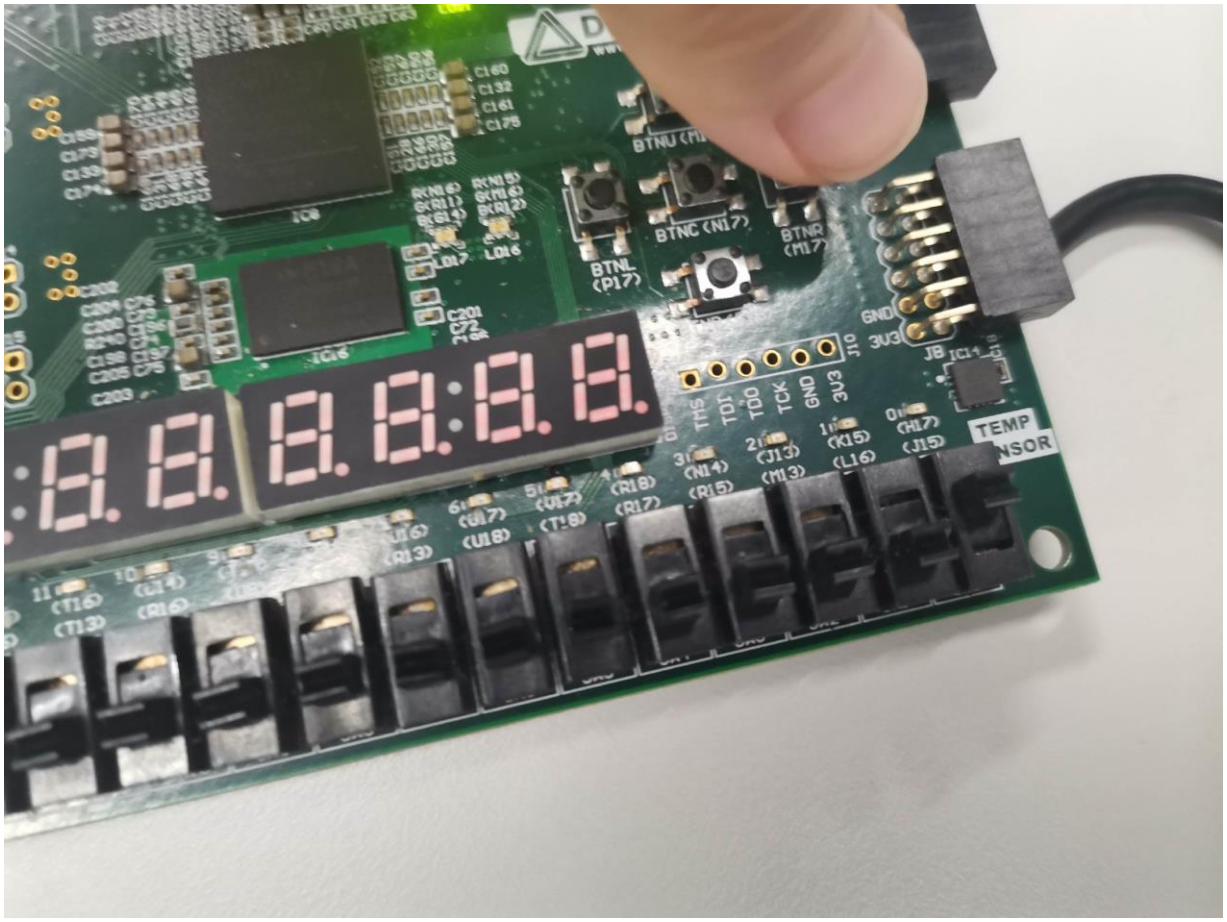

ModelSim PE 10.4c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>

同 1

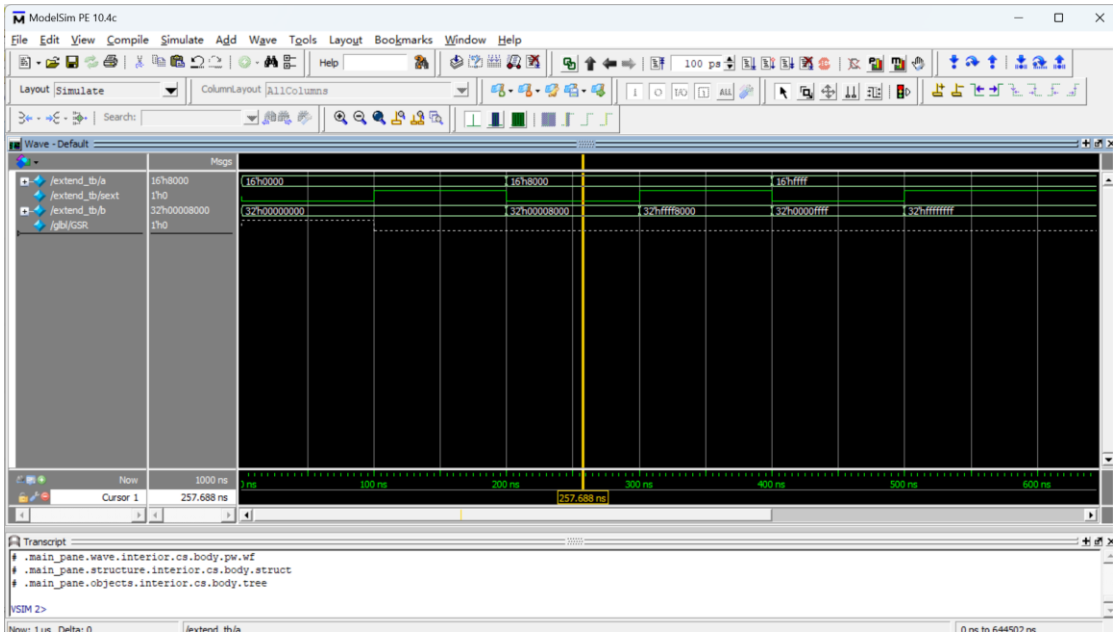
6.1_4


ModelSim PE 10.4c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Objects
Wave - Default
Processes (Active)
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>


TEMP
NSOR


BTNC (N17)
BTNL (P17)
TEMP
NSOR

6.1-5


ModelSim PE 10.4c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
/extend_tb/a
/extend_tb/sext
/extend_tb/b
/glbl/GSR
16'h8000
1'h0
32'h00008000
1'h0
16'h0000
16'h8000
16'hffff
32'h00000000
32'h00008000
32'hffff8000
32'h0000ffff
32'hffffffff
Now
1000 ns
Cursor 1
257.688 ns
Transcript
.main_pane.wave.interior.cs.body.pw.wf
.main_pane.structure.interior.cs.body.struct
.main_pane.objects.interior.cs.body.tree
VSIM 2>