Example Questions

—Computer Architecture (Part 1)

1. Describe the four basic functions of a computer.

2. From the perspectives of top-level structure, what are the four basic types of components? Which type does the mouse, monitor, cache memory, and the bus system belong to, respectively?

3. The 2nd generation computer adopts transistor as the basic elements to replace vacuum tubes. What are the advantages of this improvement?

4. Describe the key concepts of the Moore's law.

5. What are the advantages of increasing density of transistors in a chip?

6. For the following expression of a positional numbering system, how to calculate its decimal values?

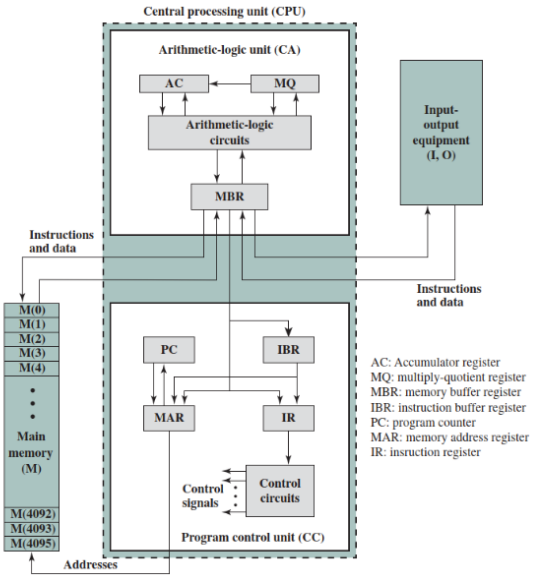
   Expression: $(a\ b\ c\ d.\ e\ f\ g\ h)_r$

7. Which one of the following expressions is NOT correct for positional numbering systems?
   (a) $(35243)_5$ (b) $(3333)_4$ (c) $(121212)_3$ (d) $(010.101)_9$ (e) $(9830)_{11}$

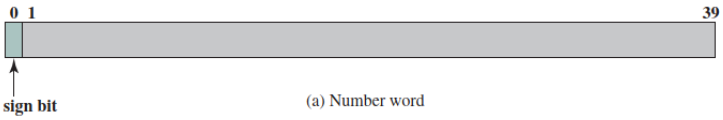
8. What is the binary expression of the hexadecimal '0xA134E5F'? And what is the hexadecimal expression of the binary format '0b101010100'?

9. According to the positional numbering system, what is the binary expression of the decimal 247? What is the binary expression of the decimal 0.250 (calculate up to 4 digits if not possible to get an accurate expression)? What is the binary expression of the decimal 247.250?

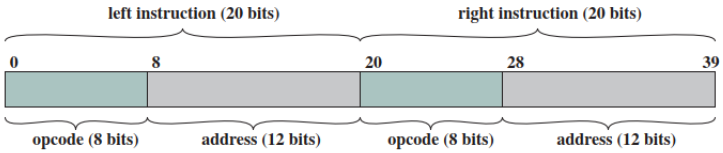
10. For IAS computer, describe the functionalities of registers, including AC, MQ, MBR, PC, MAR, IBR, and IR.



11. The memory format of IAS computer is given as the following. What is the maximum number of memory words that can be handled theoretically? How is this the maximum capacity obtained?



(a) Number word



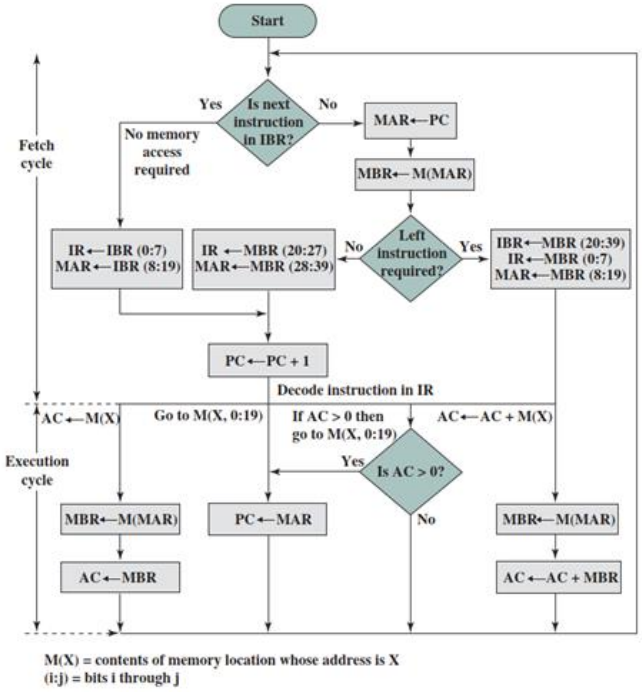
(b) Instruction word

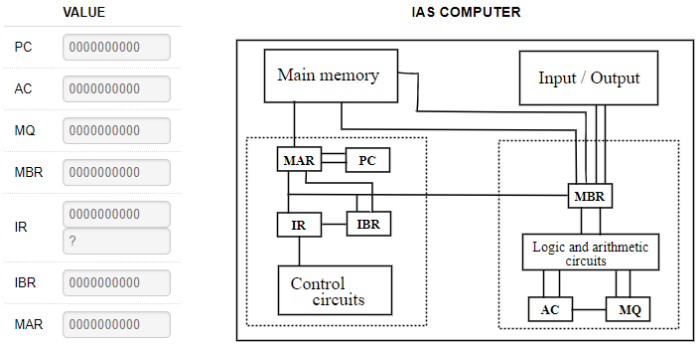
12. For an IAS computer, data A, B, C are stored in memories 0x11 (X_a)~0x13 (X_c), write a program to calculate the sum Z=A+B+C and store it in Memory unit 0x14 (X_z), given the instruction set. How does it look like after the program and data are stored starting from the memory word addressed by 0x000?

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD –M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD –|M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position
	00010101	RSH	Divide accumulator by 2; that is, shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

13. Given the operation flow chart of the IAS computer, briefly descript how the IAS computer works. For the given stored program and the initialization value of registers, what will be the values of registers after the first instruction cycle?

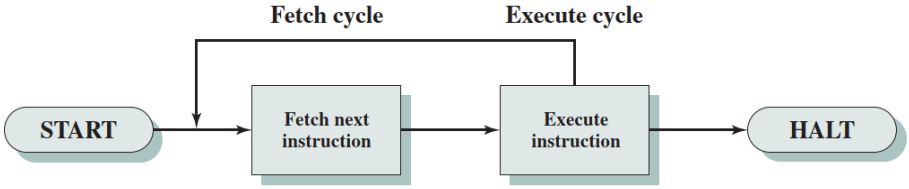
Stored program
000 01 011 05 012
001 05 013 21 014
011 00 000 00 001
012 00 000 00 002
013 00 000 00 003



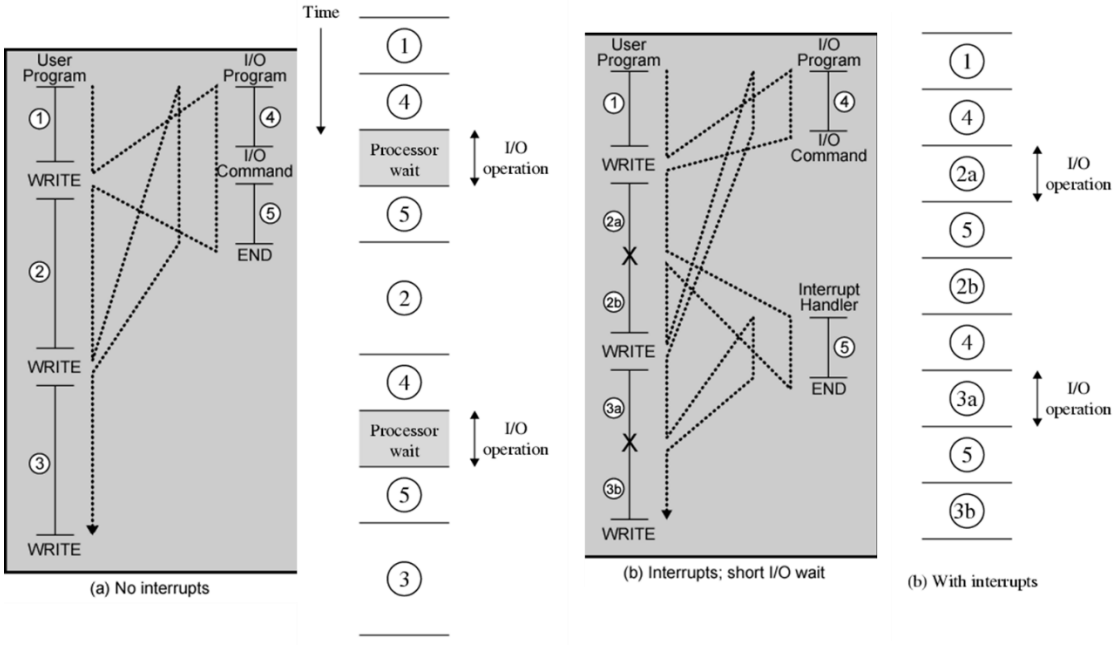


14. As we know, everything that can be done in software can theoretically be implemented with hardwired system as well. Then, what are the advantages of software programming compared to hardwired systems?

15. Given the following chart of instruction cycle, how will it be changed after introducing the interrupt scheme?

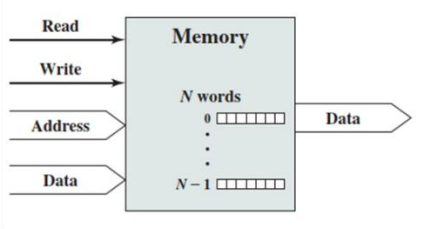


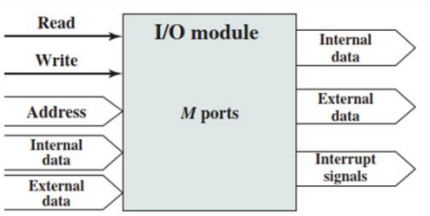
16. Based on the following graph of interacting with I/O with and without the support of interrupt scheme, analyze how interrupt scheme helps to improve the performance of a computer?

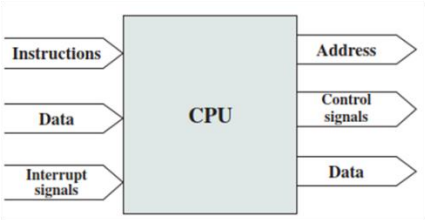


17. Describe the solutions that can be used to support multiple interrupts in a computer.

18. Describe/Draw the interconnect model for I/O, processor, and memory, respectively.
    Answer:







19. What is the bus system used for inside a computer? What are the basic lines inside a bus system? Describe the functionalities of each type of lines inside a bus. With a bus system, what if more than one device sends data at the same time?

20. What are the problems of using a single bus in nowadays' computer? And how to solve these problems?

21. What are the advantages of using point-to-point interconnections inside a computer? List two examples of commonly used point-to-point interconnections and describe what are they used for.

22. With the development of computer technologies, the processor speed has increased significantly. What is the potential problem behind the significant increase in the processor speed with the consideration of the other components inside a computer, such as the memory? How does this change the performance design of a computer?

23. What is the problem to increase of clock speed or components density of a CPU core? Which technology is adopted to further improve the computational power of nowadays processors?
    Answer: Physical obstacles are met. Multicore

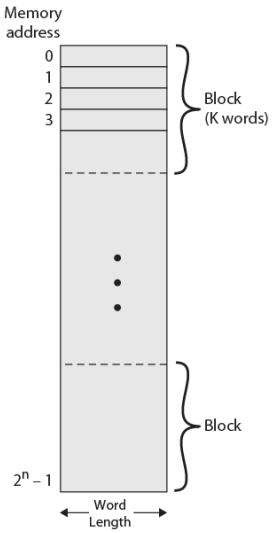
24. What are the drawbacks to use clock speed, MIPS, or CPI to evaluate the performance of a computer? Nowadays, how is the computer performance evaluated and compared among different models?

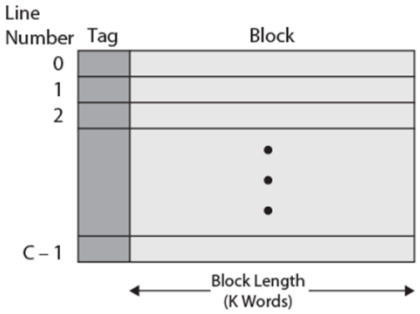
25. For the following memories, rank them in the order of reduced speed:
    Cache memory, registers, SSH, HDD, main memory, remote disk

26. What is cache memory used for? How does the cache memory help to improve the computer performance?

27. What does the principle of locality say? How is the principle of locality related to the cache memory operation?

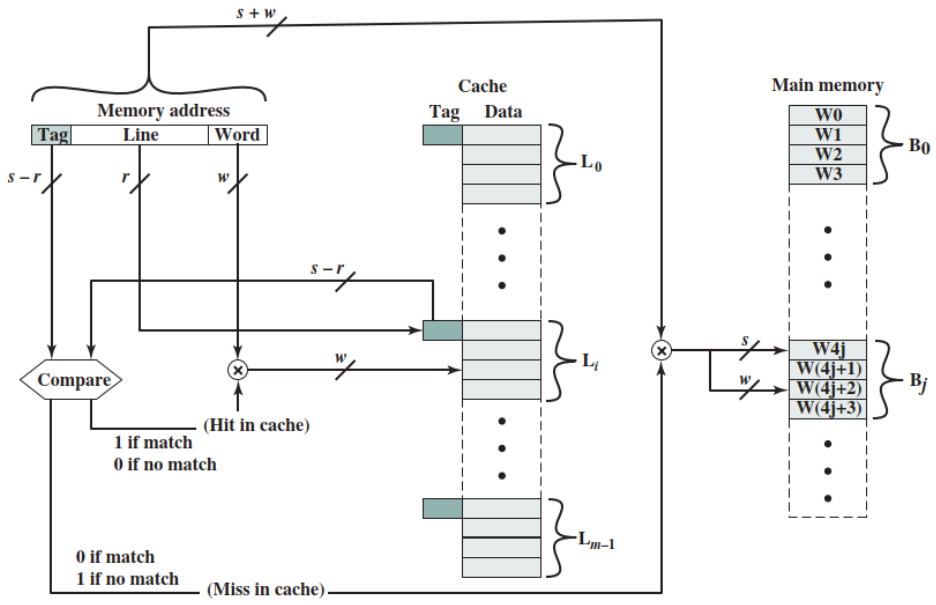
28. For the given graph as the following,
    (1) Describe the structures of main memory and cache memory.
    (2) Assuming each block consists of 4 words and each word has 1 byte length, for a main memory of 256 kB and a cache memory of 8 kB, determine parameters K, n, and C. (1k = 1024=2^10, 256 = 2^8, 8=2^3)
    (3) For the main memory and cache memory in (2), determine the address structure for direct mapping and explain how the tag in cache memory is designed.





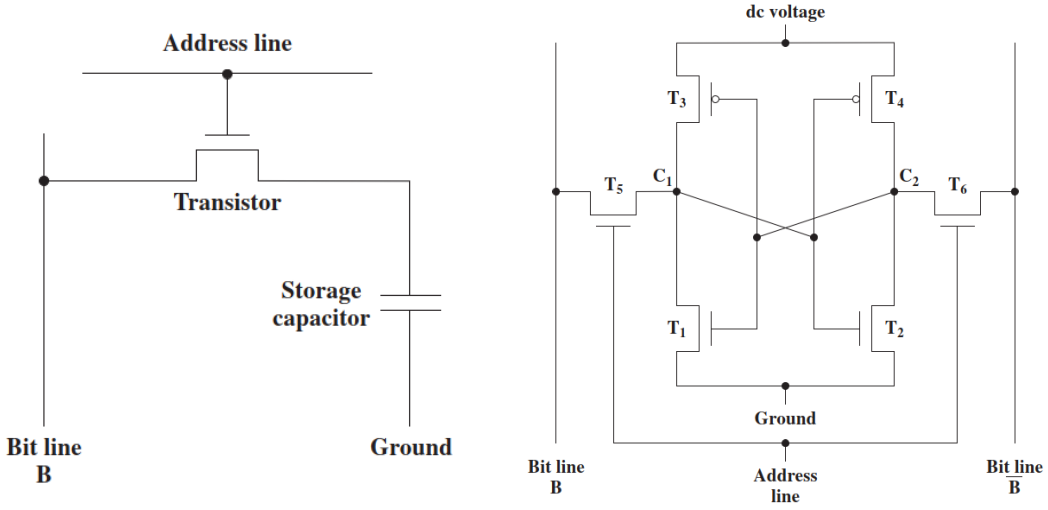
Main memory Cache memory

29. The following graph shows the memory visiting process with direct mapping function, describe how it works.

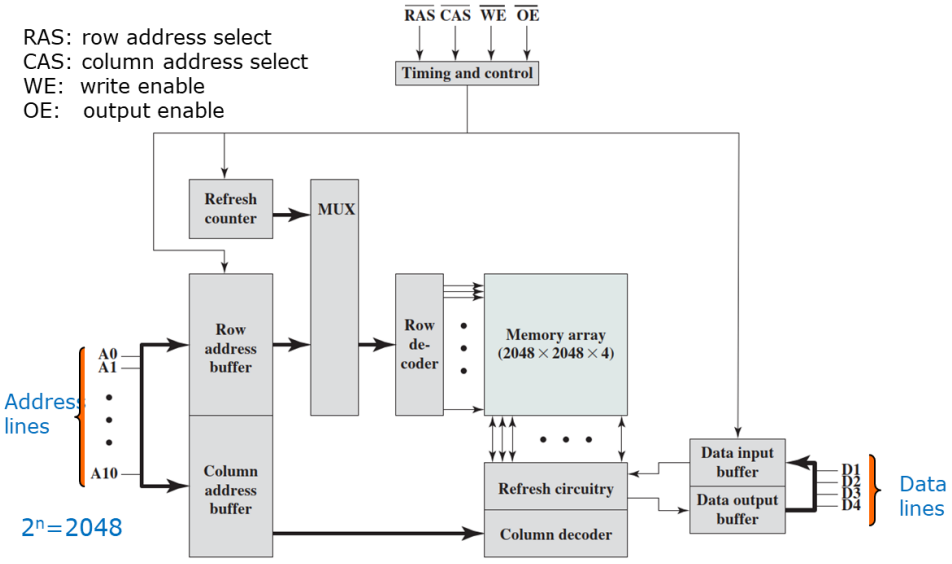


30. What are the differences among direct mapping, set associative mapping, and fully associative mapping? And what are the advantages and disadvantages of direct mapping compared to the other two?

31. Analyze the two circuits for DRAM and SRAM cell, describe:
    (1) What states are used to represent '0' and '1' in DRAM and SRAM, represented?
    (2) What are the advantages and disadvantages of DRAM compared to SRAM?
    (3) Which one is commonly used for main memory, and which one is used for cache memory?

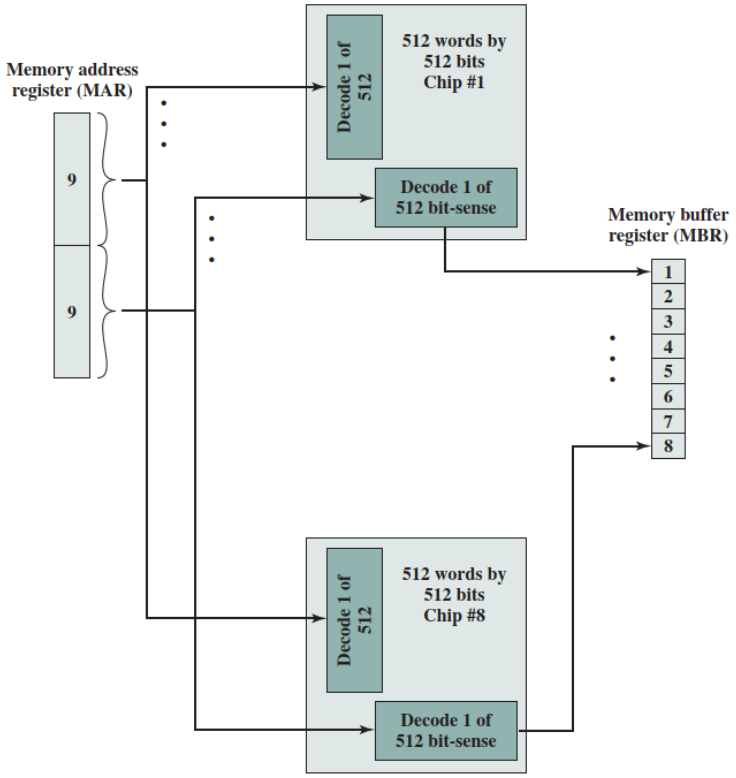


32. For the following circuit, assuming we are reading 4 bits stored in Row 0x000, Column 0x7FF, how should we set the control signals and address lines?

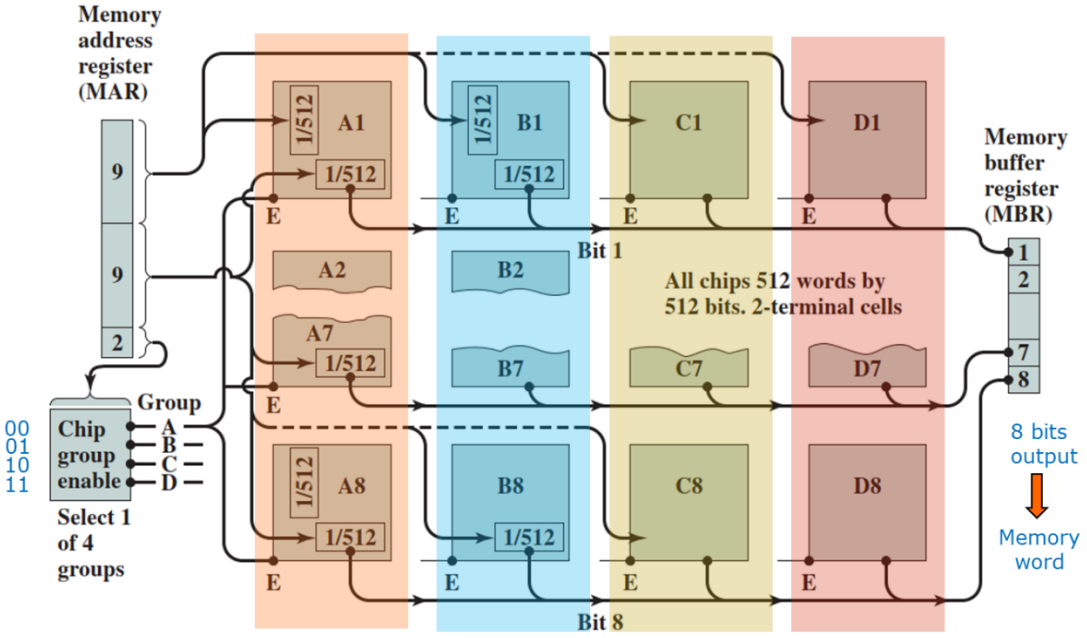


33. Referring to the following circuit of memory organization, design a new circuit with 16-bit output using the same memory module with 512 X 512 bits. For the new circuit, how many bits should be used for row and column addressing?

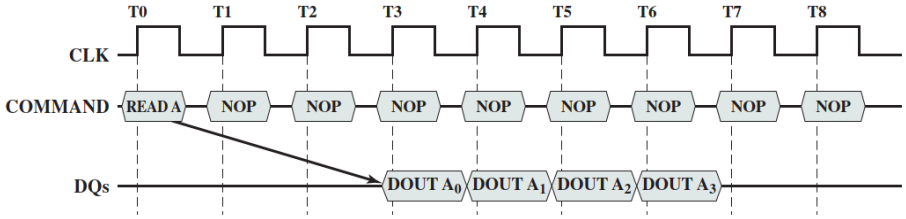
Answer: double the number of modules, 9-bit row addressing, 9-bit column addressing.



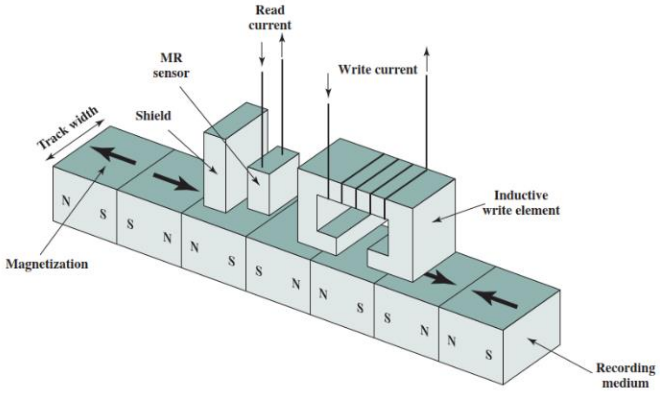
34. For the following circuits of memory organization, describe how are the first four memory (0x00000 – 0x00003) units stored (you can mark them on the graph).



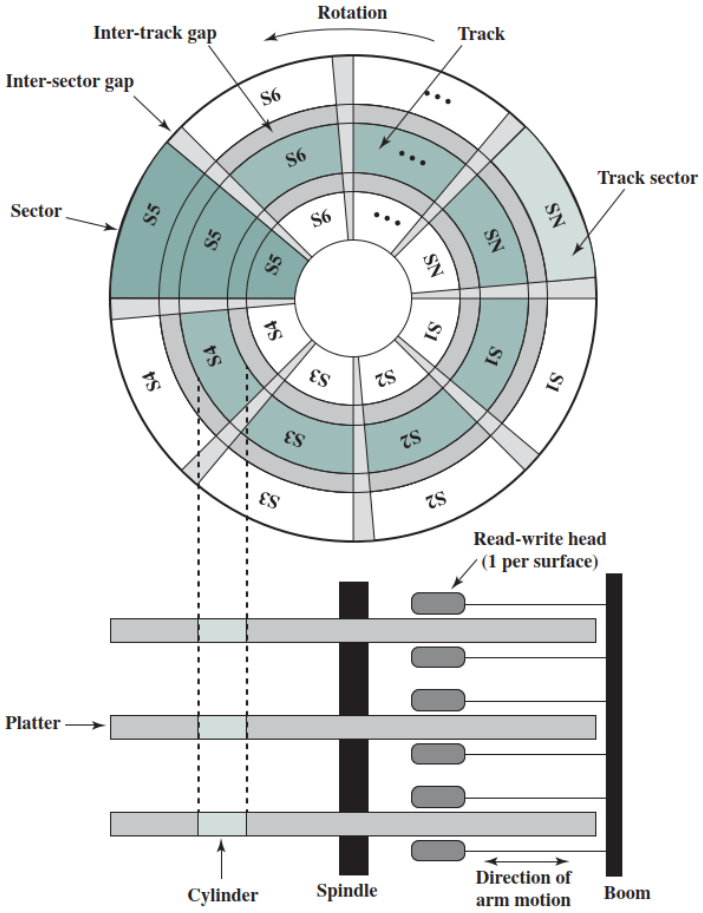
35. With the following graph of SDRAM, describe the advantages of SDRAM to use a synchronized clock for memory access. And what technology is used to double the data rate of SDRAM to have a DDR memory?



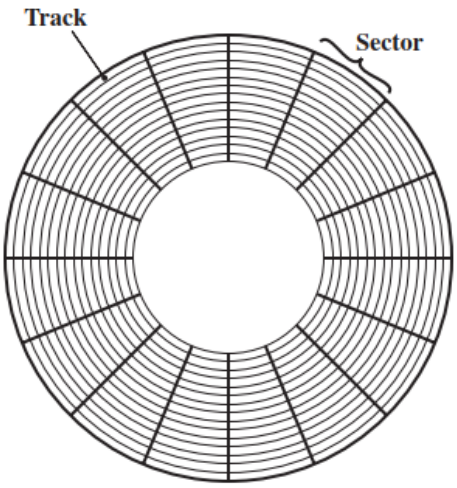
36. With the following graph, describe the process to store and retrieve data from the hard-disk drive (HDD).



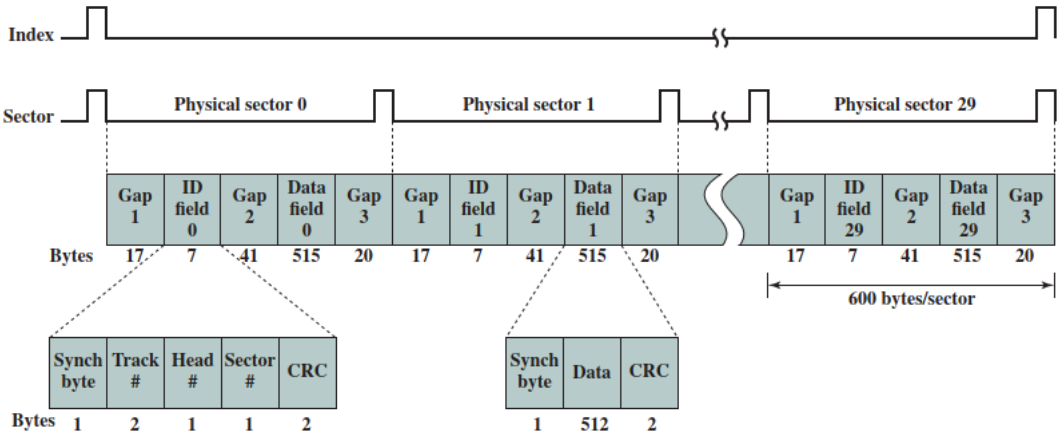
37. Referring to the following graph, describe the mechanical structure of hard-disk drive and explain how the data are organized on the surface of the plate.



38. What is the drawback of using constant angular velocity (CAV) for data reading and recording on a hard-disk drive (HDD) as shown in the following figure? And what is the technic to solve this problem?



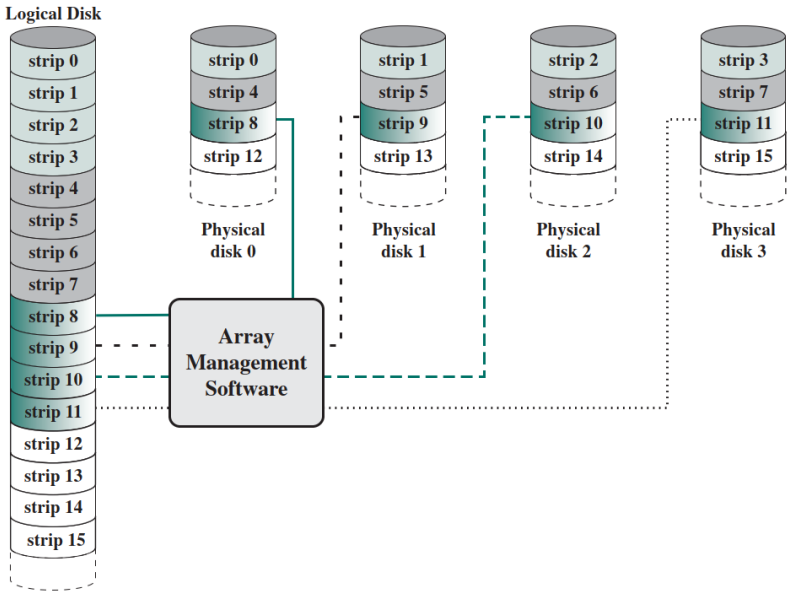
39. The following figure shows the data recording format on Winchester Disk ST506, describe how the data are organized on a sector and the functions of each field.



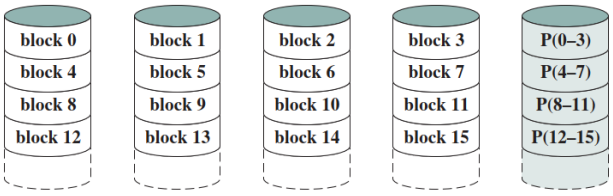
40. Assuming a disk with an advertised average seek time of 4 ms, a constant rotation speed as 250 rps, and 500 sectors per track with each sector stores 512 bytes, calculate the average access time, Ta.

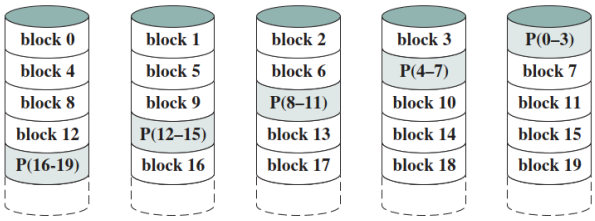
41. If we plan to record 5 tracks of data on a hard-drive disk (HDD), how to organize the storage position such that the overall access time can be minimized?

42. What is the advantage of the following data mapping for RAID 0?



43. For RAID 4 and RAID 5 as shown in the following graphs, analyze which one is more suitable for network servers? Why?





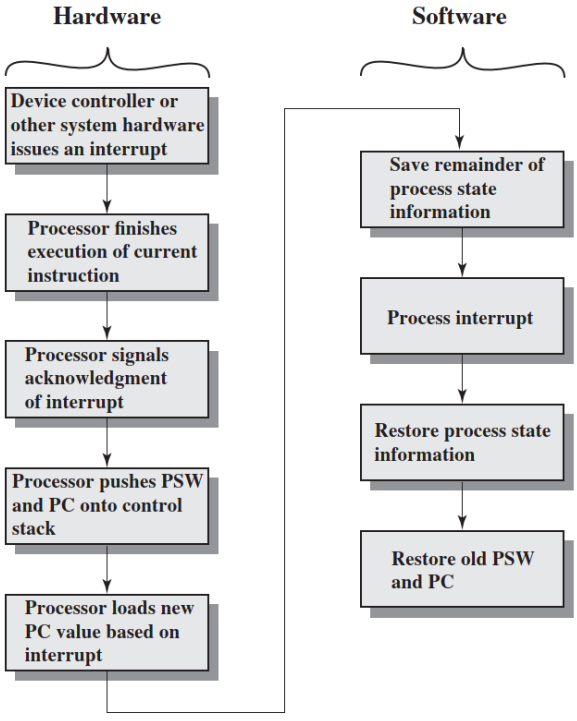
44. Which one of the following descriptions about Solid-State Disk (SSD) is NOT correct?
    (a) SSD tends to slow down as the device is used.
    (b) It is possible to update a single page in SSD without touching the other pages within the same block.
    (c) Defragmentation can be used to improve the performance of SSD
    (d) SSD is faster than HDD for data read and write

45. Which one of the following is not I/O?
    (a) Bluetooth (b) Keyboard (c) Touch pad (d) RAM (e) PCI

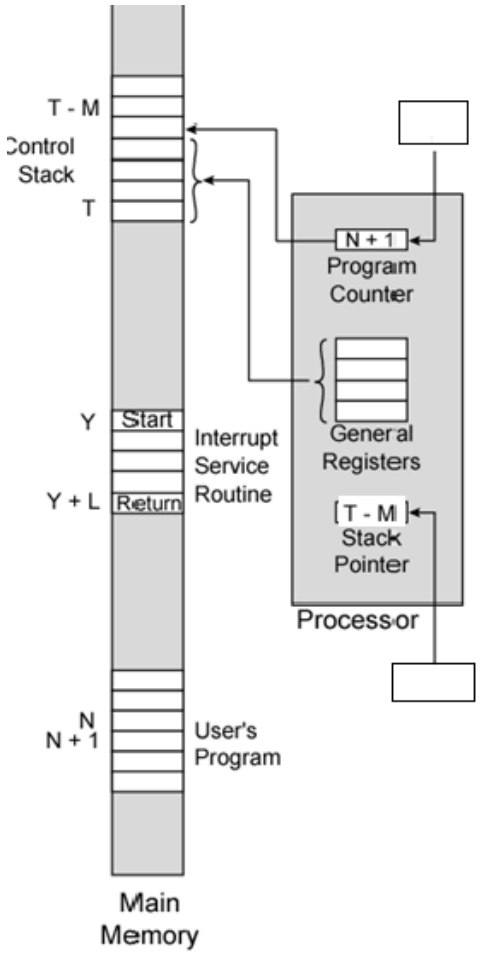
46. Which one of the following is not mandatory for external I/O in nowadays computer?
    (a) Control logic (b) buffer (c) bus (d) transducer

47. What are the advantages of using I/O modules instead of connecting I/Os directly with the CPU?

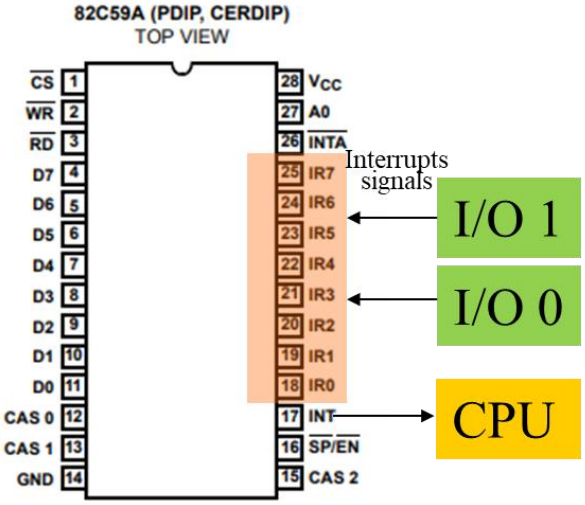
48. The following graph shows the procedures of interrupt processing, explain why it is necessary to pushes PSW and PC to the control stack and restore them after the interrupt processing is completed.



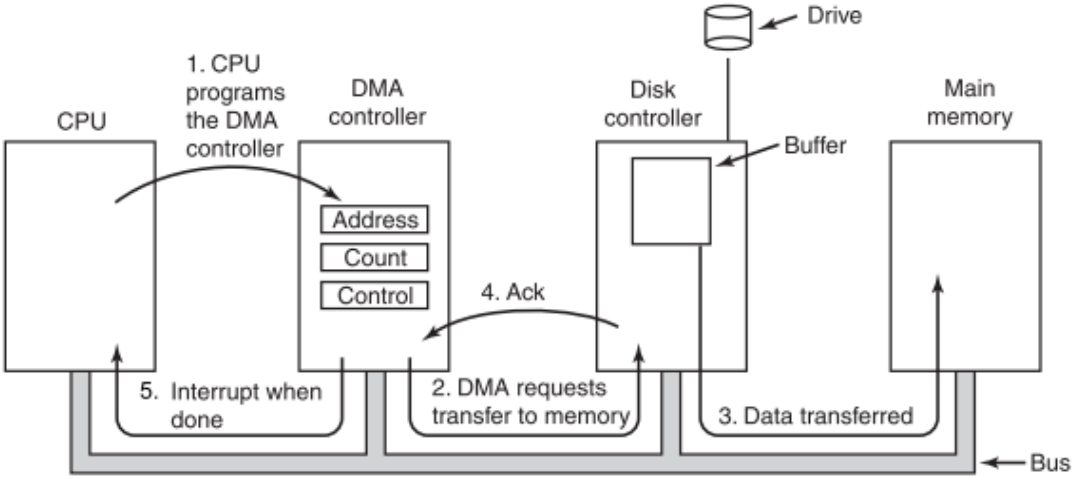
49. The following graph shows the main memory allocation and register values when interrupt occurs while the instruction at location N is being executed. How will the program counter and the stack pointer be updated?



50. The interrupter controller 82C59A provides one interrupt line to CPU and support eight interrupt lines from I/O devices. Design a circuit using 82C59 chips to handle 15 interrupts? How many 82C59 chips are required if 22 interrupts are to be handled?

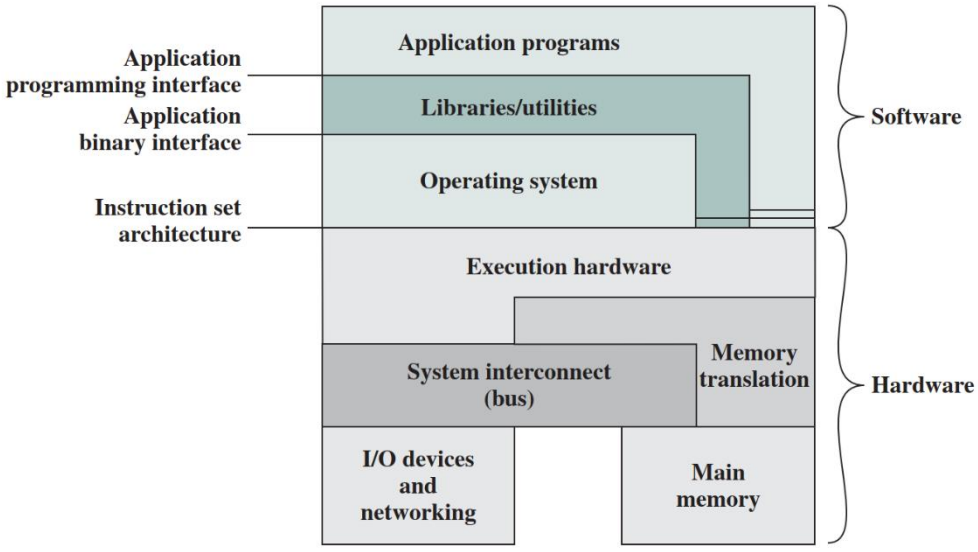


51. In addition to programmed I/O and interrupt-driven I/O, direct memory access (DMA) is proposed to further improve the computer performance. What are the advantages of DMA compared to programmed I/O and interrupt-driven I/O? Briefly describe the operation of DMA with the following figure.

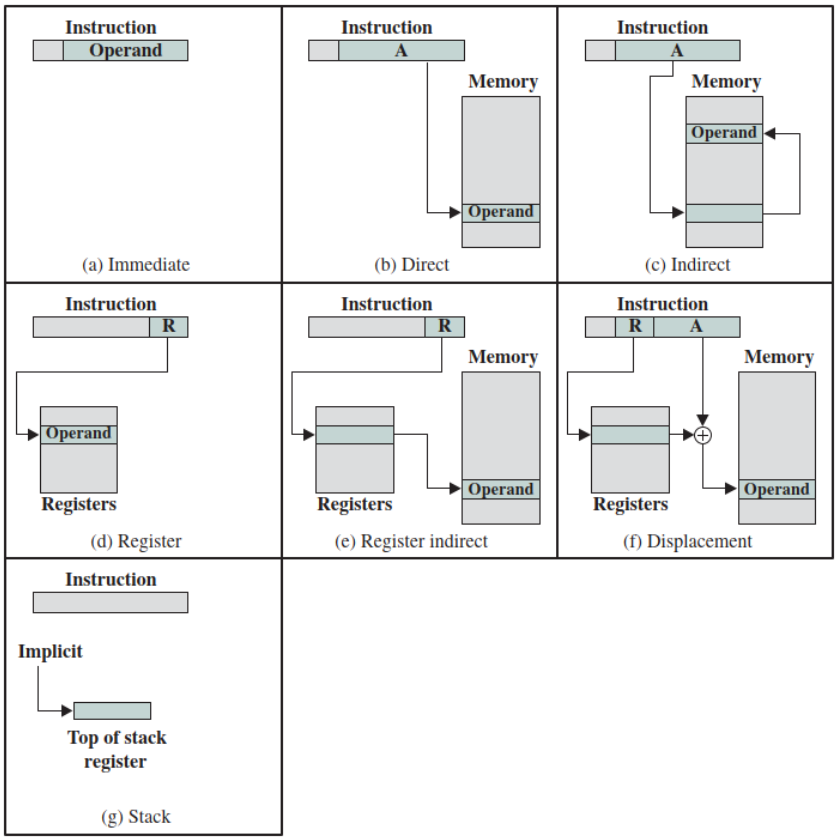


52. Based on DMA, two technologies are developed, namely Direct Cache Access (DCA) and I/O channel. What problem motivates the development of DCA? What is the advantage of I/O channel over DMA.

53. Referring to the following graph, what is the connection between an operating system and computer hardware? Why is it necessayr to have an operating system to work with nowadays' computer?

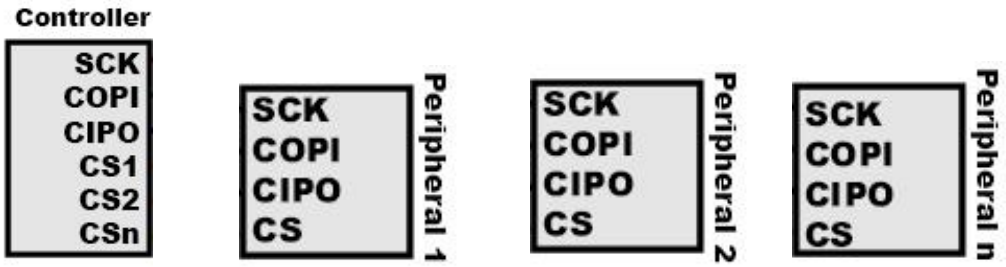


54. The following graph shows the addressing modes used in various instruction formats. Briefly describe how each mode works.

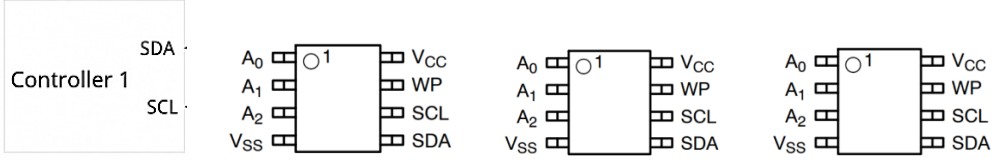


55. Which one of the following instruction sets support variant length?
    (a) PDP-8 (b) PDP-10 (c) ARM (d) Intel x86

56. For the following three peripherals supporting SPI interface, how will you design the circuit to connect all of them to a controller with only one SPI interface? For your design what is the address of each peripheral? If we have four peripherals and one 2-4 decoder chip, how could you improve the circuit to save the used controller pins? How will the address be changed?



57. For the following EEPROM chip supporting I2C interface, design a circuit to connect all of them to the controller. For your design, what is the address of each EEPROM chip?



PIN FUNCTION

Pin Name	Function
A_0, A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground