國立清華大學 電機工程學系
114 學年度第 1 學期
EE-5216 時序電路設計及應用 (Timing Circuit Designs and Their Applications)
Homework #1 (Individual Homework)
Due Date：23:59pm, Nov. 2 (Sunday), 2025, (逾時不收)
Submission: https://eeclass.nthu.edu.tw/ 作業區

- **Objective: Develop a controller that locks to a specific value by successive approximation**

- **Experience to be Learnt from this Homework:**

To get familiar with the front-end synthesis-based digital design flow (including RTL coding, Testbench development, Simulation, and Synthesis) commonly used in an all-digital circuit design.

- **Functionality**

Generate a linear function y=1000-30*x, where x is the value of an 4-bit digital code x[3:0]. As a result, y is a value in the range of [550, 1000]. Try to develop a circuit that can find a proper value of x so that the value of y is closest to a given target value, *target*. You are advised to use 10 bits for variable y, i.e., y[9:0].

- **Step-by-Step Procedure**

(a) Develop a software program in any software language (e.g., C/C++ or Python) that can solve the above problem, using the **successive approximation scheme** discussed in class. Verify your program by trying target values of 630 and 780. Report the proper values of x[7:0] for each case.
(b) Convert your software subroutine into a synthesizable RTL code (in Verilog or VHDL). Verify your RTL code with a testbench. Make sure that the results are consistent with those produced by your software program.
(c) Use a synthesis script to convert your RTL code into a gate-level netlist. Perform gate-level simulation to verify the gate-level netlist again, to ensure that its behavior is identical to your previous RTL code.
(d) Report the final gate count, the maximum operating speed (in MHz), and the estimated power consumption in (mW) of your design using *Design Compiler*.
(e) Generate the layout by running some Automatic Placement and Routing Tool (e.g., SoC Encounter or the like). Report the size of the layout. Perform post-layout simulation or analysis and report again the maximum operating speed and power consumption. Compare how these results are different from those in pre-layout analysis.

- **Deliverables: Submit the following documents (combined into a PDF file) to our EECLASS system.**
  - A cover page containing 你的系所，中英文姓名，學號等資訊
  - Your results to questions (a)-(e).