Yue Xing

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EDUCATION

Ph.D. Candidate, Department of Electrical Engineering, **Princeton University**, **Princeton, NJ** **Sep 2016 - June 2021**
Advisor: Sharad Malik
Research Topic: Effective and Efficient Verification Methods for Modern SoCs

My research interest is to explore effective and efficient methodologies for complex computing systems' design and verification. Formal methods are massively used through my research projects. So far, I've built a formal GPU model to automatically find bugs in GPU kernel programs; I also researched on automatic generation of high-level simulation models for hardware-software co-simulation. Now I'm working on a complete methodology of hierarchical SoC (system-on-a-chip) verification.
Related Courses: Computer Architecture, Compiler, Computer Network, Automated Reasoning of Software, Theory of Algorithm.

Undergraduate, Department of Electronic Engineering, **Tsinghua University**, **Beijing, P. R. China** **Sep 2012 - June 2016**
GPA: 93/100 (5th out of 238 same program students)
Related Courses: Modern Computer Architecture, Operating System, Digital Signal Processing.

TECHNICAL SKILLS

- Proficient Programming Language: C/C++, Python, Verilog, Assembly Language, Matlab.
- Familiar Software and Operation Systems: Multisim, Quartus, Verilator, Hspice, Linux.
- Familiar Machine Learning Framework: TensorFlow & TensorFlow Lite.
- Familiar Verification Tools: Z3, miniSAT, Dafny, CoSA.
- Familiar CAD Tools: Verdi, Xcelium, PTPX, JasperGold.
- Familiar Tools for Computer Architecture: Qemu, GPGPUSim, GpuOcelot, Gem5, McPAT, CACTI, Openpiton.

WORK EXPERIENCE

Google LLC **June 2018 – Dec 2018**

- Implemented a quantization framework to convert floating-point TensorFlow model into a high-precision fixed-point model for mobile device applications.
- Developed new applications on a domain specific accelerator for machine learning and image processing.
- Evaluated and characterized performance and power for hardware accelerators.
- Optimized applications by exploring runtime overhead, pipelining, and algorithm-level parallelism.
- Proposed and implemented a simulator-based power model for domain specific hardware.

RESEARCH EXPERIENCE

Hierarchical System-on-a-Chip Verification **Jun 2019 – On going**

- Developed formal models for general modules in SoC with ILA (instruction level abstraction, a formal modeling platform for hardware components).
- Improved verification efficiency by algorithmically breaking the monolithic SoC verification problem into sub-module verification and module composition verification problems.
- Designed experiments to apply this methodology to open-source SoC designs like micro-controller 8051 and RISC-V.

Automated Generation of Sound High-level Hardware Simulator **Jan 2019 – May 2019**

- Developed an automatic flow to transform ILA hardware models to sound high-level executable simulation models.
- Applied the generated hardware simulation models to QEMU and QEMU-Xilinx-SystemC-TLM hardware/software co-simulation; demonstrated 30x-1000x simulation speedup comparing with RTL-level simulator.
- Developed an automatic flow to generate test suites with complete path coverage for the high-level simulation models.

Scalable Verification Methods for GPU **June 2017 – May 2018**

- Used ILA to model the Nvidia GPU PTX (parallel execution) intermediate representation.
- Automated the modeling process by synthesizing the model from a GPU hardware.
- Utilized the GPU-ILA model to locate bugs such as data races, barrier divergence in GPU kernel functions.
- Achieved bug-free guarantee through formal models' exhaustive check and scaled up to practical programs with hundreds of LoC (lines of code).

Approximate Computation Design and Methodology **Oct 2014 - June 2016**

- Ran all experiment and simulation using C++ in this project.
- Designed a high-performance approximate circuit with hybrid predictor and error compensation scheme, achieving 2.79X speedup and 49.3% energy efficiency compared with traditional designs.
- Built a simulation platform to apply the approximate circuit units into image processing applications.
- Analyzed and designed the model of approximate circuits in power, performance, and precision, proposing a 5-dimensional lookup table with a regression algorithm to analyze error propagation.

Non-Volatile Processor **April 2015 - June 2015**

- Explored cache usage in non-volatile processors by utilizing snapshots in Gem5.
- Developed a simulator for non-volatile processors in python based on Gem5 and McPAT, providing simultaneous simulation for energy and run time.
- Analyzed different memory backup and recovery strategies in battery failure environment, exploring novel backup method like dead-block prediction algorithm.

PROJECT EXPERIENCE

Evaluation of Distributed L2 Cache Allocation Strategy on Openpiton (Course Project) **Nov 2016 - Jan 2017**

- Implemented different last-level cache allocation strategies on Openpiton using Verilog.
- Evaluated performance in different strategies by designing various assembly tests.

Exploration of Machine Learning Technique in Detecting Program Misbehavior (Course Project) Apr 2017 - May 2017

- Collected hundreds of test cases from different application classes for exploration.
- Learned to use Intel Pin tool to generate program raw features.
- Extended PCA to extract features and truncate redundant features.
- Evaluated the performance of different machine learning algorithms (SVM, etc.) to detect program misbehaviors.

Design and Analysis of Decoding Methods for Secure Caches (Course Project) **Nov 2016 - Jan 2017**

- Designed secure caches using CAM (content-addressable memory) and drew their layout with Cadence tools.
- Built a simulation tool for performance, power and area in a combination method of CACTI, Python, and Nanosim.

ECG Identity Verification System **July 2015 - Sep 2015**

- Investigated machine learning algorithms and utilized non-fiducial method to extract features for identity verification.
- Mixed multiple classification algorithms to process user data to improve verification accuracy, using grid traversal algorithm to optimize parameters for classification.
- Reorganized legacy code and realized a real-time identity verification application on IOS.
- Coordinated group discussion with a lab group of more than 10 members.

Gesture Recognition System **March 2015 - June 2015**

- Learned original gesture capture codes and found critical code section (written in C#) in Intel RealSense.
- Designed template matching and dynamic threshold schedule algorithm to extend RealSense for the task of gesture recognition in card games, using specially designed cards to improve the recognition rate.
- Developed interface for higher-level application designer's use (Like Bang!, Poker).

PUBLICATION

Yue Xing, Bo-Yuan Huang, Aarti Gupta, Sharad Malik "Formal Instruction Level GPU Model for Scalable Verification", in Proceedings of the International Conference on Computer-Aided Design, p. 130. ACM, 2018

Xinghua Yang, **Yue Xing**, Fei Qiao, Huazhong Yang "Multistage Latency Adders Architecture Employing Approximate Computing" accepted by Journal of Circuits, Systems, and Computers, vol. 26 no.3, 2017

Yue Xing[1], Xinghua Yang[1], Fei Qiao, Huazhong Yang "Approximate Multistage Latency Adder with Hybrid Prediction and Error Compensation Technique" accepted by ISVLSI 2016

AWARDS AND HONORS

CSC-IBM Scholarship (2 out of 300 students) July 2015

Academic Excellence Scholarship (twice) Oct 2015 & Oct 2014

Scholarship for Comprehensive Excellence Oct 2013

LANGUAGE

- **Mandarin:** Native speaker.