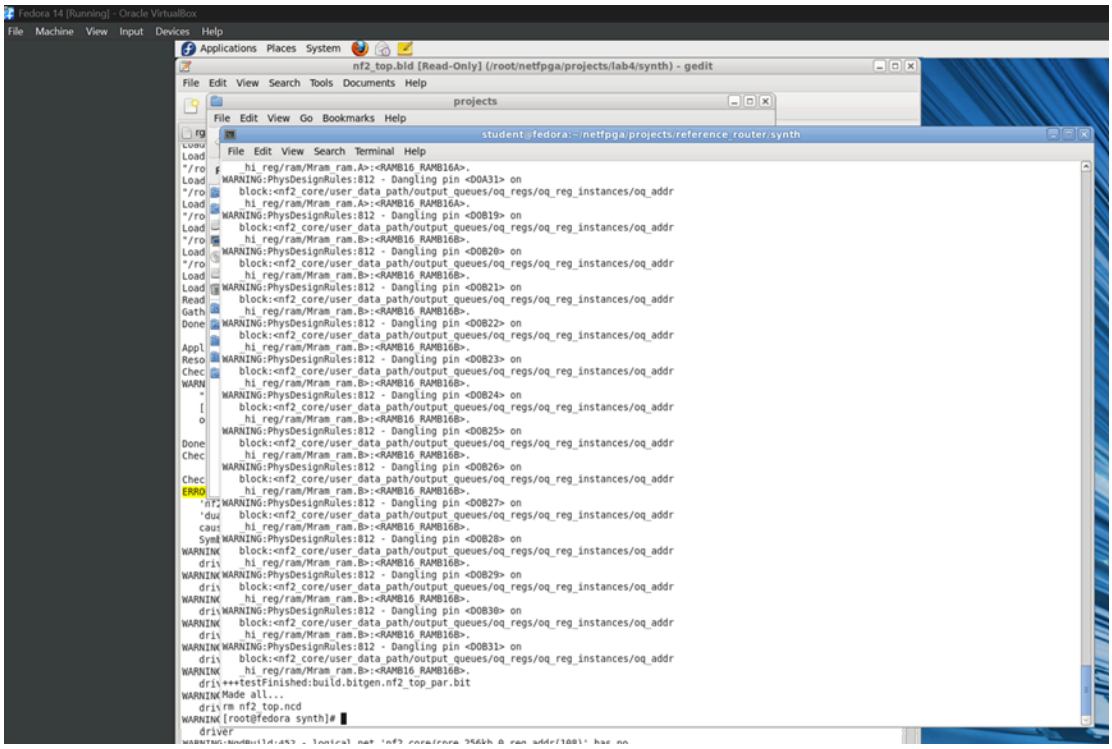
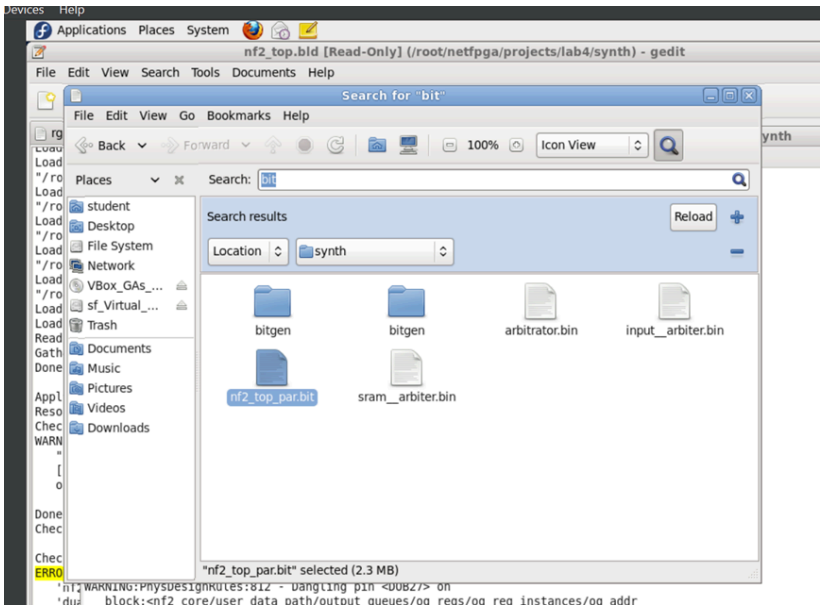
here is the github link to the files that we used and generated in this lab: https://github.com/yuezhenglingluan/USC_EE533_lab4

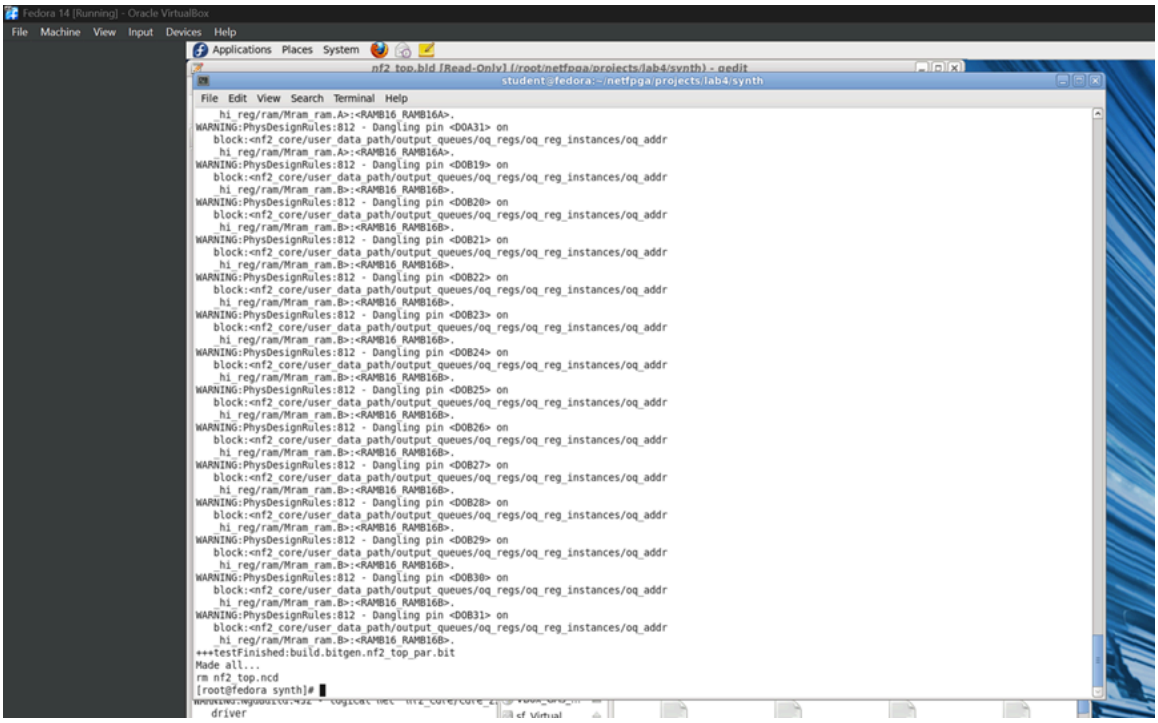
1. Here is the screenshot of the result after running make to generate a bitfile for the reference router:



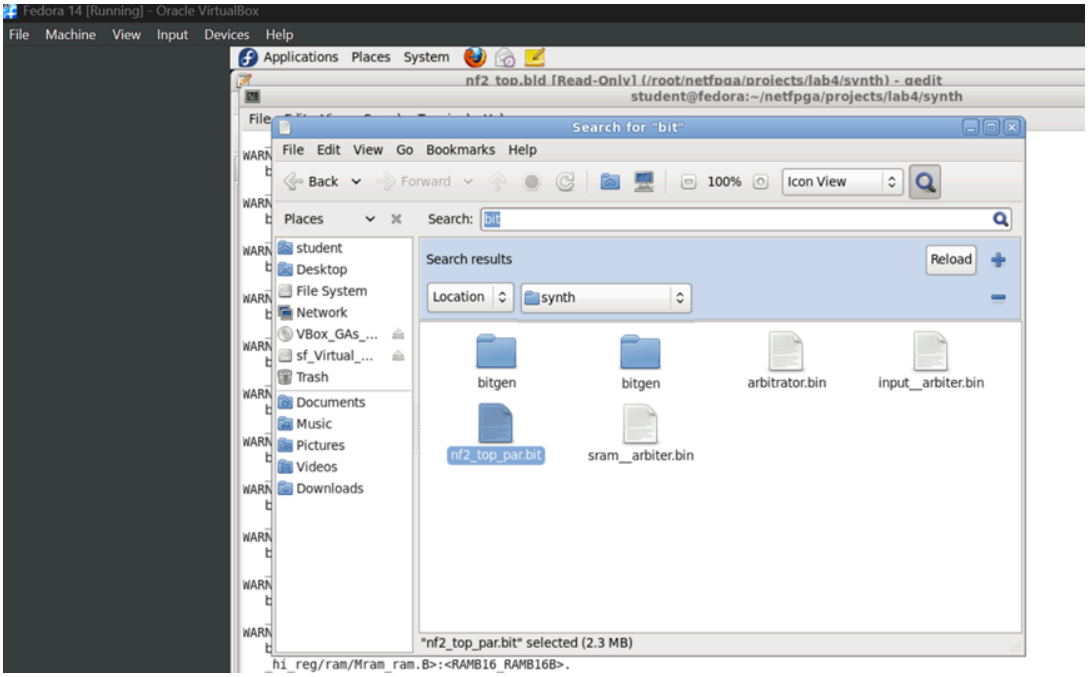
And here is the generated bit file:



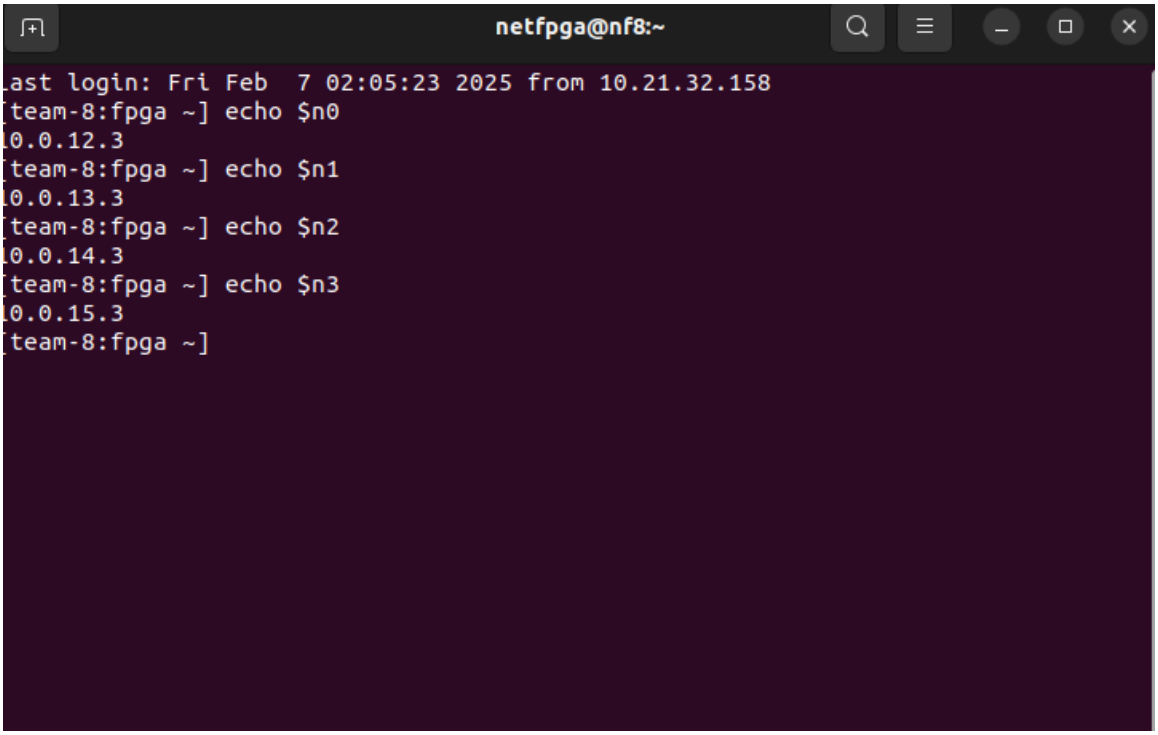
2. here is the screenshot of the result after we copy the .v and .xco file from lab 3 to the src folder and run make in synth to generate a bit file:



And here is the generated bit file:



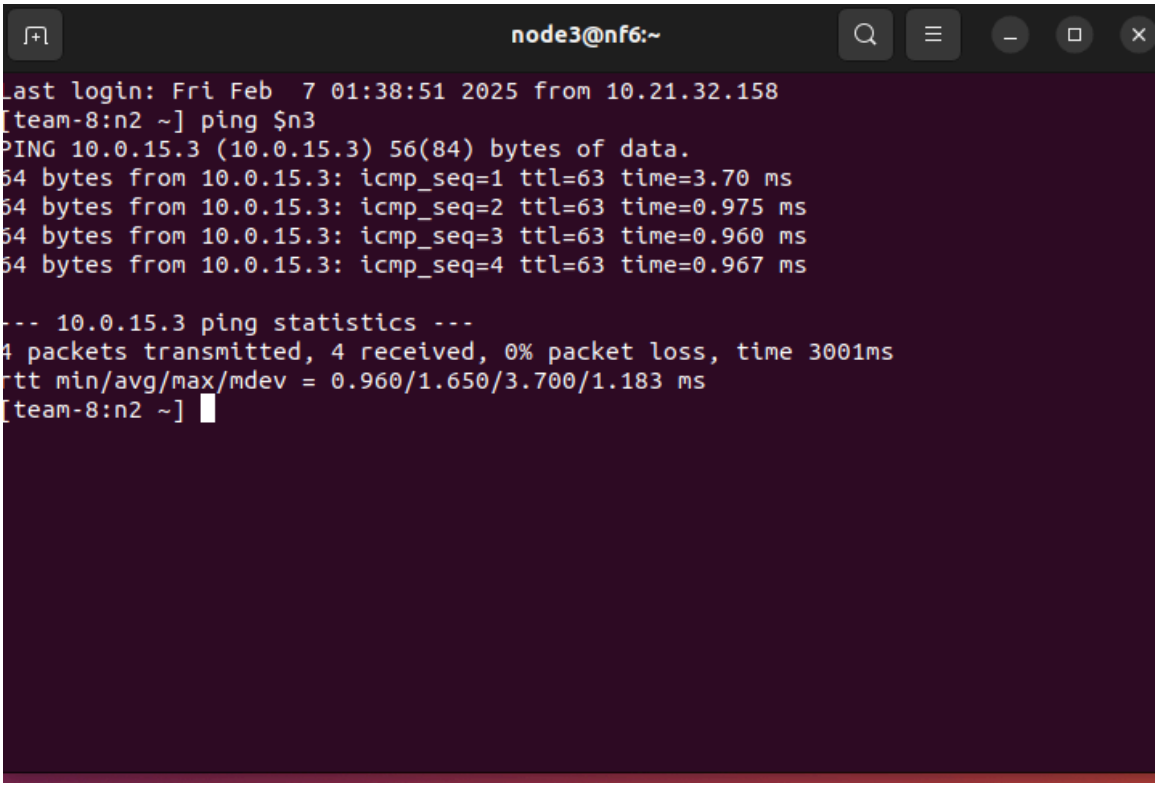
Echo each node from fpga



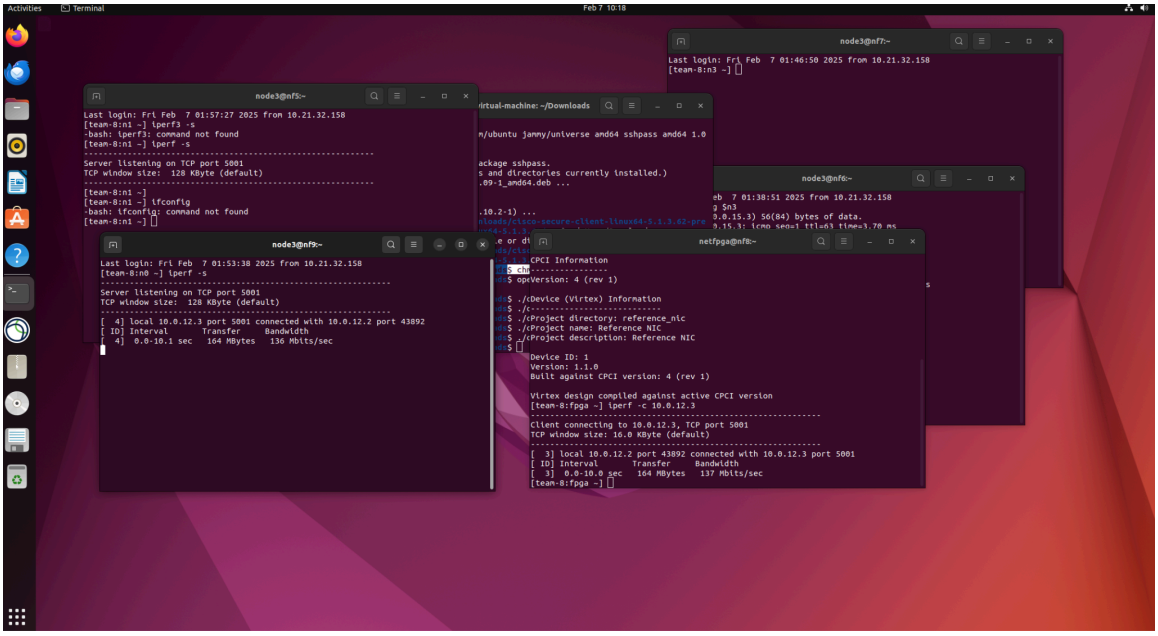
reference router test

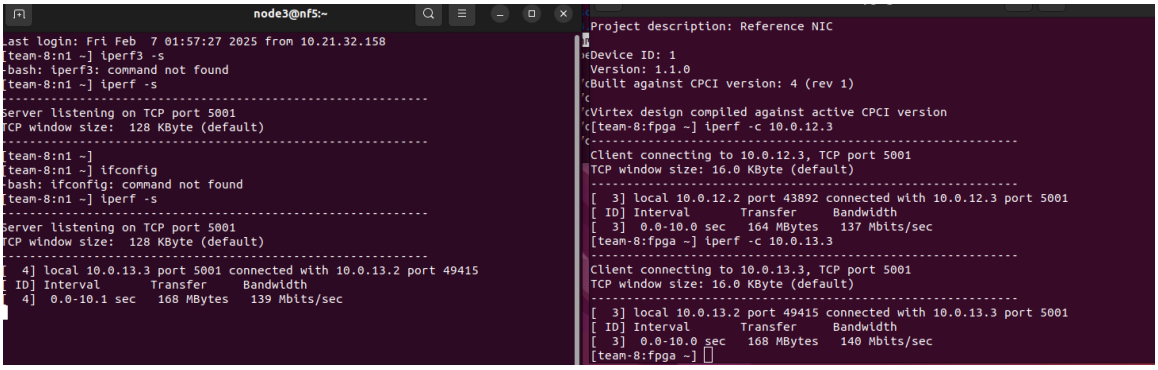

netfpga@nf8:~
Bit file built from: nf2_top_par.ncd;HW_TIMEOUT=FALSE
Part: 2vp50ff1152
Date: 2011/11/17
Time: 16:21:17
Error Registers: 0
Good, after resetting programming interface the FIFO is empty
Download completed - 2377668 bytes. (expected 2377668).
DONE went high - chip has been successfully programmed.
CPCI Information
Version: 4 (rev 1)
Device (Virtex) Information
Project directory: reference_nic
Project name: Reference NIC
Project description: Reference NIC
Device ID: 1
Version: 1.1.0
Built against CPCI version: 4 (rev 1)
Virtex design compiled against active CPCI version
[team-8:fpga ~]

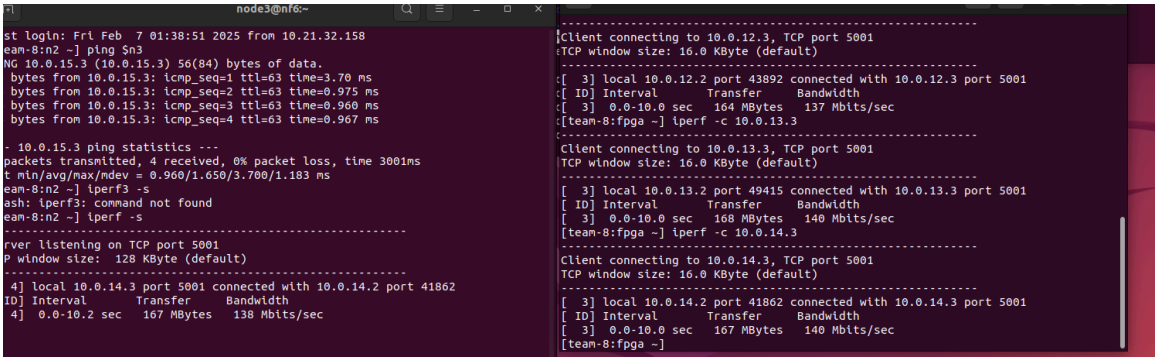
ping test


node3@nf6:~
ast login: Fri Feb 7 01:38:51 2025 from 10.21.32.158
team-8:n2 ~] ping $n3
ING 10.0.15.3 (10.0.15.3) 56(84) bytes of data.
4 bytes from 10.0.15.3: icmp_seq=1 ttl=63 time=3.70 ms
4 bytes from 10.0.15.3: icmp_seq=2 ttl=63 time=0.975 ms
4 bytes from 10.0.15.3: icmp_seq=3 ttl=63 time=0.960 ms
4 bytes from 10.0.15.3: icmp_seq=4 ttl=63 time=0.967 ms
-- 10.0.15.3 ping statistics ---
4 packets transmitted, 4 received, 0% packet loss, time 3001ms
tt min/avg/max/mdev = 0.960/1.650/3.700/1.183 ms
team-8:n2 ~]

iperf test from fpga to nodes







iperf test node to node