EE 533 Lab #9
Design and Integration of Hardware for Multiple Threads
Young Cho - youngcho@isi.edu

1. Hardware Augmentation

Design, implement, integrate, and demonstrate an integrated Network Processor with an accelerated four context-switching mechanism for this Lab. You must build the hardware register file and PC counter(s) to support four threads such that your core can work on four threads in parallel with minimal overhead.

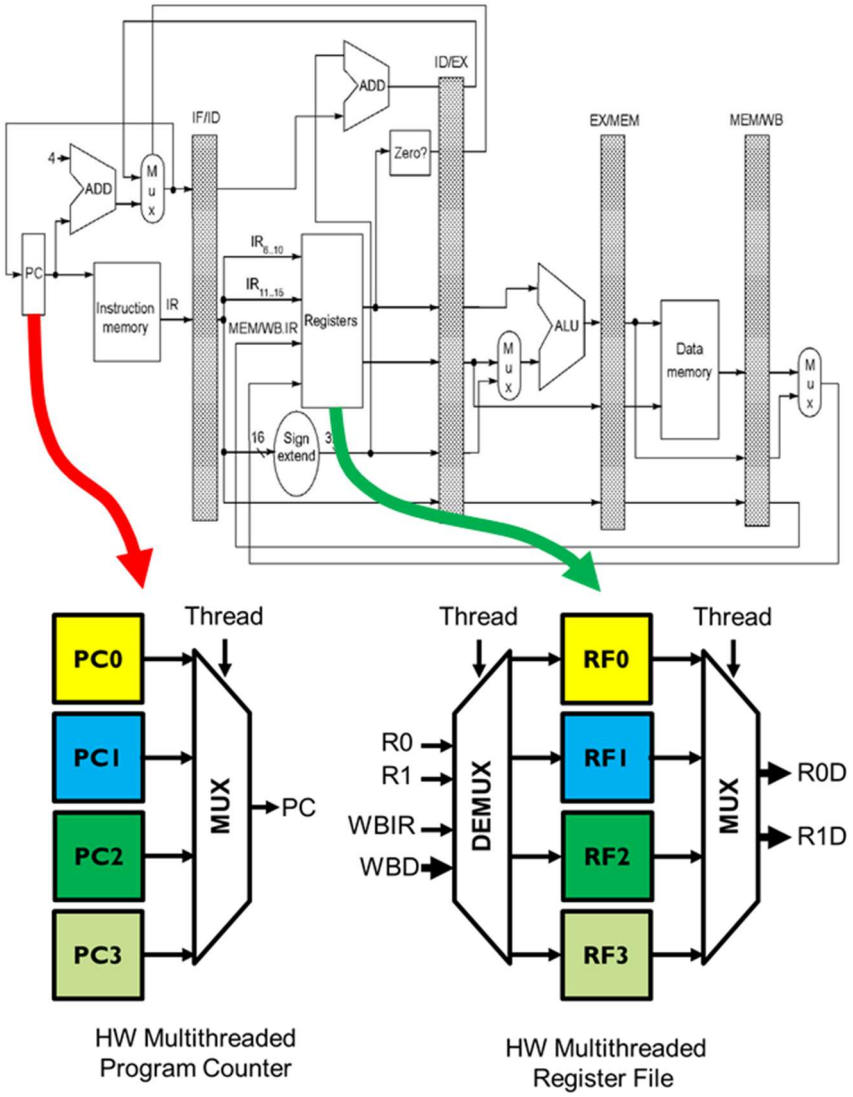

Figure 1: An example of a hardware modification for a Zero Overhead Multiple Threads

One suggestion is to build the register files out of a single block memory. The upper 2-bits of the memory address for the block memory can be used in place of the De-multiplexer and Multiplexer of the above register file design, and the rest of the bits to indicate the register number. Since there are only two read/write ports and you need the third for the writeback, you can simply double clock the memory to read at one cycle and write during the other cycle.

2. Software Verification

Write and compile four independent network packet processing programs in C. Then execute them as four parallel threads and prove their workings. In your report, you will need to describe the design of your software and hardware support for the parallel execution of your programs. You will need to get the hardware to work with your software on NetFPGA and demonstrate multiple network packet processing threads working on your processing core.

3. Submission and Demonstration

- Draw a high-level design of the datapath. The figure should depict the communication between the components.
- Include the following in your report:
  - Screen Capture of Schematics
  - Generated Verilog Files
  - GitHub records and descriptions per team member
  - The transcript of a sequence of commands typed to the interface
  - Software examples of Multiple threads
  - Program and data upload/download procedures
  - Screenshots of the results
- Demonstration YouTube video must also show your interface to your processor via software/hardware registers.