

XuanTie C906 Datasheet



Overview

The C906 processor (openc906) is based on the RV64GC instruction set and includes customized arithmetic enhancement extension, bit manipulation extension, load store enhancement extension and TLB/Cache operations enhancement extension. The processor adopts a state of the art 5-8 stages in-order pipeline. The C906 supports the Sv39 virtual memory system with custom page attribute extensions. In addition, C906 includes standard CLINT and PLIC interrupt controllers, supports RV-compatible performance monitors.

XuanTie C906

| RV64GCV Core | | |
|--------------|--------------|------------|
| PLIC | I-cache | AXI Master |
| HPM | Turbo Engine | RAS |
| PMP | D-cache | BHT |
| Debug | Watchpoint | BTB |

Features

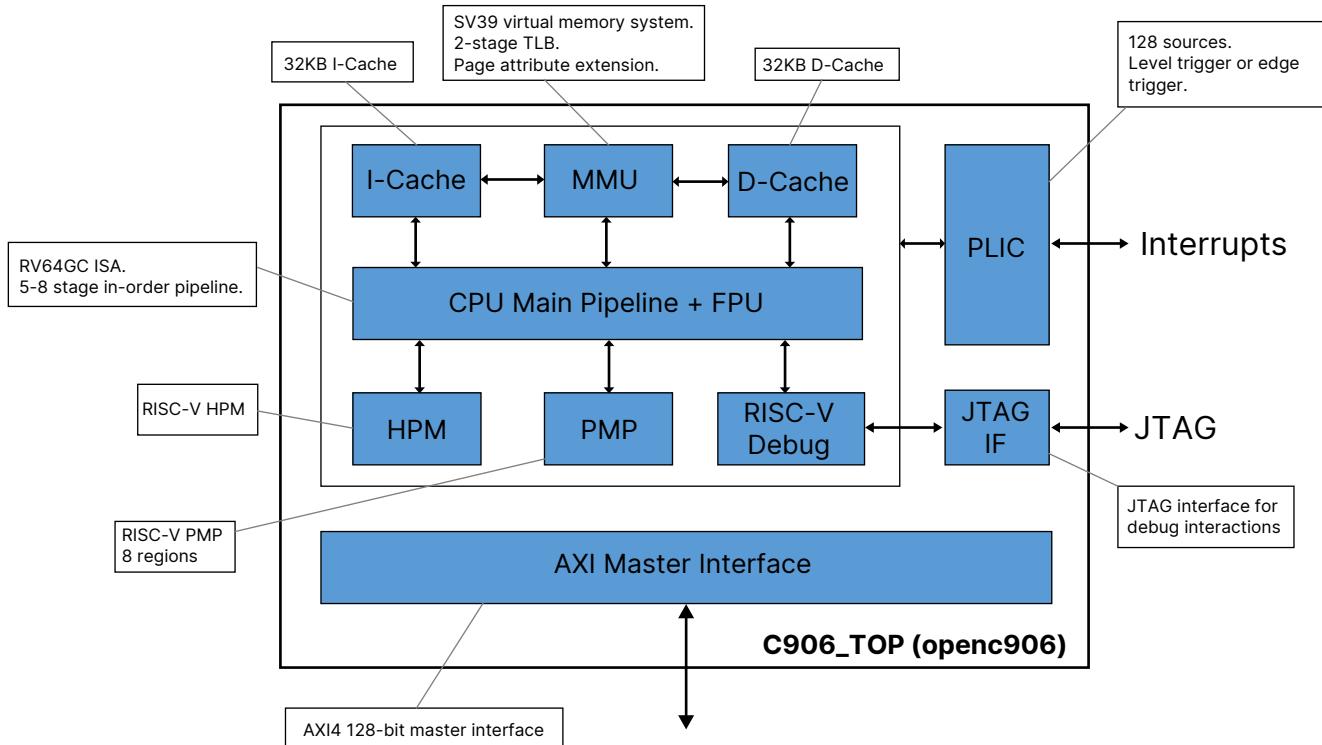
| Feature | Description |
|----------------------------------|---|
| Architecture | RV64GC |
| FPU | Support RISC-V F, D instruction extension Support IEEE 754-2008 standard |
| Physical Memory Protection (PMP) | 8 regions |
| Master Interface | AXI4.0 128-bit |
| Instruction Cache | 32KB |
| Data Cache | 32KB |
| Interrupt controller | Platform-Level Interrupt Controller (PLIC) 128 interrupts |
| XuanTie turbo instructions | Supported |

- Applications

- Surveillance
- Artificial intelligence

- Interfaces

- Master AXI (M-AXI)
- RISC-V Debug (JTAG)
- Interrupt
- Power control



XuanTie C906 Components

- Memory sub-system

The C906 has 32KB instruction and data caches.

- The L1 instruction memory system has the following key features:
 - ◆ VIPT, two-way set-associative instruction cache.
 - ◆ Fixed cache line length of 64 bytes.
 - ◆ FIFO cache replacement policy.
- The L1 data memory system has the following features:
 - ◆ VIPT, four-way set associative L1 data cache.
 - ◆ Fixed cache line length of 64 bytes.
 - ◆ FIFO cache replacement policy.
 - ◆ 128-bit read interface.

- Memory Management Unit (MMU)

- ◆ Sv39 virtual memory systems support.
- ◆ 10-entry fully associative I-uTLB/D-uTLB.
- ◆ 128-entry 4-way set-associative shared TLB.
- ◆ Hardware page table walker.
- ◆ Virtual memory support for full address space and easy code/data sharing.
- ◆ Support for full-featured OS such as Linux.
- ◆ Hardware for fast address translation.
- ◆ Page table entries are extended for additional attributes.

- Physical Memory Protection (PMP)

- ◊ 8 regions basic read/write/execute memory protection with low cost.

- Platform-Level Interrupt Controller (PLIC)

- ◊ Support multi target interrupt control
- ◊ 240 PLIC interrupt sources
- ◊ 32 PLIC interrupt priority levels
- ◊ Selectable edge trigger or level trigger

- FPU

- ◊ RISC-V F and D extensions
- ◊ Support half/single/double precision
- ◊ Fully IEEE-754 compliant
- ◊ Does not generate floating-point exceptions
- ◊ User configurable rounding modes

- RV Compatibility with Custom Extensions

The C906 is fully compatible with the RV64GC instruction set and supports the standard M/S/U privilege program model. The C906 includes a standard 8-region PMP and Sv39 MMU, which is fully compatible with RISC-V Linux. The C906 includes standard CLINT and PLIC interrupt controllers, RV compatible HPM.

- Hardware Performance Monitor (HPM)

- ◊ Program code performance tuning.

- JTAG Debug

- ◊ Support RISC-V Debug Spec 0.13.2 version
- ◊ JTAG debug interface support several triggers
- ◊ Support software breakpoints
- ◊ Check and modify CPU register resource
- ◊ Single step or multi step flexibly supported
- ◊ High speed program downloading through JTAG

- Branch Predictor

- ◊ Branch Target Buffer (BTB) and Branch History Table (BHT) to speed up control codes
- ◊ Return Address Stack (RAS) to speed up procedure returns

Configurations

| Configuration | Options |
|----------------------|----------------|
| FPU | SP+DP |
| L1 Instruction Cache | 32KB |
| L1 Data Cache | 32KB |
| Branch History Table | 8Kb |
| PMP | 8 regions |
| PLIC | 240 interrupts |
| jTLB entry | 128 |

Software Ecosystems

- ◇ Compiler, assembler, linker, debugger and binary tools are contributed to GNU and supported officially
- ◇ Linux kernel is contributed to Linux foundation and supported officially
- ◇ QEMU is contributed and supported officially
- ◇ Integrated Development Environment (CDS), compatible with Eclipse development
- ◇ Graphical profiling and statistical analysis tools base trace data (simulator)
- ◇ ICE, CK-Link Pro, high speed (1.1Mbytes/s) JTAG debug hardware

Linux System

C906 support official RISC-V Linux and its software applications ecosystem. eg: GNU toolchain, Fedora, Debian, buildroot and thousands of open source software based on Linux. XuanTie will continue to make contributions on RISC-V architecture port in Linux ecosystem.