1 Pseudo Three-dimensional Surface Code

In this section, we describe the pseudo three-dimensional Surface Code on the looped pipeline architecture introduced in Section **??**. First, we describe how computation is performed on multiple 2D Surface Codes in a processor. Then, we extend this concept into a pseudo three-dimensional structure with a periodic cycle in the direction of the third dimension.

1.1 Quantum Processor

In fault-tolerant quantum computation, the Surface Code, introduced in Section **??**, is the most promising error correction code for the calculations required in many quantum algorithms. On the other hand, quantum low-density parity-check codes (qLDPC) are often considered more suitable for quantum memory due to their high encoding rate. However, while a single Surface Code can encode only one logical qubit, it offers many advantages, such as a simple approach for universal logical operations using lattice surgery combined with magic state distillation.

When designing the processor for computation, we simplify a single Surface Code into a "patch," which features dashed and solid lines. Simply put, a patch represents a logical qubit. In Fig. 1(a), three patches are allocated on the processor, and the corresponding Surface Codes are shown in Fig. 1(b), which are numbered. The rest of the qubits in Fig. 1(b) are unused data qubits for lattice surgery, as introduced in Section **??**.

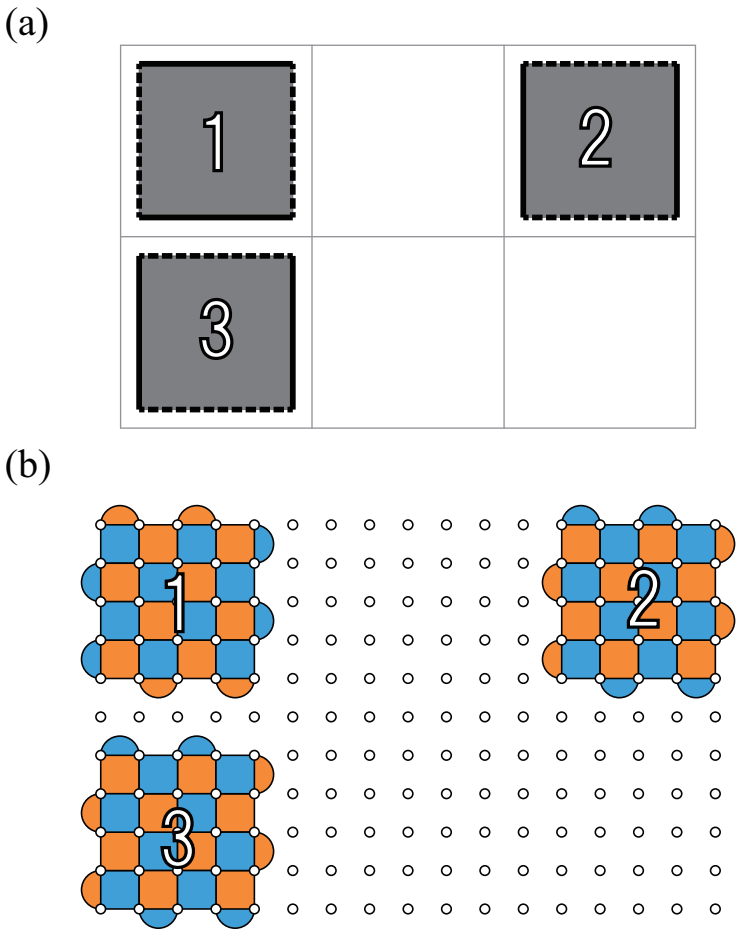

Fig. 1

Using lattice surgery, we can perform logical operations between two patches, three patches, or more. Additionally, we can perform commutative surgery operations in parallel when there exists a route from the control qubit to the target qubit by using unused data qubits in the processor. In this scheme, the efficiency of computation depends on how many parallel operations we can execute, thus requiring careful decision-making regarding the routing of operations. For instance, a certain logical 2-qubit operation between patch 2 and patch 3 is shown in Fig. 2. In this case, we cannot perform a logical operation between patch 1 and patch 2 in parallel.

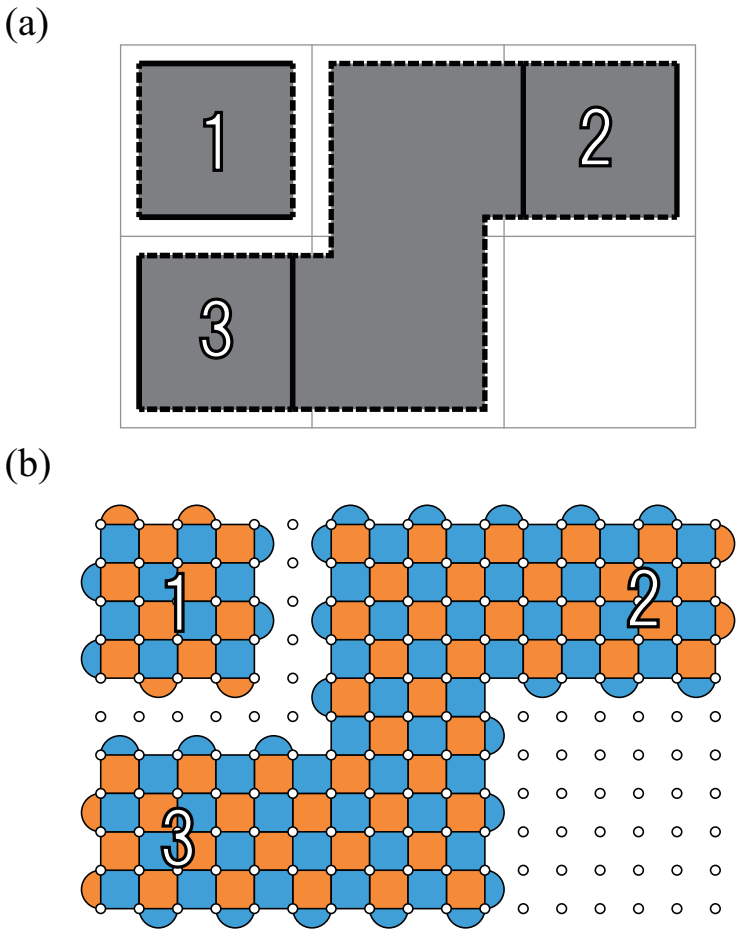

Fig. 2

In Fig. 3, some logical operations performed in parallel are illustrated with blue routes, while the orange route is prohibited since it intersects with an existing blue route at their intersection.

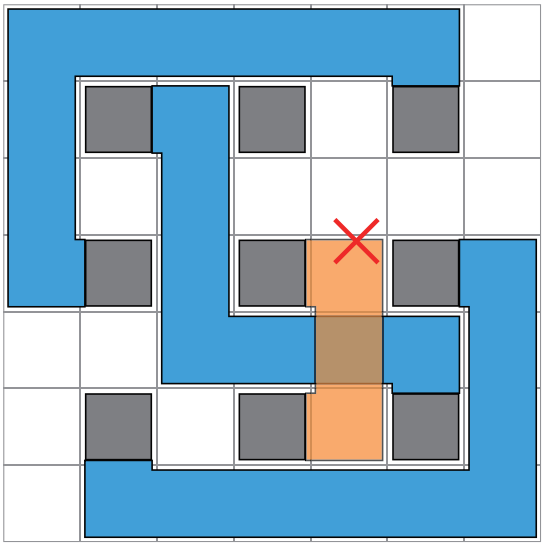

Fig. 3

1.2 Pseudo Three-dimensional Surface Code

First, we introduce the Surface Code implemented in the looped pipeline as described in Section **??**. In the looped pipeline architecture, we consider a single looped pipeline as a qubit in the Surface Code, as shown in Fig. 4. The red dashed lines represent a two-qubit gate for the two physical qubits in the looped pipeline. In the following description, the devices for measurement and initialization are not shown for simplicity.

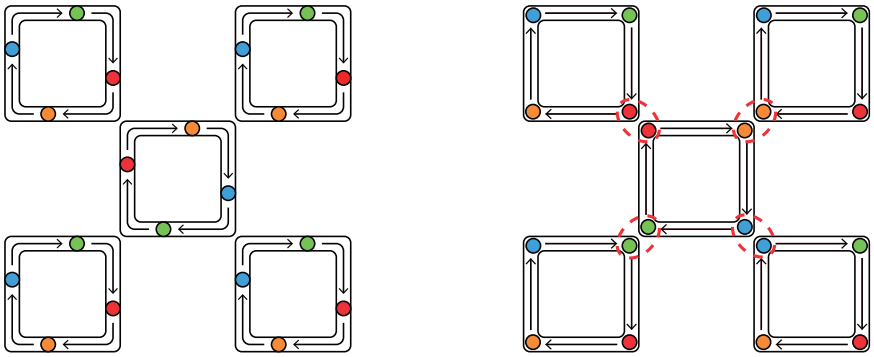

Fig. 4

Considering the looped pipeline in the middle of the five pipelines as the ancilla qubit for syndrome measurement, and the looped pipelines surrounding the ancilla qubit as the data qubits, we can see that the allocation of looped pipelines corresponds to the Surface Code, as shown in Fig. 5. There exist synchronized qubits with the same color in the looped pipeline.

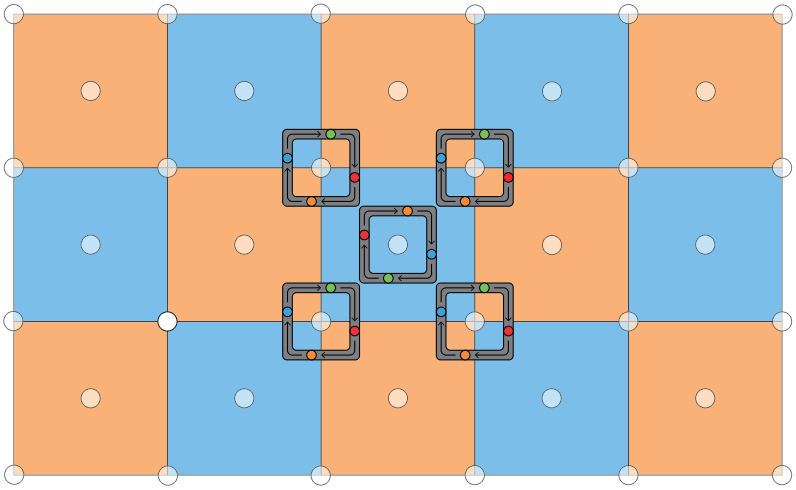

Fig. 5

In addition to the interloop interactions shown in the right half of Fig. 4, we can perform intraloop interactions as shown in Fig. 6.

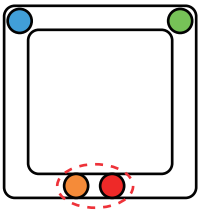

Fig. 6

Now, we have four qubits in a single pipeline; thus, we have four stacks of Surface Codes, as shown in Fig. **??**. In the following description, we refer to each stacked Surface Code as a "layer." Furthermore, when representing the pseudo-3D Surface Code as shown in Fig. 7, we refer to each layer as a "floor." For example, we designate the red layer as floor 0 and the blue layer as floor 2. On the one hand, by introducing interloop interactions, as shown in Fig. 5, we enable the construction of the Surface Code. On the other hand, by introducing intraloop interactions, we can perform logical two-qubit operations between qubits, each present in adjacent layers. Lastly, it is worth noting that in Fig. 7, floor 0 and floor 3 are adjacent since the red qubits and orange qubits are adjacent in the looped pipelines.

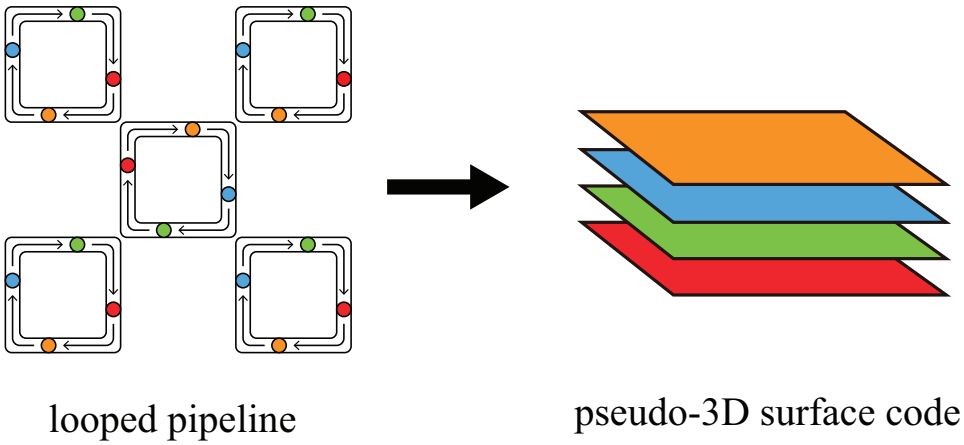

Fig. 7

1.3 Lattice Surgery Routing

In this subsection, we will show the advantage with using the psuedo-3D surface code for the lattice surgery routing. The numerical results are shown in Section.**??**.

In Fig. 8, we are showing the distance advantage of the pseudo-3D Surface Code. When the blue operation in Fig. 8 is being processed, the orange operation needs to make a detour in the 2D Surface Code. However, in the pseudo-3D Surface Code, the orange operation can bypass the blue operation by utilizing the upper layer. Thus, the total cost for routing the blue and orange operations is less in the pseudo-3D Surface Code than in 2D.

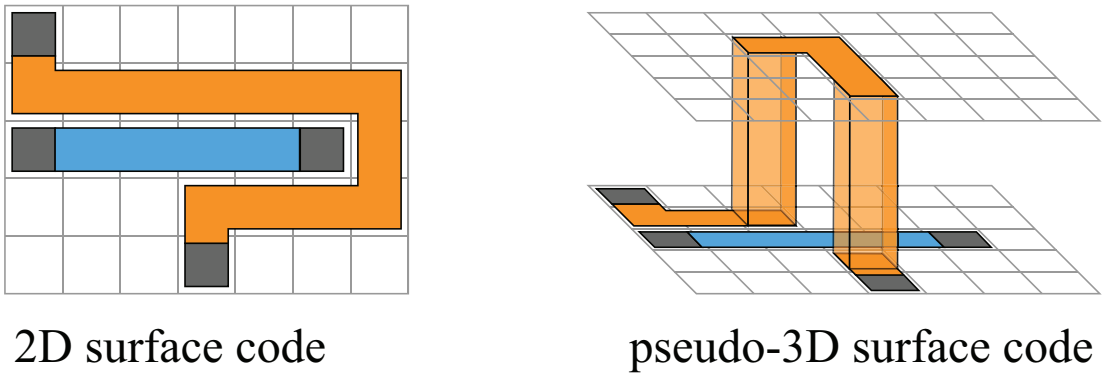

Fig. 8

In Fig. 9, we are showing the parallelization advantage of the pseudo-3D Surface Code. When the blue operation in Fig. 9 is being processed, the orange operation cannot be executed in the 2D Surface Code because there is no available route for the orange operation. However, in the pseudo-3D Surface Code, the orange operation can bypass the blue operation by utilizing the upper layer. Thus, the total time for executing the blue and orange operations is reduced in the pseudo-3D Surface Code compared to the 2D Surface Code.

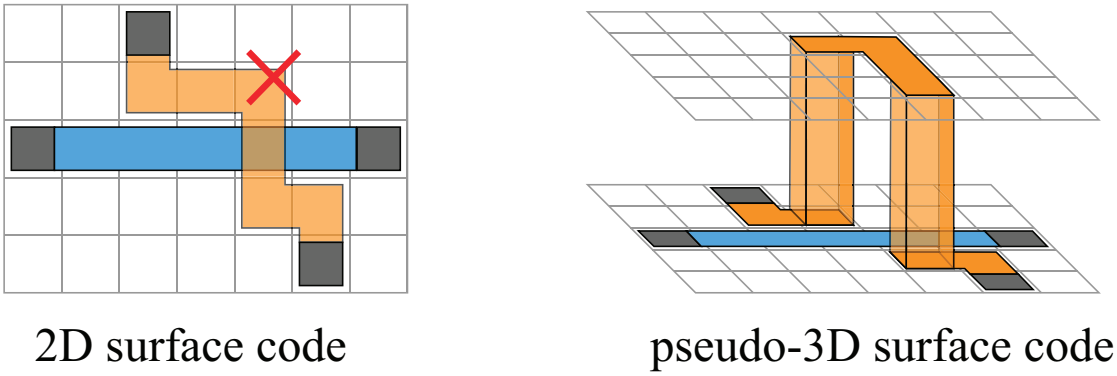

Fig. 9