1 Introduction

Recent years have witnessed experimental demonstrations of fault-tolerant quantum computation (FTQC) on real devices [1, 2]. These experiments highlight two-dimensional (2D) surface codes as the most promising quantum error correction codes for FTQC due to their high physical error rate threshold. In the 2D surface code, lattice surgery [3] can be performed, enabling logical operations between two distinct surface codes, each encoding a logical qubit. Furthermore, to achieve universal computation, it is necessary to implement magic state distillation [4] for non-Clifford gates such as the T gate or the CCZ gate. However, magic state distillation is a highly costly operation. Therefore, magic state cultivation [5] has recently emerged as an alternative method for implementing the T gate with a cost comparable to that of a CNOT gate.

Representative quantum computing platforms include neutral atoms, superconducting circuits, semiconductors or quantum dots, and photonic quantum computers. In this paper, we study a pipeline architecture [6] for semiconductor quantum computers that utilize one-dimensional shuttling operations. A shuttling operation involves moving a qubit, such as an electron in semiconductors, to enable gate operations between two qubits that are initially far apart before the shuttling process. Neutral atom quantum computers also adopt shuttling operations, enabling the realization of a transversal CNOT gate between two distinct codes, each encoding a logical qubit [7].

In the pipeline architecture, we realize a pseudo-three-dimensional (pseudo-3D) surface code by stacking multiple two-dimensional (2D) surface codes on top of one another. Our research demonstrates that the pseudo-3D surface code enhances routing operations for gate implementations via lattice surgery by leveraging the additional dimension for routing pathways. Specifically, the 3D structure allows the creation of routes in the third dimension when no viable path exists within the 2D plane. Furthermore, this architectural design reduces routing overhead, such as the number of qubits required, thereby optimizing resource utilization.

We also study the optimal placement of logical qubits, which are constructed using surface codes, on a quantum processor. By employing a mechanical model, such as potential energy minimization, we achieve near-optimal placement for 2D processors and extend this approach to pseudo-3D surface code processors.

The paper is structured as follows. In Section 2, we present the notations used in the subsequent sections. Section 3 describes the stabilizer formalism, which forms the backbone of quantum error correction theory, and Section 4 explains the surface code in terms of the stabilizer formalism. In Section 5, we discuss lattice surgery operations on the 2D surface code. Section 6 introduces the pipeline architecture, while Section 7 explains the implementation of surface codes within this architecture and demonstrates how the pipeline architecture enables the realization of a pseudo-3D surface code. In Section 8, we introduce a mechanical model to optimize the placement of logical qubits on the 2D or pseudo-3D surface code. Section 9 presents the results, including improvements in routing for the pseudo-3D surface code compared to the 2D surface code, as well as placement optimization. Finally, Section 10 provides the conclusions and future directions for the pipeline architecture and placement optimization on the pseudo-3D surface code.