1 Results

Firstly, we perform numerical simulations of the pseudo-3D Surface Code, introduced in Section **??**, using a circuit that executes a 2D Heisenberg model and compare it to the 2D Surface Code. The results are presented in Fig. 1, and a more complex system is shown in Fig. 2. In these figures, the horizontal and vertical axes represent the instruction number and distance, respectively, where distance refers to the number of patches required for routing operations. Additionally, the 20 magic patches that produce T gates are aligned along $x = -1$, arranged from $y = 0$ to $y = 19$. The Breadth-First Search algorithm is used for routing in the following cases.

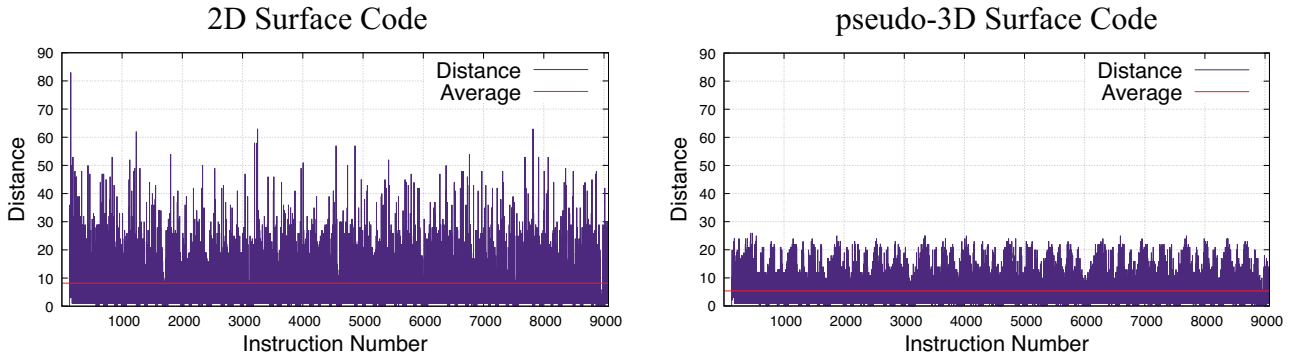

Fig. 1

In Fig. 1, the graph illustrates that in the 2D Surface Code, a substantial number of operations exceeded a distance of 30. In contrast, in the 3D Surface Code, the longest operation distance remained below 30. Furthermore, the average distance per operation was significantly reduced from 8.18 in the 2D configuration to 5.36 in the pseudo-3D configuration, resulting in an approximately 66% improvement in overall circuit distance. However, the total time required to execute the entire circuit did not change despite expanding the routing dimension to pseudo-3D.

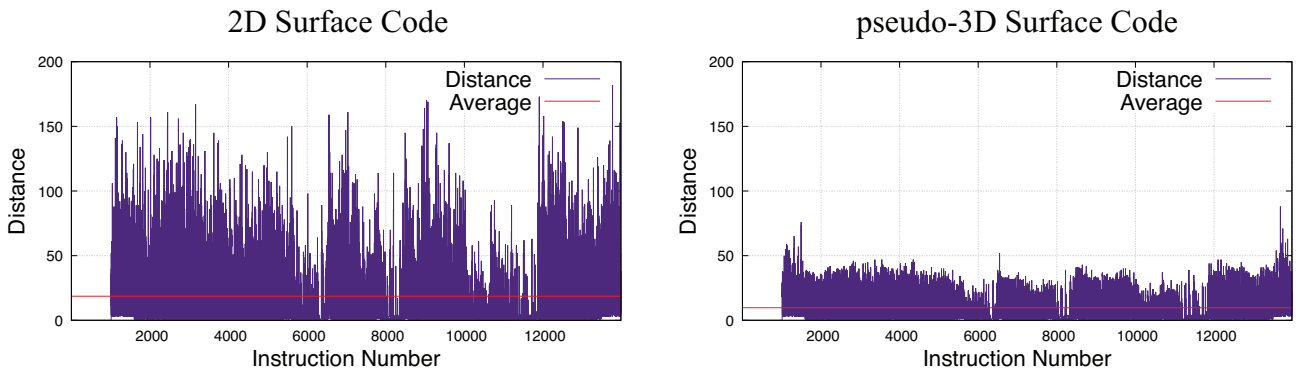

Fig. 2

In the more complex circuit, where the Heisenberg model system is the same as in the former case but is more parallelized and thus requires more ancilla qubits, similar improvements are observed, as shown in Fig. 2. This further demonstrates the effectiveness of the pseudo-3D Surface Code in reducing operation distances. The average distance per operation was significantly reduced from 18.64 in the 2D configuration to 9.74 in the pseudo-3D configuration, resulting in an approximately 52% improvement in overall circuit distance. However, the total time required to execute the entire

circuit did not change in the more complex system. Therefore, the pseudo-3D Surface Code does not improve the parallelization of the circuit.

Secondly, we perform numerical simulations of the placement optimization method introduced in Section **??**. The results are presented in Fig. 3 for the 2D case and Fig. 4 for the pseudo-3D case. Additionally, the graphs optimized by the potential energy model are shown in Fig. 5 and Fig. 6. Each figure in Figs. 3–6 displays the results of a smaller circuit in the top row and a larger circuit in the bottom row. The system for the Heisenberg model is the same as in the previous case; thus, the results on the left-hand side of Figs. 3–6 have already been discussed in the preceding paragraph. The 20 magic patches that produce T gates are aligned along $x = -1$, arranged from $y = 0$ to $y = 19$, while logical patches are allocated in the range of $x \geq 0$ and $y \geq 0$. The parameter l, introduced in Section **??**, was tuned to a value of 3 in all the following cases, and the Breadth-First Search (BFS) algorithm is used for routing in the following cases.

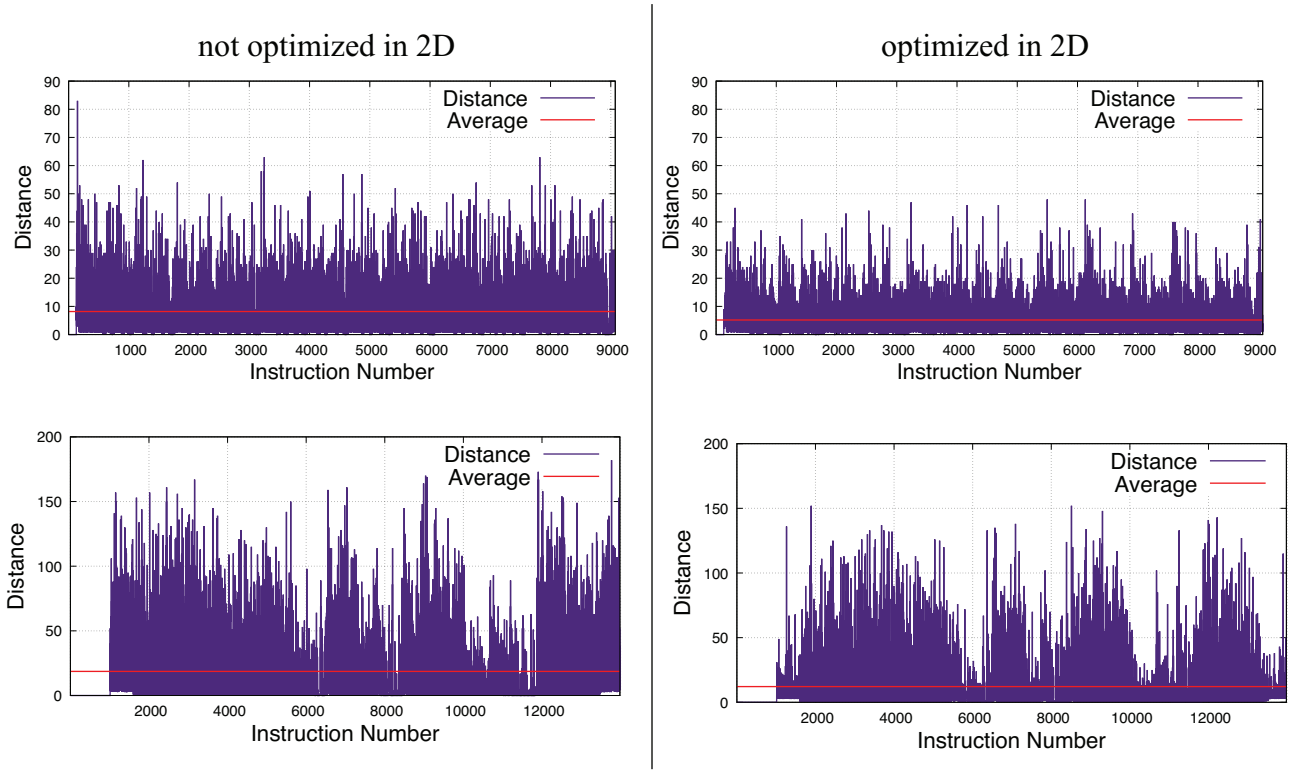

Fig. 3

In Fig. 3, we obtained results showing that placement optimization decreases routing distances. Specifically, the average distance in the 2D optimized configuration was reduced to 5.18 for the smaller circuit and to 12.15 for the larger circuit, resulting in a 63% improvement in the smaller circuit and a 65% improvement in the larger circuit.

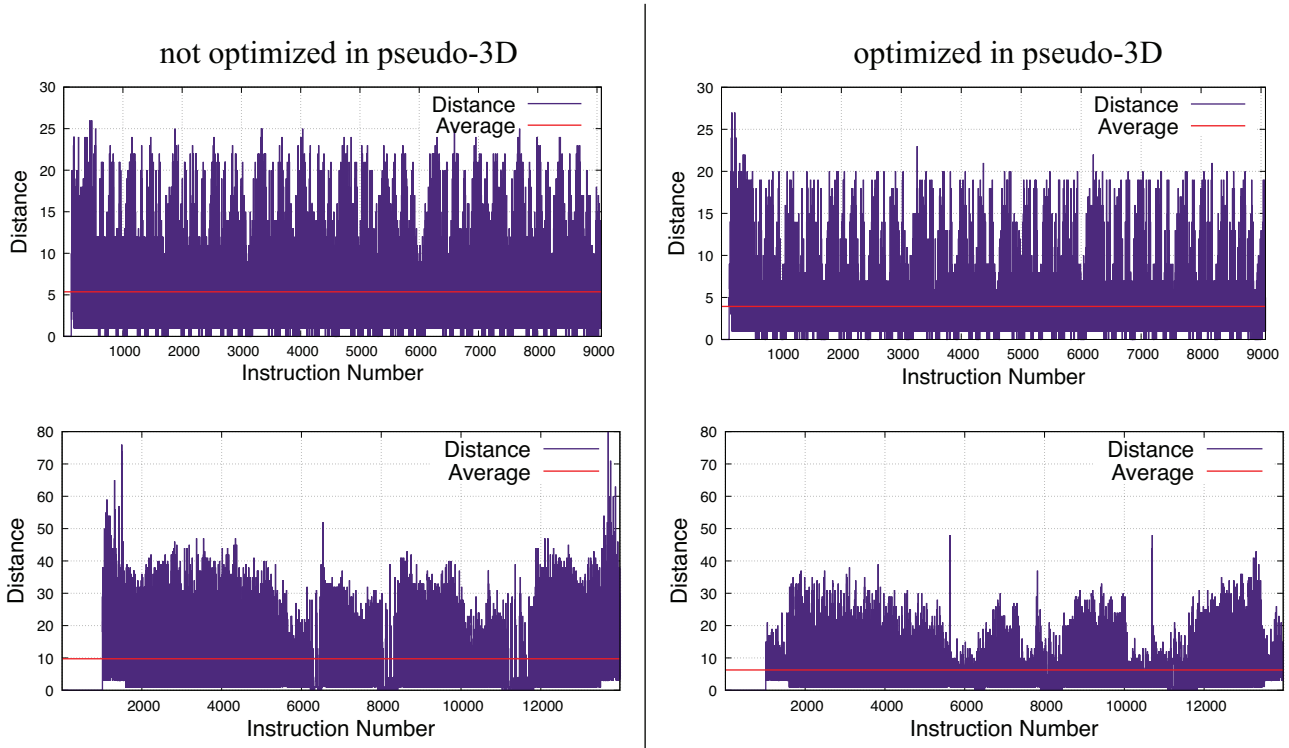

Fig. 4

Similarly, in Fig. 4, we observed that placement optimization effectively decreases routing distances in the pseudo-3D configuration. Specifically, the average distance in the pseudo-3D optimized configuration was reduced to 3.93 for the smaller circuit and to 6.28 for the larger circuit, resulting in a 73% improvement in the smaller circuit and a 64% improvement in the larger circuit.

Throughout the all results, the distances needed to routing is more effectively reduced in the larger cicuit than that in smaller circuit. But there exists a trade-off that the BFS algorithm is more complicated in pseudo-3D, thus the routing time cannot be ignored in a larger circuit in the pseudo-3D. Moreover, placement optimization time in a graph also cannot be ignored in a larger circuit in the pseudo-3D.

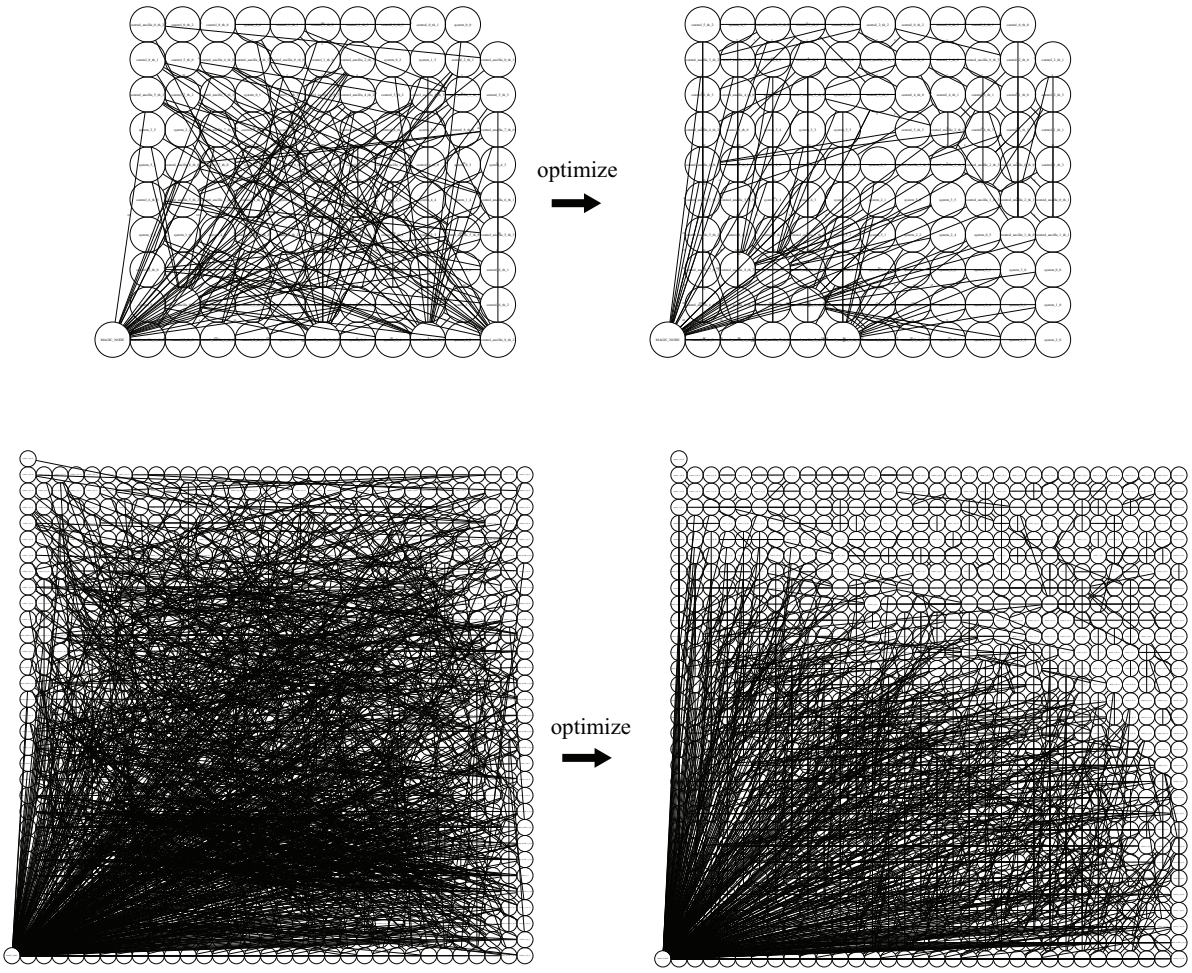

Fig. 5

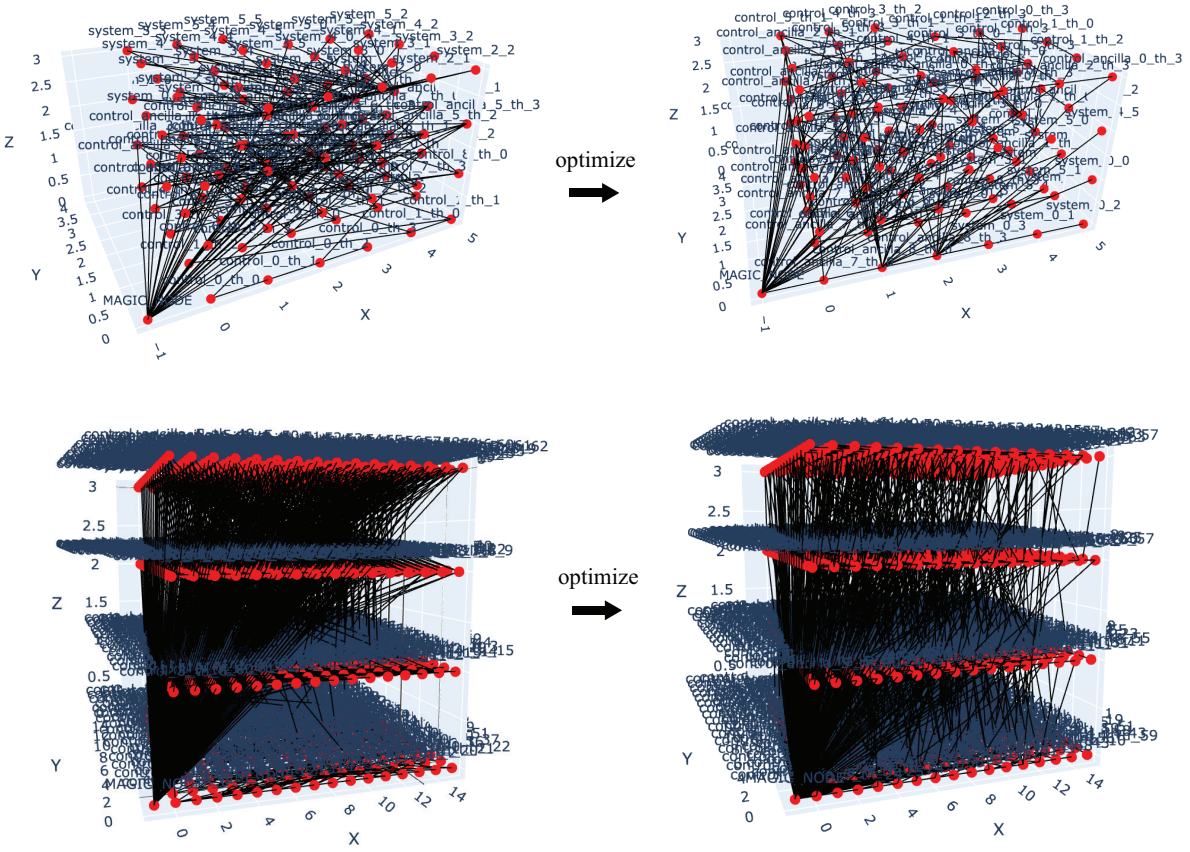

Fig. 6