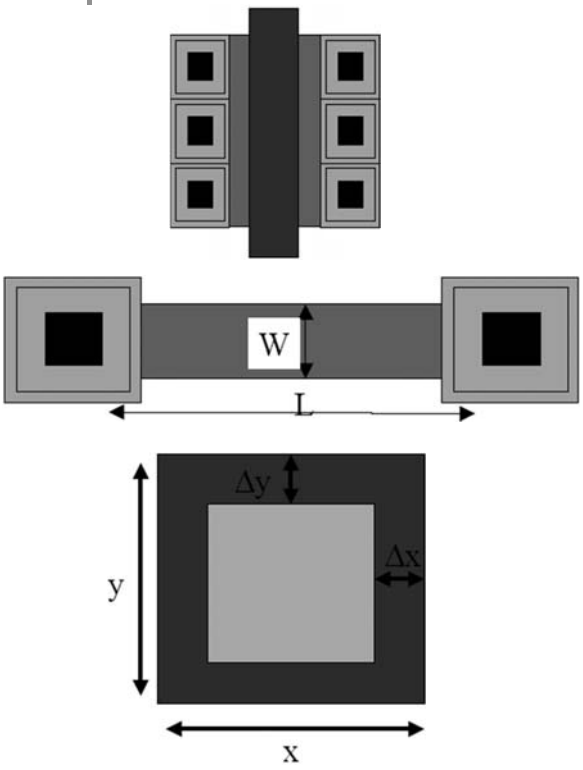
Mismatches vs Strategies

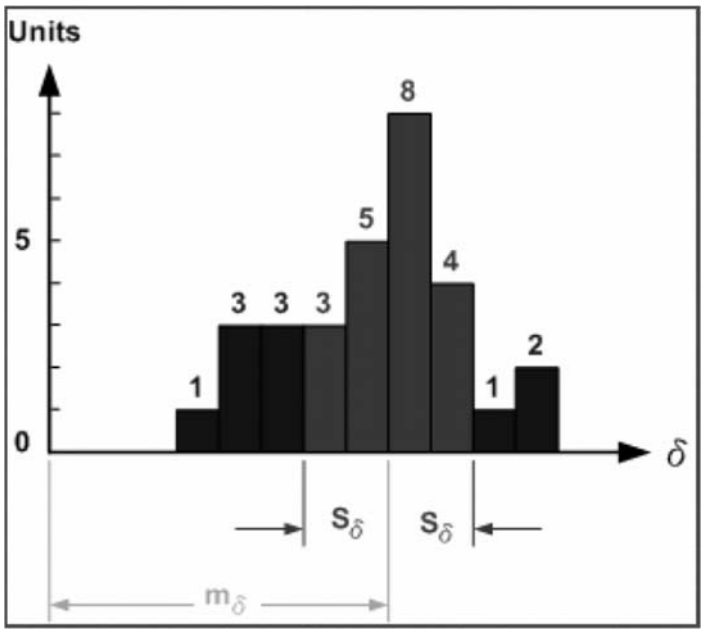
Poki Chen

What Should We Care?

- parametric mismatch fluctuations hamper the performance and yield of deep-submicron CMOS ULSI systems
  - it will most likely get worse in the future...
- Physical variations:
  - Critical Dimensions ΔCD
  - layer thickness Δt
  - furnace Temperatures ΔT
  - uniformity of chemicals ΔC
- electrical variations include wafer-to-wafer & lot-to-lot
  - currents: ~ 5 -30%
  - voltages: 10 -100 mV
- parametric spread and fluctuation specs give rise to an everlasting battle between process technology development and system designers
- small feature sizes & low supply voltages increase the impact of variation of transistor properties on chip or system performance

Histogram of the mismatch, δ, of 30 units, showing mean, m_δ, and standard deviation, s_δ.





Worst-case mismatch estimation

- *3-sigma mismatch* = $|m_\delta| + 3\, s_\delta$ ➔
  - **less than 1% of all R's have a greater mismatch**
- *6-sigma mismatch* = $|m_\delta| + 6\, s_\delta$ ➔

virtually no units have a larger mismatch than 6sd

Reasons of Mismatch

- Mismatch in IC is generally of two types :
  - Systematic mismatches which are caused by :

Fate

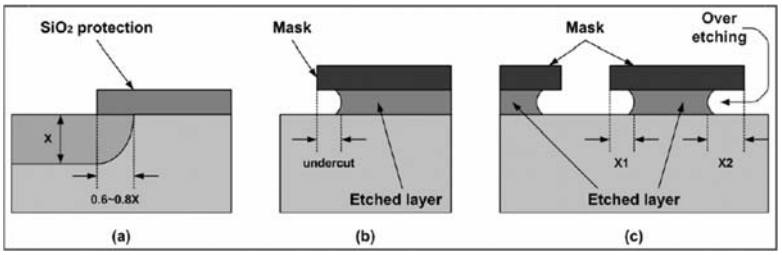
Monopoly Game

Chance

  - Process biases: **Drawn Geometry** does not get fabricated exactly: photo-mask size differences, lens aberrations, photo-resist thickness variations…
  - Mechanical stress
  - thermal gradients
  - Pattern shift
  - Etch variation
  - Diffusion interactions
  - Thermalelectrics
  - Voltage modulation
  - Charge spreading
  - Dielectric polarization
  - Random (stochastic) mismatches due to microscopic fluctuations in
    - ion implantation
    - Dopant diffusion
    - Dopant clustering
    - interface states
    - fixed charges
    - Voltage modulation
    - edge roughness
    - poly-Si grain effects

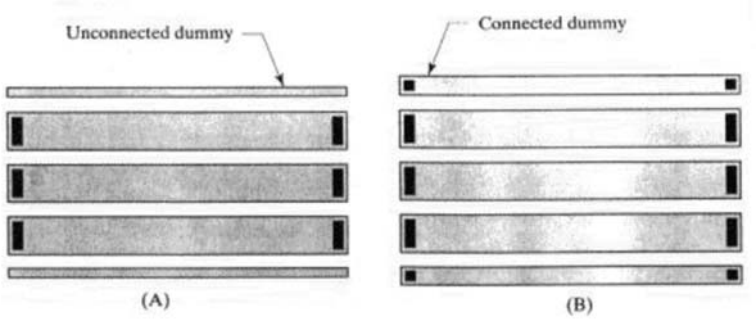
Poly Etch Rate Variation

- **Wider spacing between Poly fingers ➔ faster etch rate.**



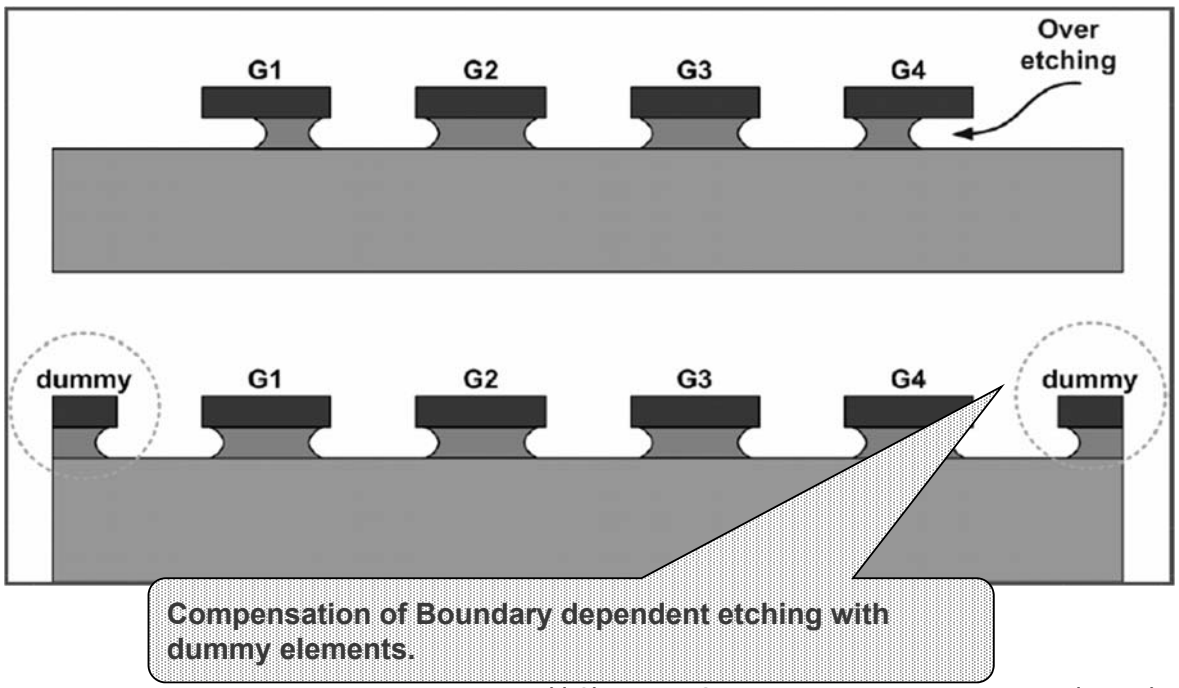
- **(a) Lateral diffusion; (b) etching under the protection; (c) boundary dependent etching.**

- **Multi strip Poly resistors ➔ strips on the ends need Dummy strips**

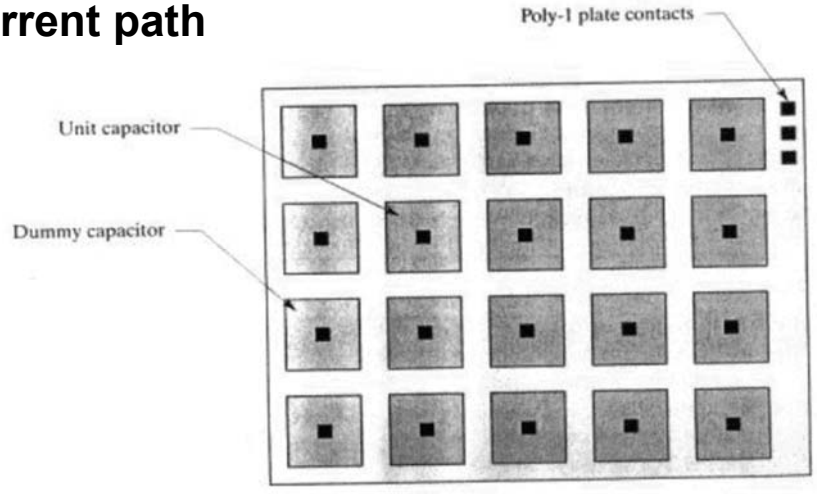


Boundary Condition

- Boundary dependent etching.

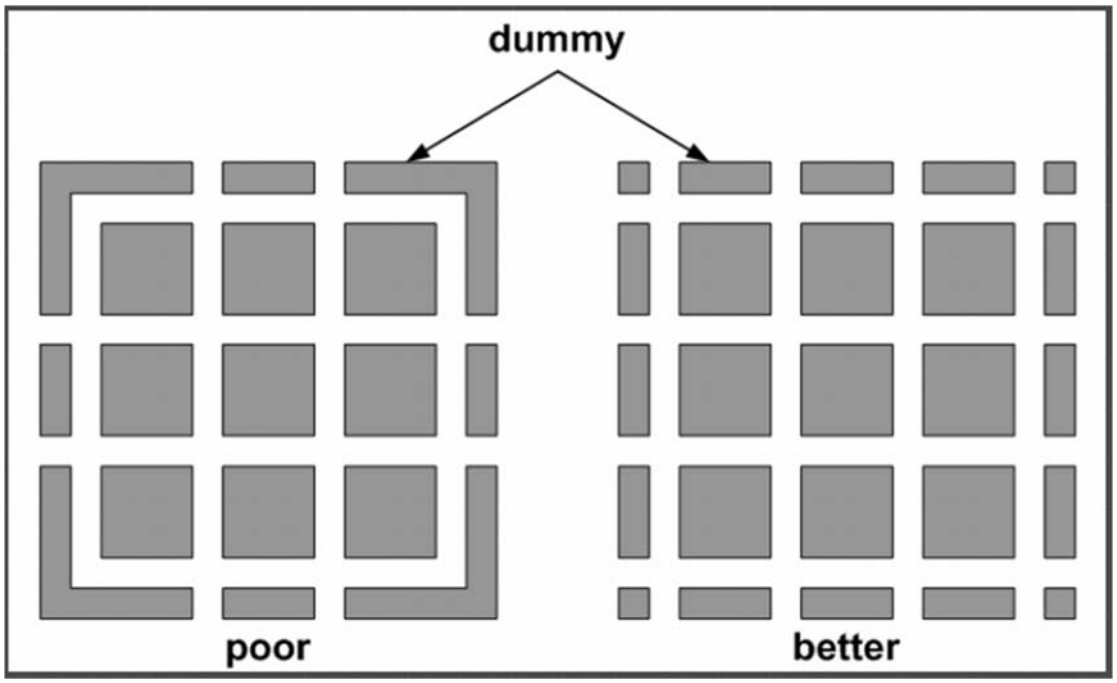


- **Closed-loop Dummies ➔ problem due to inductive interaction with EM fileds**
- **Either break them up or at least have a gap to stop current path**



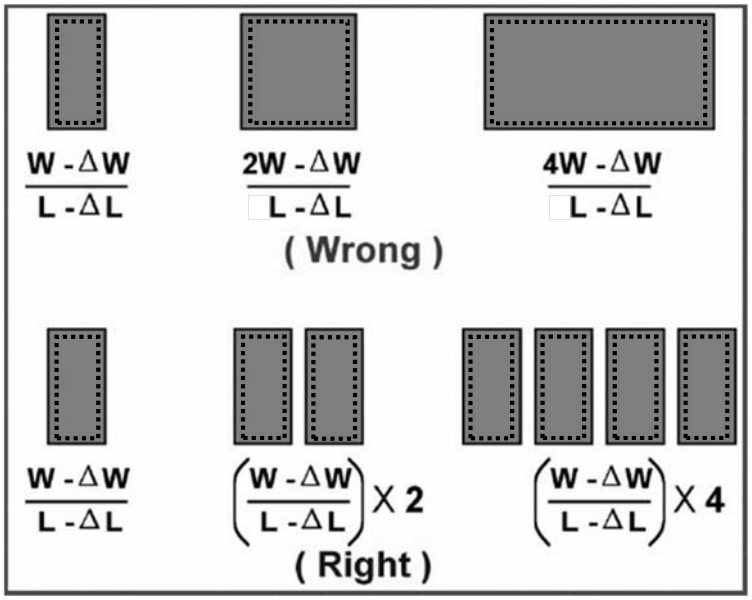
- **Dummies need electrical contact to the Tank**

Dummy Layout for Capacitor

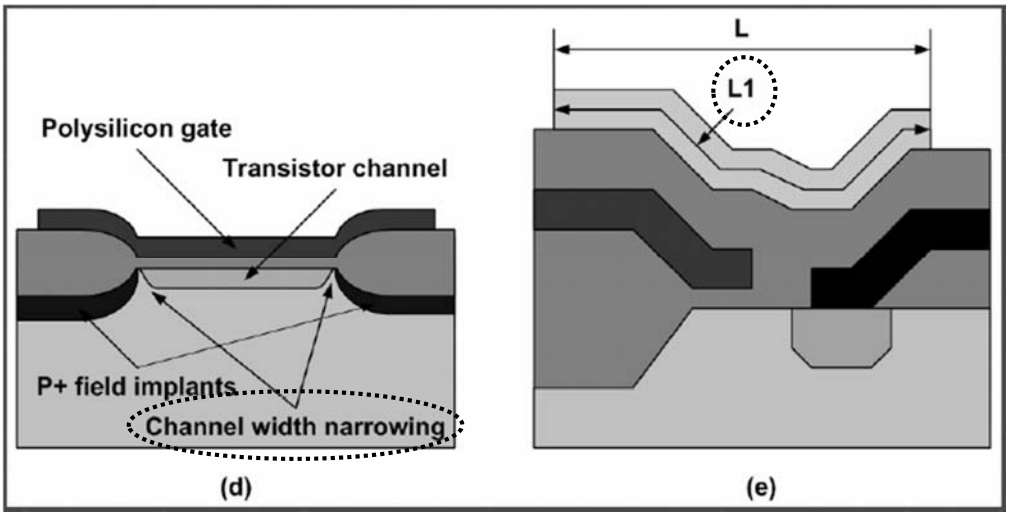


Unit Devices

- To compensate the undercut etching for matching pairs with different nominal sizes
  - Dummies should be used to promise the same boundary condition

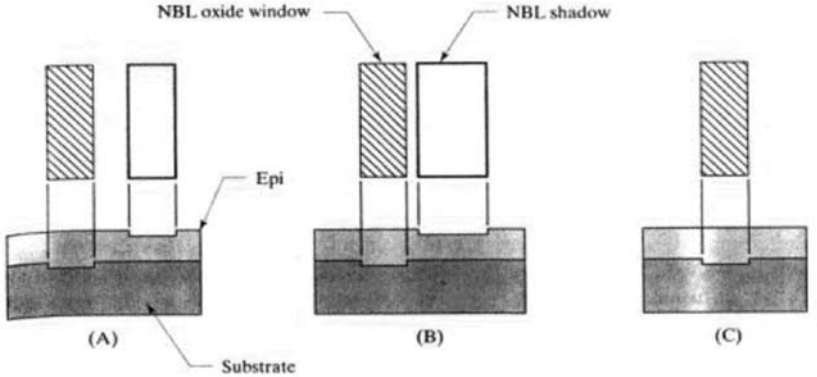


- Various two-dimensional effects causing sizes of realized microcircuit components to differ from sizes of layout masks.
- Error in the pattern size due to tri-dimensional effects.



PATTERN SHIFT

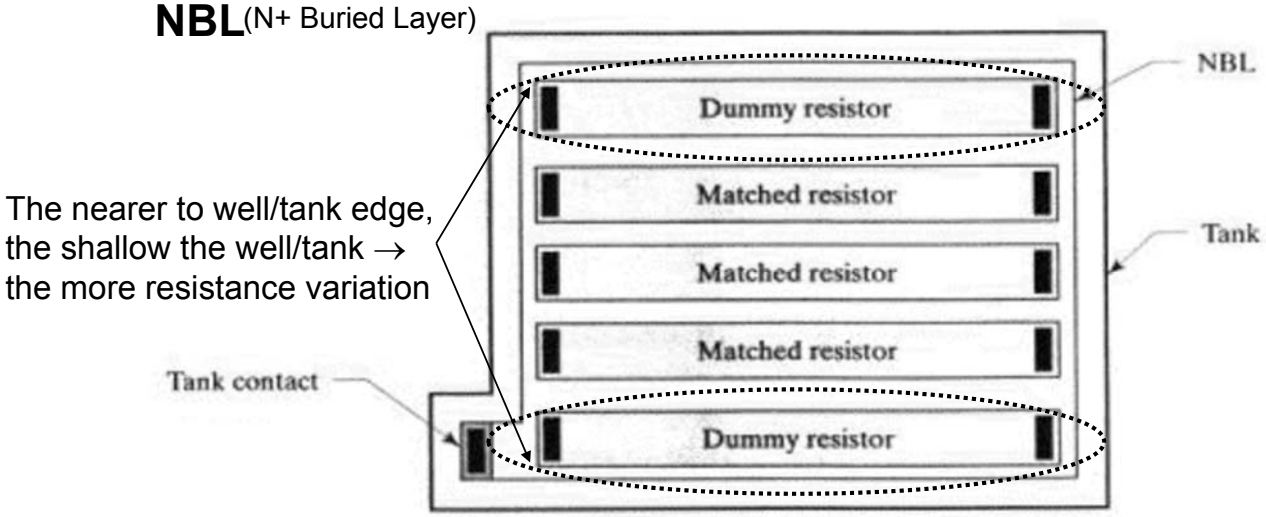
- For example, NBL affects the p-epi layer and the surface discontinuities at p-epi/substrate interface propagates to the p-epi surface but often is displaced. ➔ pattern shift
- *Pattern shift*, pattern distortion**, and** pattern washout



- (111) wafers have severe pattern shift and distortion;
- (100) wafers have distortion and no shift ➔ tilted (100) surface has minimizes the distortion.

Diffusion interactions

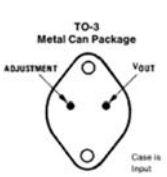
- **Diffused resistors usually are laid in a Tank with NBL**(N+ Buried Layer)

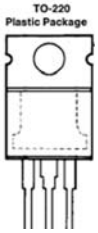


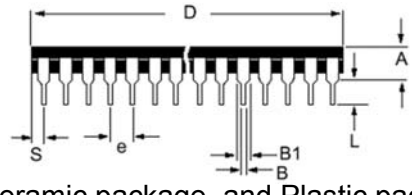
- Edges of diffused areas have diffusion *tails*. ➔ **resistors occupying the ends = slightly different values. ➔ use dummy resisotrs**

Stress Gradients and Package Shifts

- **Packaging can exert stress onto Die.**
- *Metal Can package* **or** *Ceramic package* **➔ lowest stress**
  - **Use metal header plate, mounted using Epoxy**
  - **Solder or gold eutectic mounting ➔ higher stress**
- *Plastic package* **➔ higher stress**
  - **Epoxy resin for mounting** Epoxy [Ep´AksI] 環氧樹脂
  - **Residual stress due to difference in CTE of Si and Epoxy**
  - **Shifts in Offset voltage in OpAmp, Comparators, or output ref. Voltage ➔** *Package shifts*







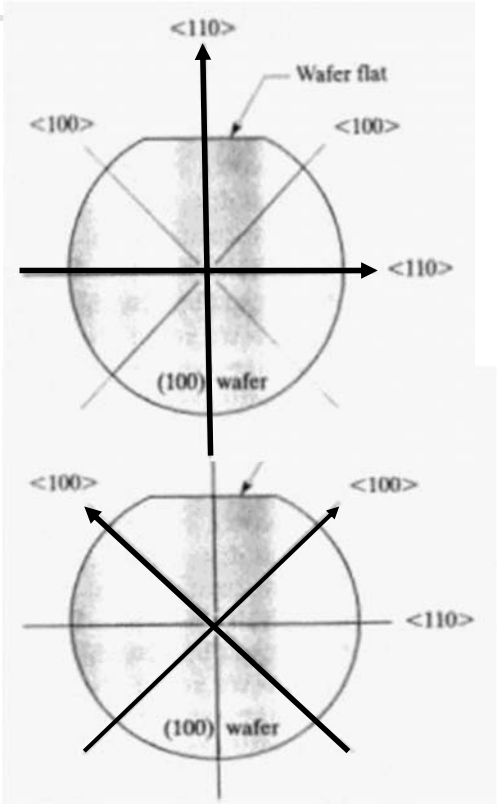
Ceramic package, and Plastic package

- Coefficients of thermal expansion (CTE) for several materials used in packaging integrated circuits.

Material	CTE ppm / °C
Epoxy encapsulation	24
Copper alloys	16~18
Alloy-42	4.5
Molybdenum	2.5
Silicon	2.5

Piezoresistivity

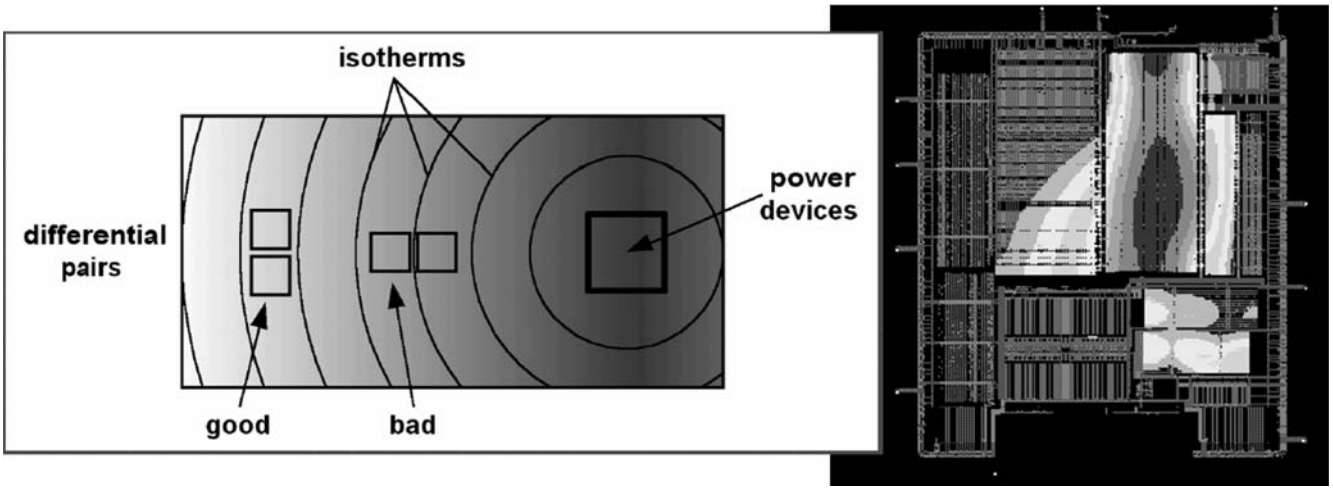
- *N-type (100) Si*
  - **Maximum piezoresistivity along <100>,** *Minimum along <110> ⇒ N-type diffused resistors along <110>*
- *P-type (100) Si*
  - **Maximum along <110>,** *Minimum along <100> ⇒ P-type diffused resistors along <100>*
- **Place matched devices at Regions of lowest stress gradients**



Isothermal Layout

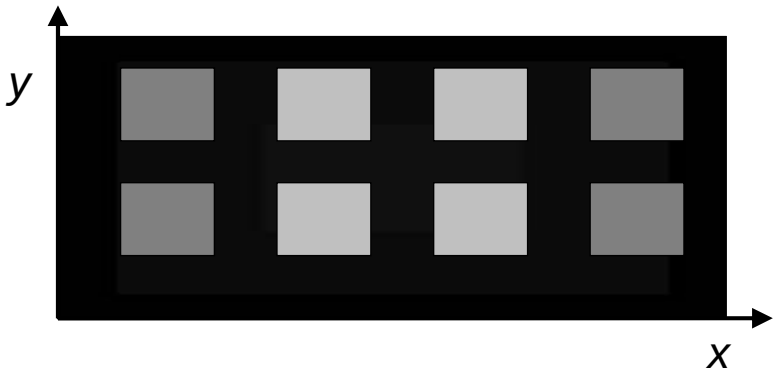
[ˌaɪsəˋθɝml]

- To compensate the thermal gradient effect



Device Matching Mechanisms

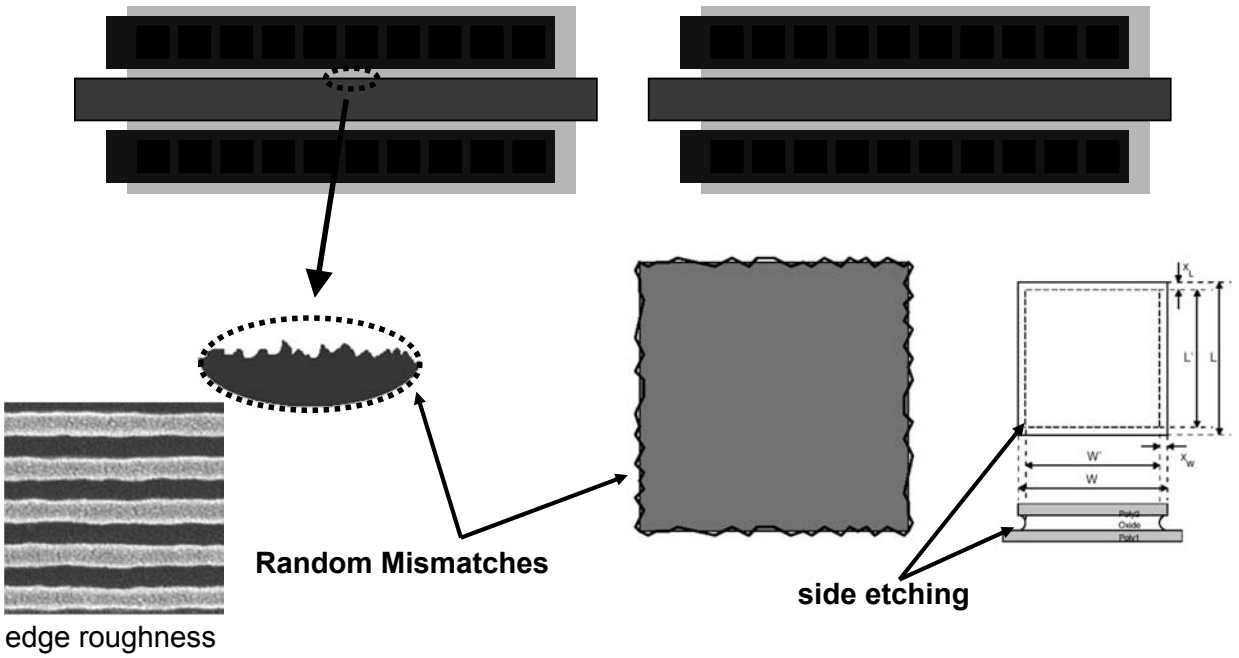
- Spatial effects
  - Wafer-to-wafer
  - Long range
    - Gradients
  - Short range
    - Statistics
- Circuit effects
  - Differential structures
    - Differential pair
    - Current mirror
  - Bias
- Layout effects



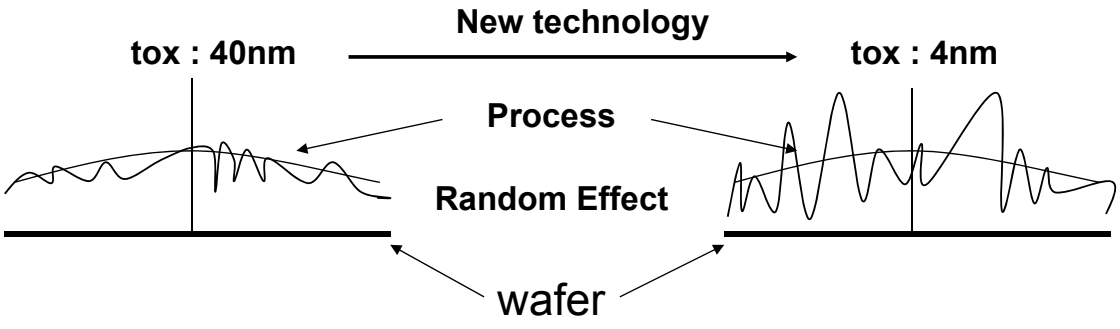
$$f(x,y) = ax^2 + bxy + cy^2 + dx + ey + f$$

a , b , c , d, e, f is fitting constant
x , y is location on wafer

❑ Random Mismatches due to Microscopic Variations



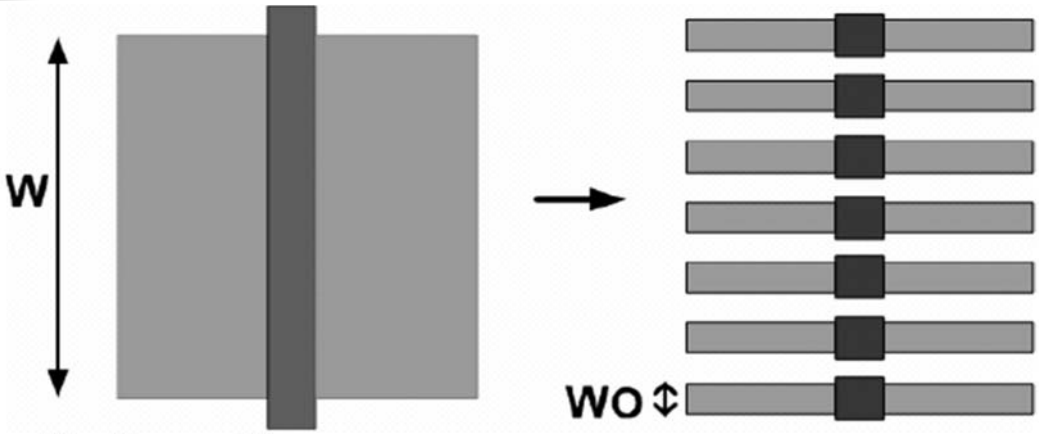
The Increasing Importance of Random Effects



•Mismatch groups closer than ever before, therefore:
REs (Random Effects) assume increased importance compared to previous technology

New models should be able to consider random effects

Wide MOSFET Viewed as a Parallel Combination of Narrow Devices



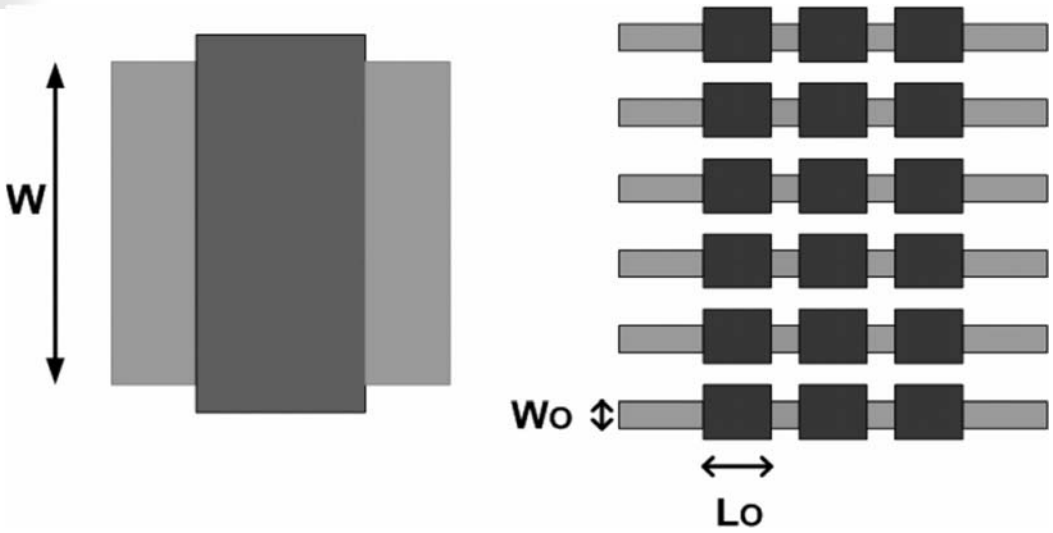
$$W_{eq} \cong \frac{W_1 + W_2 + \ldots + W_n}{n}$$

$$\Delta W_{eq}^2 \cong \frac{\Delta W_1^2 + \Delta W_2^2 + \ldots + \Delta W_n^2}{n}$$

$$\Delta W_{eq} \cong \frac{\sqrt{n\Delta W_0^2}}{n} = \frac{\Delta W_0}{\sqrt{n}}, \quad \Delta W_0 = \text{statistic width variation of a transistor with } W=W_0$$

(Law of Large Numbers for uncorrelated events)

Large MOSFET Viewed as a Combination of Small Devices



- **μC_{ox} and V_{TH} suffer from mismatch↓ as WL ↑**

$$\Delta V_{TH} = \frac{A_{V_{TH}}}{\sqrt{WL}} \quad \Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}$$

$A_{V_{TH}}$ and A_K : proportional factor

Random Mismatch Modeling

- random matching is caused by many single events of a mismatch generating process (ion implantation, diffusion, grains).
- the effect of a single event on a parameter is so small that the contributions of events can be summed.
- the effects have a correlation distance that is much smaller than the active area of the components.
- Occurrences of these events are mutually independent. (Poisson statistics applicable)

$$\sigma_{\Delta P} = \frac{A_{\Delta P}}{\sqrt{W \times L}}$$

P: physical parameter, eg: V_T, β …

$A_{\Delta P}$: area dependent coefficient

Mismatch Model

- What is modeled?
  - Short-range, random processes, e.g.
    - Dopant fluctuations
    - Mobility fluctuations
    - Oxide trap variations (Si dangling bond) 搖擺;懸蕩
- What is NOT modeled?
  - Batch-to-batch or wafer-to-wafer variations
  - Long-range effects such as gradients
  - Electrical, lithographic, or timing offsets

References

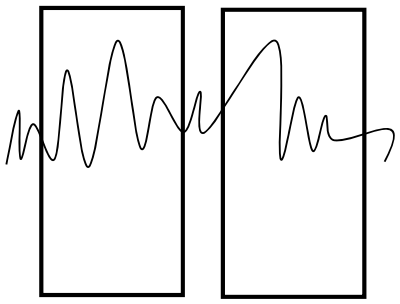
- M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits,* vol. 24, pp. 1433 - 1439, October 1989.
  - Mismatch model
  - Statistical data for 2.5μm CMOS
- Jeroen A. Croon, Maarten Rosmeulen, Stefaan Decoutere, Willy Sansen, Herman E. Maes; *An easy-to-use mismatch model for the MOS transistor*, IEEE Journal of Solid-State Circuits, vol. 37, pp. 1056 - 1064, August 2002.
  - 0.18μm CMOS data
  - Qualitative analysis of short-channel effects on matching

Mismatch Statistics

- Composed of many single events

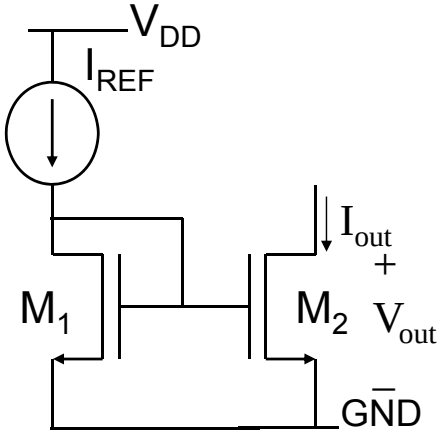
  E.g. dopant atoms
- Individual effects are small

  $\Rightarrow$ linear superposition applies
- Correlation distance << device dimensions
  - $\Rightarrow$ Mismatch has Gaussian distribution, zero mean



MOSFET Mismatch Parameter

- Experimental result applies to one particular configuration
- What about:
  - Device size
    - W
    - L
    - Area
  - Bias
    - V_{GS} [prɑk`sɪmətɪ]極接近
  - Physical proximity :diffusion, etch rate
  - …
- Need parameterized model



Experiment:

$\Delta I_D/I_D$=1%

Geometry Effects

- **Pelgrom model**
  - nominally identical devices with physical parameter P (eg: V_{TH}, β)

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2$$

$\sigma^2(\Delta P)$: standard deviation of P

WL : active gate area

D_x : distance between device centers

A_P : measured area dependent coefficient

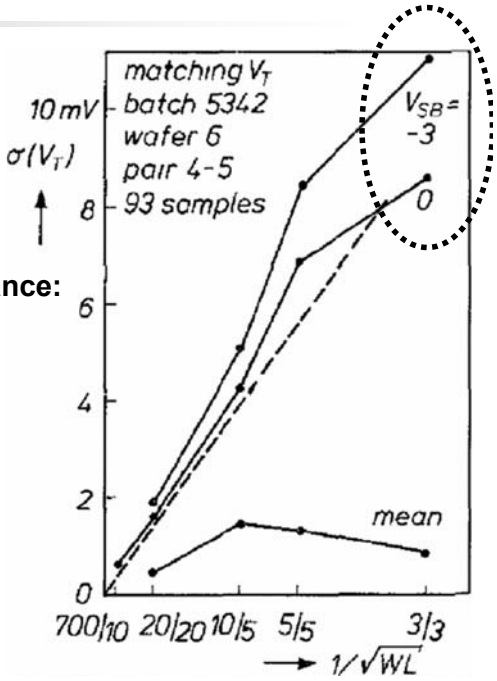
S_P : measured distance dependent coefficient,

Example: V_{TH}

$$\sigma^2(\Delta V_{TH0}) = \frac{A^2_{P,V_{TH0}}}{WL} + S^2_{P,V_{TH0}} D^2_x$$

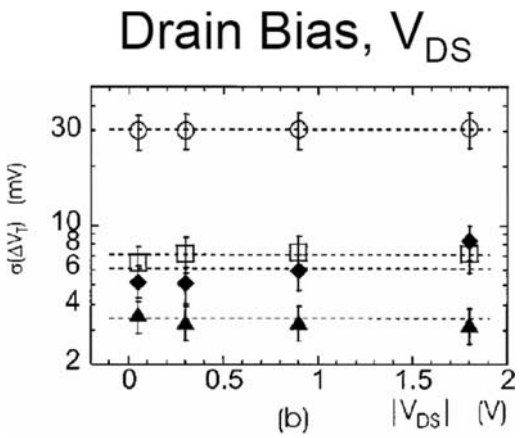
$$A_{P,NMOS} \cong 30mV\,\mu m \ (2.5\mu\text{m CMOS process})$$

$$A_{P,PMOS} \cong 35mV\,\mu m$$



benchmark for MOSFET V_T mismatch fluctuation performance:

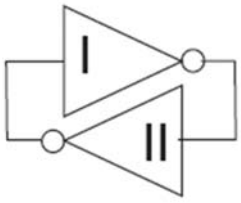
1mVμm per nm gate oxide thickness

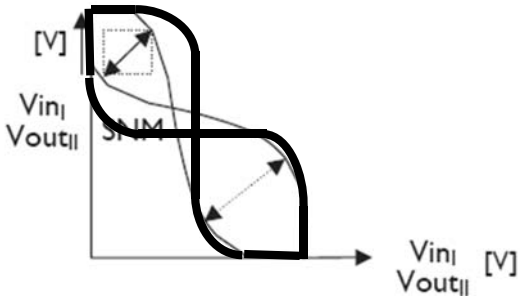


ΔV_{TH0} virtually independent of V_{DS}

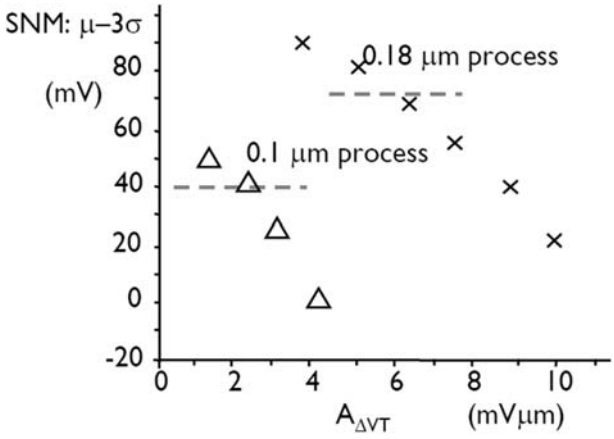
Mismatch Viewed in The Digital World

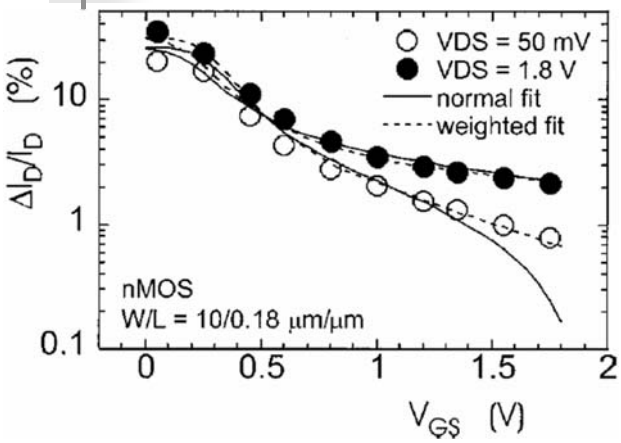
Static Noise Margin SRAM cell

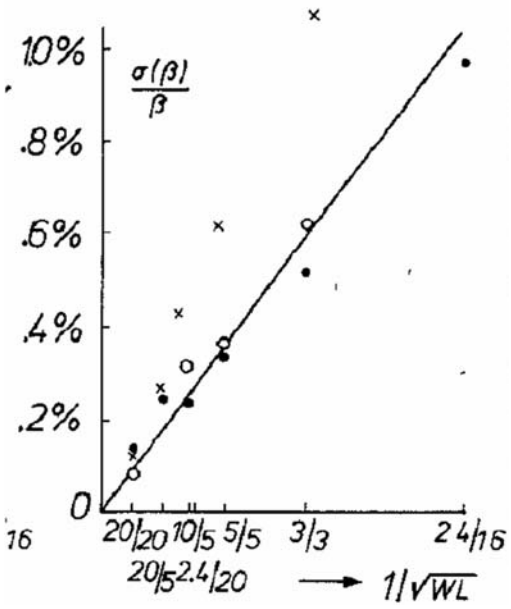




- Static Noise Margin: size of "eye" defines robustness
- good control of $A_{\Delta VT}$ becomes yield issue !!!







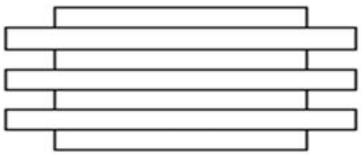
- Current Matching, $\Delta I_D/I_D$
  - Strong bias dependence
  - V_T mismatch has a larger effect at low bias levels, while β mismatch dominates at high currents
  - don't let V_{gs}-V_T drop too much
    - keep it above 200mV

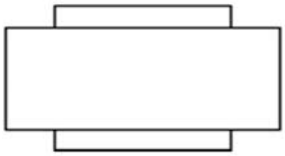
- Current factor

$$\beta = \mu C_{OX} \frac{W}{L}$$

Edge Effects

- Edge Model





$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(C_{ox})}{C_{ox}^2} + \frac{\sigma^2(\mu_n)}{\mu_n^2}$$

for $\sigma^2(W) \propto 1/W$ and $\sigma^2(L) \propto 1/L$

this simplified to

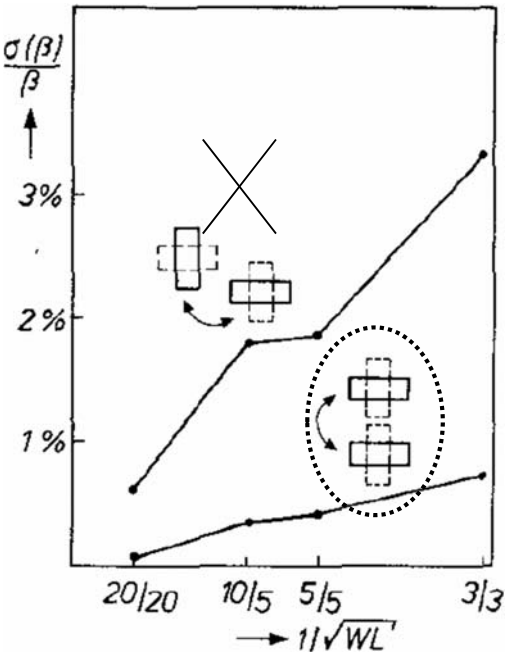
$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_L^2}{WL^2} + \frac{A_W^2}{W^2 L} + \frac{A_{C_{ox}}^2}{WL} + \frac{A_\mu^2}{WL} + S_\beta^2 D^2$$

If area A fixed, let $W = kL \Rightarrow W = \sqrt{kA}, L = \sqrt{A/k}$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_L^2}{\sqrt{k}\,A^{1.5}} + \frac{A_W^2}{\frac{1}{\sqrt{k}}A^{1.5}} + \frac{A_{C_{ox}}^2}{A} + \frac{A_\mu^2}{A} + S_\beta^2 D^2$$

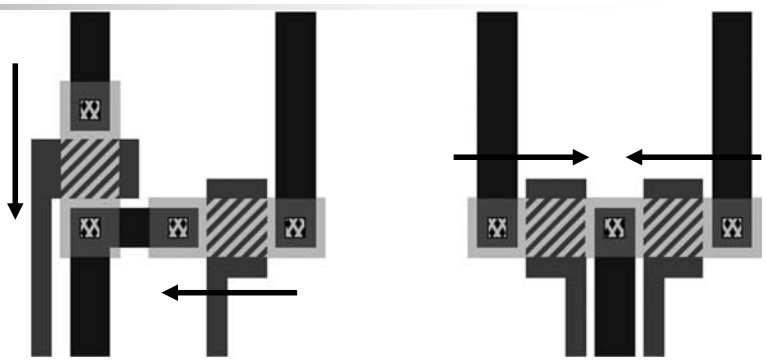
$k \to 0$ or $k \to \infty$, $\sigma(\beta) \to \infty$, $k_{optimum} = 1$

Orientation Effect



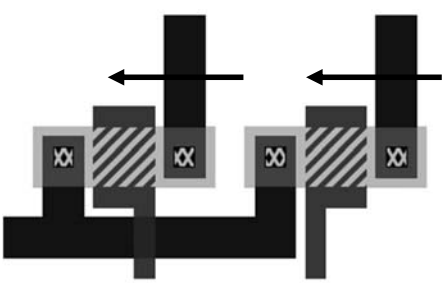
- Several % mismatch error
  For example, tilted wafer ➔ as much as 5% in matching errors
- Si and transistors are not (perfectly) isotropic 等向性的
  ⇒ keep direction of current flow same!
- Eliminate mismatch arising from:
  - Anisotropic substrate
  - Anisotropic process steps
  - Packaging-induced stresses

- Example: Differential Pair

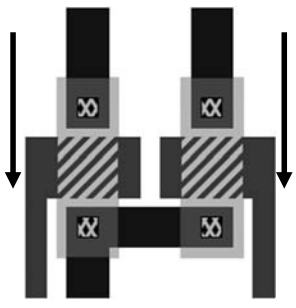


Ugly

Bad

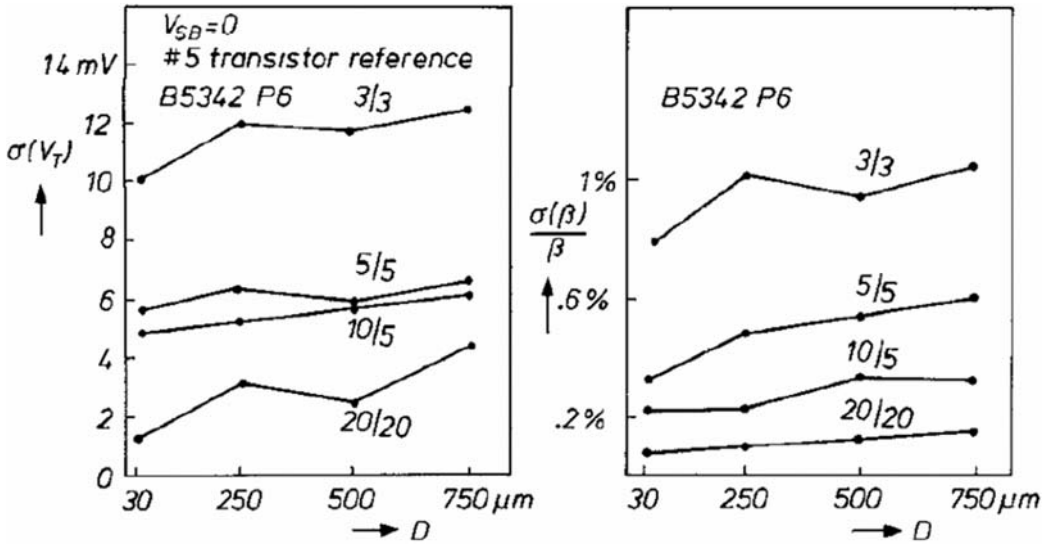


Fair



Good (same orientation & compact)

Distance Effect

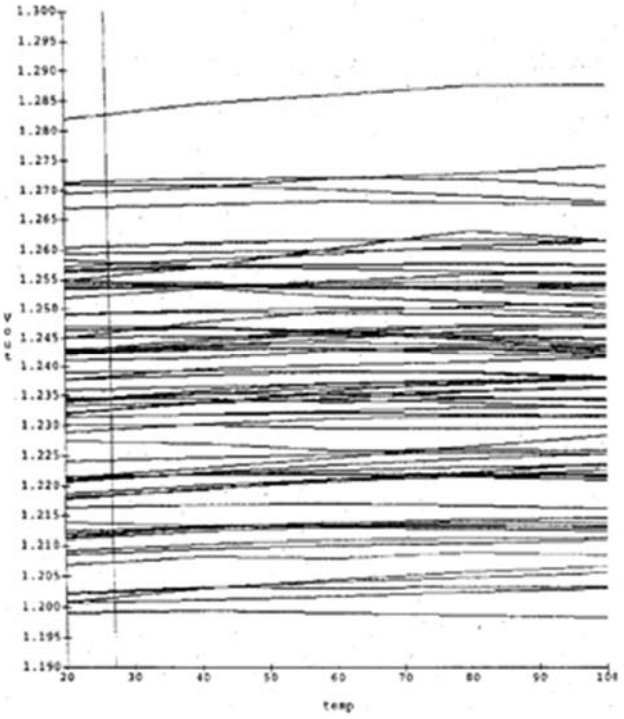


Model Summary

- **matching data for NMOS and PMOS transistor pairs in a 50nm gate oxide, 2.5µm n-well process**

parameter	n-channel s.d.	p-channel s.d.	unit
A_{VT0}	30	35	mV µm
A_β	2.3	3.2	% µm
A_K	16×10^{-3}	12×10^{-3}	$V^{0.5}$ µm
S_{VT0}	4	4	µV/µm
S_β	2	2	10^{-6}/µm
S_K	4	4	$10^{-6}V^{0.5}$/µm

Bandgap Reference



- σ_{VBG} = 25 mV
- Dominated by amplifier offset
- Area – offset tradeoff

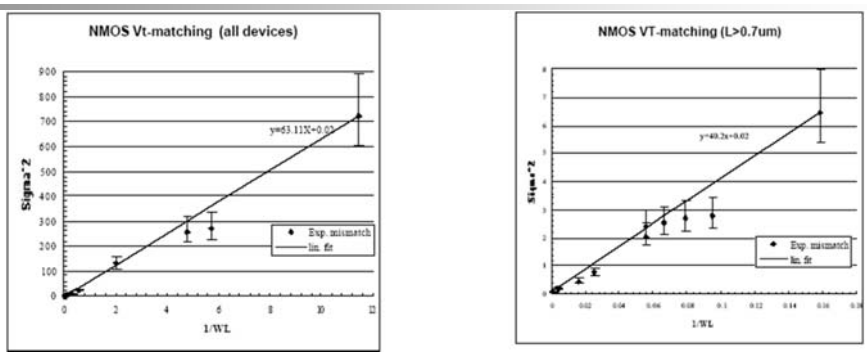
Measured Matching data for NMOS and PMOS transistor pairs

- **C035 - C025 MOS transistor Matching results**

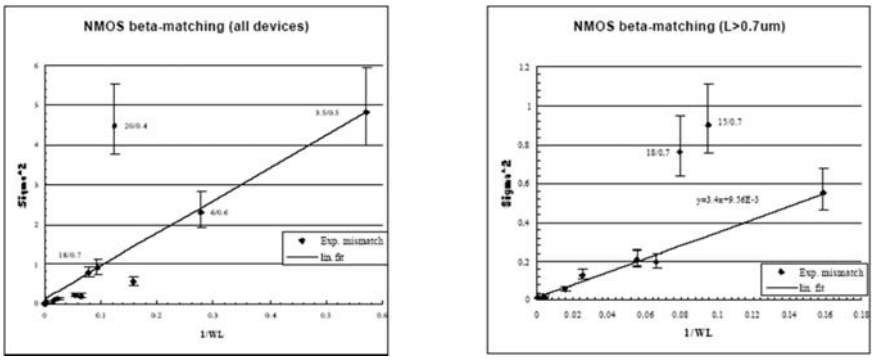
ALCATEL

	C035 Technology			C025 Technology		
	L	A^2_{VT} & A^2_{β}	C^2_{VT} & C^2_{β}	L	A^2_{VT} & A^2_{β}	C^2_{VT} & C^2_{β}
NMOS_VT		124.89	-0.12		63.11	0.02
NMOS_Beta		9.21	0.014		8.21	0.11
PMOS_VT		133.93	-7.61		64.83	2.81
PMOS_Beta		4.03	0.66		3.12	0.67
NMOS_VT	L>0.7μ	147.46	-0.37	L>0.7μ	40.2	0.08
NMOS_Beta	L>2μ	6.22	0.03	L>2μ	3.38	0.0096
PMOS_VT	L>0.7μ	78.45	-0.25	L>0.7μ	54.36	0.06
PMOS_Beta	L>2μ	5.82	0.11	L>2μ	2.98	0.0093

May be caused by the normal field mobility reduction for L < 2μm



C025 - NMOS V_T Matching without and with L-restrictions



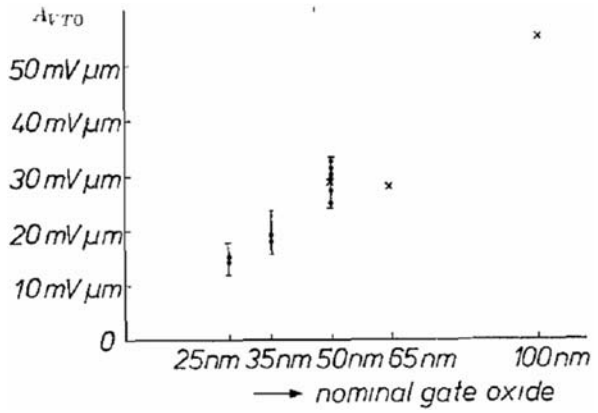
C025 - NMOS β Matching without and with L restrictions

Measured Matching data for Resistors

	C035 technology		C025 technology	
	A^2	S^2	A^2	S^2
N+ MOPO	89.9	0.087	45.5	0.091
P+ MOPO	15.82	0.018	8.72	**0**
N+ AA	68.37	-0.11	**---**	**---**
N-well	0.323	0.003	**---**	**---**

Process Dependence

- Example: ΔV_{TH} vs. t_{ox}
  - V_{TH} matching appears strongly correlated with t_{ox}
- Reason?
  - t_{ox} is not only difference
  - Doping concentration?



MOS Transistor Matching

- **MOS transistors can be optimized either for voltage matching or for current matching, but not for both !**
- **Voltage matching**
  - **Suppose M1,M2 operate at equal drain currents. Then, the possible voltage mismatch:**
    OFFSET Voltage: $\Delta V_{GS} = \Delta V_t - \mathbf{V_{gst}}\,(\Delta k/2\mathbf{k_2})$
    - To minimize ΔVGS:
    - use **large W/L** and low operating currents.
    - minimize Vgst: Vgst = 0.1 volts or less
- Current matching
  - $I_{D2}/I_{D1} = k_2/k_1\,(1 + 2\Delta V_t/\mathbf{V_{gst}})$
  - $\Delta I_d / I_d = \Delta k/k + 2\Delta V_t/V_{gst}$
  - $\Rightarrow$ use reasonably large Vgst: V_{gst} = 0.3 V or more

Strategies for Matching Layout

- Minimize systematic errors
  - Systematic Mismatch
    - refers to a spatial gradient in component values.
    - be caused by processing gradients and inadequate layout
  - Geometry
    - Proximity effects: diffusion, etch rate
    - Orientation
  - Gradients
    - Process
    - Temperature
    - Stress
- Ref: A. Hastings, "The art of analog layout," Prentice Hall, 2001

Layout Tradeoffs

- Matching often involves tradeoffs:
  - Increased channel length
  - Increased circuit area
  - $\Rightarrow$ increased power dissipation, reduced speed, …
- Determine required level of matching
  - Minimal:
    - $3\sigma_{Vos} > 10mV$, $3\sigma_{\Delta ID/ID} > 2\%$
    - Unit elements, matched orientation, compact layout
    - often used for constructing bias current networks, inadequate for voltage matching applications
  - Moderate:
    - $3\sigma_{Vos} > 2mV$, $3\sigma_{\Delta ID/ID} > 0.1\%$
    - Apply most or all layout rules, Useful for constructing **input stages of noncritical op-amps and comparators**
  - Precise:
    - Trimming or self-calibration

Design for Low Offset and Drift

- global performance of analog circuit is strongly dependent on absolute and relative accuracy of basic component
- accuracy depends on relevant properties of materials and geometry of components
- absolute accuracy can be controlled at technology level only
- relative inaccuracy, due to gradients and local variation, controlled at technology level, can be compensated with suitable layout techniques
- parameters depend on different technology steps, assume to be statistically independent, by summing up various error contribution
- use dimensions larger than ones indicated to have inaccuracy not dominated by geometry parameters
- distance of matched elements increases, matching accuracy worsens

- compensate gradient effects with interdigitized and common centroid layout
- matched devices operated at same temperature, realign to same isothermal [AIsD´OGml]
- increasing sizes of devices for better matching
- minimum distance from each other
- layout devices with same orientation with respect to silicon crystal, putting them in parallel, current tack same direction (MOS has different mobility in different orientation)
- same area to perimeter ration
- easier to match round devices than square devices, the number of bends and corners in the connection between pairs must be the same

The Guidelines for Matching Layout

- 1. Unit elements
  - Equal L
  - Equal W (Use M's that are even, preferably factors of 4)
- 2. Large Active Areas (Moats)
  - Reduce random variations ($\propto A^{-0.5}$)
  - Moderate matching usually requires active areas of several **$10^2 \mu m^2$**, while precise matching requires several **$10^3 \mu m^2$**
- 3. Bias Point
  - Voltage matching (differential pair):
    - Small Vgst (<0.1V) by using larger W/L ratios
    - Long L (reduce line width variations and channel length modulation, **Mismatch ~ ΔV_{DS} / L, L ~ 15-25 μm**, adequate for *noncritical* use such as current distribution network)
  - Current matching (mirror):
    - Large Vgst (>0.3V, moderate matching with Vgst >0.5V)
    - Same V_{DS}

- **4.** Same Orientation
  - Transistors "look" symmetrical, real devices are not:
    - Silicon is not isotropic 等向性的
    - Implants are not isotropic
  - each transistor contains an equal number of segments oriented in each direction
  - What about ac?
- 5. Compact Layout
  - Minimize stress and temperature variations & random fluctuations
  - Avoid poor MOSFET aspect ratio
    - E.g. W/L = 1000/0.35
    - Use fingers: 50/0.35, M=20

      $\Rightarrow$ **square layout**

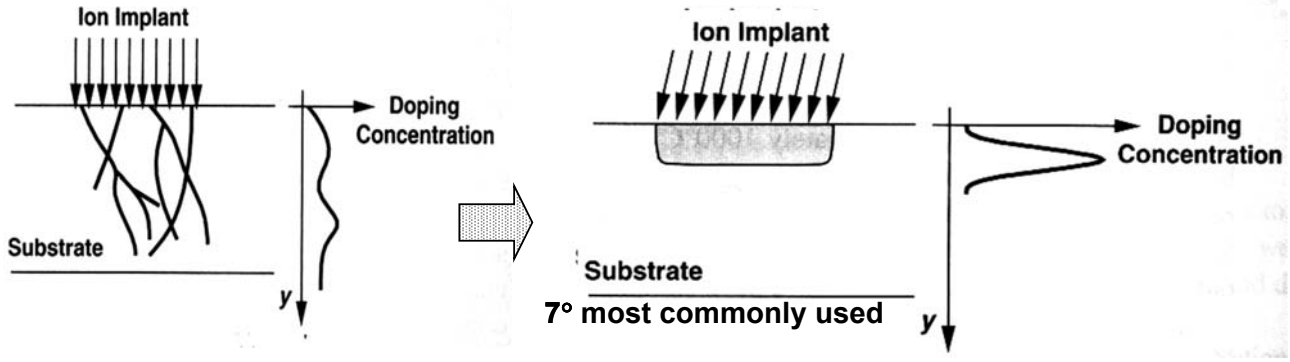
6. Common Centroid Layout

- Cancels linear gradients
  - Make D_x=0 in **Pelgrom model**
- Required for moderate matching
- Common-centroid rules:
  - Coincidence
    - The centroids of the matched devices must at least approximately coincide
  - Symmetry
    - The array should be symmetric with respect to both X- and Y-axes
  - Dispersion
    - The segments of each device should be distributed throughout the array as uniformly as possible
    - High dispersion reduces sensitivity to higher order (nonlinear) gradients, EG:
      - **ABBAABBA: 2 runs (ABBA) of 2 segments (AB, BA)**
      - **ABABBABA: 1 run of 2 segments (AB, BA) ⇒ ABABBABA has higher dispersion (preferable)**

- Compactness
  - The array should be as compact as possible. Ideally, nearly square
  - 2D patterns
    - **Better approximation of square layout**
    - **Usually higher dispersion possible, e.g.**

$$\begin{matrix} {}_{D}A_{S}B_{D} \\ {}_{D}B_{S}A_{D} \end{matrix} \qquad \begin{matrix} {}_{D}A_{S}B_{D}B_{S}A_{D} \\ {}_{D}B_{S}A_{D}A_{S}B_{D} \end{matrix} \qquad \begin{matrix} {}_{D}A_{S}B_{D}B_{S}A_{D} \\ {}_{D}B_{S}A_{D}A_{S}B_{D} \\ {}_{D}A_{S}B_{D}B_{S}A_{D} \\ {}_{D}B_{S}A_{D}A_{S}B_{D} \end{matrix}$$

- Orientation
  - Stress induced mobility variations: several percent error
    - **Tilted wafers: ~5% error**
  - matched device should possess equal Chirality 手性(左手性和右手性)



Define Chirality of a Transistor:

Chirality = (the fraction of right-oriented segments) – (the fraction of left-oriented segements)

Examples:

Three right-oriented and One left-oriented segements = ¾ - ¼ = ½

Nine right-oriented and Three left-oriented segements = 9/12 – 3/12 = ½

➔ they can be matched together w/o worry of orientation-dependent mismatch.

❑ Common-Centroid Layout Procedure

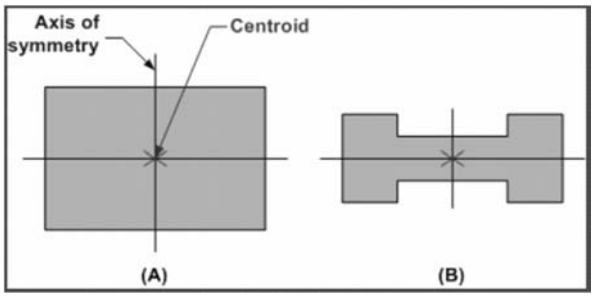
- Determine groups of matched components
  - Depends on circuit function, eg:
    - ⊠ All transistors in a mirror
    - ⊠ Diff-pair and load in an amplifier
    - ⊠ Should they be matched individually or jointly?

- Divide into segments
  - Unity element
  - Avoid small (<70%) fractional elements if no GCD (greatest common divisor)
- Apply everything you've learned to layout: interdigitization, stacked layout, …

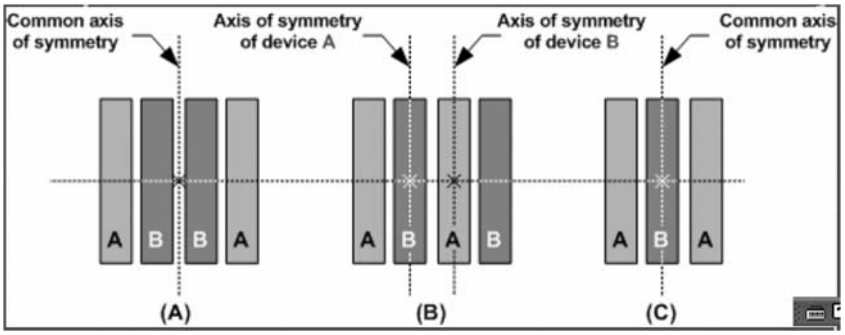
❑ 7. Dummy Segments

- Place dummy segments at ends of arrayed devices
- takes out poly etch loading and mask misalignment effects
- the dummy gates and the actual gates must be equal-spacing
- dummy gates must be properly biased to prevent channel formation beneath them and to prevent spurious signal ⇒ connected to **backgate (Body) potential usually**

- Locating (a) the centroids of a rectangle and (b) dogbone resistor.



- **Examples of one-dimensional common-centroid arrays.**

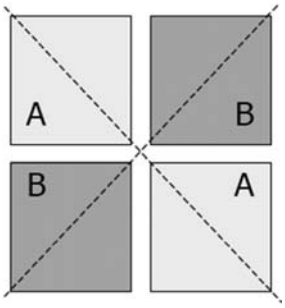


- **Sample interdigitation patterns for arrays having one axis of symmetry.**

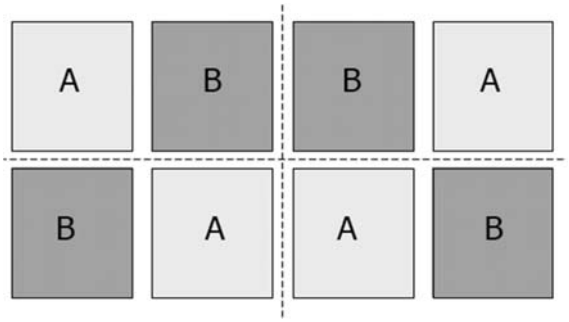
A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCDBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAAB	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAAABAAABA*	AABAABAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

- **Note: not all the patterns permit a stacked layout!**

❑ Examples of two dimensional common centroid arrays.



Cross coupling



Tiling: more sensitive to high-order gradients

❑ Sample interdigitation patterns for two-dimensional common-centroid arrays.

ABBA	ABBAABBA	ABBAABBA	ABBAABBA
BAAB	BAABBAAB	BAABBAAB	BAABBAAB
		ABBAABBA	BAABBAAB
			ABBAABBA
ABA	ABAABA	ABAABA	ABAABAABA
BAB	BABBAB	BABBAB	BABBABBAB
		ABAABA	BABBABBAB
			ABAABAABA
ABCCBA	ABCCBAABC	ABCCBAABC	ABCCBAABC
CBAABC	CBAABCCBA	CBAABCCBA	CBAABCCBA
			CBAABCCBA
			ABCCBAABC
AAB	AABBAA	AABBAA	AABBAA
BAA	BAAAB	BAAAB	BAAAB
		AABBAA	BAAAB
			AABBAA

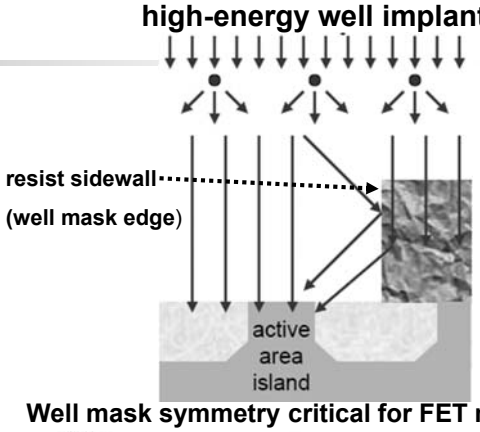
8. Stress Gradients

- Global: from package
  - Place devices in areas of low stress
  - Generally center of chip
  - At odds mixed-signal floor plans
- Local: metalization
  - Do not route metal across active area
  - If unavoidable: add dummies so that each device sees same amount of metal

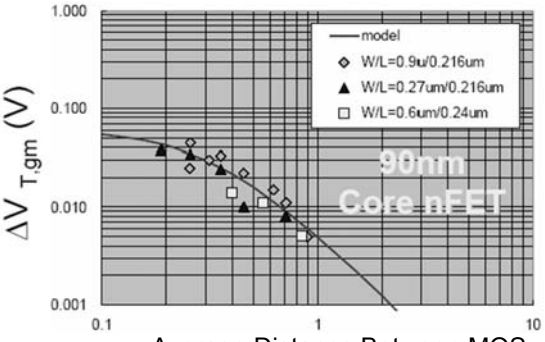
9. Contacts

- Contacts in the active Gate region Induce threshold mismatch
  - extend the gate poly beyond the moat and place the gate contacts over thick-field oxide
- Annular MOSFETs ➔ particularly problem with gate contatcs
  - use identical arrangements, and minimal number of small contacts

Well Proximity Effect



Well mask symmetry critical for FET matching



Average Distance Between MOS Channel & Well Mask Edge
Source: TSMC (CICC 2005)

10. Junctions

- Keep all junctions and deep diffusions away from transistors (except S/D)
  - Extend well boundary at least 2x junction depth
  - Just because the layout rule permits it, minimum spacing is not always the best solution
    - ⌧ Not all spaces are critical for overall layout area

11. Oxide thickness

- Devices with thinner oxide usually exhibit better matching
  - Use minimum t_{ox} devices for best matching if the process offers a choice

- 12. NMOS vs PMOS
  - NMOS usually exhibit better matching than PMOS
  - Random matching, 0.18μm data:
    - VTH of PMOS has better matching (2x)
    - β of NMOS matches better (4.5x !)
- 13. Power Devices
  - Power devices create temperature gradients and inject carriers into the substrate
    - $dV_{TH} / dT = -2mV/^{\circ}C$!
  - Keep matched devices away from power sources (>50mW)
  - Beware of "Temperature Memory Effect":
    - Use common-centroid layout for matched devices with different current density

- **14.** Make clean and well balanced routing
- **15.** Route currents a long way, not voltages - IR drops can cause big mismatches
- 16. avoid routing metal across the active gate region of precisely matched MOS transistors
  - **Leads may route across moderately matched MOS transistors, but additional dummy leads should be added so that every section of the array of matched devices is crossed at the same location along its channel by an identical**
  - **length of lead**

- **17. Use thin-oxide devices in preference to thick-oxide devices**
  - *Some processes offer multiple thicknesses of gate oxides*
  - **transistors with thinner gate oxides generally exhibit better matching characteristics**
- **18.** Connect the ***gate fingers of moderately and precisely matched*** transistors using metal rather than poly
  - To prevent the proximity effects when connecting multiple gates with poly
  - Poly connectors on either side of transistor can be used instead

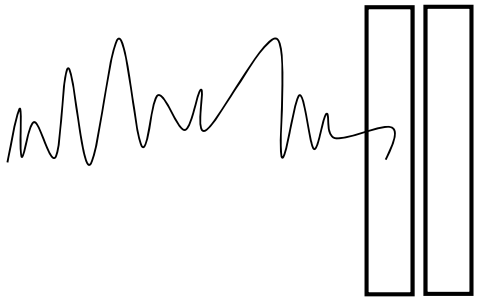
Layout-Based Statistical Modeling for the Prediction of the Matching Properties of MOS Transistors

Massimo Conti, Paolo Crippa, Simone Orcioni, and Claudio Turchetti
IEEE TRANSACTIONS ON CIRCUITS AND SYSREMS, VOL, NO 5,MAY 2002

A9302011 學生: 任永星

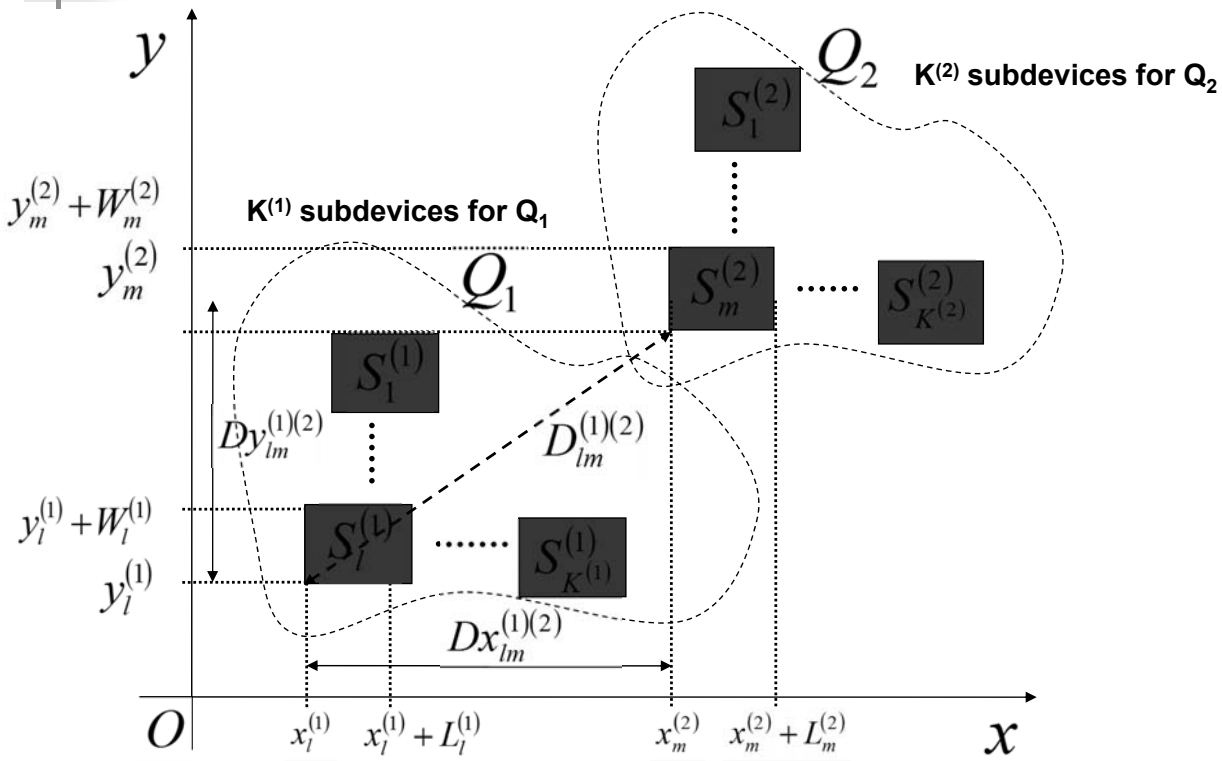
Outline

- Mismatch Modeling
  - Mean value
  - Covariance matrix
  - standard deviation
  - Gaussian function
- Experimental characterization
- Transistor pair structure
- Yield of differential amplifier



If device dimensions < correlation distance, Then what?

Mismatch Modeling(1/4)



Mismatch Modeling (2/4)

- $\alpha(x,y)$ be a process parameter (such as gate oxide thickness t_{OX}) depend on two coordinates (x,y).
- There are a couple of MOS transistors Q_1 and Q_2, each partitioned as a set $K^{(k)}$ of subdevices $S_l^{(k)}$ occupying a rectangular surface $q_l^{(k)}$.
- Mean of random variable $\hat{\alpha}_k$:

$$\hat{\alpha}_k = \frac{1}{\sum_{l=1}^{K^{(k)}} W_l^k L_l^{(k)}} \cdot \sum_{l=1}^{K^{(k)}} \int_{x_l^{(k)}}^{x_l^{(k)}+L_l^{(k)}} \int_{y_l^{(k)}}^{y_l^{(k)}} \alpha(x,y)dxdy = \frac{1}{A^{(k)}} \sum_{l=1}^{K^{(k)}} \int_{S_l^{(k)}} \alpha(x,y)dS$$

Mismatch Modeling-(3/4)

Mean and Covariance

- The expectation value of mean are defined as:

$$m_{\hat{\alpha}_k} = E\{\hat{\alpha}_k\} = \frac{1}{A^{(k)}} \sum_{l=1}^{K^{(k)}} \int_{S_l^{(k)}} m_\alpha(x,y)dS; k = 1,2 \qquad (1)$$

- The 2x2 covariance matrix is defined as follow:

$$[C_{\hat{\alpha}\hat{\alpha}}]_{ij} = \frac{1}{A^{(i)}A^{(j)}} \bullet \sum_{l=1}^{K^{(i)}} \sum_{m=1}^{K^{(j)}} \int_{S_l^{(i)}} \int_{S_m^j} [R_{\alpha\alpha}(x',y',x'',y'') - m_\alpha(x',y') \bullet m_\alpha(x'',y'')]dS'dS''$$

Where $R_{\alpha\alpha}(x',y';x'',y'') = E\{\alpha(x',y')\alpha(x'',y'')\}$ (2)

Mismatch Modeling-(4/4)

Standard Deviation and Gaussian Function

Standard Deviation:

$$\sigma^2_{\Delta\hat{\alpha}} = \left[C_{\hat{\alpha}\hat{\alpha}}\right]_{11} + \left[C_{\hat{\alpha}\hat{\alpha}}\right]_{22} - 2\left[C_{\hat{\alpha}\hat{\alpha}}\right]_{12} = 2\left(\left[C_{\hat{\alpha}\hat{\alpha}}\right]_{11} - \left[C_{\hat{\alpha}\hat{\alpha}}\right]_{12}\right) \quad (3)$$

Gaussian Function:

$$R(\Delta\alpha) = \frac{1}{\sqrt{2\pi}\sigma_{\Delta\alpha}} \exp\left[-\frac{(\Delta\alpha - \Delta\hat{\alpha})^2}{2\sigma^2_{\Delta\alpha}}\right] \quad (4)$$

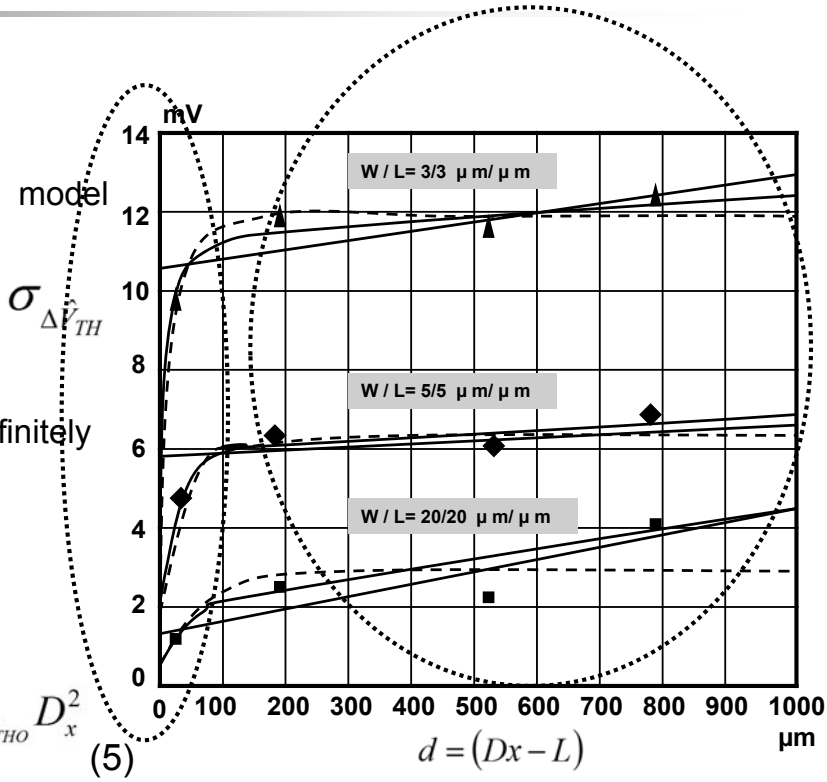
Experimental characterization

- Red- Pelgrom's model
  Blue- autocorrelation-based model
  Black- Experimental data

- Saturation constraint:
  Variance can't increase indefinitely with distance.

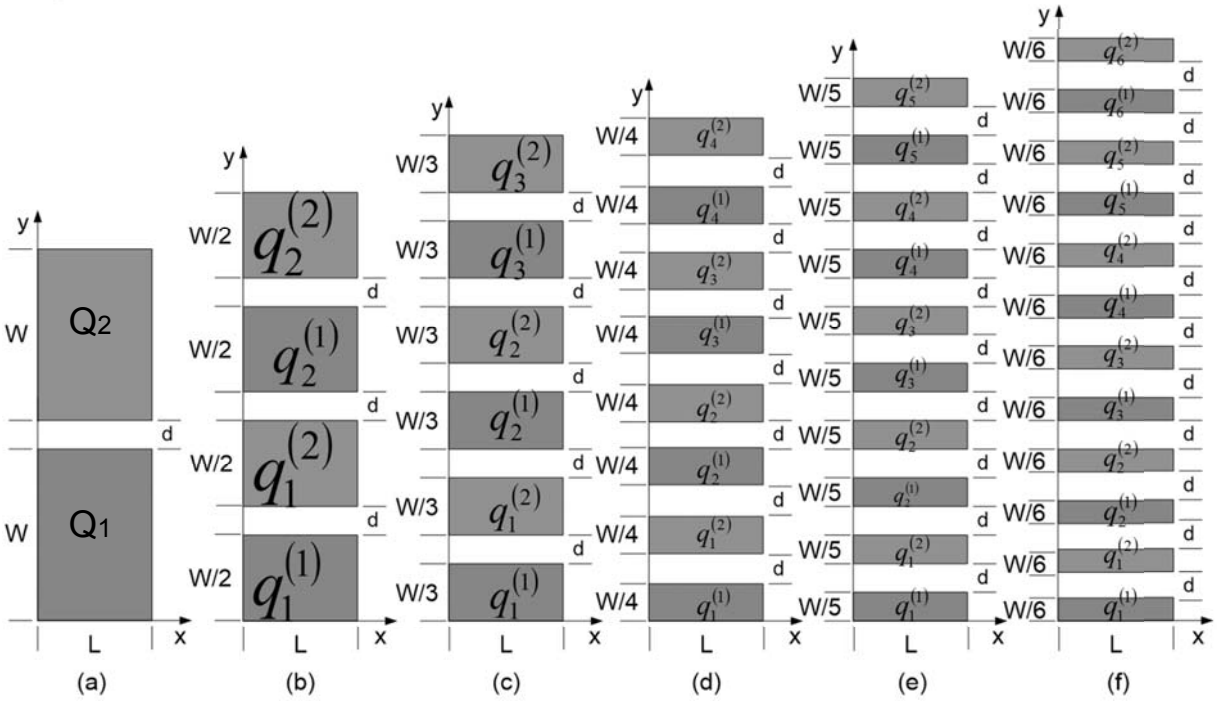
- Pelgrom's model:

$$\sigma(\Delta V_{THO}) = \frac{A^2_{P,V_{THO}}}{WL} + S^2_{P,V_{THO}} D^2_x \quad (5)$$



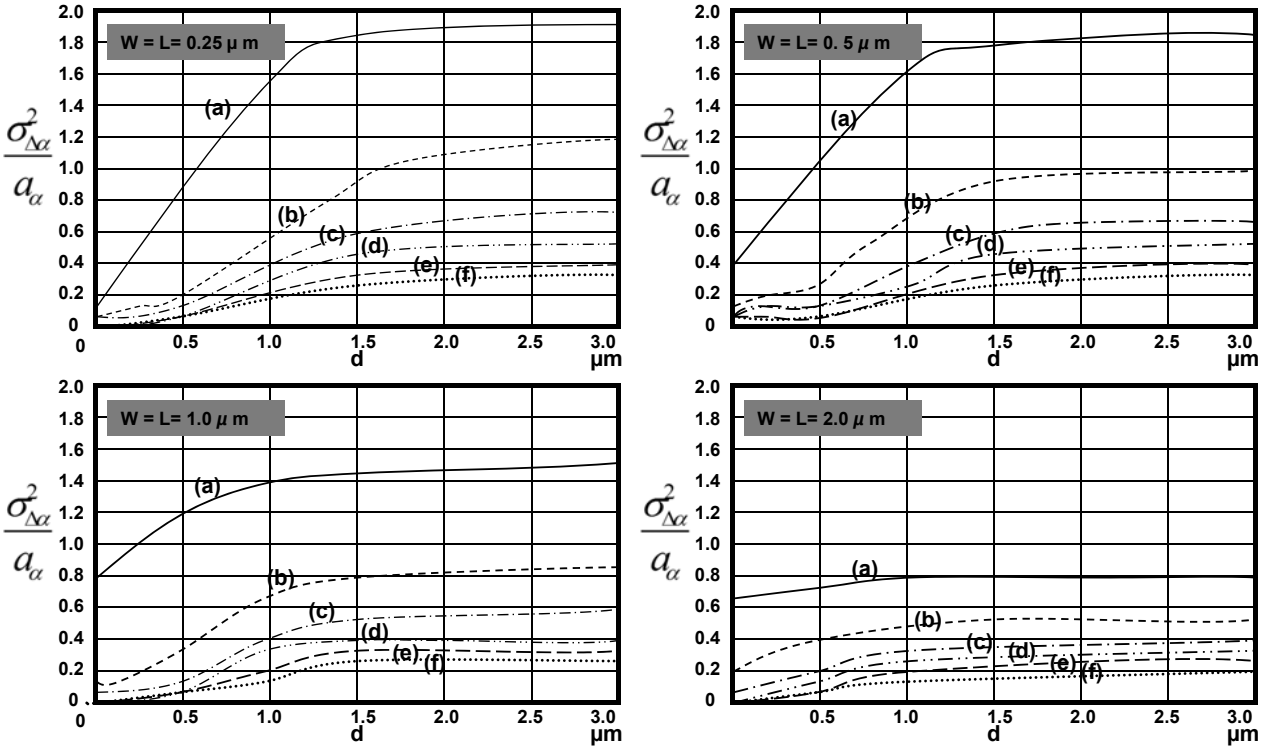
Transistor pair structure-(1/5)

Interdigitated Layouts



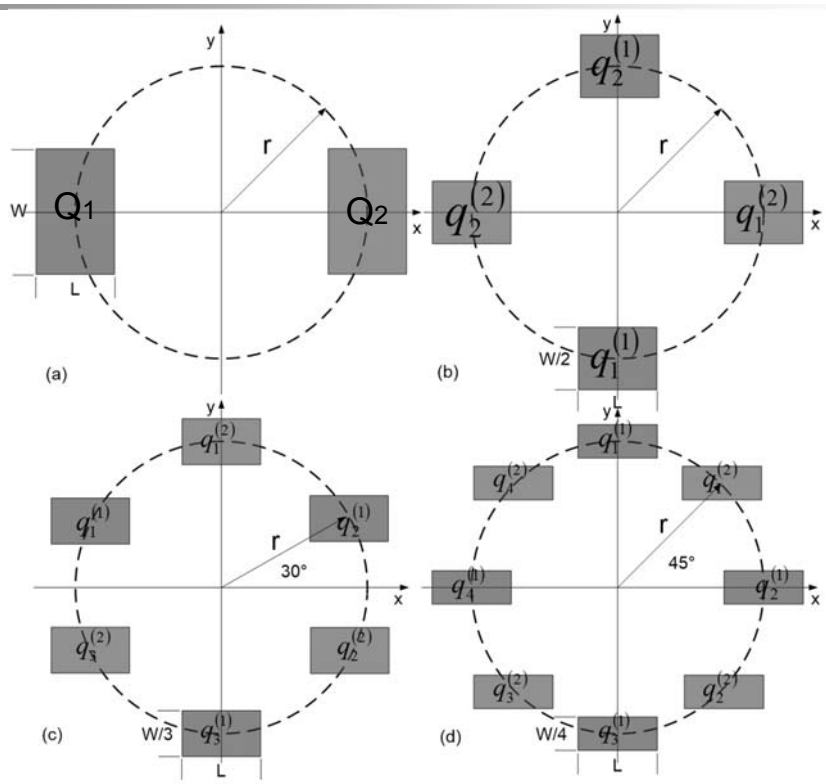
Transistor pair structure-(2/5)

Normalized Parameter Mismatch Variance versus d



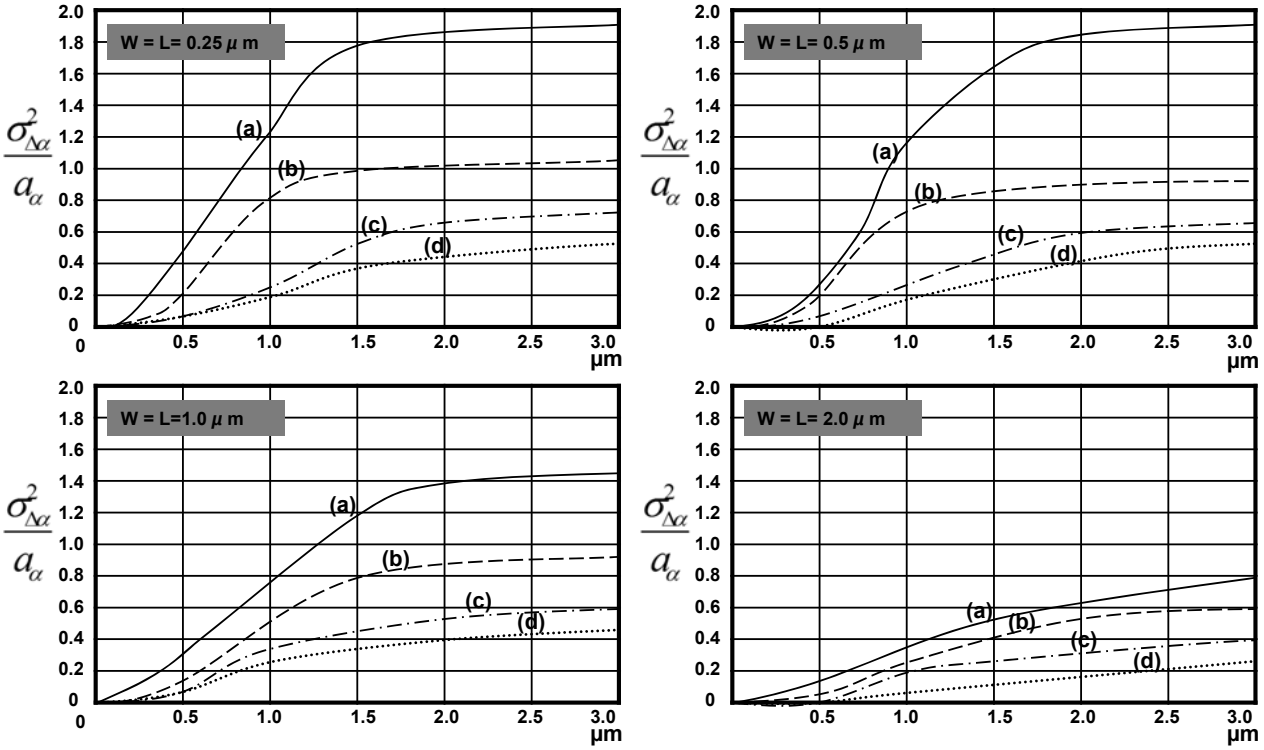
Transistor pair structure-(3/5)

common-centroid Layouts



Transistor pair structure-(4/5)

Normalized Parameter Mismatch Variance versus d



Discussion of Transistor Pair Structure(5/5)

- As distance increase, the variance tends to become a constant.
- Transistor partitioning into subdevices reduces the mismatch regard of layout structure.
- The asymptotic value of variance decreases as the number of subdevices increases.
- The asymptotic value of variance decreases as the total device area increases.
- The advantages of partitioning tend to vanish as the number of subdevices increases in that partitioning augments the total area occupied.

Yield of Differential Amplifier(1/3)

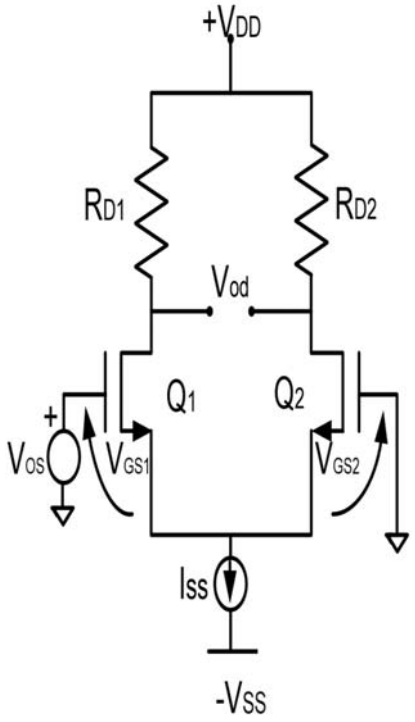
■Subthreshold region:

$$I_{D1} = ke^{\left(\frac{V_{DS1}-\hat{V}_{TH1}}{v_T}\right)} \quad (6) \qquad I_{D2} = ke^{\left(\frac{V_{DS2}-\hat{V}_{TH2}}{v_T}\right)} \quad (7)$$

$$V_{OS} = V_{GS1} - V_{GS2} = v_T \ln\left(I_{D1}/I_{D2}\right) + \hat{V}_{TH1} - \hat{V}_{TH2} \quad (8)$$

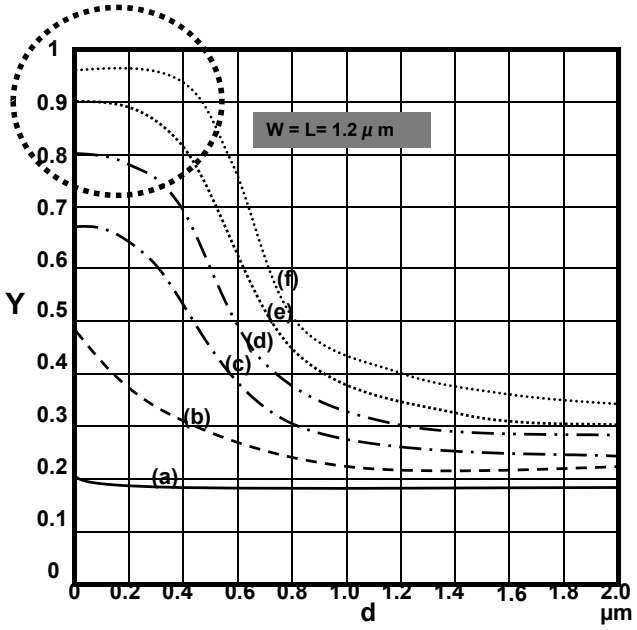
$$\rho V_{OS}(V_{OS}) = \frac{1}{\sqrt{2\pi}\cdot\sigma_{V_{OS}}} \exp\left(-\frac{V_{OS}^2}{2\sigma_{V_{OS}}^2}\right) \quad (9)$$

$$Yield = \int_{-V_M}^{V_M} \rho V_{OS}(V_{OS})\, dV_{OS} \quad (10)$$

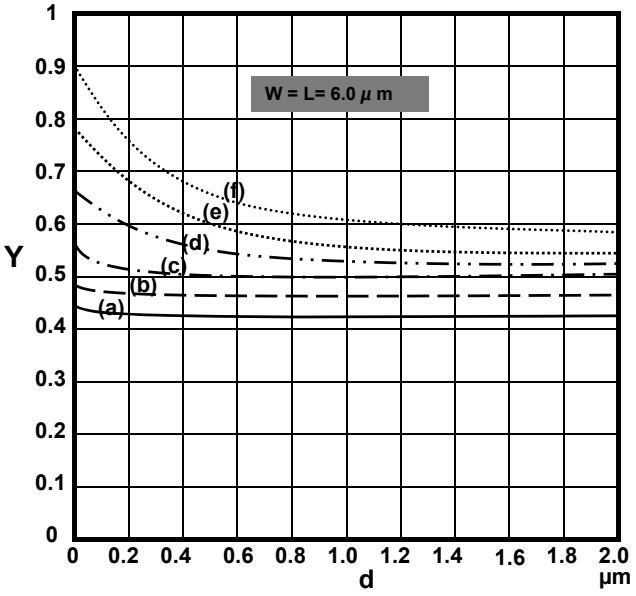


Differential amplifier

Yield of Differential Amplifier(2/3)



(a)



(b)

Discussion of the Yield of Differential Amplifier(3/3)

- The yield decreases as distance increases.
- When distance increase the yield tends to a minimum constant value that depends on the number of subdevices into which the transistors are partitioned.
- This asymptotic value increase when the number of subdevices increases.
- The yield increases for a given layout when device size increases.

As process sclaed down, the fabrication accuracy enhanced but the MOSFETs need more steps to fabricate

Will our dream for low complexity, high accuracy layour come true?