Yield Issues

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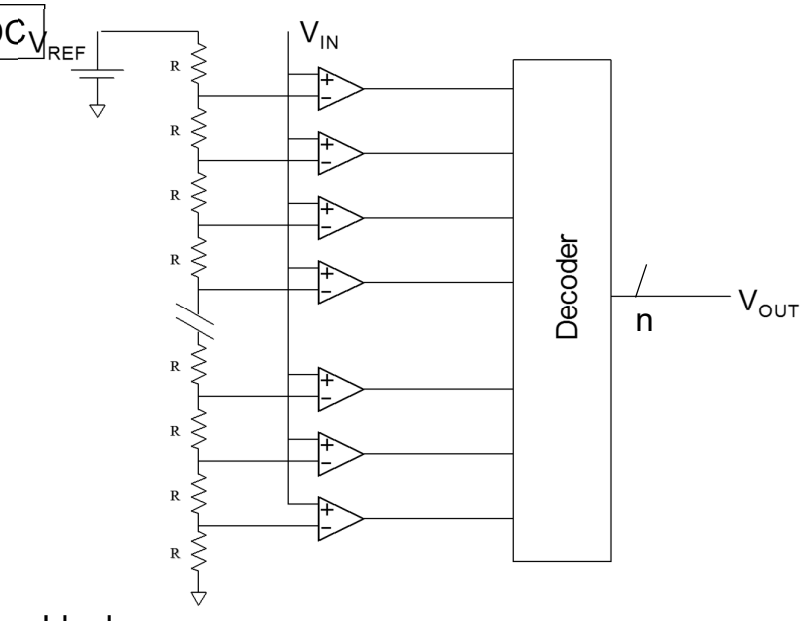
Modified from Prof. Geiger's Notes

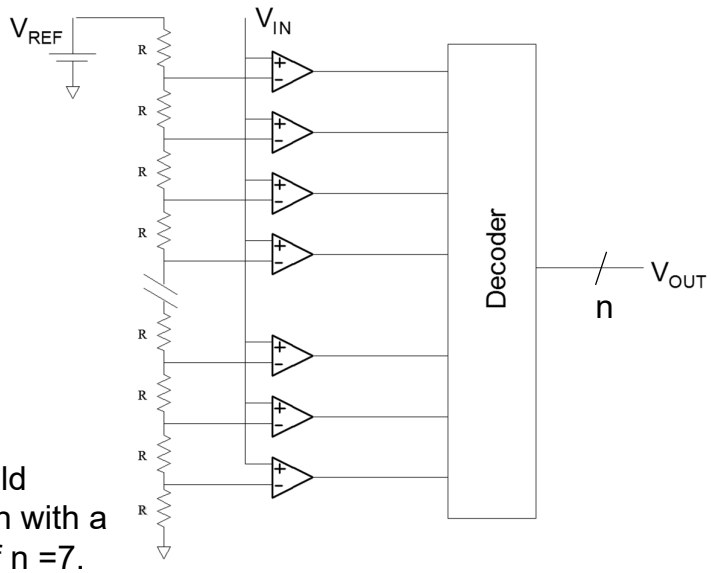
Yield Issues

Example – R-String ADC



Assumptions: R-string Ideal
Only errors due to offset voltage of comparators

Example – R-String ADC



If V_{REF} = 5V, determine the yield if the offset voltage is gaussian with a standard deviation of 10 mv if n =7. Assume the device meets performance specs if the trip point is within .5 LSB of The ideal trip point.

If V_{REF} = 5V, determine the yield if the offset voltage is gaussian with a standard deviation of 10 mv if n=7. Assume the device meets performance specs if the trip point is within .5 LSB of the ideal trip point.

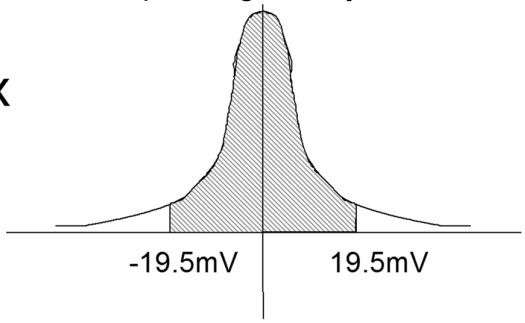
Solution:

$$V_{LSB} = \frac{5V}{2^7} = 39mV \quad \text{and} \quad .5V_{LSB} = 19.5mV$$

Consider trip point k

The probability that trip point k meets the .5 LSB spec is given by

$$p_{|VOS|} \le 19.5\ mV = \int_{x=-19.5}^{19.5} f(x)dx$$



If $x_n = x/\sigma$ where σ = 10mV

$$p = \int_{x=-1.95}^{1.95} f_n(x)dx = 2F(1.95) - 1 = 2*.97441 - 1 = .9488$$

If V_{REF} = 5V, determine the yield if the offset voltage is gaussian with a standard deviation of 10 mv if n=7. Assume the device meets performance specs if the trip point is within .5 LSB of the ideal trip point.

Solution:

Thus, the soft yield is

$$Y = p^{127} = .9488^{127} = .0013$$

This soft yield of 0.13% would be unacceptable in almost all situations

Repeat the yield if the offset voltage of the amplifier has a standard deviation of 5mV instead of 10mV

If V_{REF} = 5V, determine the yield if the offset voltage is gaussian with a standard deviation of 5 mv if n=7. Assume the device meets performance specs if the trip point is within .5 LSB of the ideal trip point.

Solution:

$$p_{|VOS|} \le 19.5\,mV = \int_{x=-19.5}^{19.5} f(x)dx$$

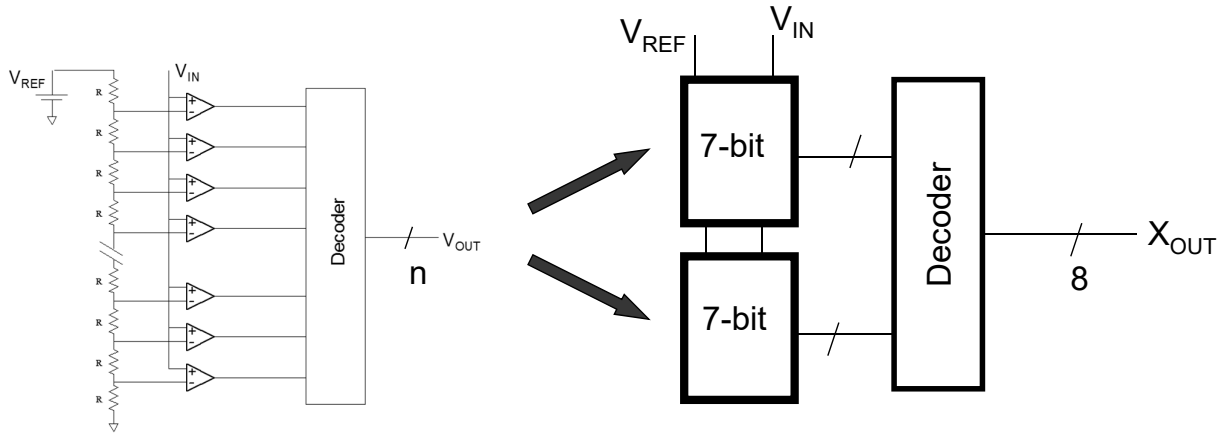
If $x_n = x/\sigma$ where σ = 5mV

$$p = \int_{x=-3.9}^{3.9} f_n(x)dx = 2F(3.9) - 1 = 2*.999952 - 1 = .999904$$

$$Y = p^{127} = .999904^{127} = .988$$

This factor of 2 change in the offset voltage increased the soft yield from 0.13% to 98.8% !

What would be the yield if two of the previous R-string ADCs were combined to increase the resolution to 8 bits if VOS remains at



This is a very simple modification that would take minimal effort to make !

If V_{REF} = 5V, determine the yield if the offset voltage is gaussian with a standard deviation of 5 mV if n=8. Assume the device meets performance specs if the trip point is within .5 LSB of the ideal trip point.

Solution:

$$V_{LSB} = \frac{5V}{2^8} = 19.5mV \quad \text{and} \quad .5V_{LSB} = 9.75mV$$

If $x_n = x/\sigma$ where σ = 5mV

$$p = \int_{x=-1.95}^{1.95} f_n(x)dx = 2F(1.95) - 1 = 2 * .97441 - 1 = .9488$$

$$Y = p^{255} = .9488^{255} = 1.51E-6$$

This seemingly modest change has a dramatic affect on yield.

Design for Yield in ADCs

- A statistical analysis of soft yield is very important if undesirable surprises are to be avoided
- Even modest changes in specifications can have dramatic affects on yield
- When a statistical problem starts to occur, it often does so in a relentless way
- Area dependent standard deviations of performance paramaters often require a factor of 4 increase in area for a factor of 2 reduction in standard deviation
- A factor of 2 change in standard deviation is generally required for every additional bit of resolution
- the real yield is dependent upon the combined yield loss mechanisms, not one of the individual yield loss mechanism

Develop a realistic error budget and use it wisely!

Yield-based Area Determination

Tailored from Prof. Geiger's lecture
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Yield-based Area Determination

- Component Ratio Accuracy Affects Soft Yield if Calibration is not Used
- Layout and Area Affect Component Ratio Accuracy

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Theorem: If only linear gradients in capacitance density are present, the total capacitance is equal to the capacitance density at the geometric centroid multiplied by the total capacitance area

Tradeoffs Between Component Ratio Accuracy, Area and Yield

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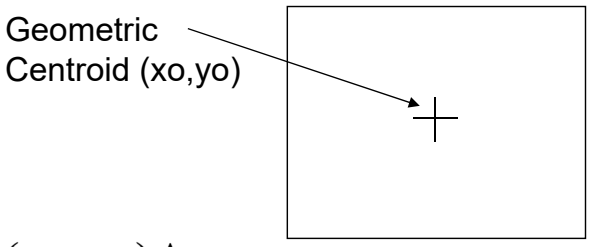
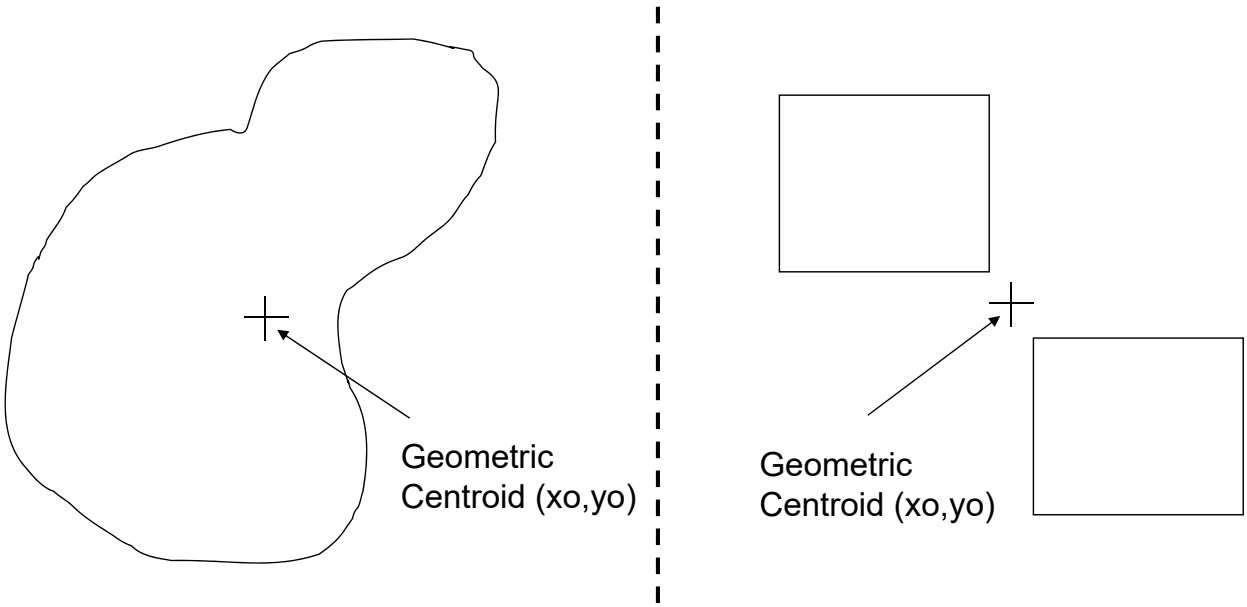


$$C = C_d(x_0, y_0)A$$

Tradeoffs Between Component Ratio Accuracy, Area and Yield



$$C = C_d(x_0, y_0)A$$

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Theorem: If only linear gradients in capacitance density are present, the total capacitance is equal to the capacitance density at the geometric centroid multiplied by the total capacitance area

Corollary: If two equal-area capacitors have the same geometric centroid, then linear gradients in the capacitance density will cause no errors in the matching of the capacitors.

- Layouts of 2 or more capacitors that have the same geometric centroid are termed common centroid layouts

- Common centroid layouts are only useful for eliminating the effects of linear gradients in capacitance density on matching

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Random Effects on Capacitor Matching:

If edge effects are negligible and the random component of the capacitance density at (x1,y1) is uncorrelated from that at (x2,y2) for (x1,y1) ≠ (x2,y2) , then the standard deviation of the value of a capacitor relative to its nominal value at a given location is given by the expression

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}$$

where A_C is a constant characteristic of the process and Area is the area of the capacitor

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Random Effects on Capacitor Matching:

If edge effects are negligible and the random component of the capacitance density at (x1,y1) is uncorrelated from that at (x2,y2) for (x1,y1) ≠ (x2,y2) , then the standard deviation of the difference of two geometrically identical capacitors is given by the expression

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}\sqrt{2}$$

where A_C is a constant characteristic of the process and Area is the area of the capacitor

Random Effects on Capacitor Matching in a Small Neighborhood:

Standard deviation of a single capacitor

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}$$

Standard deviation of mismatch between two capacitors

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}\sqrt{2}$$

- **When matching data is given, it is often not clear whether reference is for a single capacitor or difference of two capacitors**
- **Test structures often designed to measure mismatch statistics**
- **Must be sure no systematic (gradient) affects present when measuring statistical parameter A_C**
- **Must not be confused with statistics for measured component values across a die, across a wafer, or over wafer lots**

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Random Effects on Capacitor Matching in a Small Neighborhood:

Standard deviation of ratio of two nominally equal capacitors (gain of 1 for feedback amplifiers)

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}\sqrt{2}$$

Standard deviation of N:1 ratio of N+1 nominally equal capacitors (gain of N for feedback amplifiers)

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}\sqrt{N+N^2}$$

Tradeoffs Between Component Ratio Accuracy, Area and Yield

Random Effects on Capacitor Matching in a Small Neighborhood:

Standard deviation of N:1 ratio of N+1 nominally equal capacitors (gain of N for feedback amplifiers)

$$\sigma = \frac{A_C}{\sqrt{\text{Area}}}\sqrt{N+N^2}$$

- Each factor of 2 reduction in standard deviation requires a factor of 4 increase in area
- Each increase in resolution by 1-bit requires a factor of 4 increase in area
- Accurate characterization of the matching performance of a process can play a key role in design and yield
- For optimal designs, essential to know whether statistical data is for component, relative values, and whether it is the 1-σ or 3- σ value

Tradeoffs Between Component Ratio Accuracy, Area and Yield

- Capacitor Ratio Accuracy Affects Soft Yield if Calibration is not Used

- Layout and Area Determine Capacitor Ratio Accuracy

  - Good Layout is Essential for Minimizing the Effects of Systematic Variations in Matching-Critical Circuits
  - Random Variations Can Be Managed Only With Area or Calibration
  - kT/C noise May Play Dominant Role is Determining Area Requirements for a Given Application

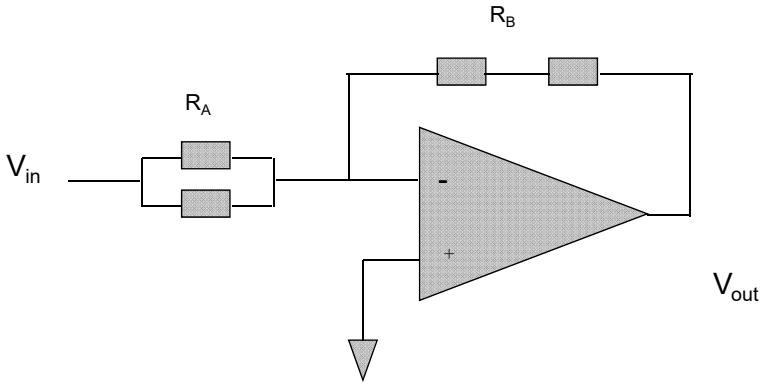
Component Value and Area Tradeoffs Also Affect Yield

❑ Observations

- **Layout styles for ratio-matched components often based upon using a number of unit cells that corresponds to the desired component ratio. This represent a component-ratio based (CRB) area allocation strategy**
- **For a given total area, it will be shown that the component-ratio based area allocation schemes often result in a substantial sub-optimal yield**

❑ Negative feedback amplifier

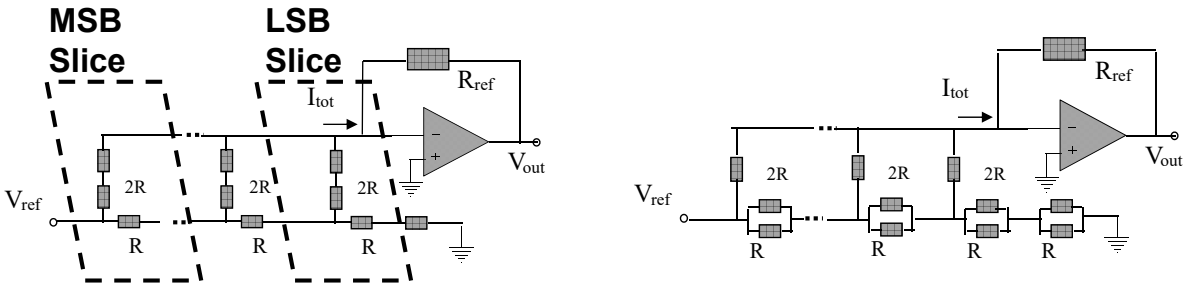
Area ratio = component ratio



For fixed total area of "gain of 4" amplifier it will be shown that

$Yield_{EAB} > Yield_{CRB}$

❑ R-2R ladders



- Area for "2R" resistor is double or half of that of the "R"resistor
- Area for MSB slices is same as area for LSB slices
- For a fixed total resistor area , it will be shown that the yield is substantially below optimal with CRB area allocation

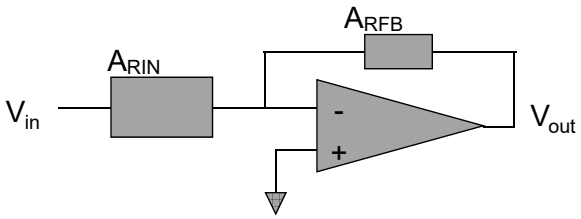
Layout and Area Affect Component Ratio Accuracy

Goal: Develop area allocation strategy to optimize yield of ratio-critical circuits

- ❑ **Feedback amplifiers**
- ❑ **R-2R ladders**
- ❑ **R-strings**

Will consider only random variations in sheet resistance and contact resistance. Sufficient partitioning must be utilized so that gradient effects can be maintained at a sufficiently low level through appropriate layout techniques such as centroiding.

Applications to capacitor layout require modifications of procedure but in some technologies the concepts apply



Theorem:

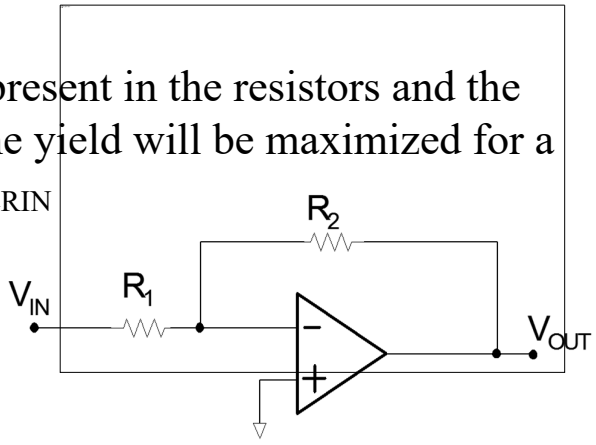
If only random effects are present in the resistors and the resistors are rectangular, the yield will be maximized for a given total area if $A_{RFB}=A_{RIN}$

This area allocation is independent of the gain

Unit cell with segmentation can be used to obtain nearly optimal area allocation for any gain

Theorem:

If only random effects are present in the resistors and the resistors are rectangular, the yield will be maximized for a given total area if $A_{RFB}=A_{RIN}$



Proof:

Define the gain θ by $\theta=-\frac{R_2}{R_1}$

R1 and R2 are random variables with nominal values R_{1N} and R_{2N}

Θ is a random variable with nominal value θ_N

$$\theta=\frac{R_2}{R_1}=\frac{R_{2N}+R_{2R}}{R_{1N}+R_{1R}}=\left[\frac{R_{2N}}{R_{1N}}\right]\frac{1+\frac{R_{2R}}{R_{2N}}}{1+\frac{R_{1R}}{R_{1N}}}\approx\theta_N\left(1+\frac{R_{2R}}{R_{2N}}-\frac{R_{1R}}{R_{1N}}\right)$$

Proof of Theorem

$$\theta = \frac{R_2}{R_1} = \frac{R_{2N} + R_{2R}}{R_{1N} + R_{1R}} = \left[\frac{R_{2N}}{R_{1N}}\right] \frac{1 + \frac{R_{2R}}{R_{2N}}}{1 + \frac{R_{1R}}{R_{1N}}} \approx \theta_N \left(1 + \frac{R_{2R}}{R_{2N}} - \frac{R_{1R}}{R_{1N}}\right)$$

$$\sigma_\theta^2 = \theta_N^2 \left(\sigma^2_{\frac{R_{2R}}{R_{2N}}} + \sigma^2_{\frac{R_{1R}}{R_{2N}}} \right)$$

For a resistor:

$$\sigma_{\frac{R_{ran}}{R_N}} = \frac{A_\rho}{\rho_N \sqrt{WL}} = \frac{A_\rho}{\rho_N \sqrt{A_R}} = \frac{K_\rho}{\sqrt{A_R}}$$

$$\sigma_\theta = K_\rho \theta_N \sqrt{\frac{1}{A_{RA}} + \frac{1}{A_{RB}}} = K_\rho \theta_N \sqrt{\frac{1}{A_{RA}} + \frac{1}{A_T - A_{RA}}}$$

$$f = \frac{1}{A_{RA}} + \frac{1}{A_T - A_{RA}}$$

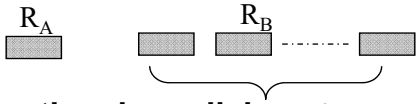
Minimizing the function under the square root wrt A_{RA} it follows that the optimal value for A_{RA} and A_{RB} are

$$A_{RA} = A_{RB} = \frac{A_T}{2}$$

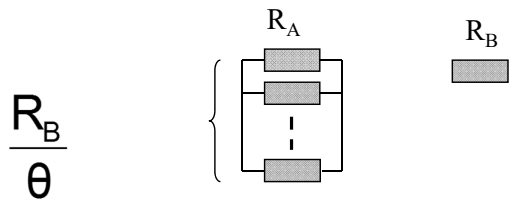
This completes the proof of the theorem.

Yield Enhancement Layout Strategies For Feedback Amplifiers

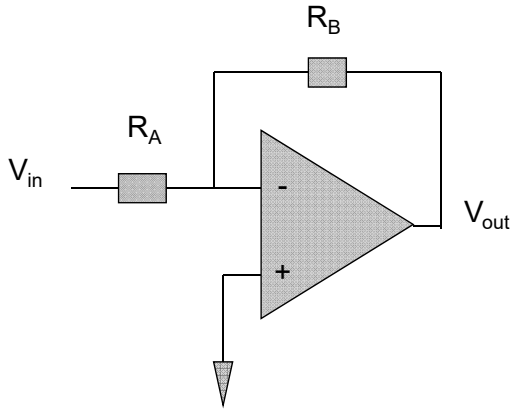
- **Standard configurations**
  - **Conventional series**



  - **Conventional parallel**



Assume gain = -θ



Question: What is the yield and how severe is the yield loss if the area is not optimally assigned?

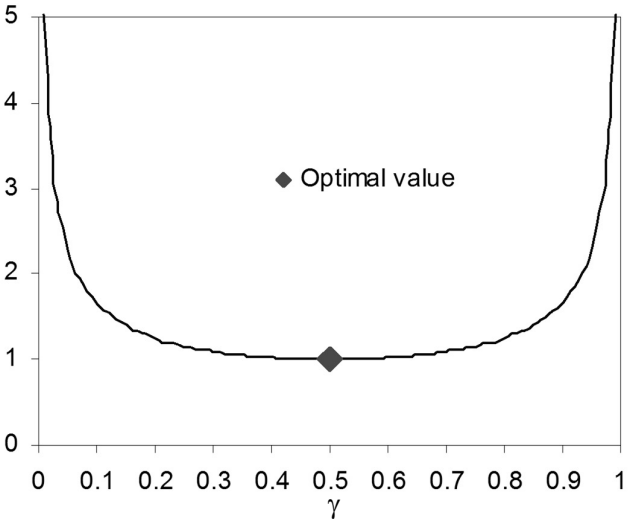
- **Define $A_{RB}/A_T = \gamma$**
- **The standard deviation of the gain can be expressed in terms of γ by**

$$\sigma_\theta = \frac{2K_\rho \theta_N}{\sqrt{A_T}} \frac{1}{2\sqrt{\gamma(1-\gamma)}} = \sigma_{\theta min} \frac{1}{2\sqrt{\gamma(1-\gamma)}}$$

Ideally γ=0.5

Simulation Results

$\frac{\sigma}{\sigma_{\theta min}}$



Minimum quite shallow but rises rapidly near extremes

❑ Yield

$$Y_A = 2F[(F^{-1}(\frac{1 + Y_{opt}}{2}) * 2\sqrt{\gamma(1-\gamma)}] - 1$$

- **F is the standard CDF of a N(0,1) Gaussian Distribution**
- **Y is the yield of an optimal layout and Y_A is the corresponding actual yield with the same resistor areas i.e. $Y_A = Y_{opt}$ when $\gamma = 0.5$**

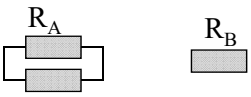
- **The optimal area-partitioned configuration may not be practical to realize**
- **A near-optimal configuration can be achieved**

Near-optimal configurations

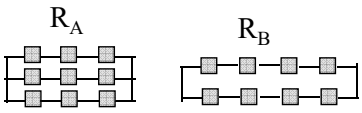
- **θ = 2 (same total resistor area)**

case1: γ=2/3

case2: γ=1/3



case3: γ=8/17



∗ Notice : spacing and edge effects can cause problem if unit cell is too *Small*!

γ

Yield Comparisons for Feedback Amplifiers

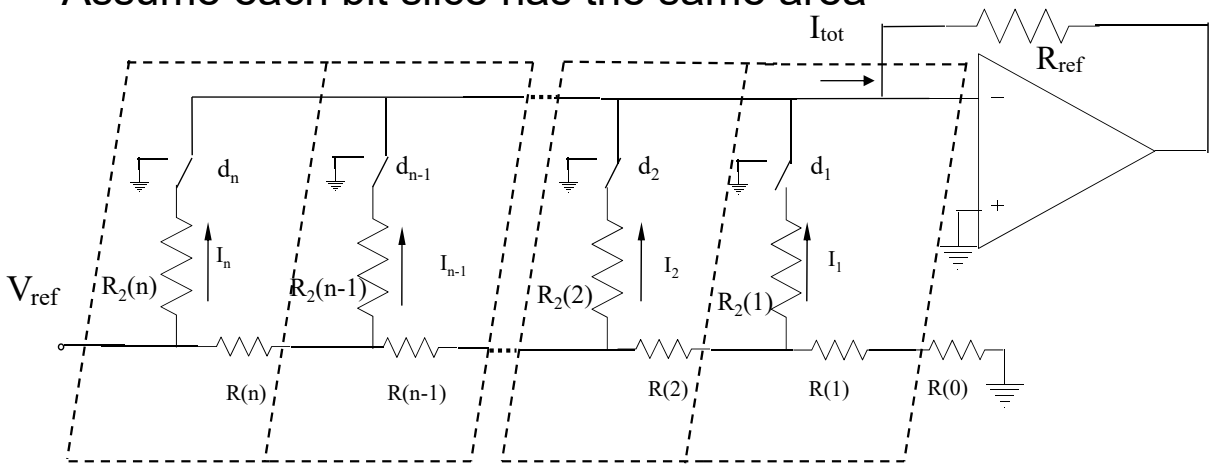
- **Simulation Results**

Gain	Optimal approach Yield	Conventional approach yield
5	99%	95%
10	99%	86%
25	99%	68%
100	99%	39%

- **Total area for both approaches is the same**
- **Substantial yield improvement with proposed layout scheme**

R-2R Current Steering DAC

Assume each bit slice has the same area



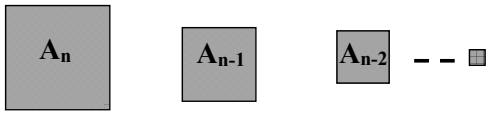
Interest is in INL yield

This is a 2n+1 variable optimization problem

R-2R ladders :
Two-parameter INL optimization

Slice to slice area allocation

$$\frac{A_k}{A_{k-1}} = m$$



Internal slice area allocation

$$\frac{A_{2R}}{A_R} = k$$

Interested in optimizing the INL Yield

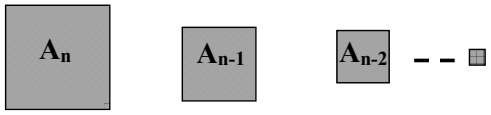
The probability density function of the INL is unwieldly making a complete closed-form analysis very difficult (maybe impossible)

Will attempt to address the problem by simulation initially using a two-parameter model for a 2n+1 variable problem

R-2R ladders :
Two-parameter INL optimization

Slice to slice area allocation

$$\frac{A_k}{A_{k-1}} = m$$



Internal slice area allocation

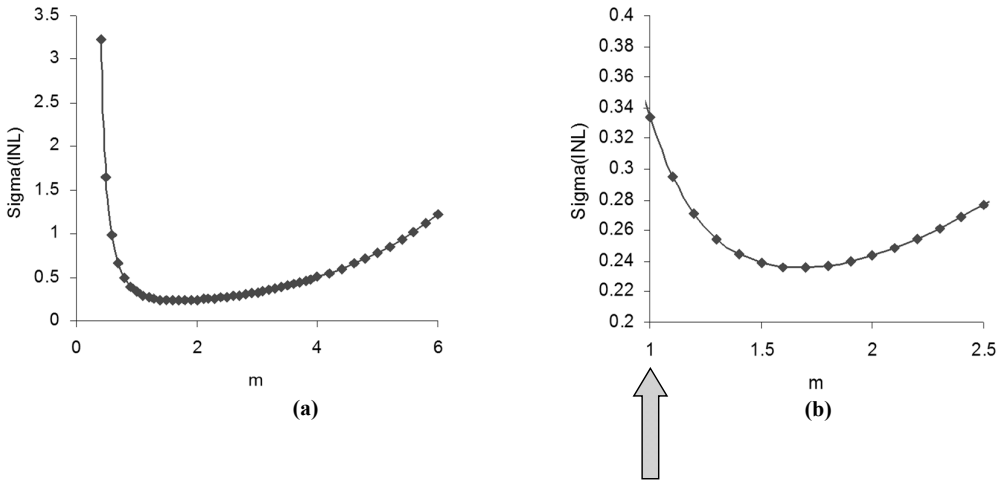
$$\frac{A_{2R}}{A_R} = k$$

Simulation supported conjecture:

If only random effects are present in the resistors, the yield will be maximized for a given total area if

$$m \approx 1.7 \text{ and } k \approx 2.2$$

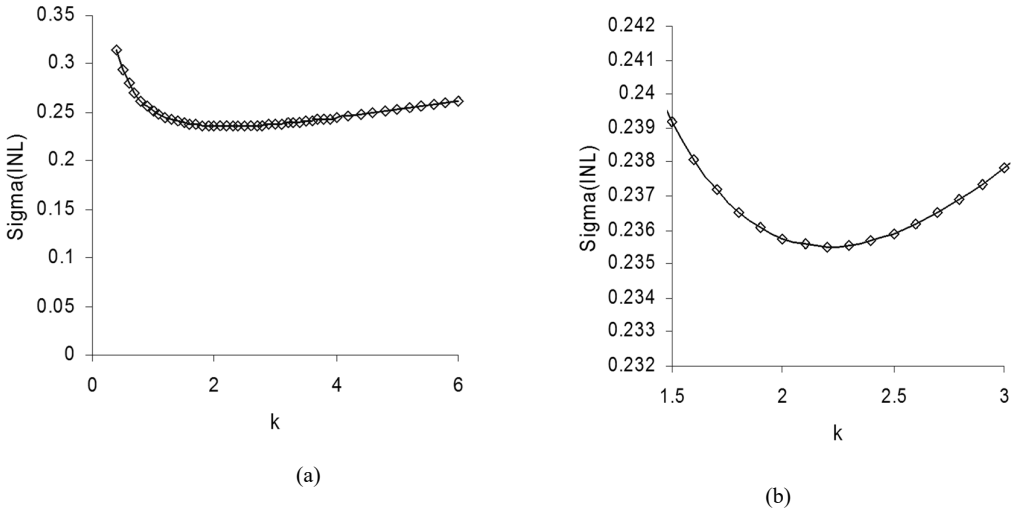
Two-parameter optimization



Standard deviation of INL vs. m for an 8-bit R-2R ladder with k = 2 a) coarse view (b) expanded view

The standard equal area per slice allocation is far from optimal !

Two-parameter optimization



Standard deviation of INL vs. k for an 8-bit R-2R ladder with m=1.7
(a) coarse view (b) expanded view

The local minimum is quite shallow suggesting the standard series area allocation
Is near optimal but a significant yield penalty with a standard parallel area allocation

R-2R ladders :
Two-parameter INL optimization

Series: $A_{2R}=2A_R$
Parallel: $A_R=2A_{2R}$

❑ Simulation Results

n	Optimal approach Yield	Series approach Yield	Parallel approach Yield
10	99%	90.60%	82.10%
12	99%	87.00%	78.30%
14	99%	84.00%	75.70%
16	99%	82.00%	72.00%

- **Total area for both approaches is the same**
- **Substantial yield improvement with proposed layout scheme**
- **Standard layout is far from optimal!**

R-2R ladders : Simplified Optimization

- **Restrict the Latter LSB slices to have the same total resistor area**
  - **Reduce the layout effort**
  - **The standard deviation of INL has a minor degradation that is within 1% from the optimal value**

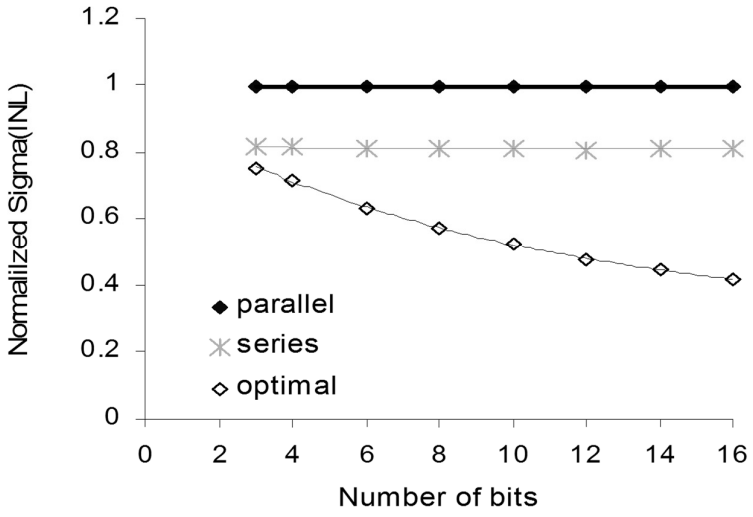
Simplified optimization

- **Simulation Results**

n	s	σ_{INCR}
8	3	0.5445%
10	4	0.6819%
12	5	0.6445%
14	6	0.5302%
16	8	0.9915%

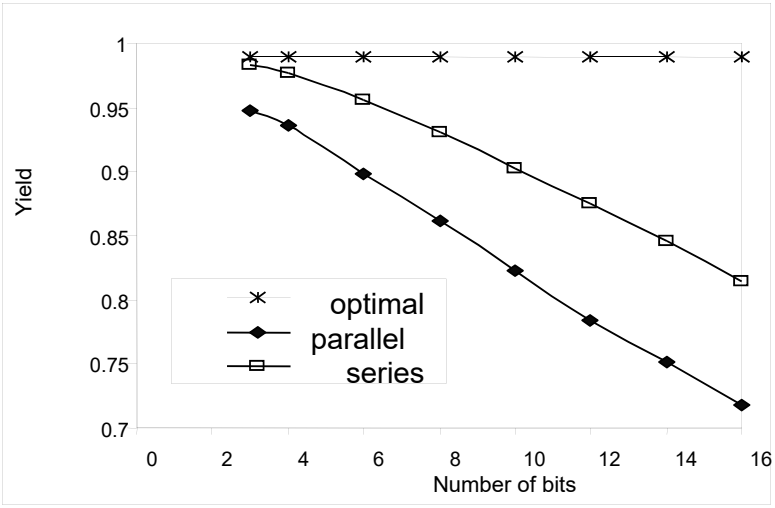
- **s is the # of LSB slices with the same resistor area**
- **The first n-s+1 slices with m=1.7 and θ=2.2**
- **Near-optimal yield**

Comparison with existing strategies



The normalized sigma INL of R-2R ladder vs. resolutions

Comparison with existing strategies



Area allocated so optimal yield Is 99%

The yield of different area configuration of R-2R ladder vs. resolutions with same total resistor area

❑ 8-bit R-2R ladder

	1	2	3	4	5	6	7	8
"R"	12×12	9×9	7×7	5×5	4×4	3×3	3×3	3×3
"2R"	24×12	18×9	14×7	10×5	8×4	6×3	6×3	6×3
m	1.78	1.65	1.96	1.56	1.78	1	0.75	
k	2	2	2	2	2	2	2	2

* m is the area ratio of the adjacent slices
* k is the area ratio of "2R" and "R" in the same slice

$$\sigma_{INCR}=0.9\ \%$$

R-2R Area Allocation Summary

- ❑ Significant yield improvements with allocating more area to MSB slices
- ❑ Allocating twice the area to the 2R resistors as to the R resistors is near optimal
- ❑ Allocating twice the area to the R resistors as to the 2R resistors will incur significant yield penalty
- ❑ LSB resistor slices can all have same area without significant yield penalty
- ❑ Segmentation and placement must still be used to mitigate gradient effects