

Failure Mechanisms

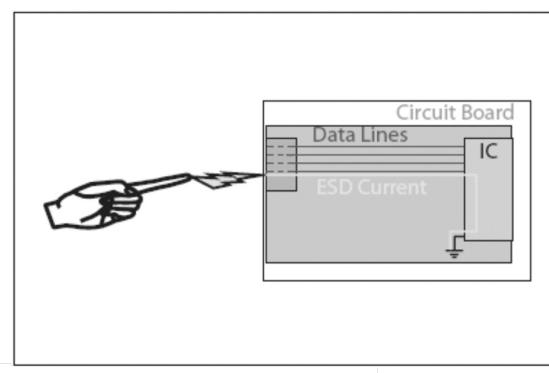
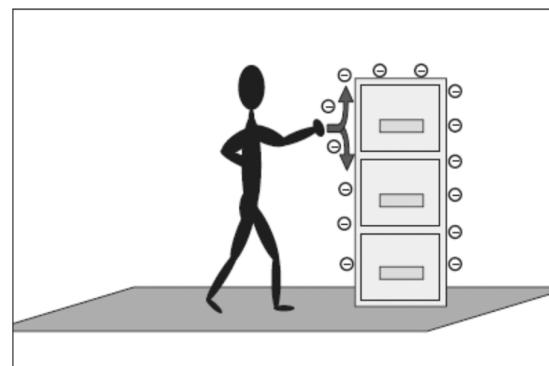
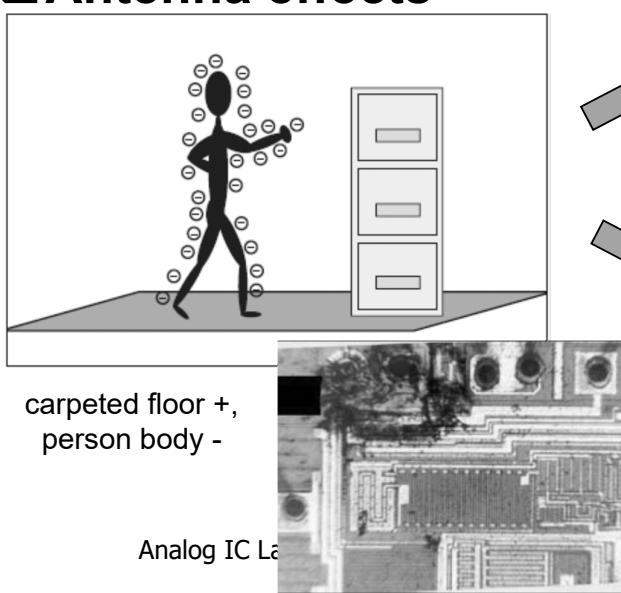
Lecturer : Poki Chen

Analog IC Design

Failure-1

Electrical Overstress (EOS)

- Due to excessive V or I
- ESD
- Electromigration
- Antenna effects



An ESD latch-up failure caused the
charring of this RS-232 transceiver
and the surrounding pc board.

Failure-2

Electrostatic Discharge (ESD)

- Human body as a capacitance
 - suffling/rubbing across the carpet charge to 10,000 volts !
- Gate dielectric of MOS
 - Destroyed by a discharge of 50 volts !
- CMOS IC's much more fragile than standard Bipolar IC's.
- Measure the vulnerability of IC to ESD
 - Human Body Model (HBM) : 2kV thru $1.5\text{k}\Omega$ to DUT
 - Machine model (MM) : 200V w/o R, directly to DUT
⇒ much harsher than HBM

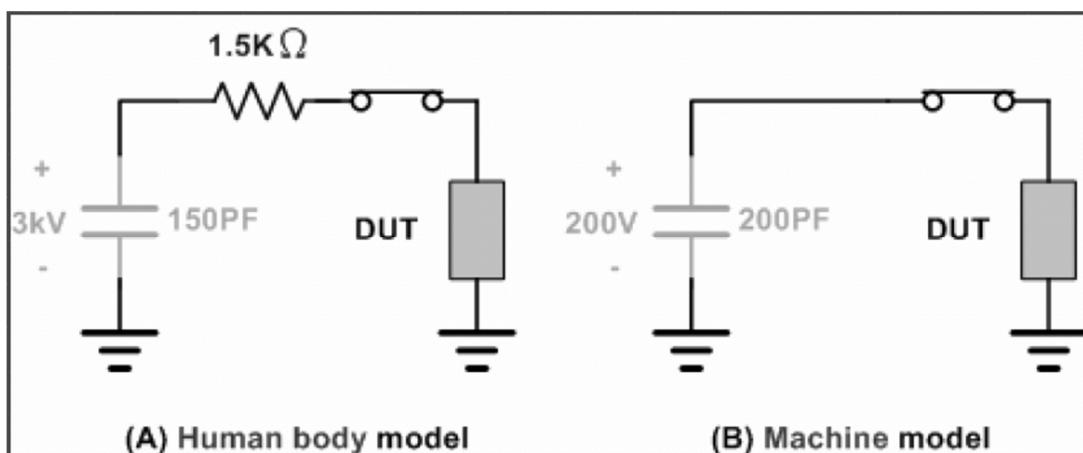
Analog IC Layout

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Failure-3

Failure Mechanisms

- Representative ESD tests:
 - (a) 2kV human body model and (b) 200V machine model In both circuits, DUT stands for device under test.



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Failure-4

Charged Device Model (CDM)

- Charge IC package ($<< 200\text{pF}$ usually) to 1-1.5kV
discharge one pin to GND

ESD damages

- Pin to MOS gate → <50 volts can rupture gate oxide in nanoseconds → shorts gate to backgate
- pin to Capacitors → oxide rupture, oxide degradation ...
- pin to diffusion → avalanche → increased junction leakage
- Can vaporize metal or shatter silicon



OK against ESD

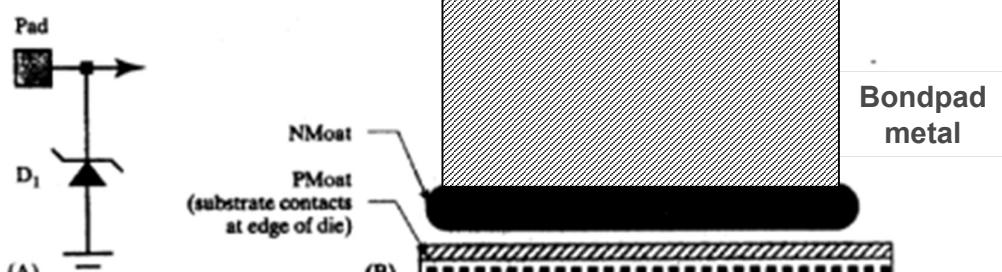
- Pin to Substrate
- Pin to large diffusions (e.g., collector of power NPN)
- Power supply pins connected to many diffusions

Vulnerable to ESD

- Pins to small diffusions: Base pin, Emitter pin of small NPN
- Pins to only MOS Gates
- Pins to deposited Capacitors
- 500Ω - $5\text{k}\Omega$ series resistors → cannot be used for $>0.3\text{ mA}$
- Leads that connect to external bondpads must NOT cross thin Gate or Emitter oxides

ESD Structures

- These structures require a low impedance return path to the substrate terminal → scribe seal metallization can do the job → ESD structure positions between bondpad and scribe seal, or between adjacent bondpads
- To limit peak voltages seen at bondpads
- (1) Zener Clamp



NSD/P-epi Zener Diode

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Failure-7

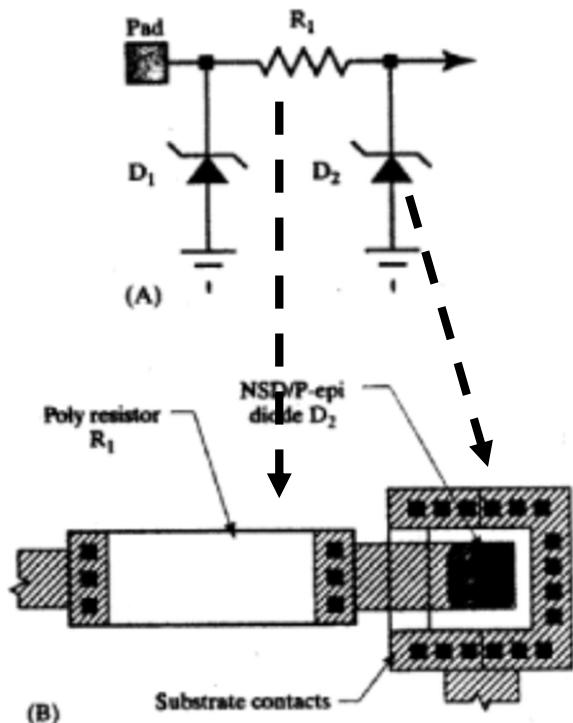
- Zener between Bondpad and Substrate return line
→ Simplest ESD
- Analog CMOS: NSD/P-epi and PSD/N-well
- Avalanche: Positive ESD transients on NSD/P-epi (NMOS) and Negative ESD transients on PSD/N-well (PMOS)
→ energy dumped into depletion region Si
- Larger transistors are more robust than smaller ones.
- A 10V nonsilicided, single-diffused drain MOS with drawn drain area of 1000 μm^2 will withstand → ESD strikes from 2kV HBM and 200V MM
- Increased overlap between S/D diffusions and respective contacts → improved ESD.
- Low-voltage CMOS: shallow S/D diffusions, higher backgate doping level (to prevent punch-through), ... → vulnerable to ESD damage.
- NSD/P-epi Zener: elongated NMos along side of substrate contact strip (part of scribe seal)
- Contact-to-NMos (of at least 500 μm^2) overlap should exceed min. layout dim. by 1-2 μm to keep gate oxide away enough.
- Should be surrounded by electron-collecting guard-ring; as many substrate contacts as area permits.

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Failure-8

- (2) Two-stage Zener Clamps
 - A single Zener can still have over a few 10s volts:
 (Ex) Zener series resistance = a few 10 Ω ;
 2kV HBM produce a peak current of 1.3A →
 $(\text{a few } 10\text{W}) * (1.3\text{Amp}) = \text{a few } 10\text{ volts} \rightarrow$
 can damage gate oxide at the peak of ESD transients.
 - A second Zener can reduce the peak transients to acceptable level.



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Failure-9

- First Zener (D1): limit transient to about 100 volts
- Second Zener (D2): limit transients to below 1 few 10volts.
- R_1 = several times the series resistance of the second Zener to limit current through D2: If the second Zener is small (of several 100 Ω s), then R_1 is a few k Ω s → can affect slew rate and nanoseconds of additional delay.

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Failure-10

• R_1

- Limits currents to safe levels.
- If Polyresistor and several 100Ω s, ***at least 5-8 μm wide, and at least 6-8 contacts*** → can survive 2kV HBM or 200V MM
Never be bended.
- Diffused resistors are suggested to be better (due to additional avalanche in R_1 to substrate which can dissipate currents).

• D_2 (the 2nd Zener)

- Substrate contacts → minimize *debiasing* of D_2 . Debiasing can be **10s of volts** if substrate contacts are farther away.
- $D_2 = 50-100 \mu m$ away from D_1 . For example, D_1 between *bondpad* and *scribe*, R_1 alongside *bondpad*, and D_2 on the inner ~~side of bondpad~~.

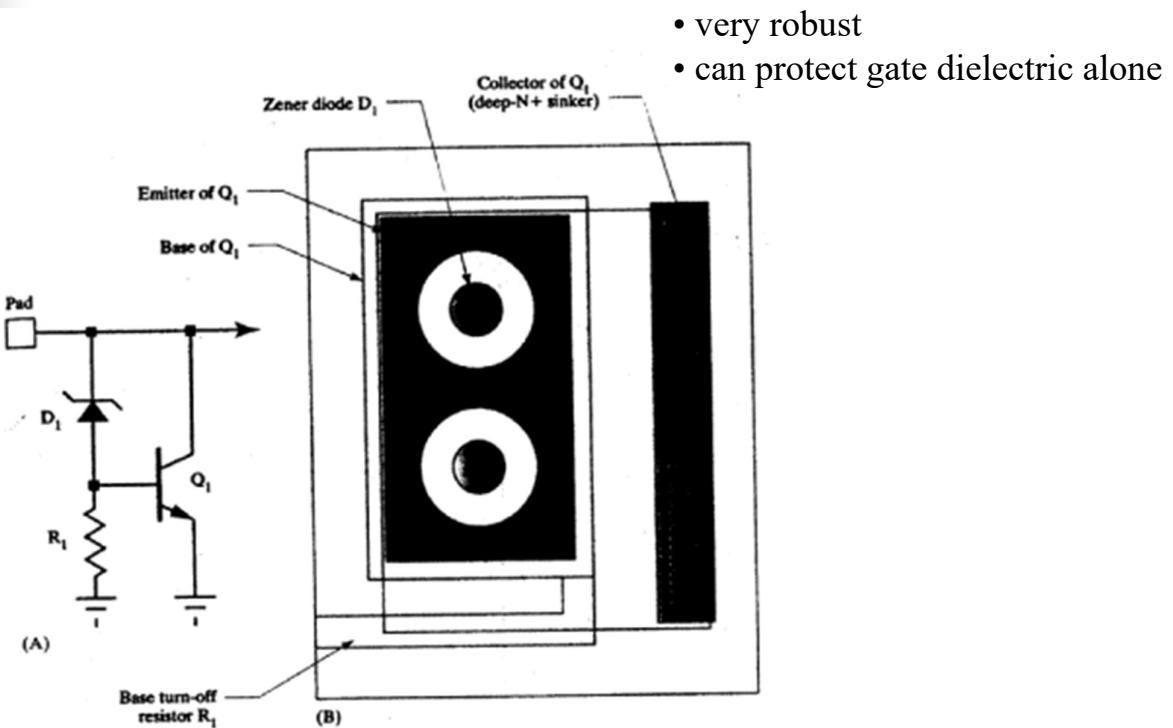
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Failure-11

• Examples of 2stage Zener ESD

- Protect *input MOS gates* in moderate voltage CMOS, large R_1 = OK for high impedance input terminal → ***input ESD device***
- Low-impedance applications: D_1 =the same; R_1 =reduced to $50-500\Omega$; D_2 =S/D diffusions of MOS transistor as secondary Zener.
- Larger output transistors: Smaller R_1 → ***output ESD device*** → can protect min.-area S/D implants
- If a pin (i.e., bondpad) to both Gate electrode & S/D diffusions, Then a combination of input ESD for gate, and output ESD for S/D diffusions

(3) Buffered Zener Clamp



- very robust
- can protect gate dielectric alone

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Failure-13

The antenna Effect

- In deep submicron era, more stringent process requirements make some advanced high-density plasma (HDP) reactors adopted in the production lines to achieve fine-line patterns.
- Plasma-based processes have a tendency to charge conducting components of a fabricated structure.
- The existing experimental evidence indicates that charging may affect the quality of the thin oxide.
- the damage increases with an increase in the area of the exposed conductor (antenna) during the plasma process.
- Recent studies show that the damage considering all plasma-based manufacturing operations increases in proportion to both the area and the perimeter of the antennas.

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Failure-14

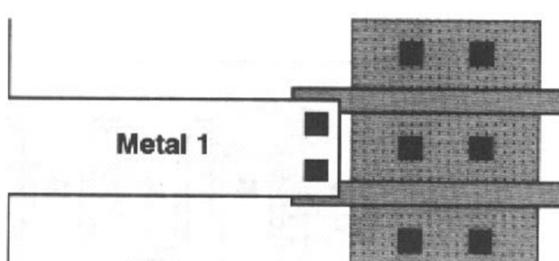
Three solutions to reduce antenna effect

☐ Router options

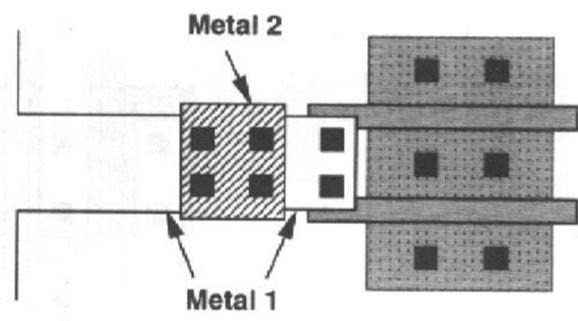
■ The gate of a small MOSFET is tied to a metal 1 interconnect having a large area

- During the etching of metal 1, the metal area acts as an “antenna,” collecting ions and rising in potential
- The gate oxide breaks down during fabrication

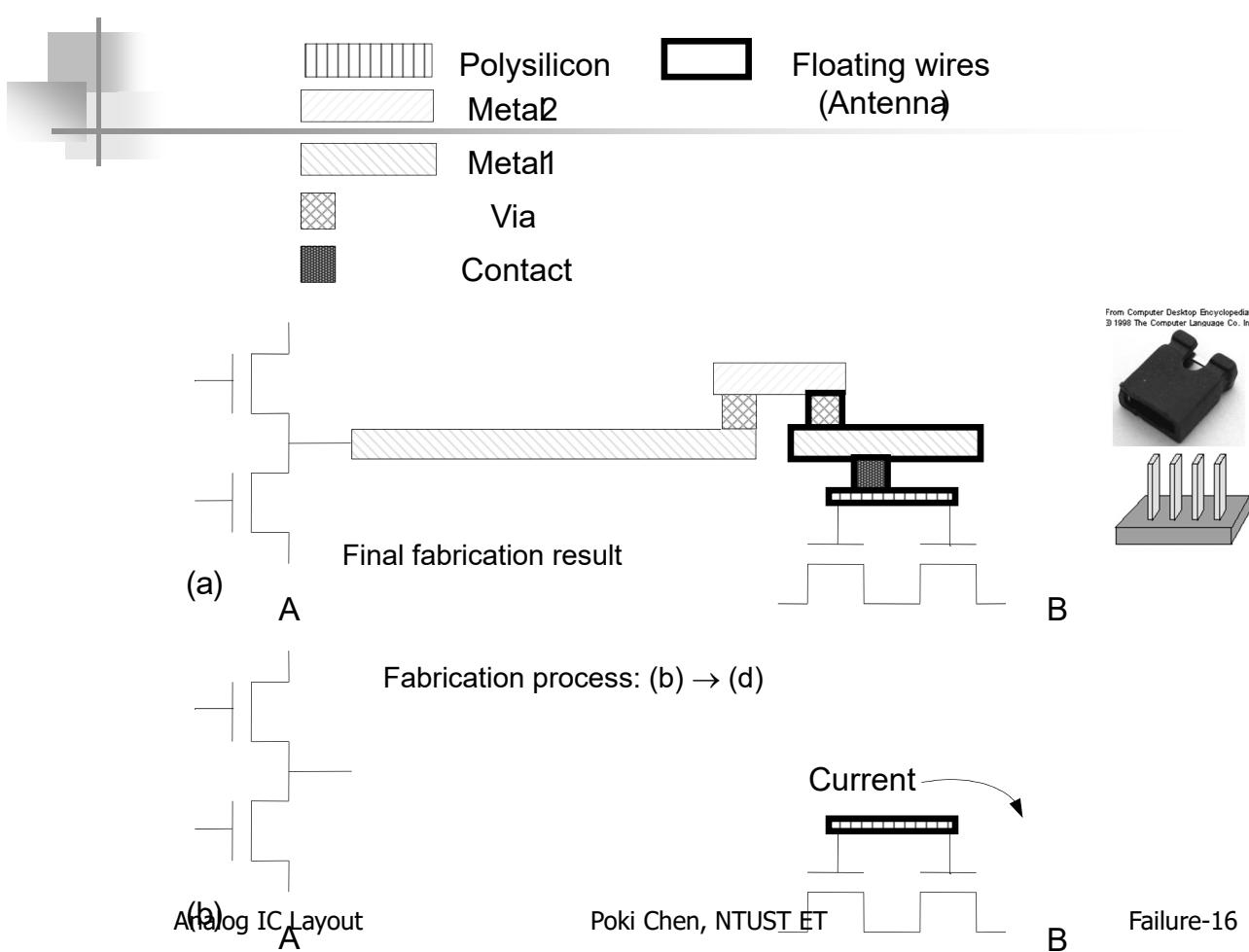
■ Discontinuity in metal 1 to avoid antenna effect (b)

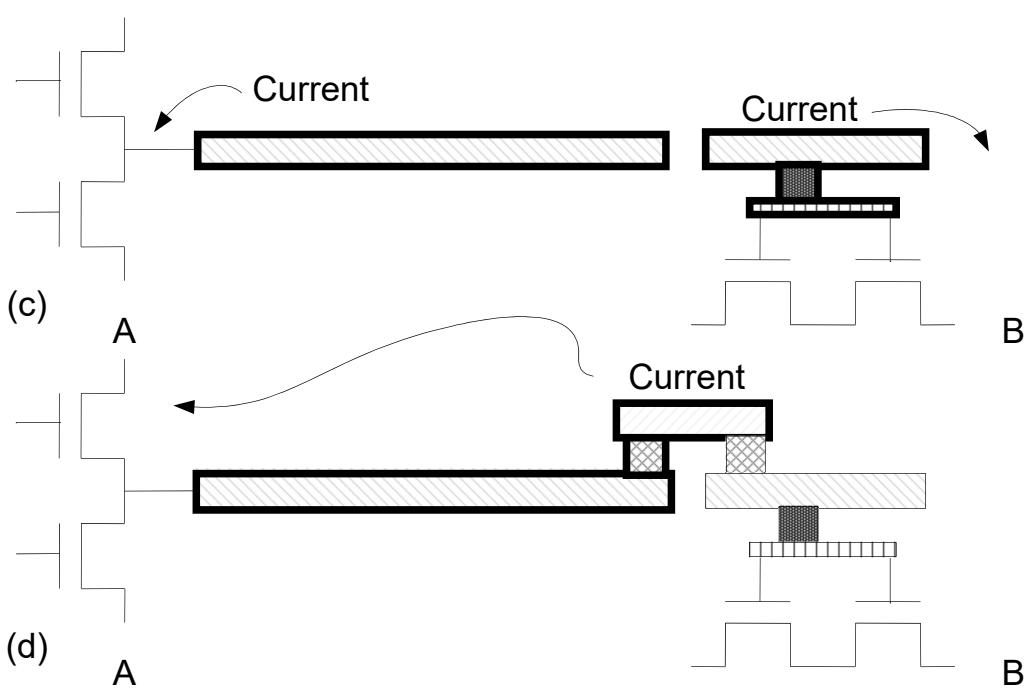


(a)
Analog IC Layout



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Failure-15





Analog IC Layout

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Failure-17

- Embedded protection diode
- Diode inserting after placement and route

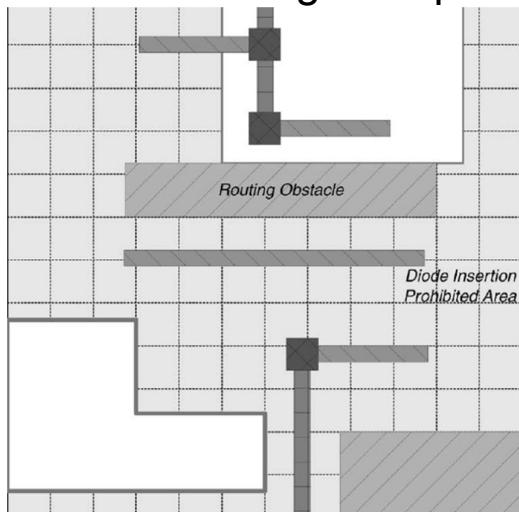
Analog IC Layout

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Failure-18

- ☐ Embedded protection diode

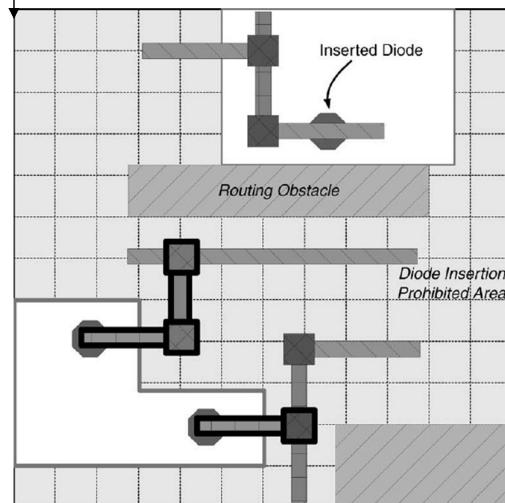
- ☐ Diode inserting after placement and route



↑ Routing obstacle and diode insertion obstacles are scattered over the routing space.

Analog IC Layout

Diode could be inserted under the violating wire. The violating wires in the diode insertion obstacles need wire extension to reach the diodes.



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Failure-19