Yuhan Qiu

Electrical Engineering Undergraduate - Embedded systems, Firmware & FPGA

☐ +1 236-868-7782 | @ qiuyuhan66@gmail.com | in LinkedIn | GitHub | Vancouver, BC, Canada

TECHNICAL SKILLS

Programming / Software Skills: C, C++, Python, Verilog/SystemVerilog, Vivado, ModelSim, Quartus, MATLAB

Embedded & Systems: MCU and FPGA-based systems (STM32, ESP32, DE1-SoC, Xilinx), peripheral communication(ADC, UART, SPI, I2C), real-time systems, system-level debugging and validation

Laboratory & Testing: Waveform generator, oscilloscope, multimeter, soldering, power supply

TECHNICAL EXPERIENCE

UBC Agrobot   Vancouver, BC
Navigation & Embedded Systems Member   *Sep 2025 – Present*

- Designed and tested real-time motor control logic for an autonomous field robot to support navigation and speed regulation under varying load conditions
- Implemented ROS and micro-ROS interfaces for embedded motor command and feedback exchange
- Interfaced motor drivers, encoders, and controllers for closed-loop control
- Developed PID-based motor control and communication in C++ and Python

Uterine Health Research Lab, UBC Faculty of Medicine   Vancouver, BC
AI Research Assistant   *Jun 2025 – Nov 2025*

- Annotated and validated 200+ ultrasound imaging datasets for AI model development, ensuring compliance with de-identification, ethics, and licensing standards
- Evaluated dataset quality by reviewing medical publications and metadata, documenting findings in a structured spreadsheet for team-wide use
- Collaborated with researchers to define data quality and selection criteria, supporting downstream model development

TECHNICAL PROJECT

Miniature Ultrasound Transducer for Wearable Medical Imaging   *Sep 2025 – Present*

- Designed an FPGA preprocessing pipeline for a 16-channel ultrasound system, including synchronized multi-channel acquisition, filtering, envelope detection, and decimation for wireless transmission
- Defined and implemented FPGA–AFE control interfaces for programmable excitation timing, channel selection, VGA gain control, and Doppler processing support
- Contributed to a modular PCB, separating the FPGA SoM, high-voltage pulser, and 16-channel AFE to support scalable system bring-up and future upgrades

FPGA SD-card Reader   *Jun 2025 – Sep 2025*

- Developed an FPGA-based SD-card host in SystemVerilog using the SD bus, supporting SDv1/SDv2/SDHC cards and FAT16/FAT32 file systems
- Built sector-level read logic and file-system parsing to locate and stream non-contiguous files, with full RTL simulation and on-board validation

Cardio Health Monitor   *Feb 2024 – Mar 2024*

- Implemented a heart rate monitoring system in C, enabling real-time visualization of heart rate variations on an oscilloscope and cardio health feedback on an LCD display
- Created a PPG sensor for amplified pulse detection with an AFE and ADC, and verified signal integrity and timing using laboratory instrumentation

EDUCATION

University of British Columbia   Vancouver, BC
Bachelor of Applied Science in Electrical Engineering   *Expected Graduation: May 2026*