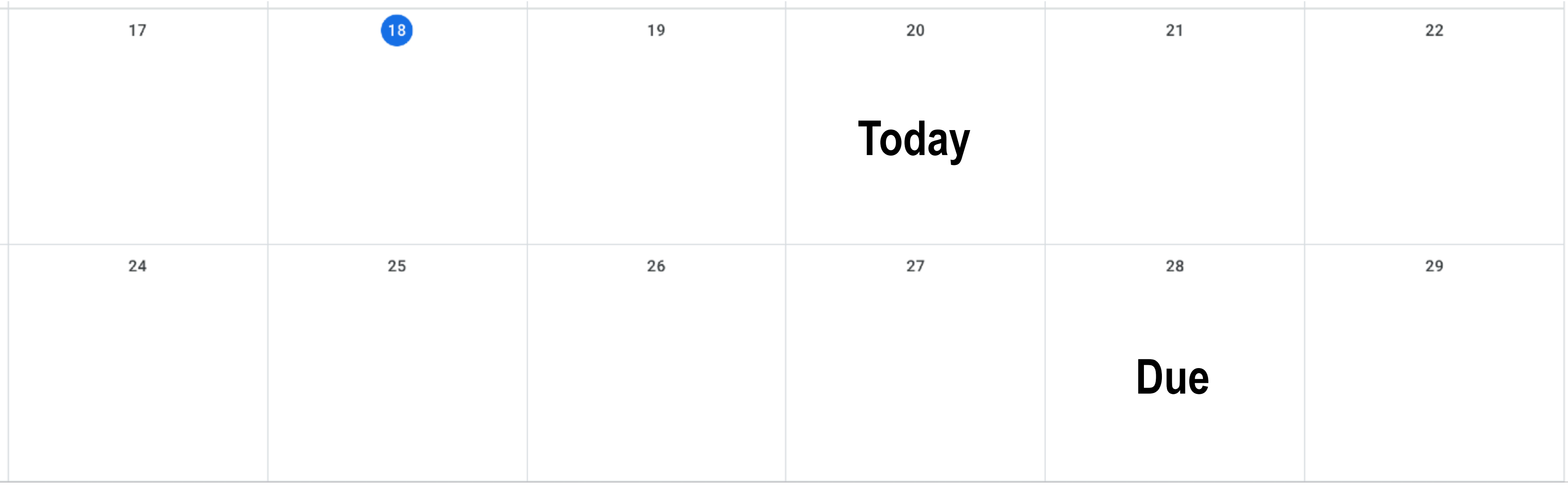
CSC 252: Computer Organization
Spring 2020: Lecture 11

Instructor: Yuhao Zhu

Department of Computer Science
University of Rochester

Announcement

- Programming assignment 3 is out
  - Details: https://www.cs.rochester.edu/courses/252/spring2020/labs/assignment3.html
  - Due on **Feb. 28**, 11:59 PM
  - You (may still) have 3 slip days



17	18	19	20 **Today**	21	22
24	25	26	27	28 **Due**	29

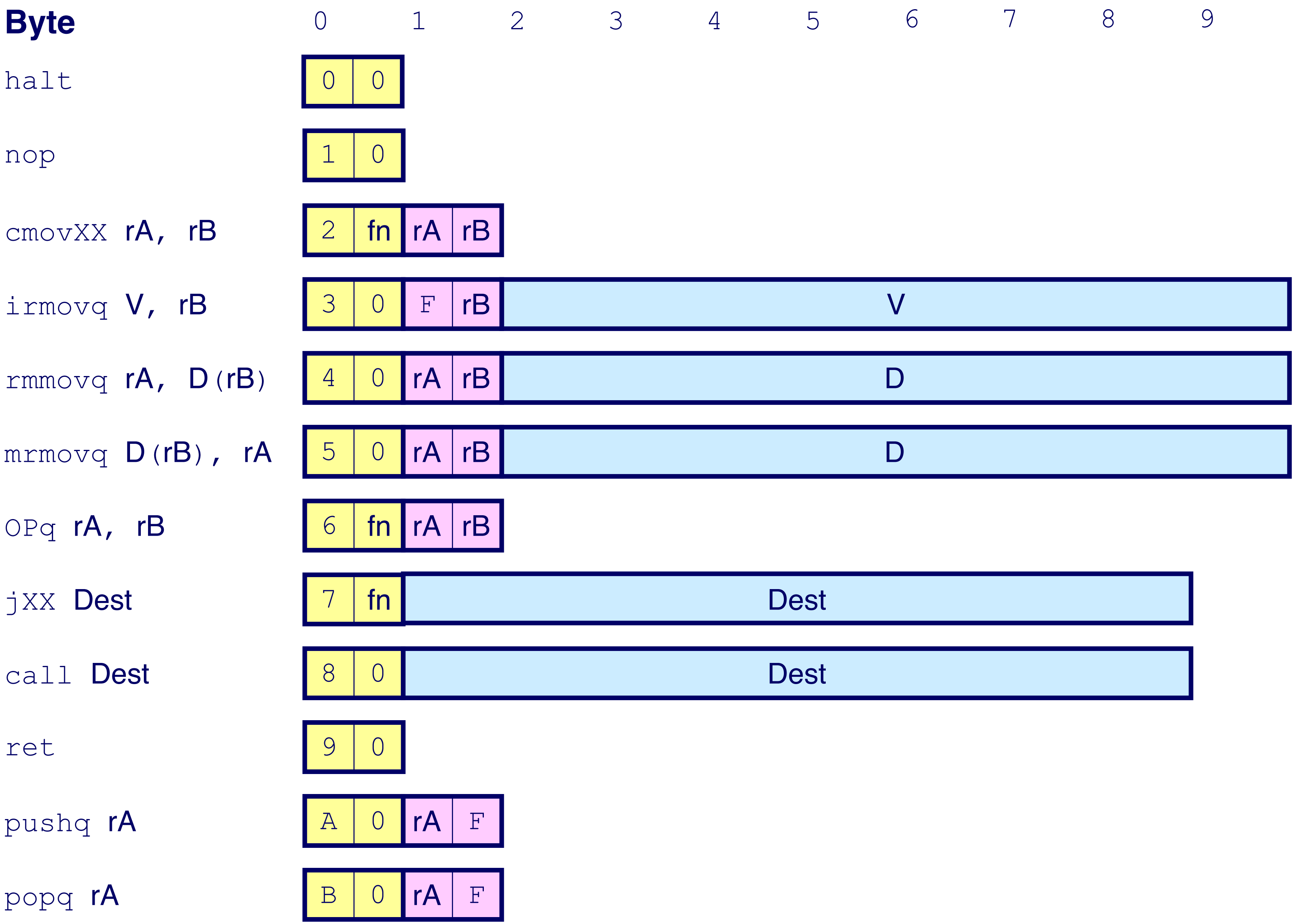
Announcement

- Grades for lab2 are posted.
- If you think there are some problems
  - Take a deep breath
  - Tell yourself that the teaching staff like you, not the opposite
  - Email/go to Shuang or Sudhanshu's office hours and explain to them why you should get more points, and they will fix it for you

Announcement

- Programming assignment 3 is in x86 assembly language. Seek help from TAs.
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

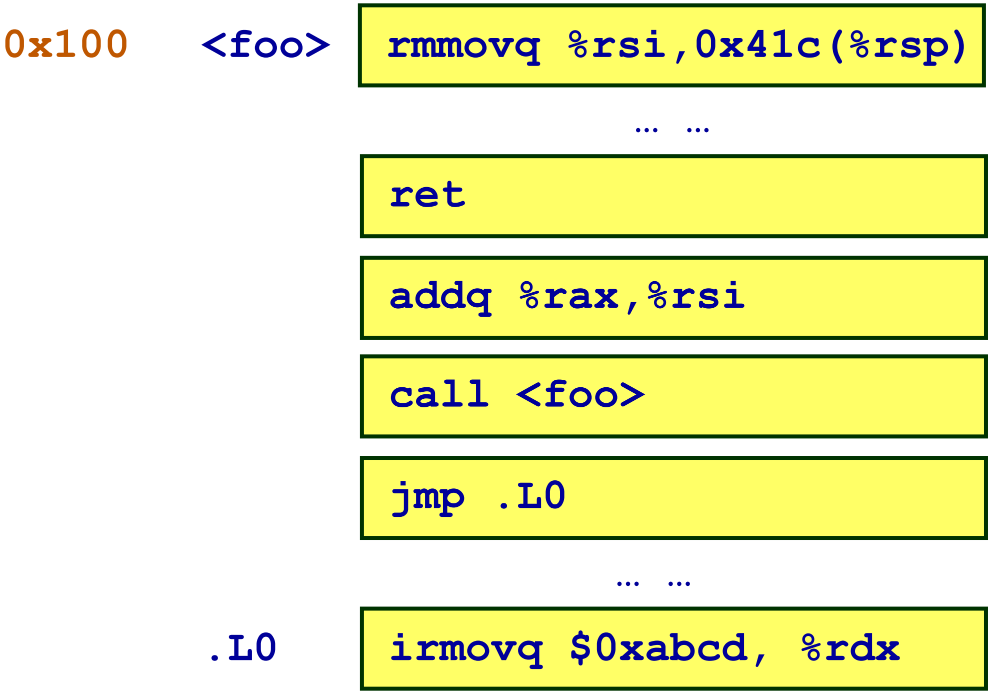
Y86 Instruction Encoding



Byte	0	1	2	3	4	5	6	7	8	9
`halt`	0 0									
`nop`	1 0									
`cmovXX` rA, rB	2 fn	rA rB								
`irmovq` V, rB	3 0	F rB	V							
`rmmovq` rA, D(rB)	4 0	rA rB	D							
`mrmovq` D(rB), rA	5 0	rA rB	D							
`OPq` rA, rB	6 fn	rA rB								
`jXX` Dest	7 fn	Dest								
`call` Dest	8 0	Dest								
`ret`	9 0									
`pushq` rA	A 0	rA F								
`popq` rA	B 0	rA F								

How Does An Assembler Work?

How Does An Assembler Work?



```
0x100    <foo>   rmmovq %rsi,0x41c(%rsp)
                        …  …
                 ret
                 addq %rax,%rsi
                 call <foo>
                 jmp .L0
                        …  …
          .L0    irmovq $0xabcd, %rdx
```

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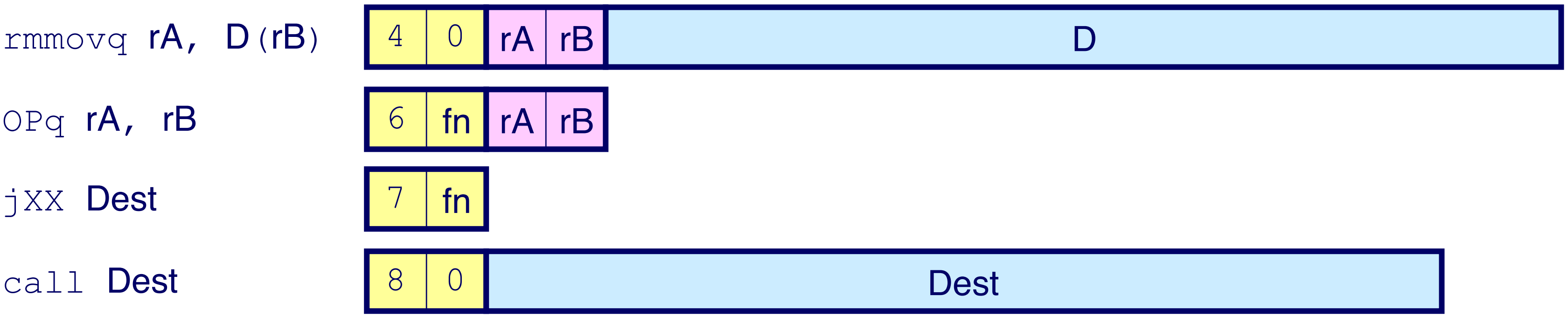

rmmovq rA, D(rB) | 4 | 0 | rA | rB | D

OPq rA, rB | 6 | fn | rA | rB

jXX Dest | 7 | fn

call Dest | 8 | 0 | Dest

```
0x100    <foo>   rmmovq %rsi,0x41c(%rsp)
                       …  …
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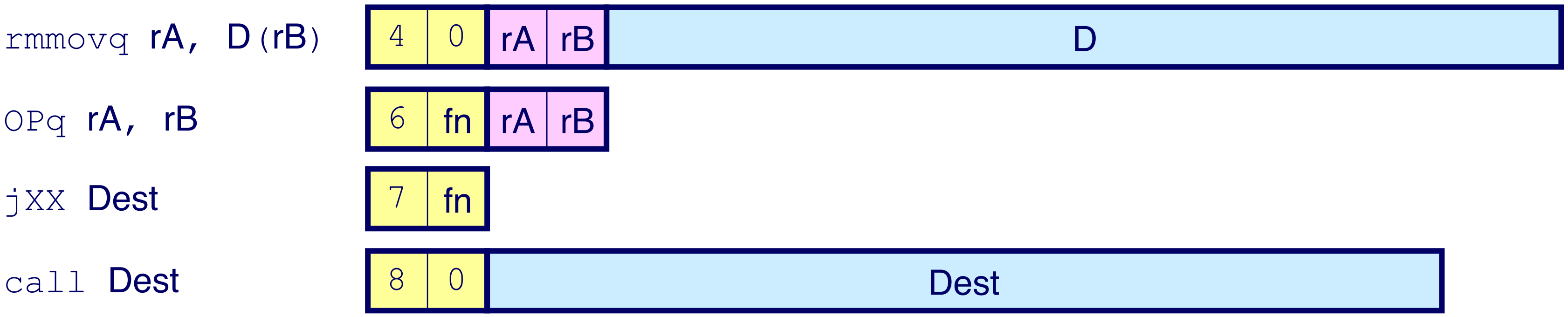
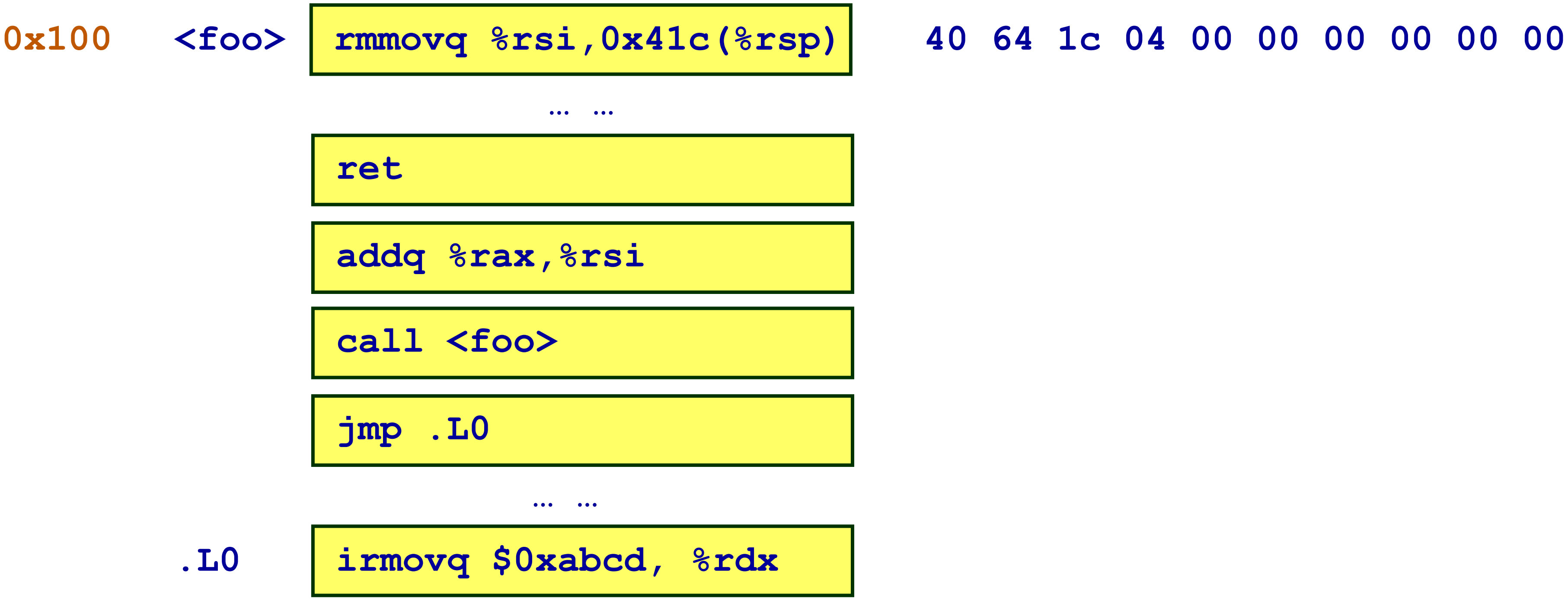


`rmmovq rA, D(rB)`	4	0	rA	rB	D
`OPq rA, rB`	6	fn	rA	rB	
`jXX Dest`	7	fn			
`call Dest`	8	0	Dest		



```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)     40 64 1c 04 00 00 00 00 00 00
                        ...  ...
                ret
                addq %rax,%rsi
                call <foo>
                jmp .L0
                        ...  ...
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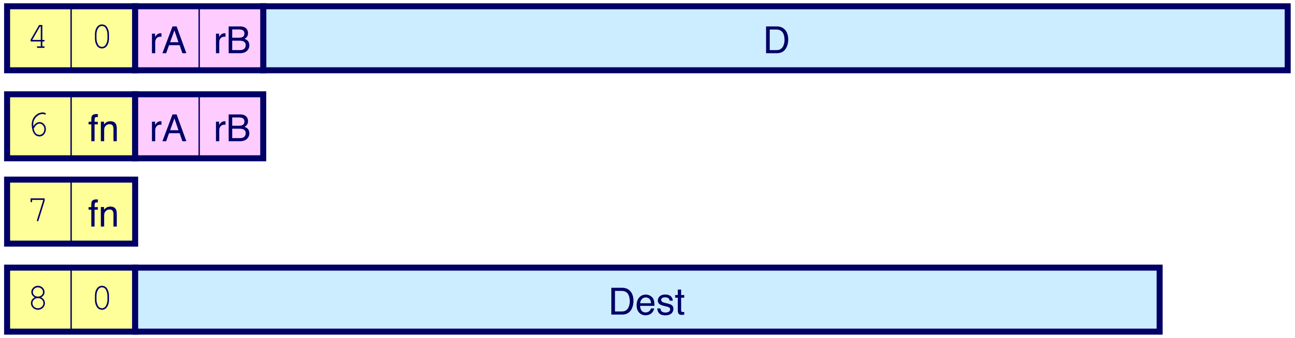

rmmovq rA, D(rB)

OPq rA, rB

jXX Dest

call Dest

```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)     40 64 1c 04 00 00 00 00 00 00
                … …
                ret                          90
                addq %rax,%rsi
                call <foo>
                jmp .L0
                … …
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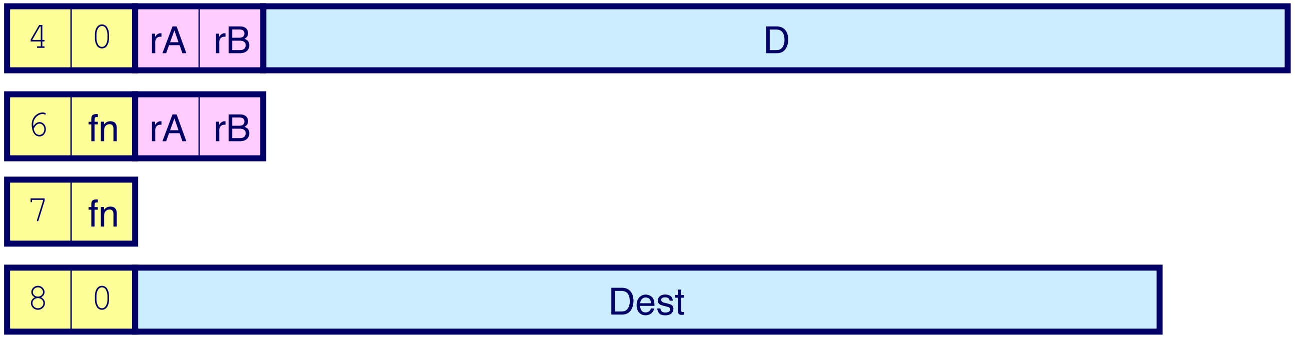
```

How Does An Assembler Work?



rmmovq rA, D(rB)	4	0	rA	rB	D
OPq rA, rB	6	fn	rA	rB	
jXX Dest	7	fn			
call Dest	8	0	Dest		

```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                      …  …
                ret                        90
                addq %rax,%rsi             60 06
                call <foo>
                jmp .L0
                      …  …
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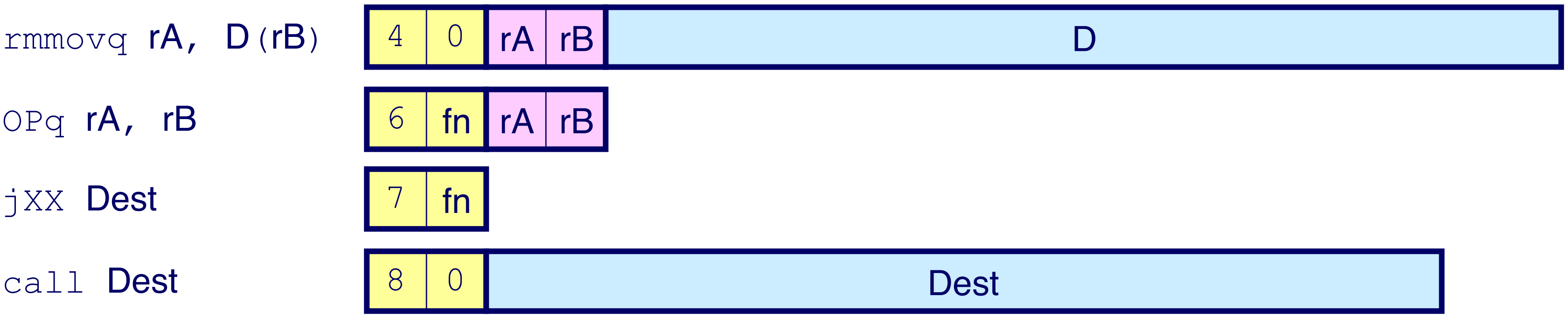
How Does An Assembler Work?



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OPq rA, rB	6	fn	rA	rB	
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                          ...  ...
                ret                         90
                addq %rax,%rsi              60 06
                call <foo>                  80 06 00 01 00 00 00 00 00 00
                jmp .L0
                          ...  ...
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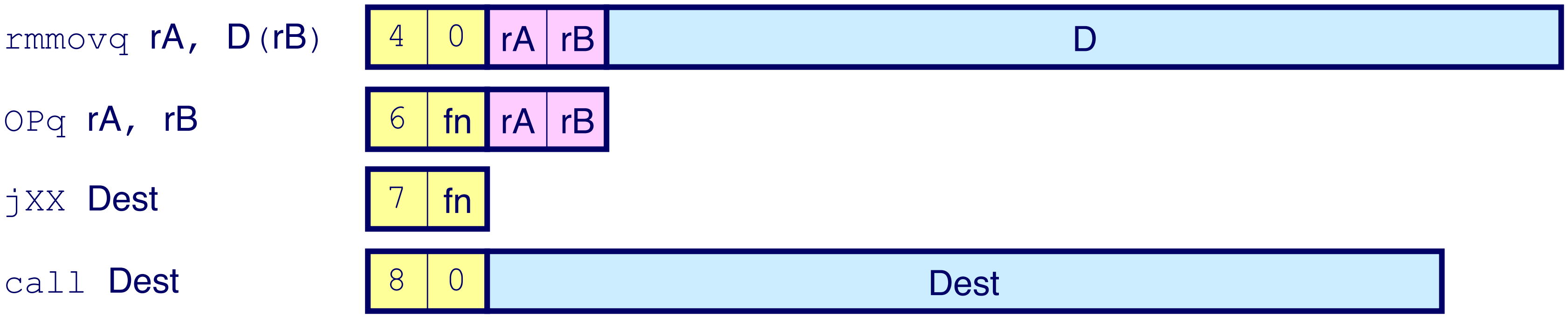

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OPq rA, rB | 6 | fn | rA | rB

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                     …  …
               ret                        90
               addq %rax,%rsi             60 06
               call <foo>                 80 06 00 01 00 00 00 00 00 00
               jmp .L0                    70 ????????
                     …  …
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rmmovq rA, D(rB)	4	0	rA	rB	D
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0x100   <foo>   rmmovq %rsi,0x41c(%rsp)     40 64 1c 04 00 00 00 00 00 00
                          … …
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                addq %rax,%rsi              60 06
                call <foo>                  80 06 00 01 00 00 00 00 00 00
                jmp .L0                     70 ????????
                          … …
        .L0     irmovq $0xabcd, %rdx        30 f2 cd ab 00 00 00 00 00 00
```

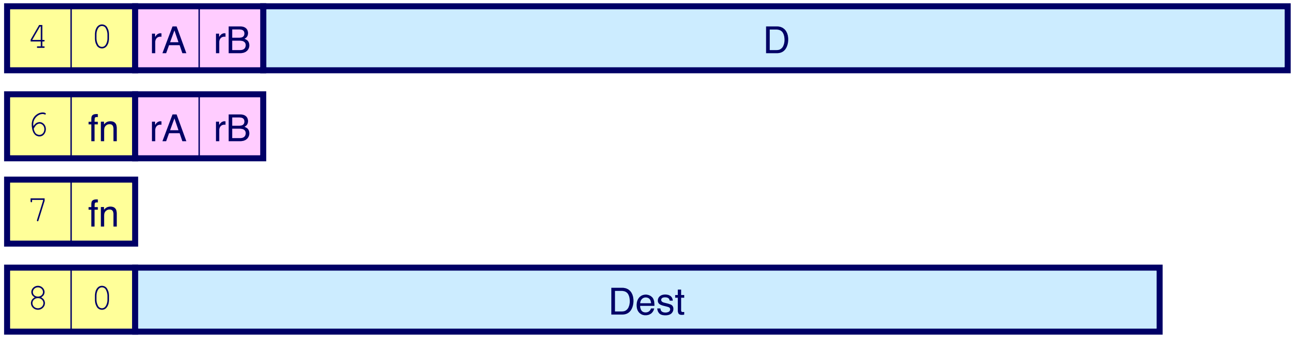
How Does An Assembler Work?

`rmmovq` rA, D(rB)

`OPq` rA, rB

`jXX` Dest

`call` Dest



```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                ...  ...
                ret                        90
                addq %rax,%rsi             60 06
                call <foo>                 80 06 00 01 00 00 00 00 00 00
                jmp .L0                    70 ????????
                ...  ...
        .L0     irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

0x100 + the lengths of all instructions in-between

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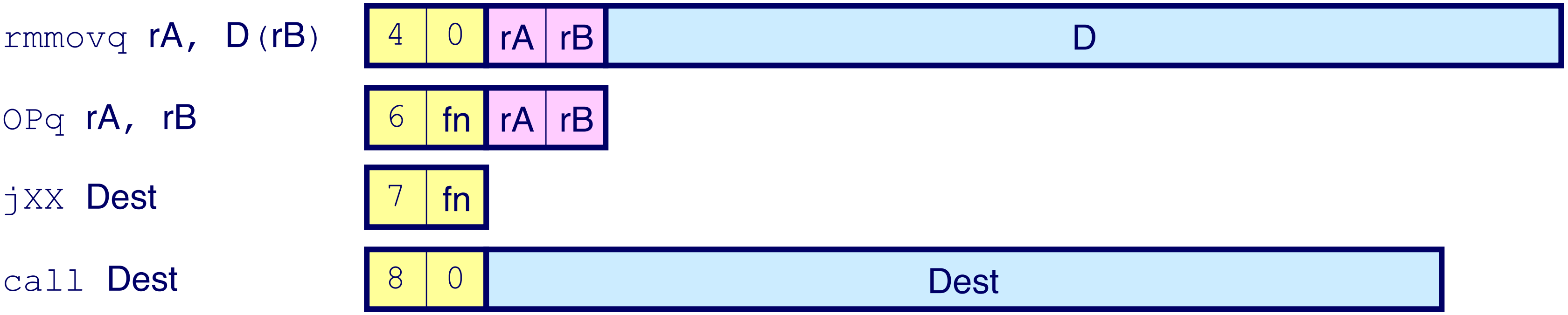

rmmovq rA, D(rB)	4	0	rA	rB	D
OPq rA, rB	6	fn	rA	rB	
jXX Dest	7	fn			
call Dest	8	0	Dest		

```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                … …
                ret                        90
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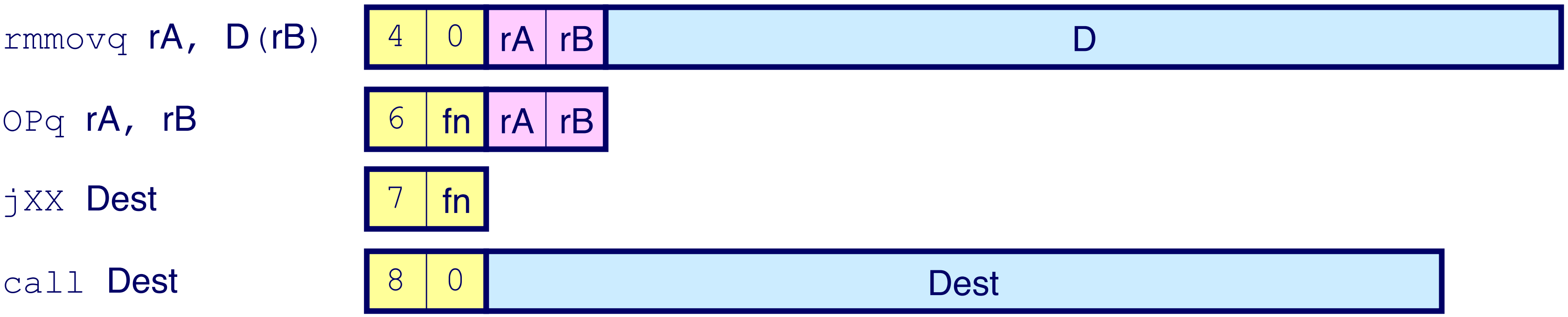
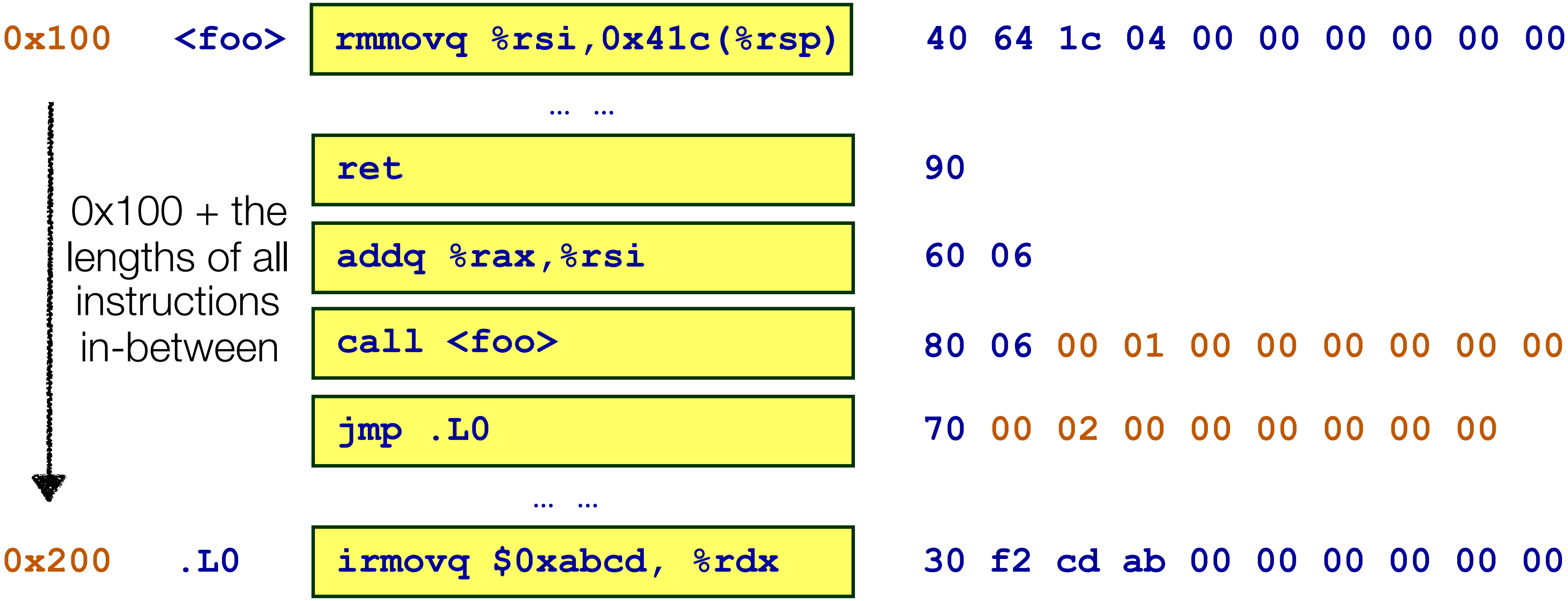


rmmovq rA, D(rB)	4	0	rA	rB	D
OPq rA, rB	6	fn	rA	rB	
jXX Dest	7	fn			
call Dest	8	0	Dest		

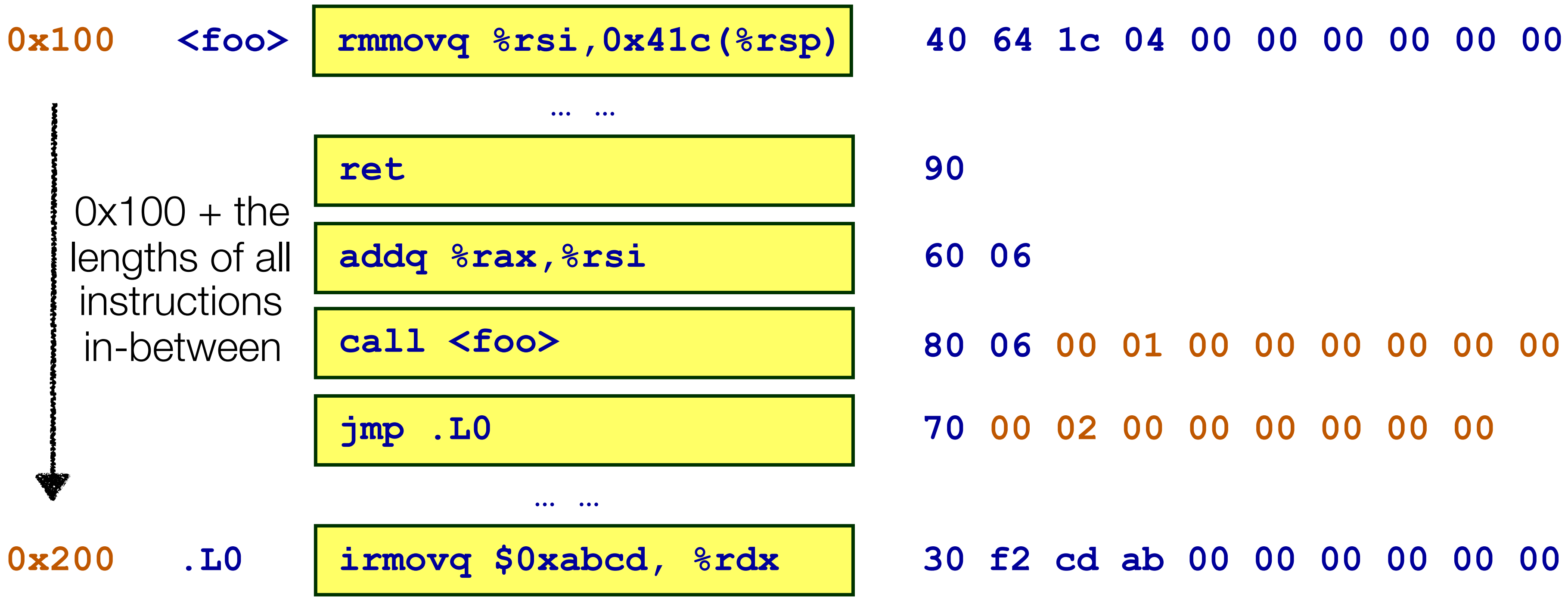


```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                ... ...
                ret                        90
                addq %rax,%rsi             60 06
                call <foo>                 80 06 00 01 00 00 00 00 00 00
                jmp .L0                    70 00 02 00 00 00 00 00 00
                ... ...
0x200   .L0     irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

0x100 + the lengths of all instructions in-between

How Does An Assembler Work?

- The assembler is a program that translates assembly code to binary code
- The OS tells the assembler the start address of the code (sort of…)
- Translate the assembly program line by line
- Need to build a “label map” that maps each label to its address



```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)   40 64 1c 04 00 00 00 00 00 00
                … …
                ret                       90
                addq %rax,%rsi            60 06
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```

0x100 + the lengths of all instructions in-between

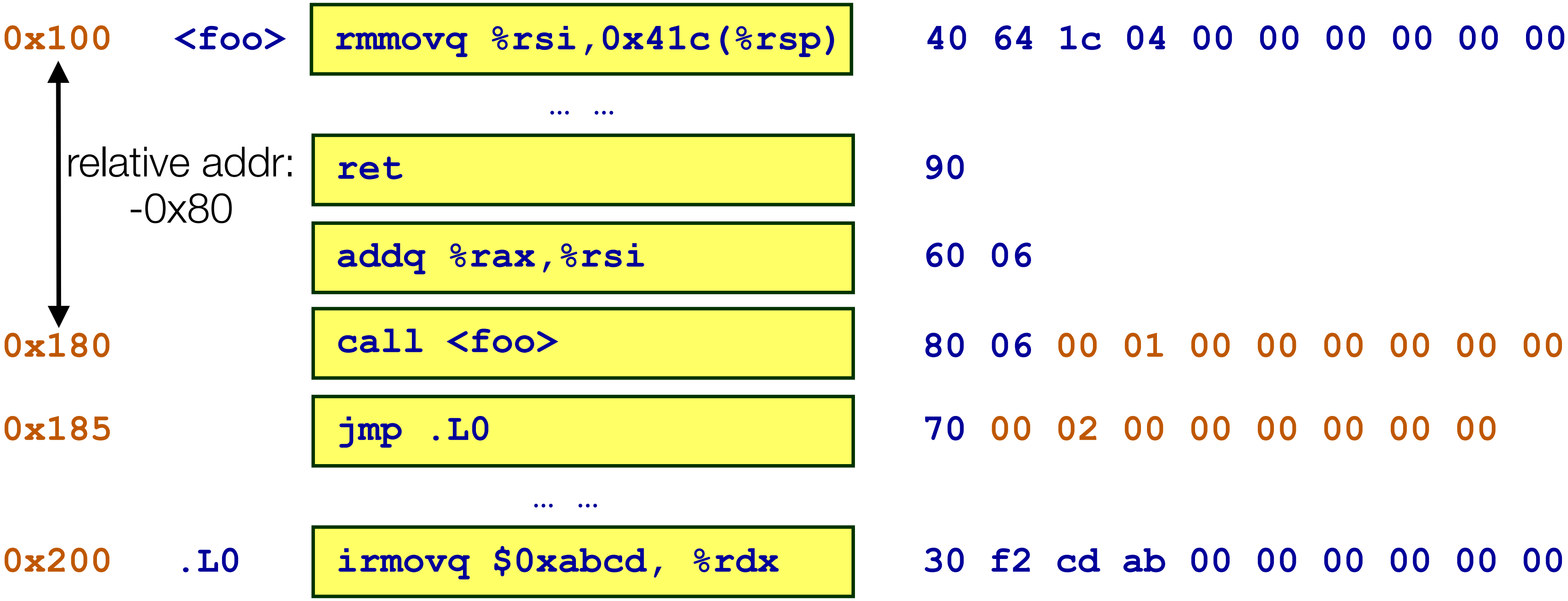
How Does An Assembler Work?

- What if the ISA encoding uses relative address for jump and call?

```
0x100   <foo>  rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                        … …
               ret                        90
               addq %rax,%rsi             60 06
0x180          call <foo>                 80 06 00 01 00 00 00 00 00 00
0x185          jmp .L0                    70 00 02 00 00 00 00 00 00
                        … …
0x200   .L0    irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

How Does An Assembler Work?

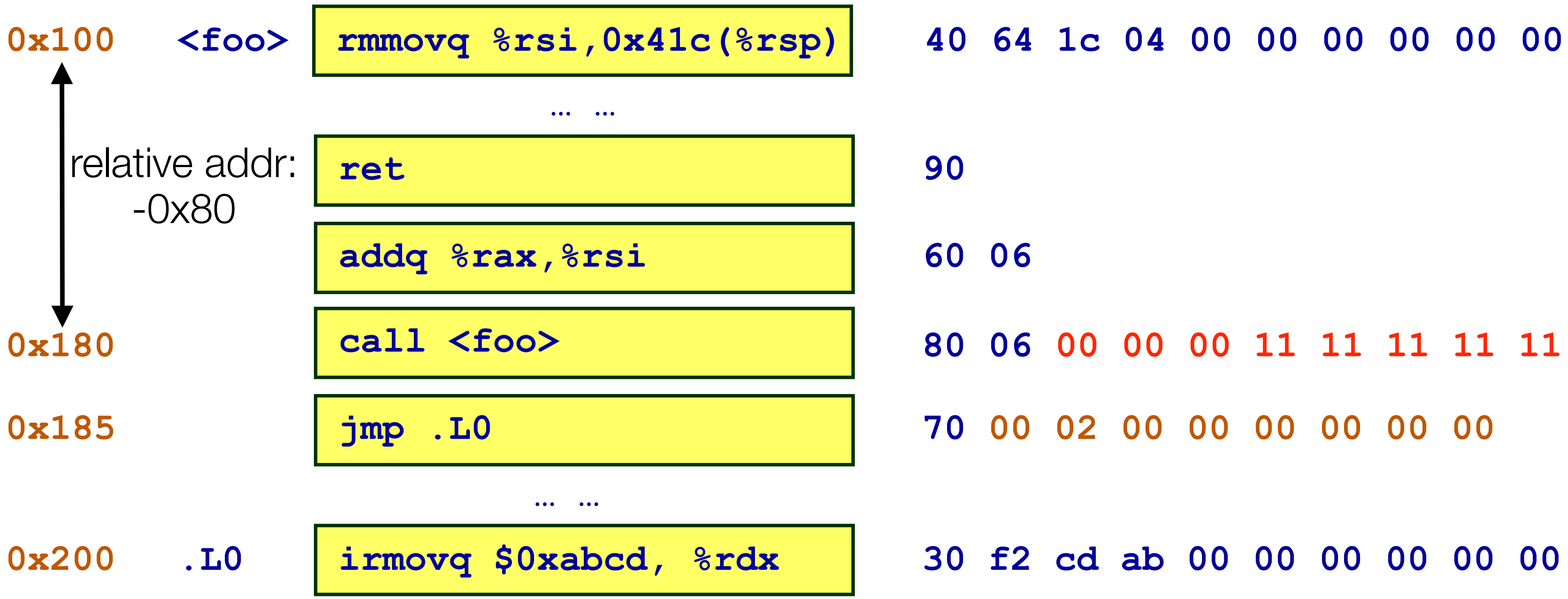
- What if the ISA encoding uses relative address for jump and call?



```
0x100   <foo>  rmmovq %rsi,0x41c(%rsp)   40 64 1c 04 00 00 00 00 00 00
                       …   …
               ret                        90
relative addr:
    -0x80      addq %rax,%rsi             60 06
0x180          call <foo>                 80 06 00 01 00 00 00 00 00 00
0x185          jmp .L0                    70 00 02 00 00 00 00 00 00
                       …   …
0x200   .L0    irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

How Does An Assembler Work?

- What if the ISA encoding uses relative address for jump and call?



```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                ... ...
                ret                        90
                addq %rax,%rsi             60 06
0x180           call <foo>                 80 06 00 00 00 11 11 11 11 11
0x185           jmp .L0                    70 00 02 00 00 00 00 00 00
                ... ...
0x200   .L0     irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

relative addr: -0x80

How Does An Assembler Work?

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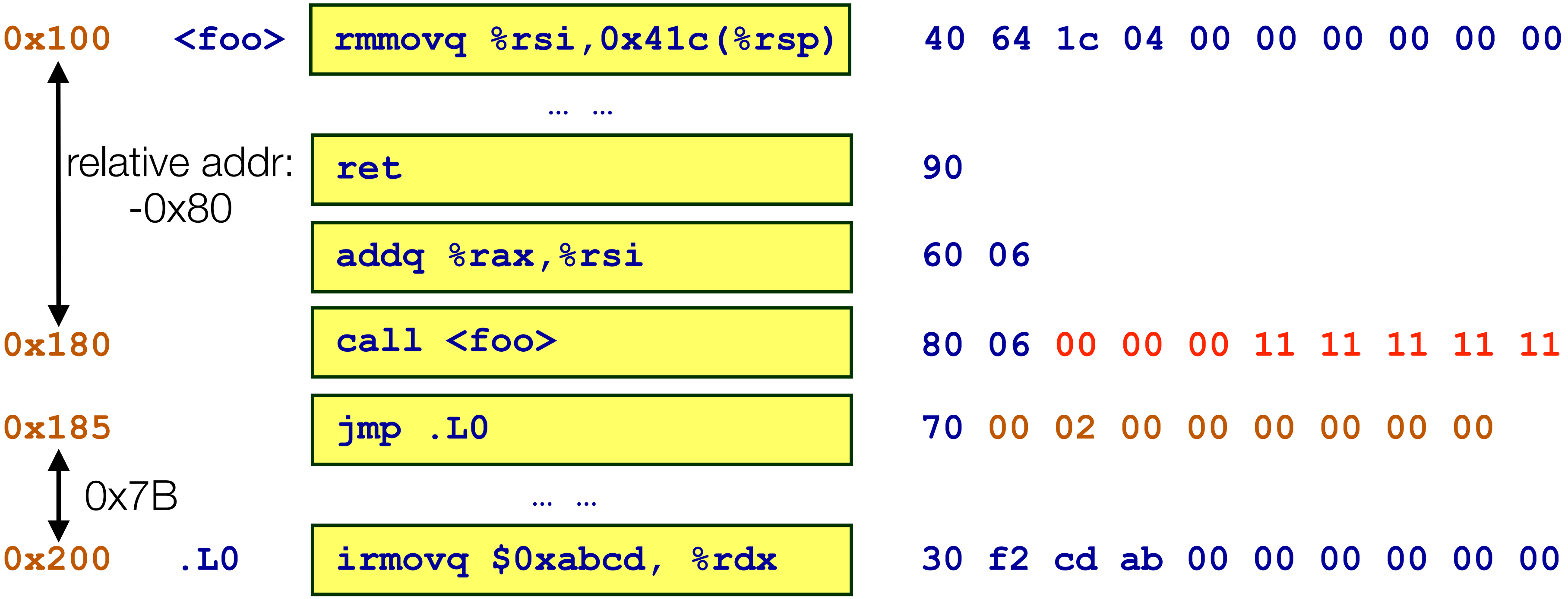

```
0x100  <foo>  rmmovq %rsi,0x41c(%rsp)   40 64 1c 04 00 00 00 00 00 00
                      ... ...
relative addr:
   -0x80      ret                       90
              addq %rax,%rsi            60 06
0x180         call <foo>                80 06 00 00 00 11 11 11 11 11
0x185         jmp .L0                   70 00 02 00 00 00 00 00 00
   0x7B               ... ...
0x200  .L0    irmovq $0xabcd, %rdx      30 f2 cd ab 00 00 00 00 00 00
```

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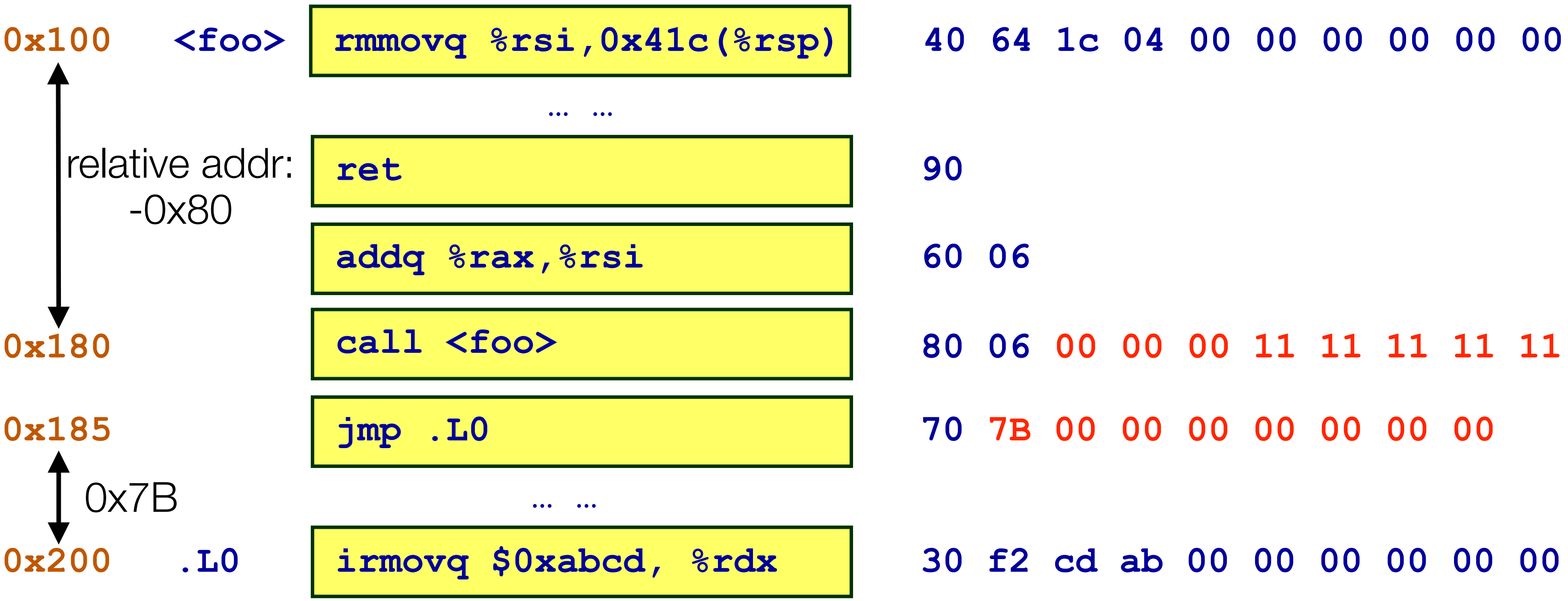
- What if the ISA encoding uses relative address for jump and call?



```
0x100   <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                       ...  ...
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                addq %rax,%rsi             60 06
0x180           call <foo>                 80 06 00 00 00 11 11 11 11 11
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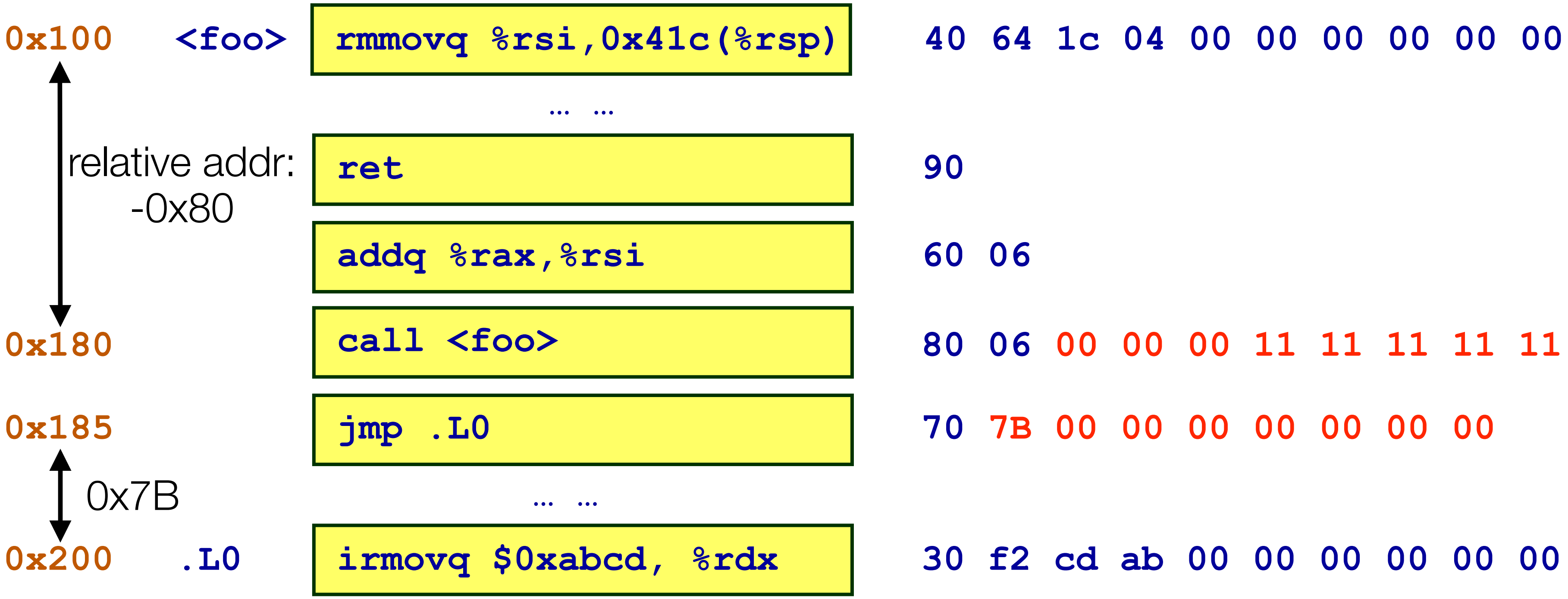
                       ...  ...
0x200   .L0     irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

relative addr:
-0x80

0x7B

How Does An Assembler Work?

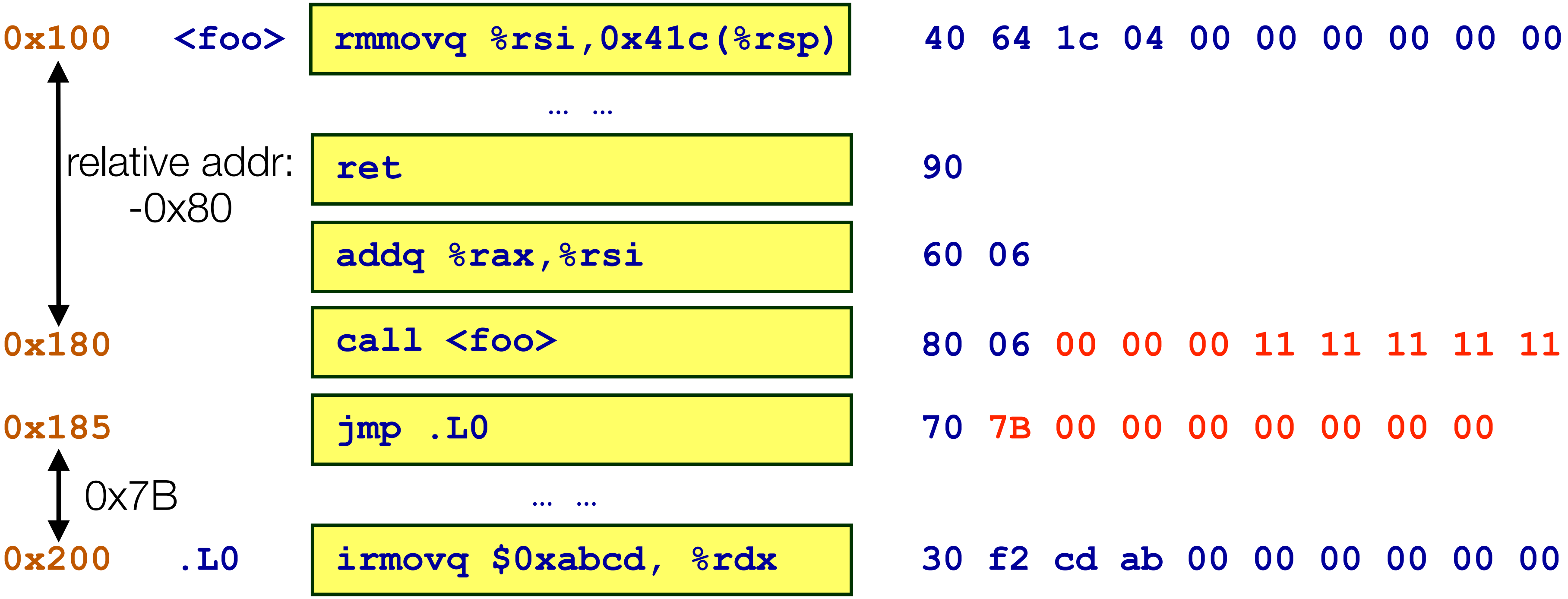
- What if the ISA encoding uses relative address for jump and call?
- If we use relative address, the exact start address of the code doesn't matter. Why?



```
0x100   <foo>  rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                     … …
relative addr:  ret                        90
   -0x80        addq %rax,%rsi             60 06
0x180          call <foo>                 80 06 00 00 00 11 11 11 11 11
0x185          jmp .L0                    70 7B 00 00 00 00 00 00 00
  0x7B               … …
0x200   .L0    irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```

How Does An Assembler Work?

- What if the ISA encoding uses relative address for jump and call?
- If we use relative address, the exact start address of the code doesn't matter. Why?
- This code is called Position-Independent Code (PIC)

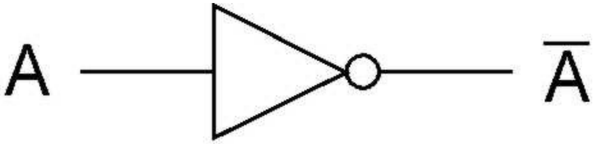


```
0x100  <foo>  rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
              … …
              ret                         90
              addq %rax,%rsi              60 06
0x180         call <foo>                  80 06 00 00 00 11 11 11 11 11
0x185         jmp .L0                     70 7B 00 00 00 00 00 00 00
              … …
0x200  .L0    irmovq $0xabcd, %rdx        30 f2 cd ab 00 00 00 00 00 00
```

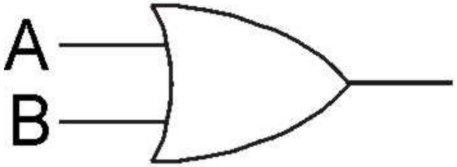
Today: Circuits Basics

- Transistors
- Circuits for computations
- Circuits for storing data

Basic Logic Gates

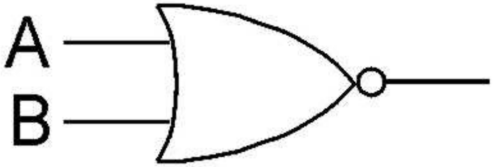


NOT



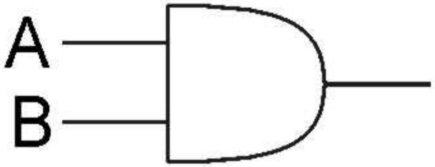
A | B

OR



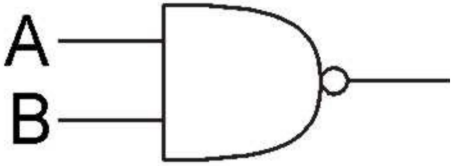
~(A | B)

NOR



A & B

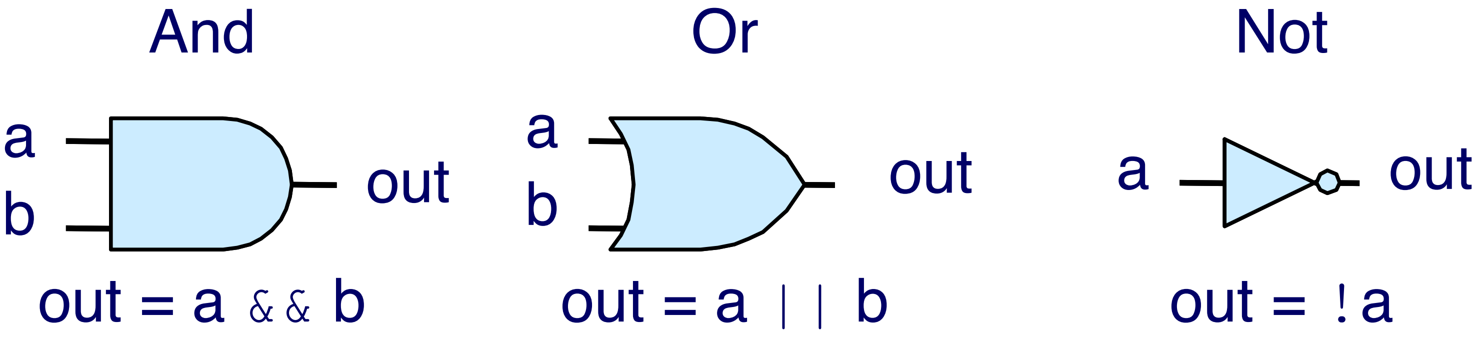
AND



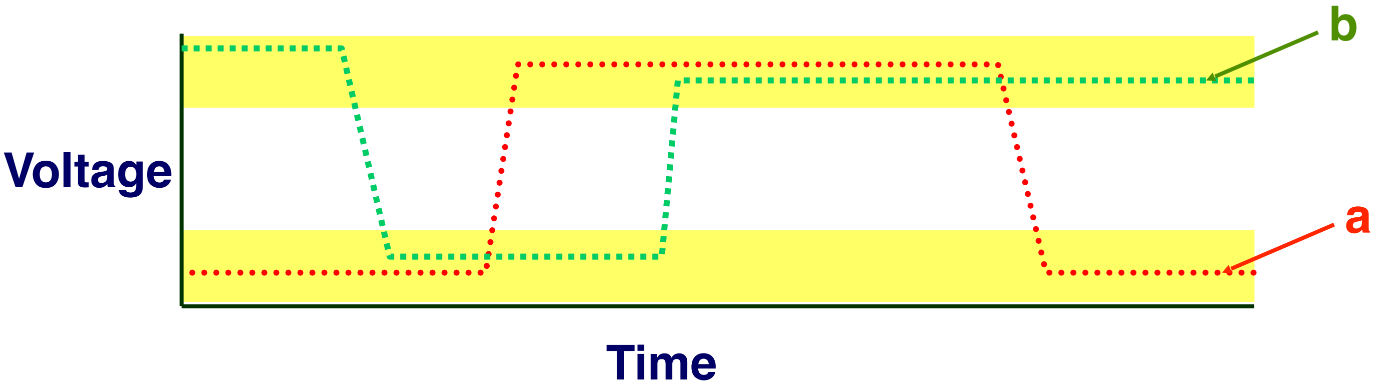
~(A & B)

NAND

Computing with Logic Gates



- Outputs are Boolean functions of inputs
- Respond continuously to changes in inputs with some small delay
- Different gates have different delays (b/c different transistor combinations)



Computing with Logic Gates

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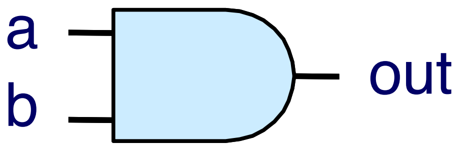
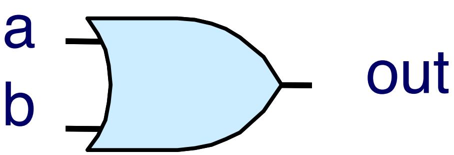


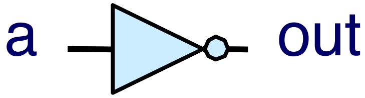
out = a && b

Or



out = a || b

Not



out = !a

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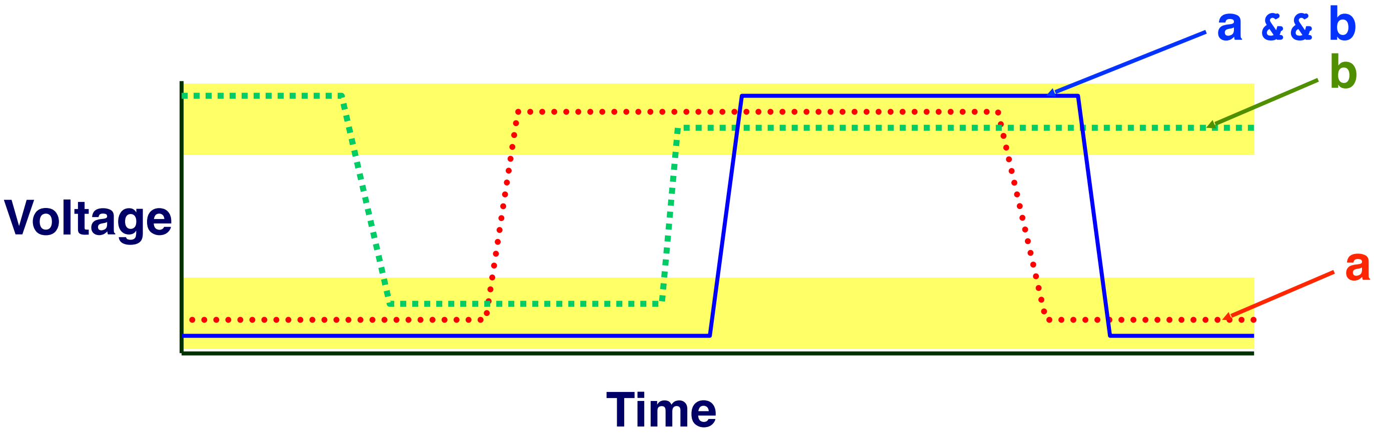

Computing with Logic Gates

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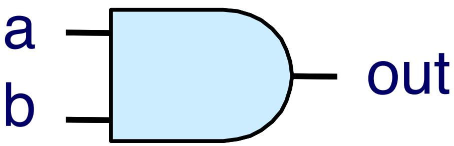

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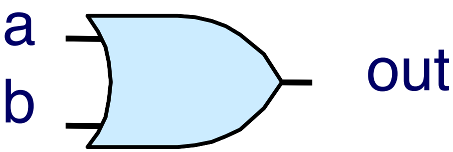

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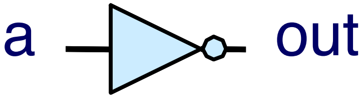

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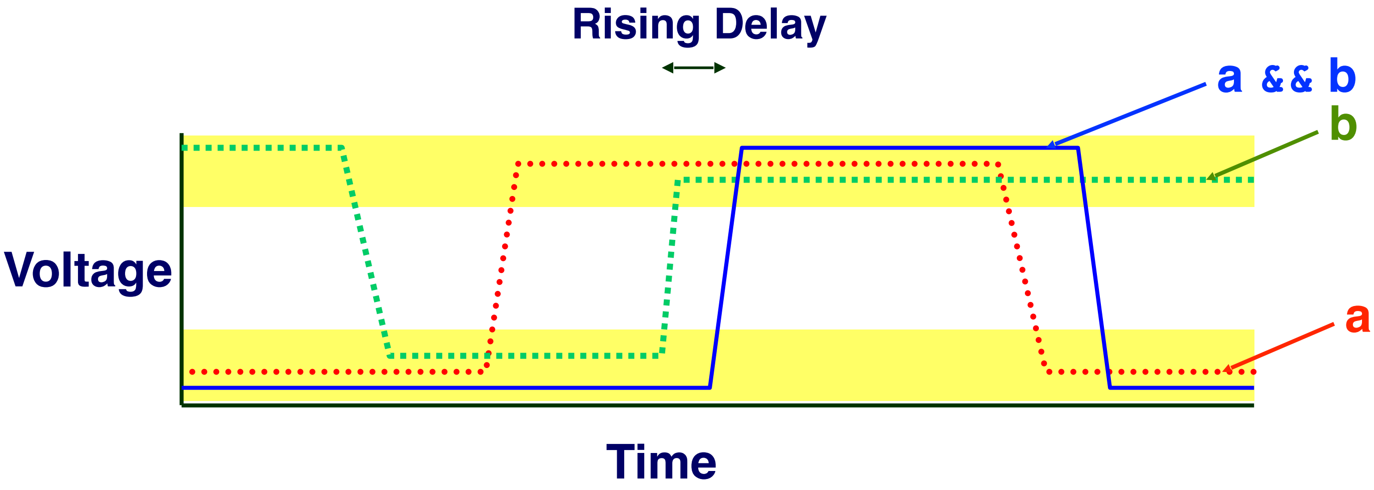
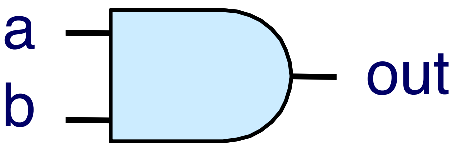


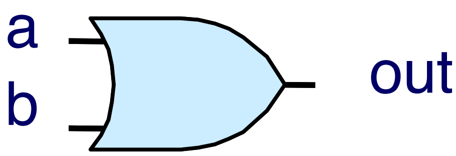
Computing with Logic Gates

And



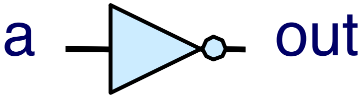
out = a && b

Or



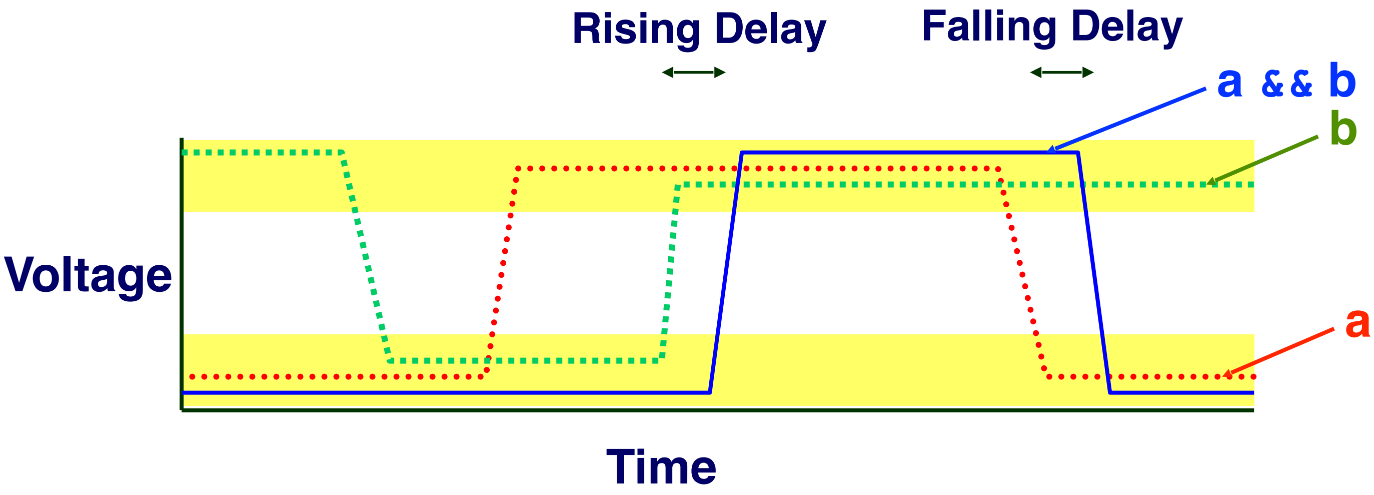
out = a || b

Not

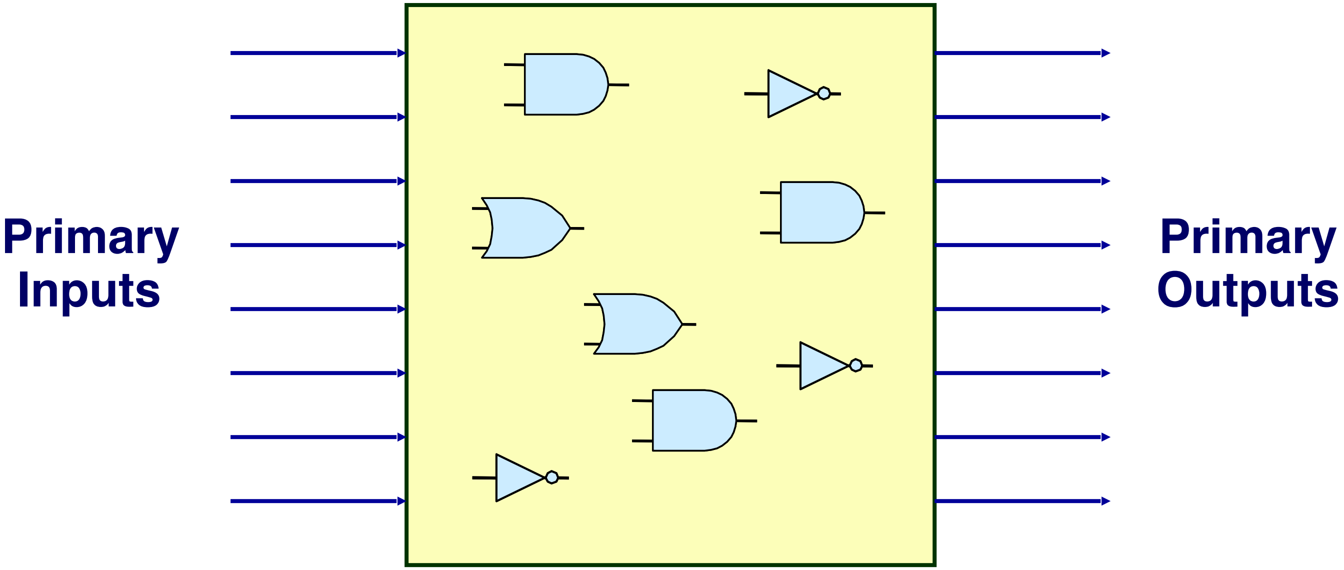


out = !a

- Outputs are Boolean functions of inputs
- Respond continuously to changes in inputs with some small delay
- Different gates have different delays (b/c different transistor combinations)



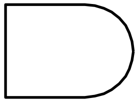
Combinational Circuits



- A Network of Logic Gates
  - Continuously responds to changes on primary inputs
  - Primary outputs become (**after some delay**) Boolean functions of primary inputs

Bit Equality

Bit Equality



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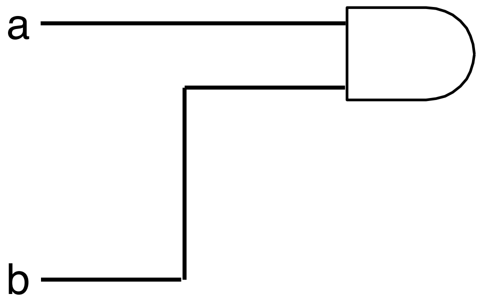

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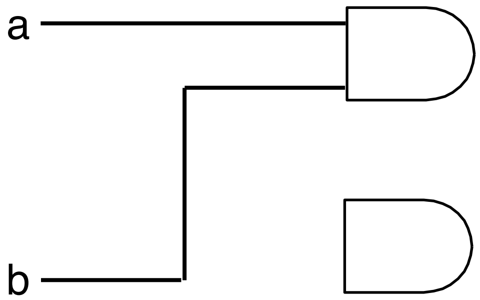

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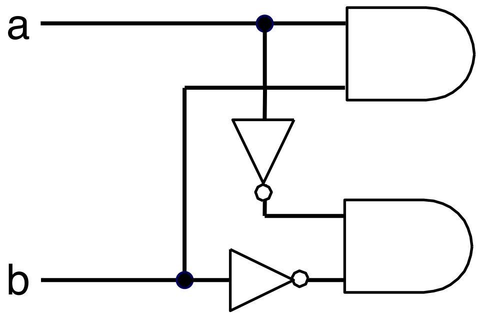

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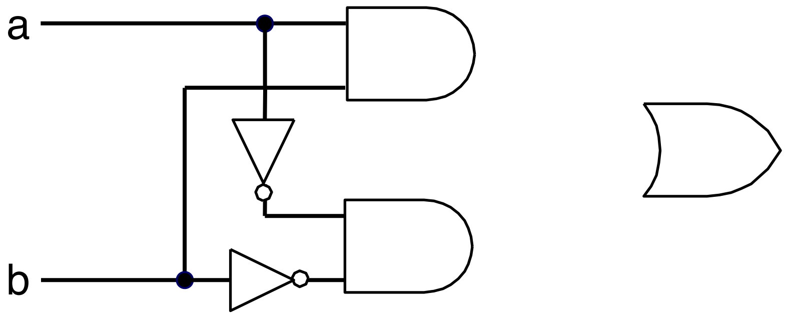

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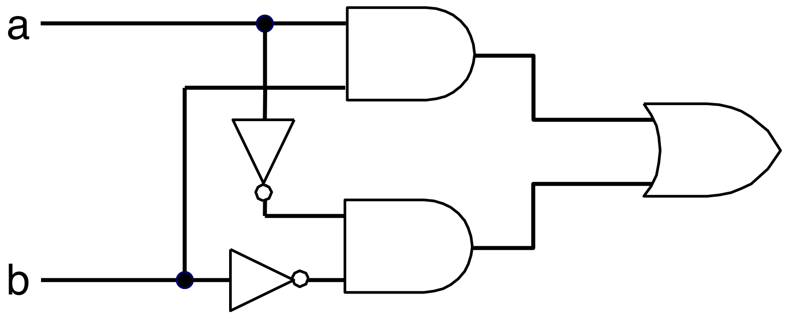

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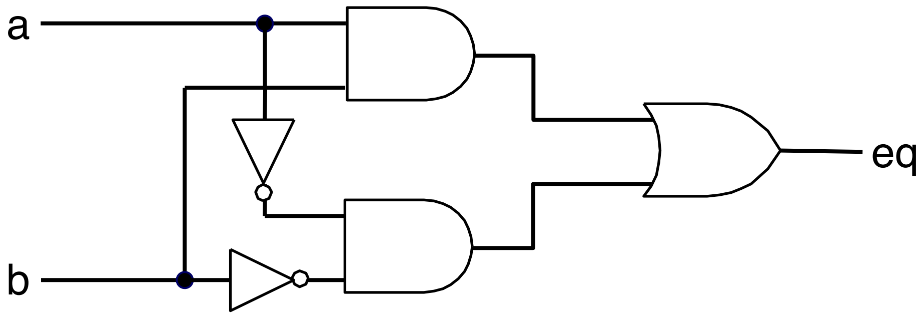

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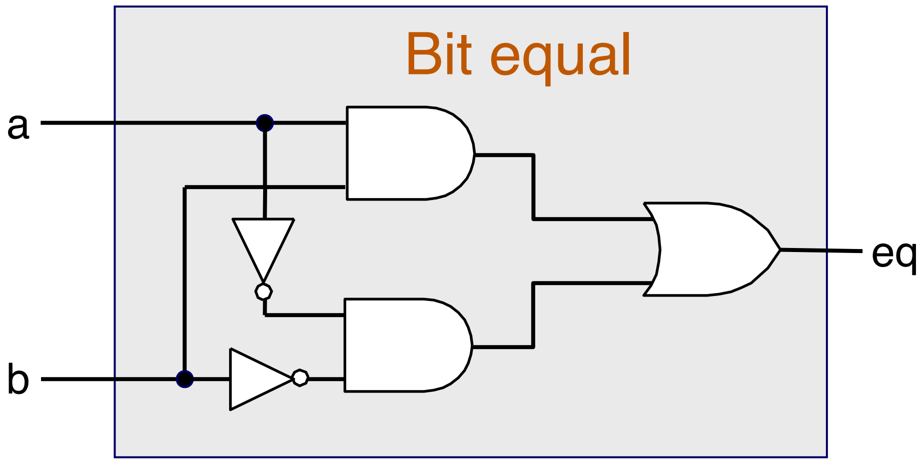
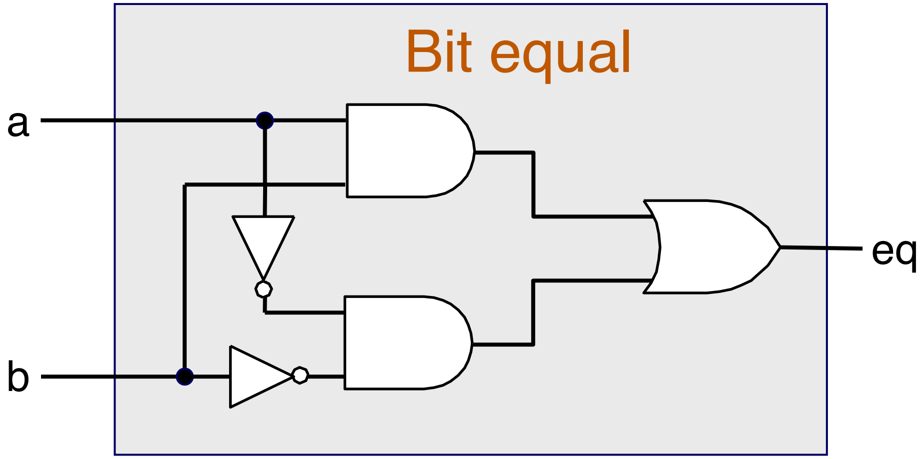


Delay of Bit Equal Circuit



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  - Assuming 1-input NOT takes 1 unit of time, 2-input AND takes 4.3, and 2-input OR takes 4.7

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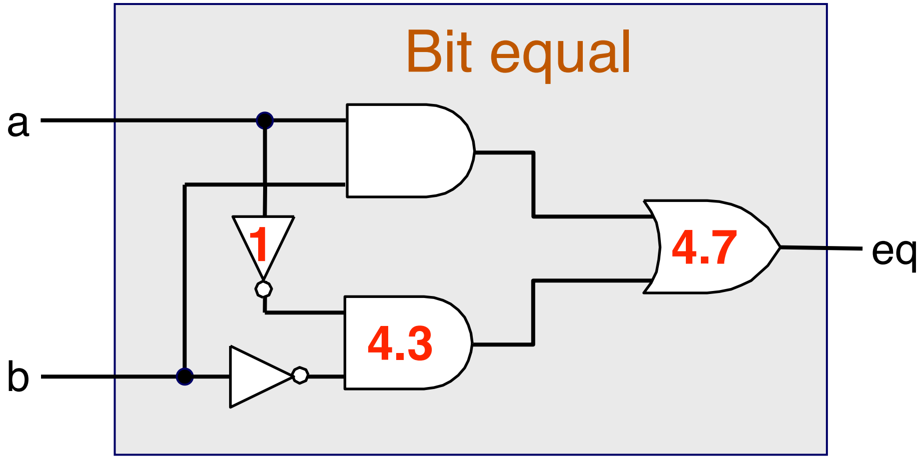

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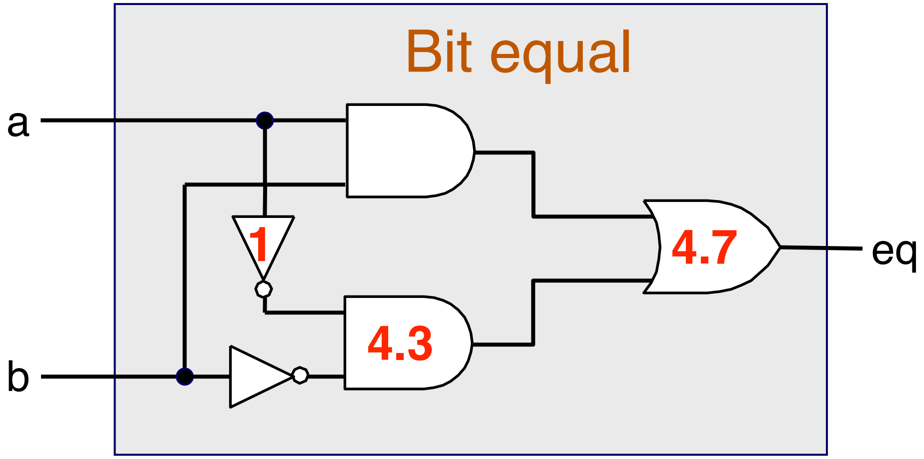

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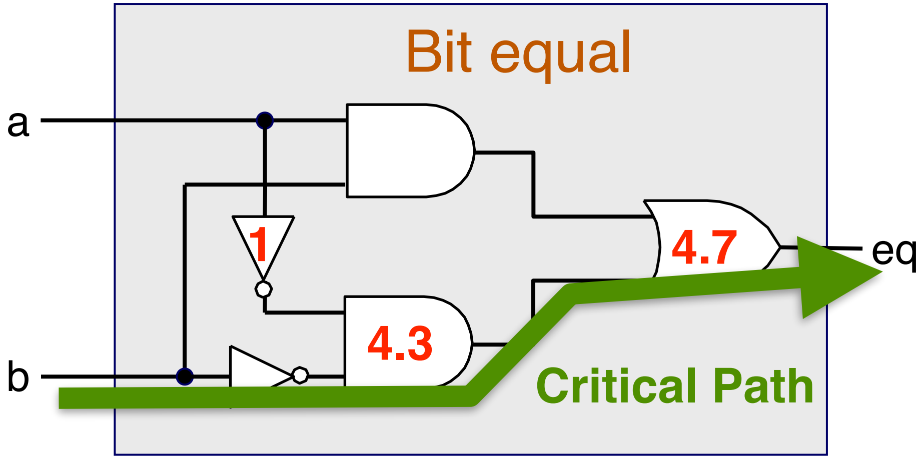

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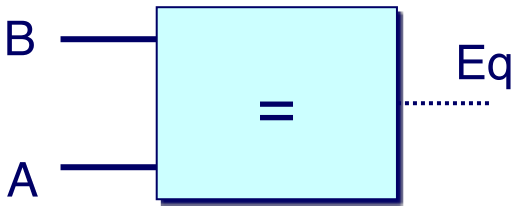
64-bit Equality



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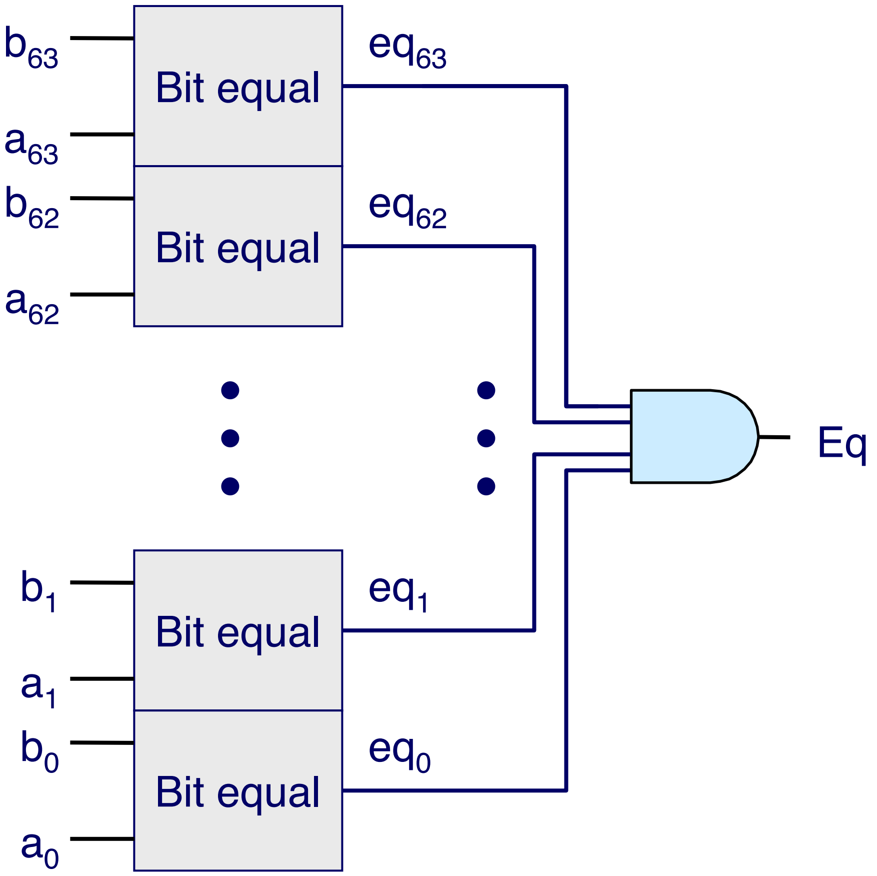
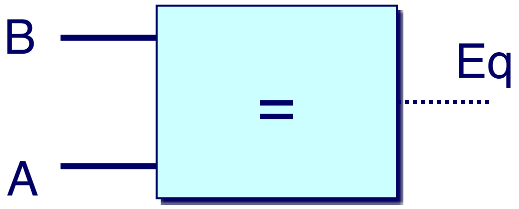
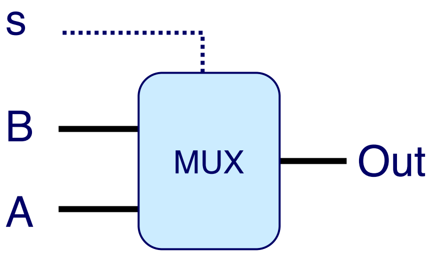




Bit-Level Multiplexor (MUX)

- Control signal s
- Data signals A and B
- Output A when s=1, B when s=0



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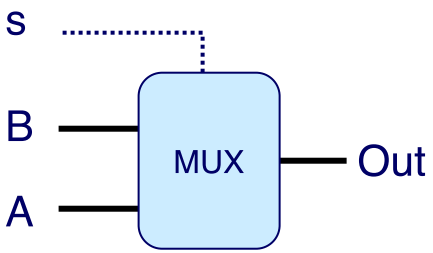

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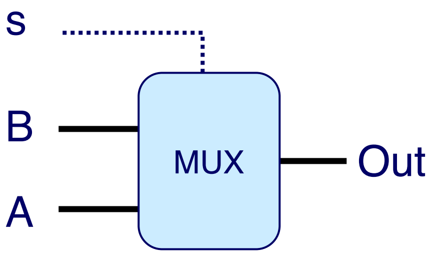

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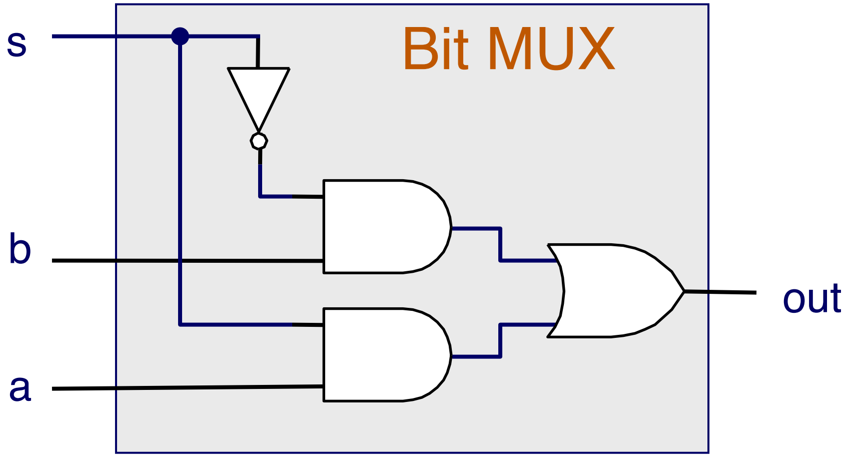

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- Control signal s; Data signals A, B, C, and D
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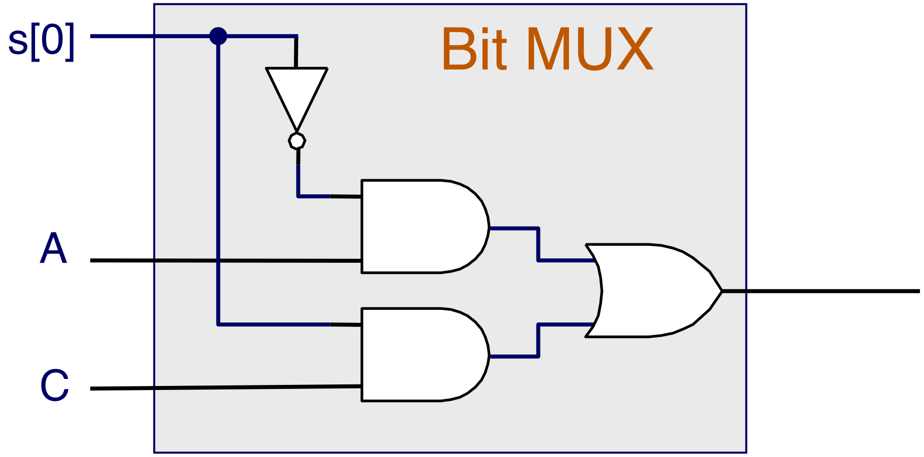

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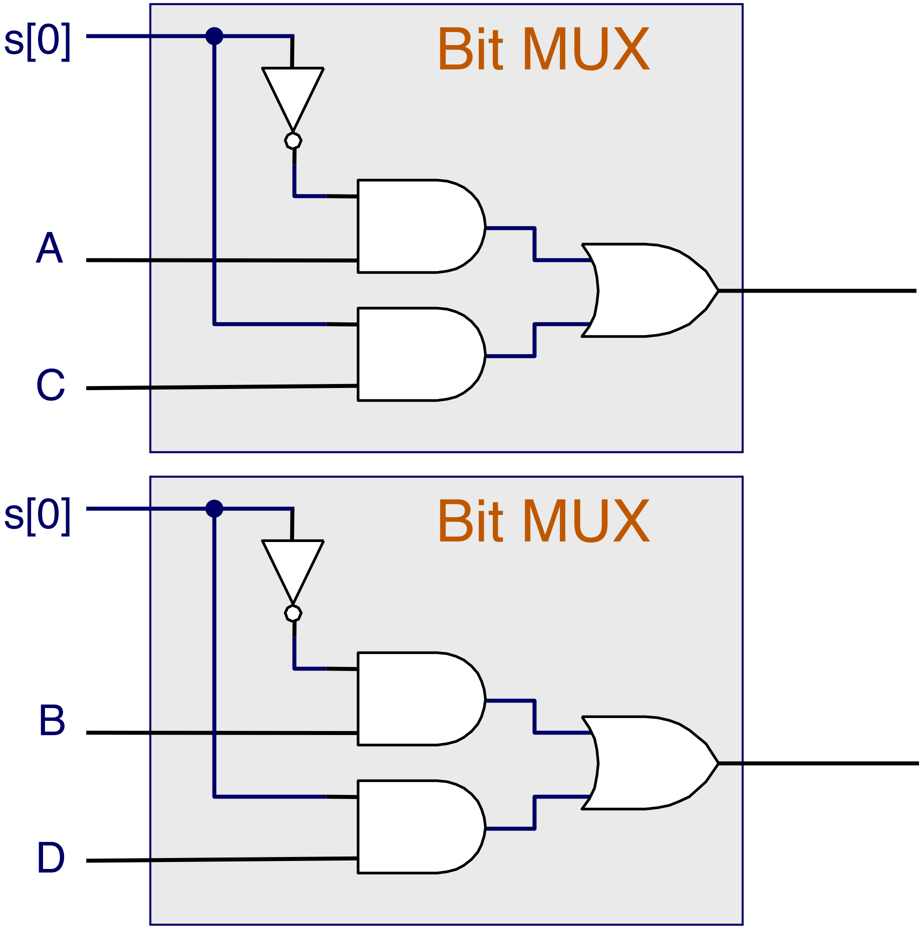

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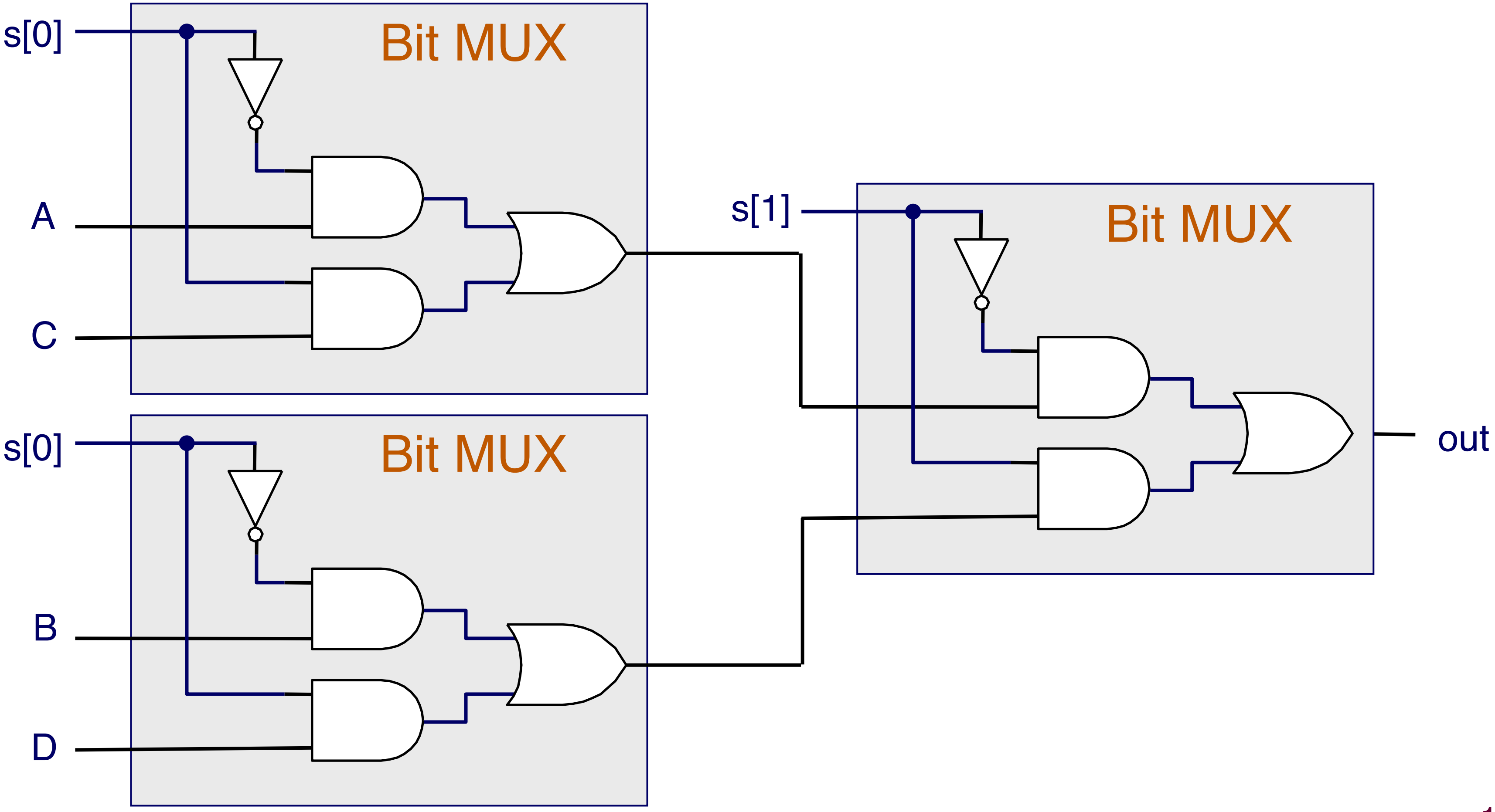

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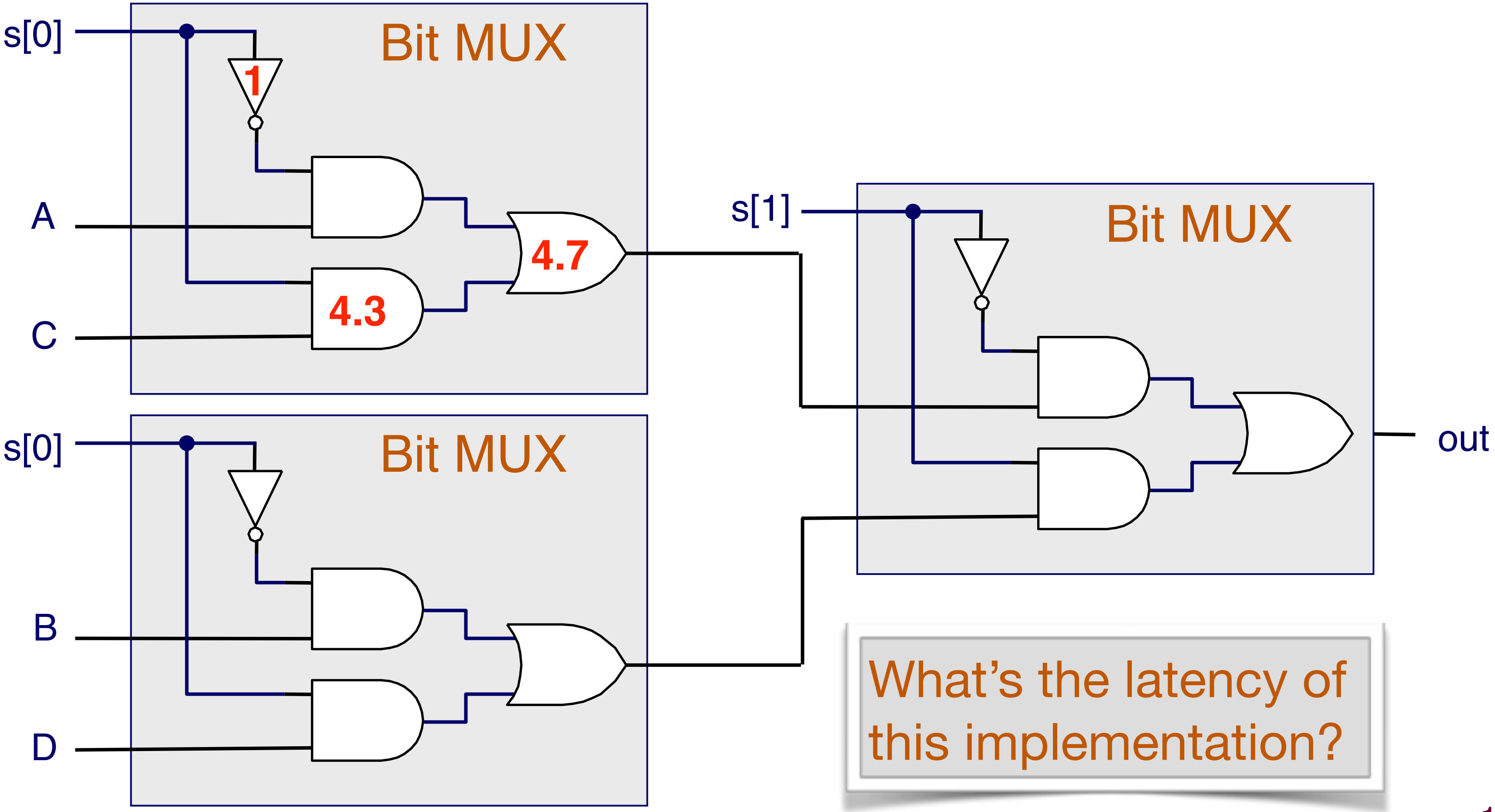

What's the latency of this implementation?

Logic Design and VLSI

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- Take a Logic Design or Very Large Scale Integrated-Circuit (VLSI) course if you want to know more about circuit design.
    - Logic design uses the gate-level abstractions
    - VLSI tells you how the gates are implemented at transistor-level

Full (1-bit) Adder

Add two bits and carry-in,
produce one-bit sum and carry-out.

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full (1-bit) Adder

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$$S = (\sim A \ \& \ \sim B \ \& \ C_{in})$$

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0	0	0	0	0
0	0	1	1	0
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1	1	0	0	1
1	1	1	1	1

Full (1-bit) Adder

Add two bits and carry-in,
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S = (~A & ~B & C_{in})
| (~A & B & ~C_{in})
| (A & ~B & ~C_{in})

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
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$$\begin{aligned} S = {} & (\sim A \;\&\; \sim B \;\&\; C_{in}) \\ & \mid (\sim A \;\&\; B \;\&\; \sim C_{in}) \\ & \mid (A \;\&\; \sim B \;\&\; \sim C_{in}) \\ & \mid (A \;\&\; B \;\&\; C_{in}) \end{aligned}$$

A	B	C_{in}	S	C_{out}
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0	1	0	1	0
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S = (~A & ~B & C_{in})
| (~A & B & ~C_{in})
| (A & ~B & ~C_{in})
| (A & B & C_{in})

C_{ou} = (~A & B & C_{in})
| (A & ~B & C_{in})
| (A & B & ~C_{in})
| (A & B & C_{in})

A	B	C_{in}	S	C_{ou}
				t
0	0	0	0	0
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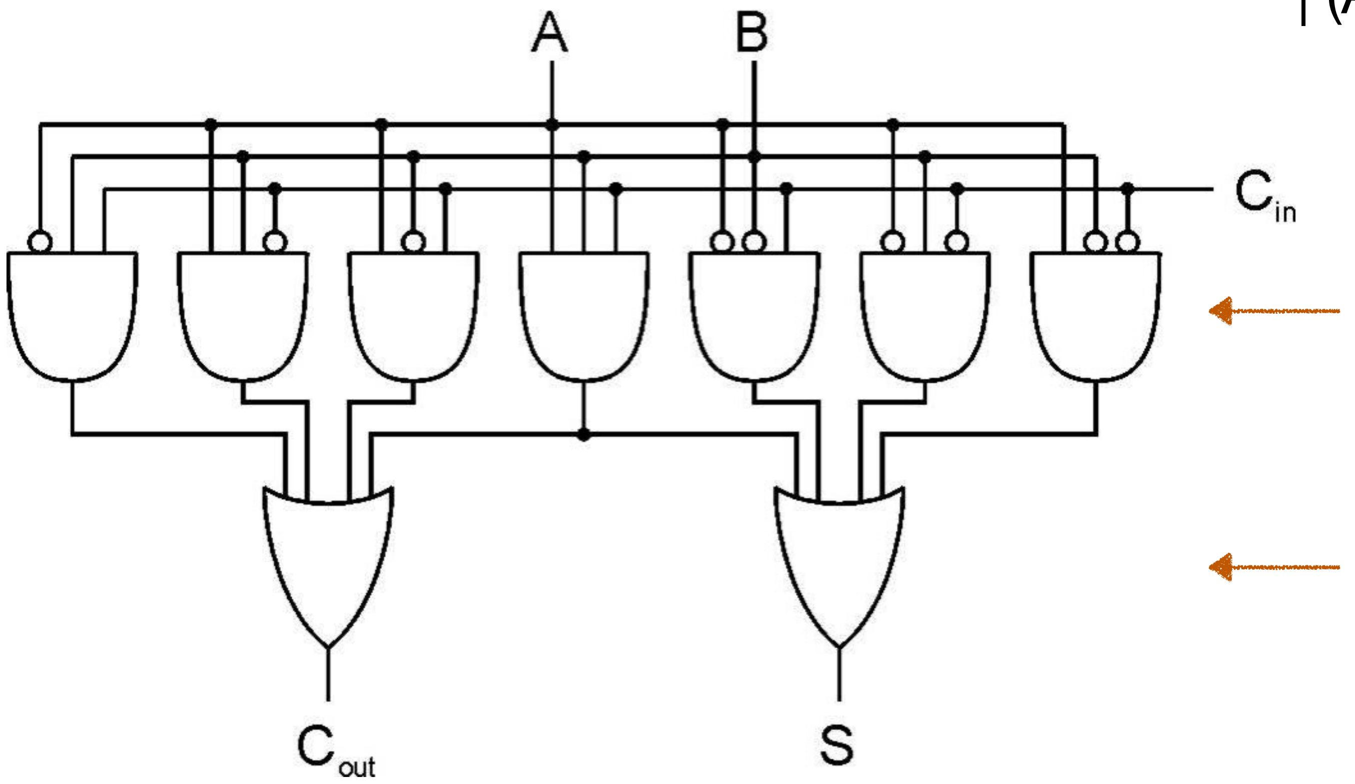

AND Gates

OR Gates

1-bit Full Adder

$C_{ou} = \boxed{(\sim A \;\&\; B \;\&\; C_{in})}$

$|\ (A \;\&\; \sim B \;\&\; C_{in})$

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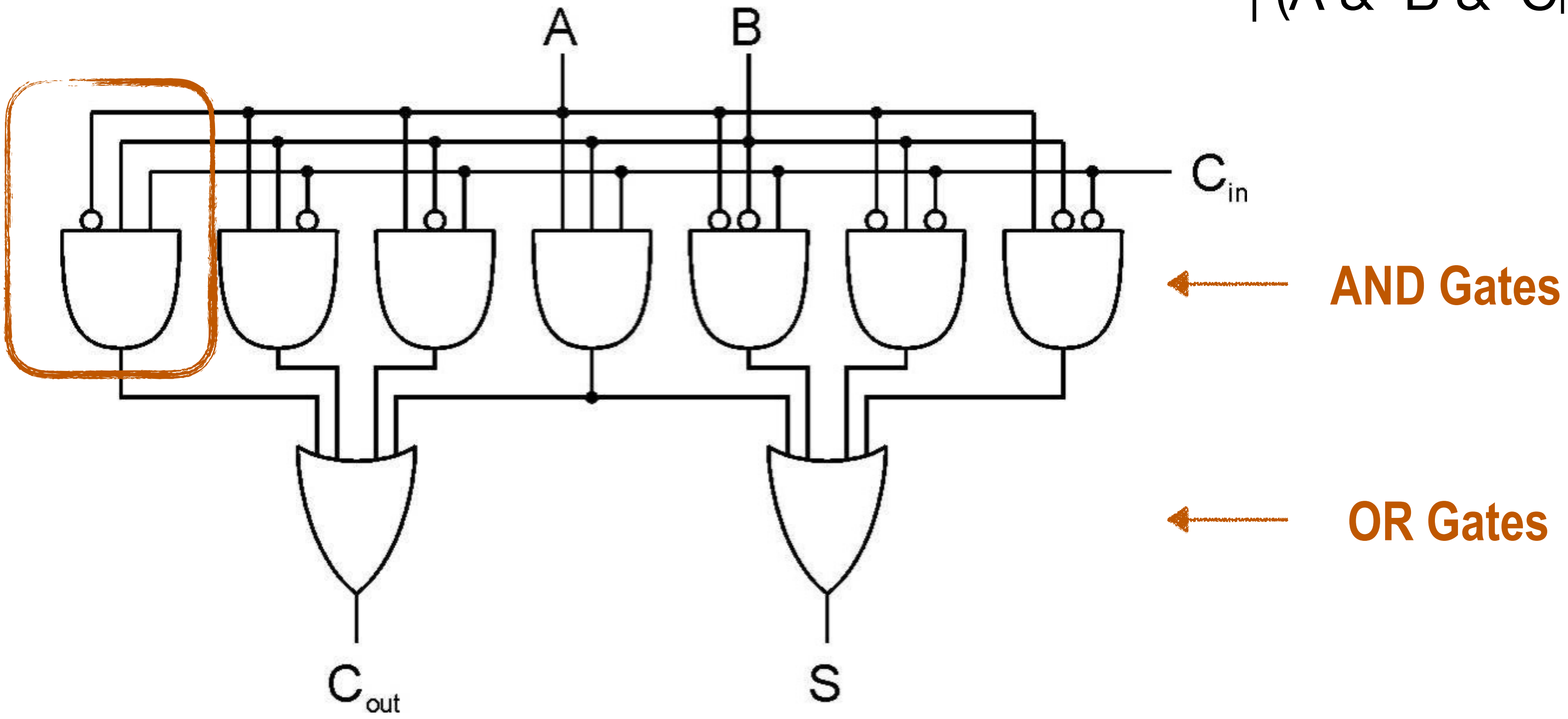
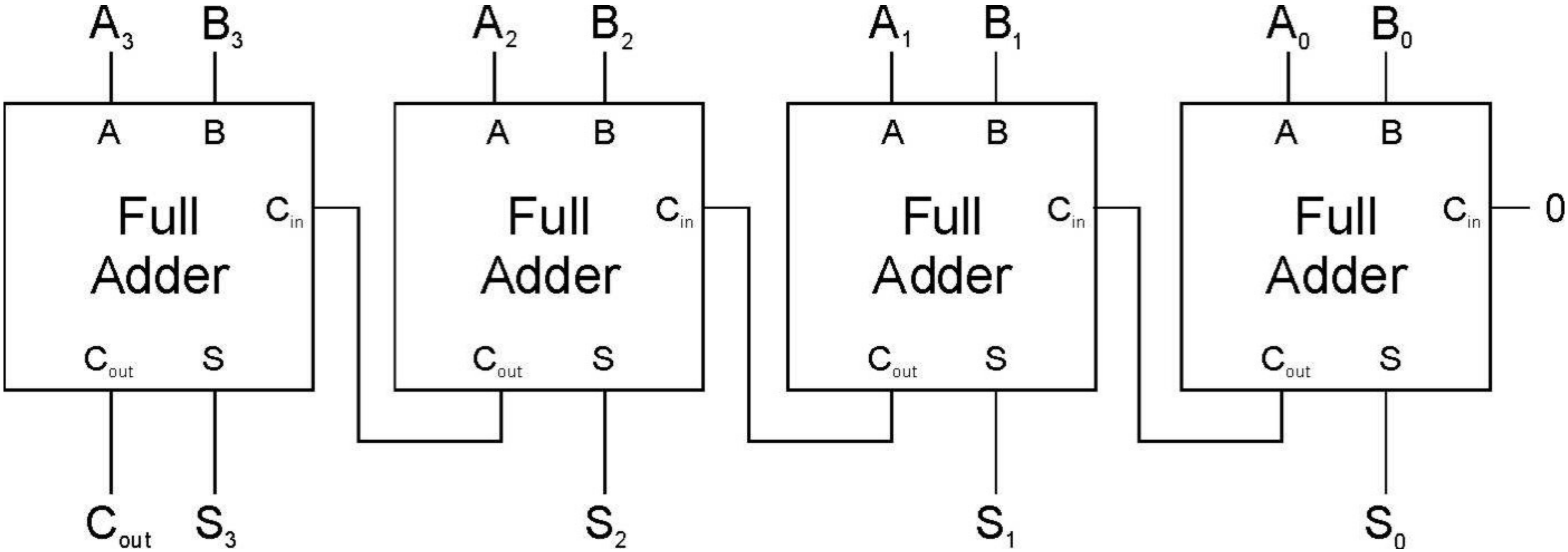
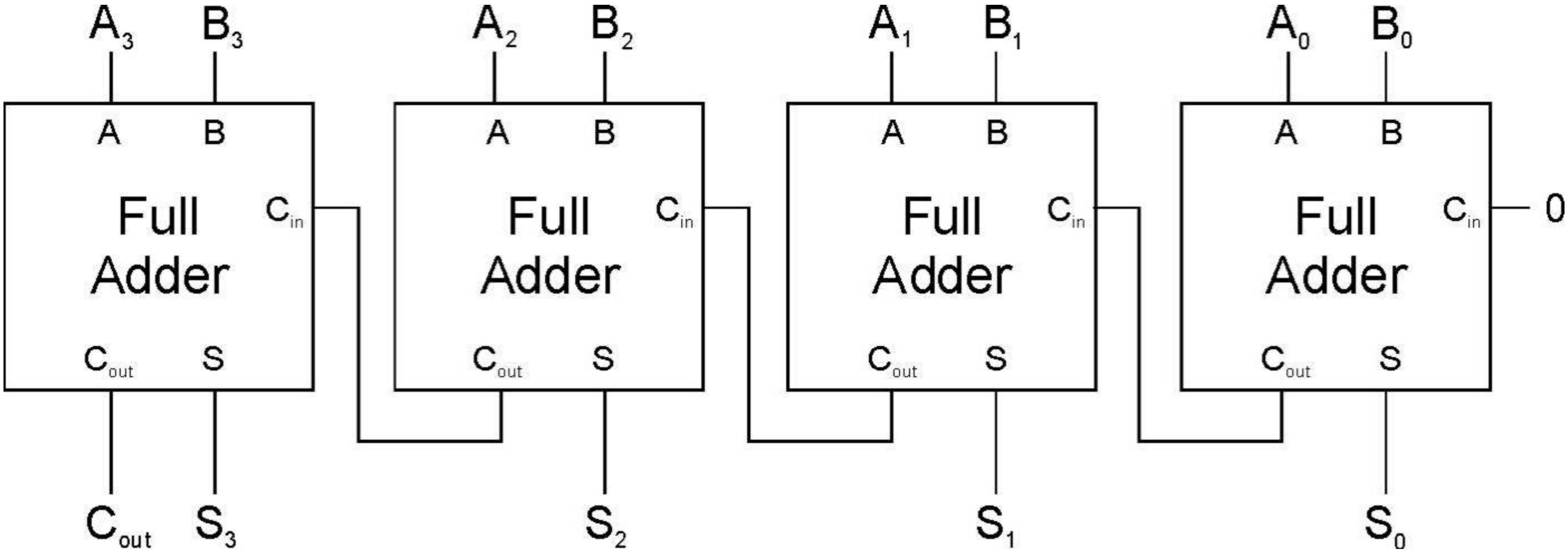


Four-bit Adder



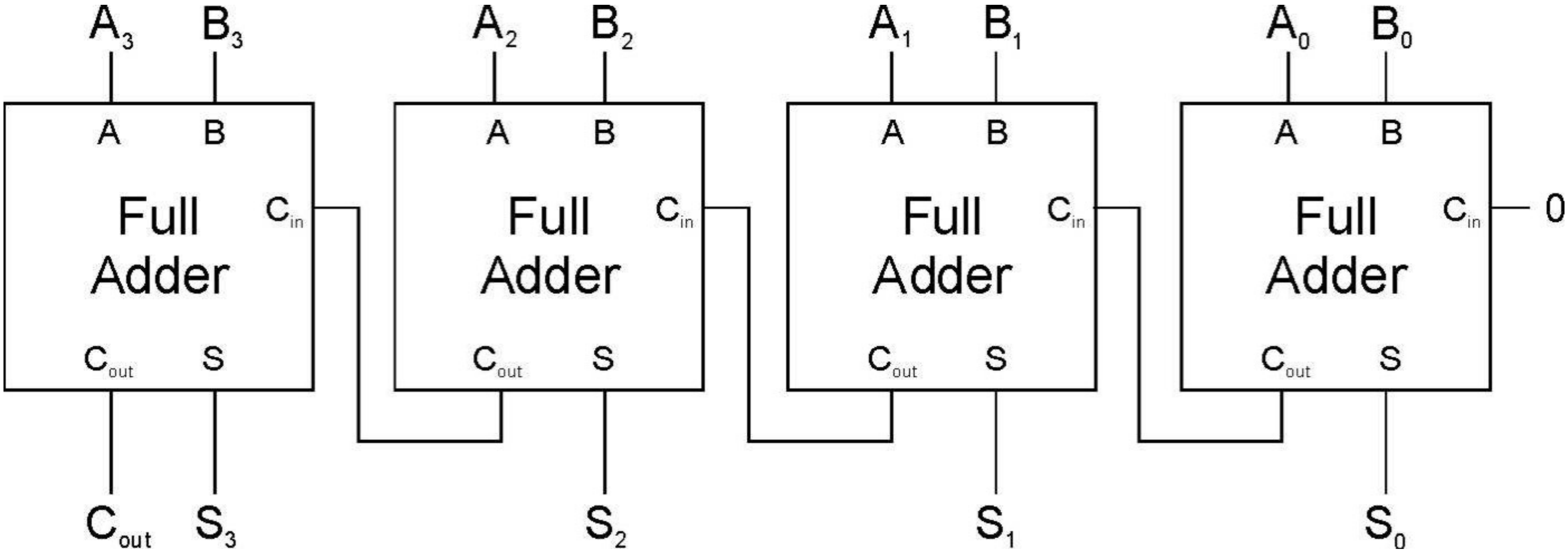
Four-bit Adder

- Ripple-carry Adder
  - Simple, but performance linear to bit width

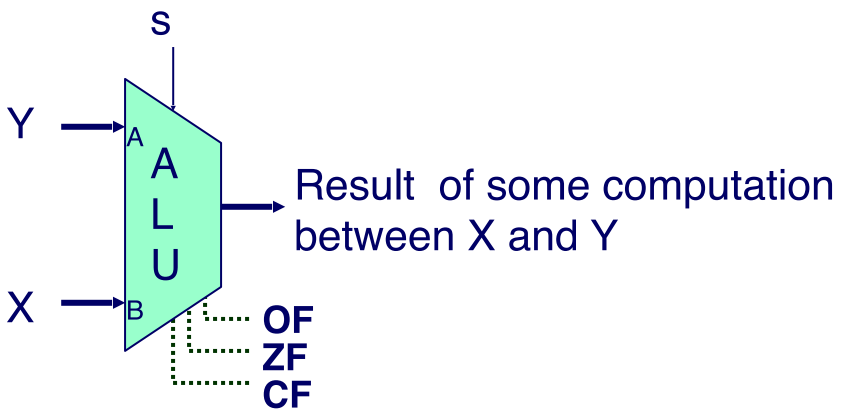


Four-bit Adder

- Ripple-carry Adder
  - Simple, but performance linear to bit width
- Carry look-ahead adder (CLA)
  - Generate all carriers simultaneously



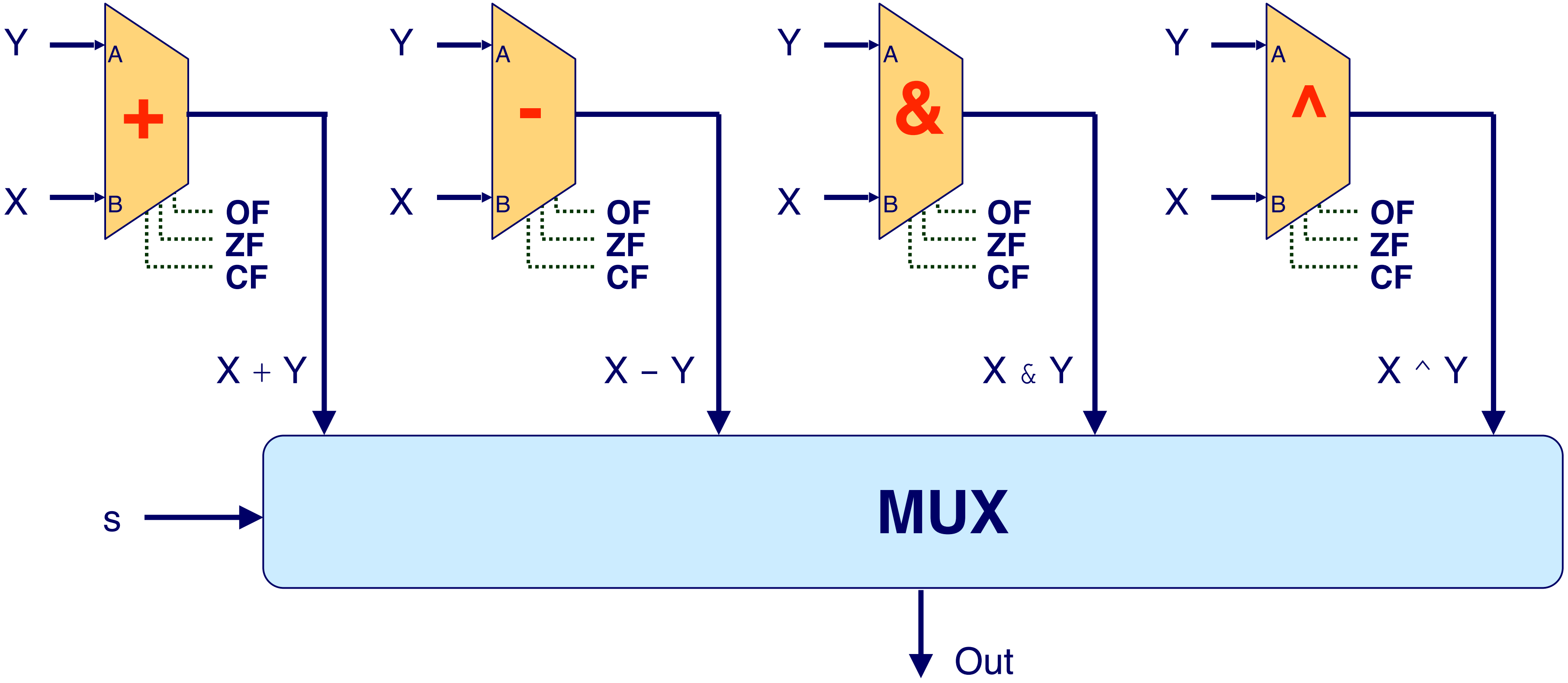
Arithmetic Logic Unit



- An ALU performs multiple kinds of computations.
- The actual computation depends on the selection signal s.
- Also sets the condition codes (status flags)
- For instance:
    - X + Y when s == 00
    - X - Y when s == 01
    - X & Y when s == 10
    - X ^ Y when s == 11
- How can this ALU be implemented?

Arithmetic Logic Unit

- Implement 4 different circuits, one for each operation.
- Then use a MUX to select the results



Today: Circuits Basics

- Transistors
- Circuits for computations
- Circuits for storing data

The Need for Storing Bits

- Assembly programs set architecture (processor) states.
  - Register File
  - Status Flags
  - Memory
  - Program Counter

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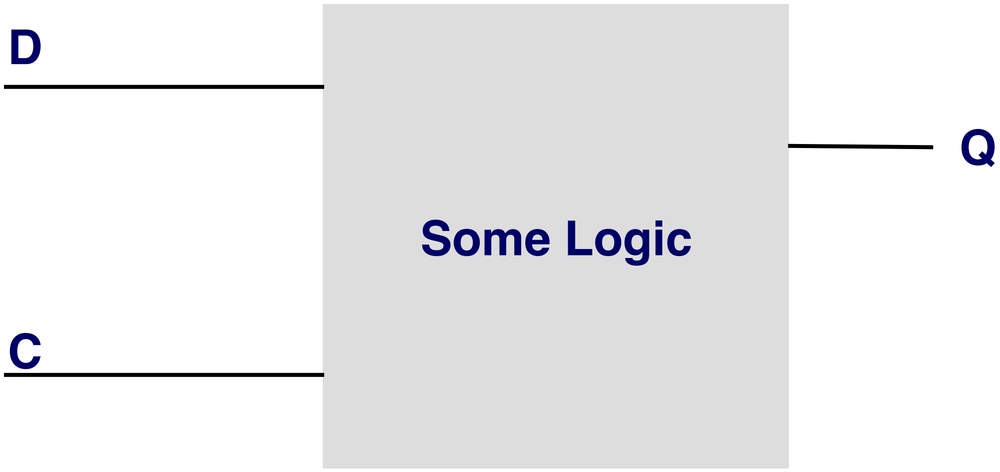
- Every state is essentially some bits that are stored/loaded.
- Think of the program execution as an FSM.
- The hardware must provide mechanisms to load and store bits.
- There are many different ways to store bits. They have trade-offs.

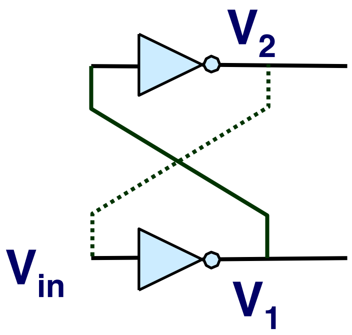
Build a 1-Bit Storage



- What I would like:
  - D is the data I want to store (0 or 1)
  - C is the control signal
    - When C is 1, Q becomes D (i.e., storing the data)
    - When C is 0, Q doesn't change with D (data stored)

Bitstable Element

$V_{in} = V_2$



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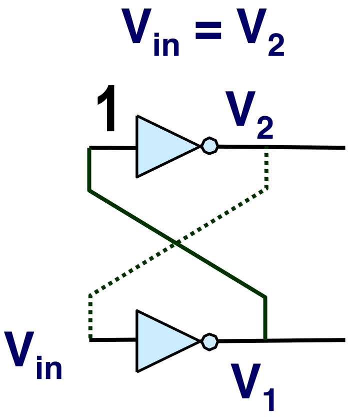

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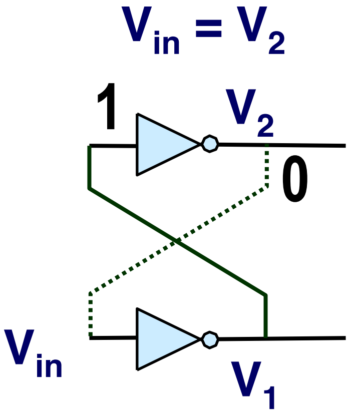

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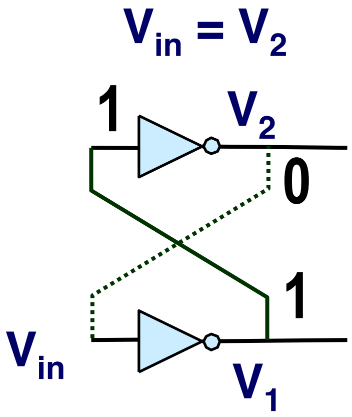
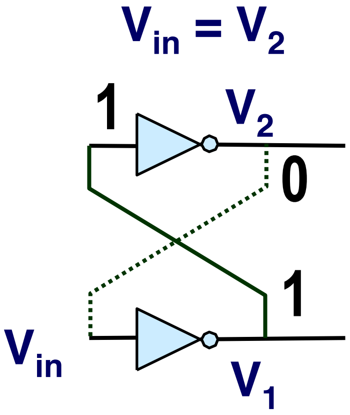
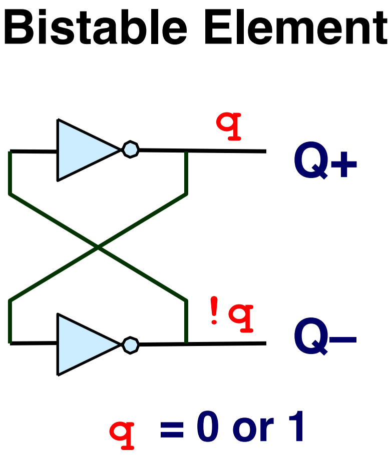
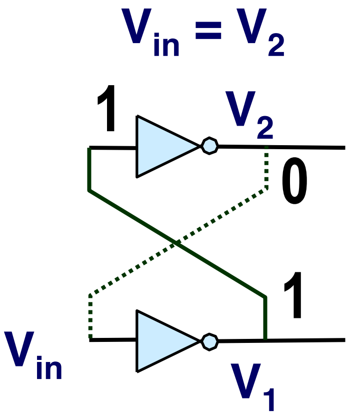


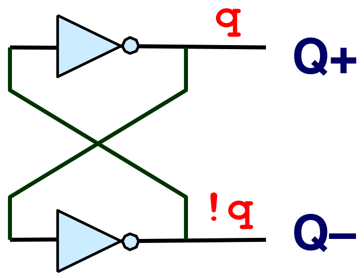
Bitstable Element





Bitstable Element



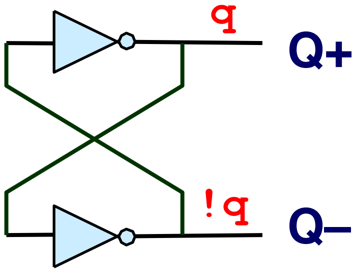


q = 0 or 1

Q+ ***continuously*** outputs q.

Storing and Accessing 1 Bit

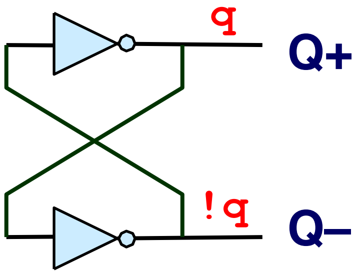
Bistable Element



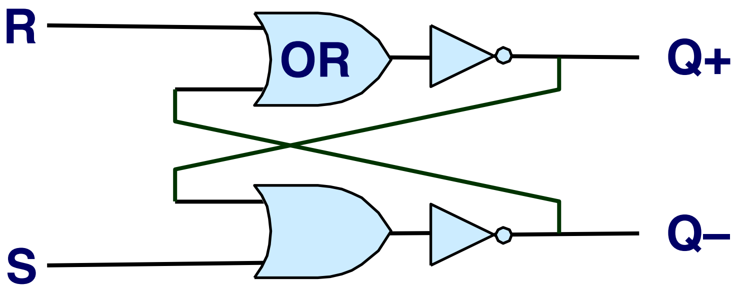
q = 0 or 1

Storing and Accessing 1 Bit

Bistable Element

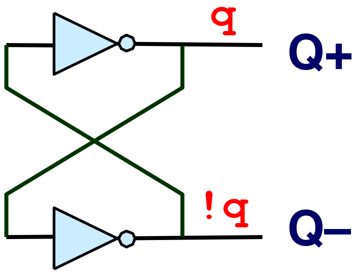


q = 0 or 1

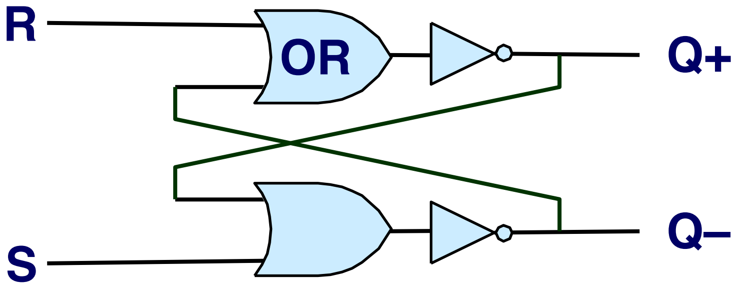


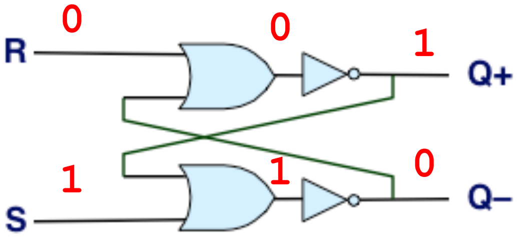
Storing and Accessing 1 Bit

Bistable Element



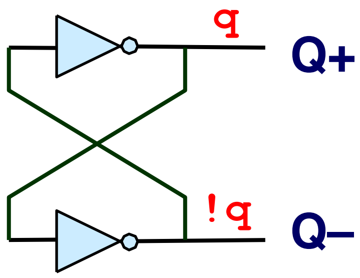
q = 0 or 1



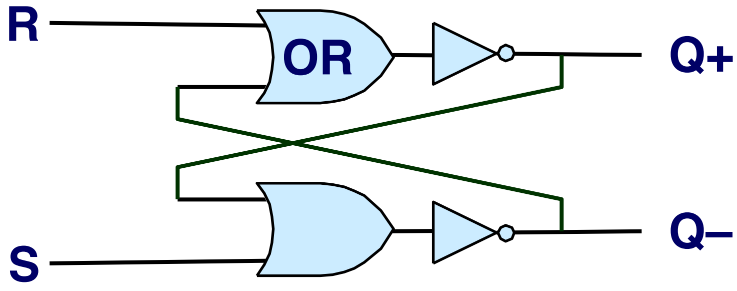


Storing and Accessing 1 Bit

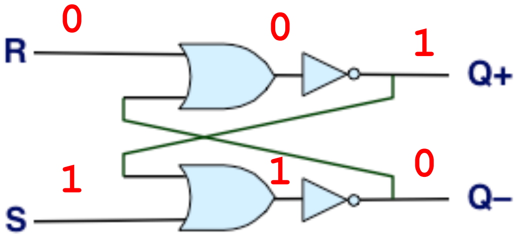
Bistable Element



q = 0 or 1

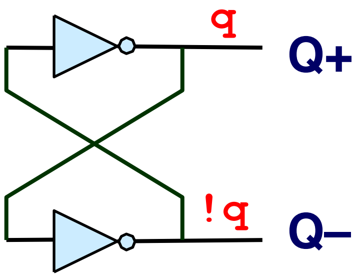


Setting Q+ to 1

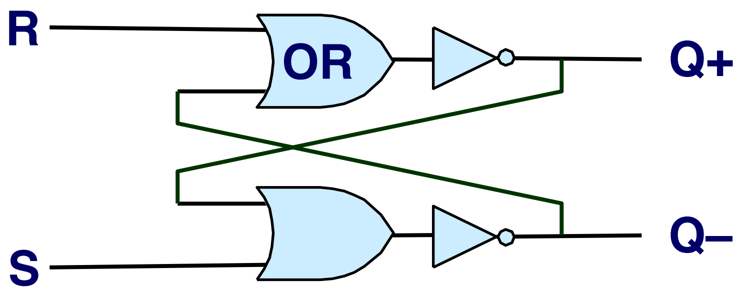


Storing and Accessing 1 Bit

Bistable Element



q = 0 or 1



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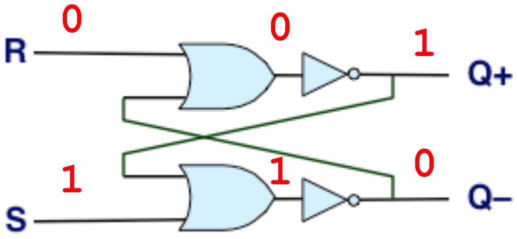
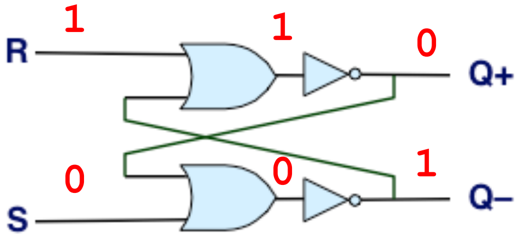
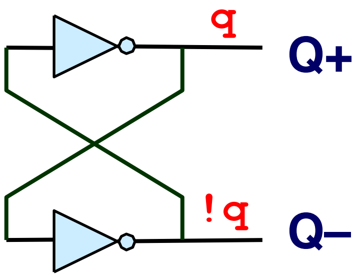


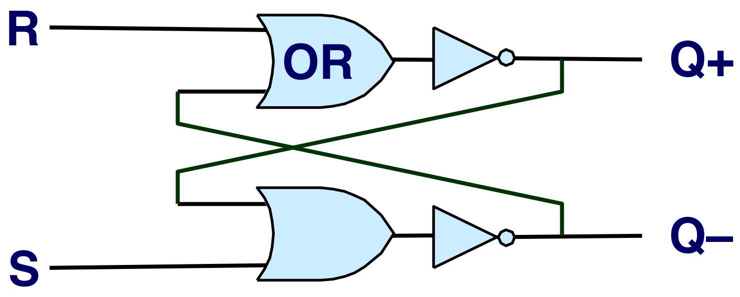


Storing and Accessing 1 Bit

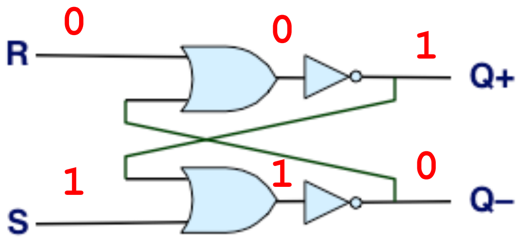
Bistable Element



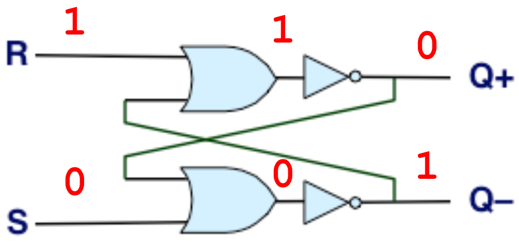
q = 0 or 1



Setting Q+ to 1

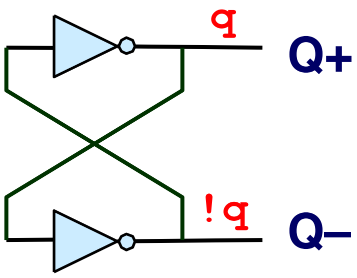


Setting Q+ to 0

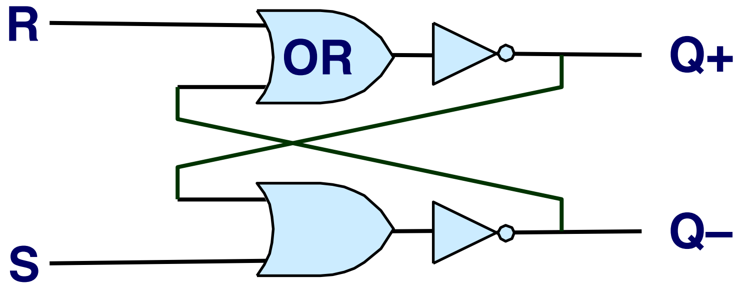


Storing and Accessing 1 Bit

Bistable Element



q = 0 or 1



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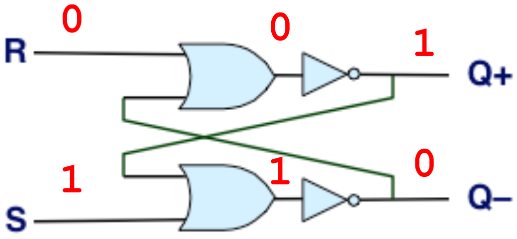
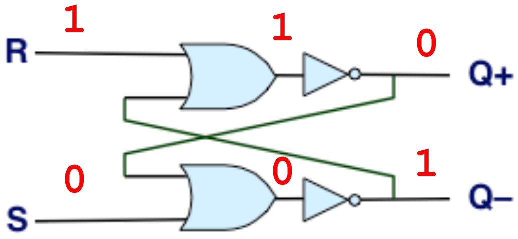
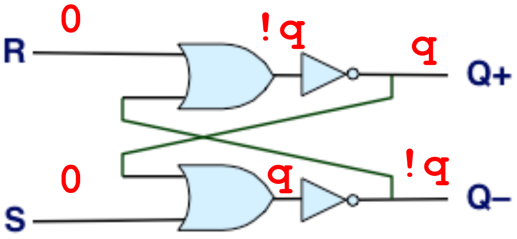


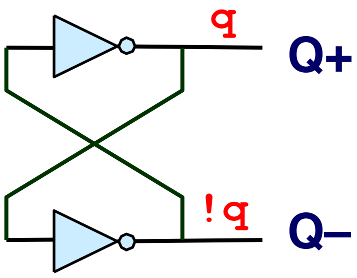
Setting Q+ to 0



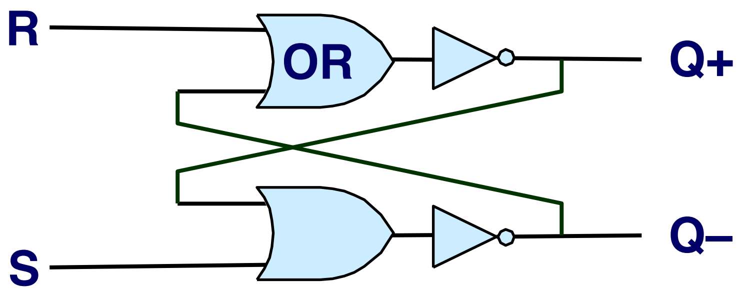


Storing and Accessing 1 Bit

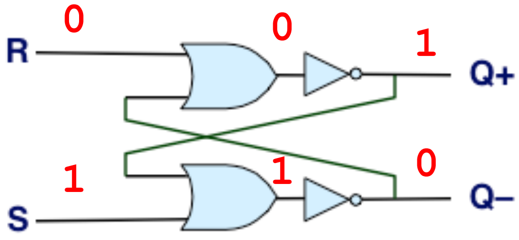
Bistable Element



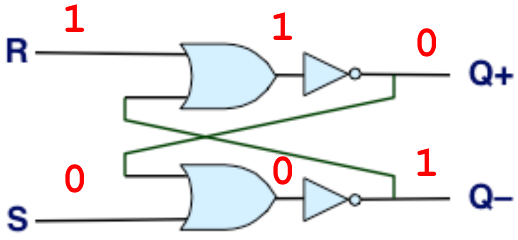
q = 0 or 1



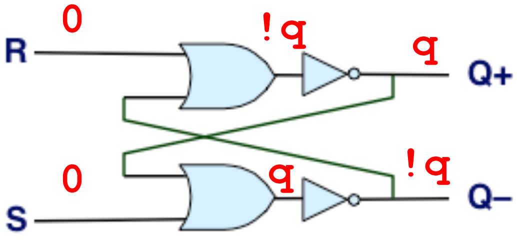
Setting Q+ to 1



Setting Q+ to 0

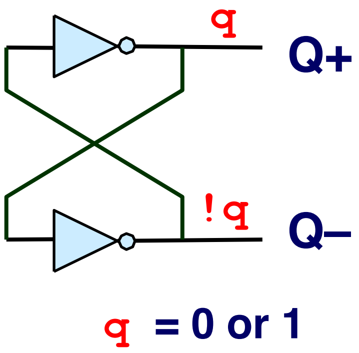


Q+ value unchanged i.e., stored!

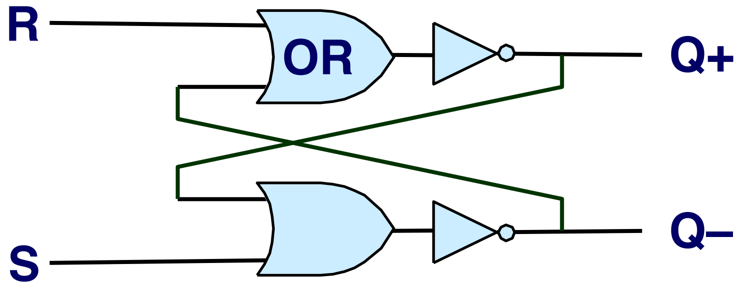


Storing and Accessing 1 Bit

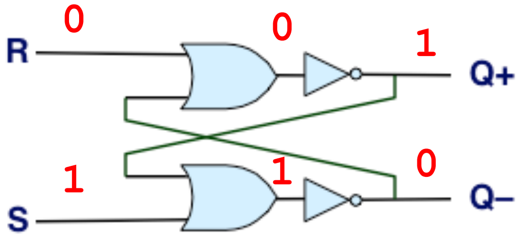
Bistable Element



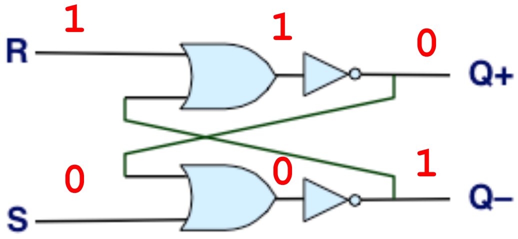
R-S Latch



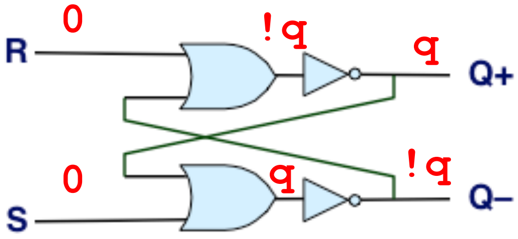
Setting Q+ to 1



Setting Q+ to 0

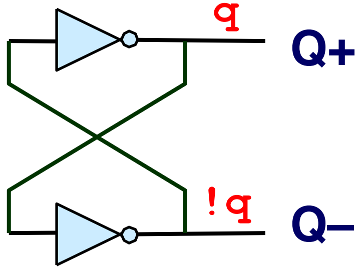


Q+ value unchanged i.e., stored!



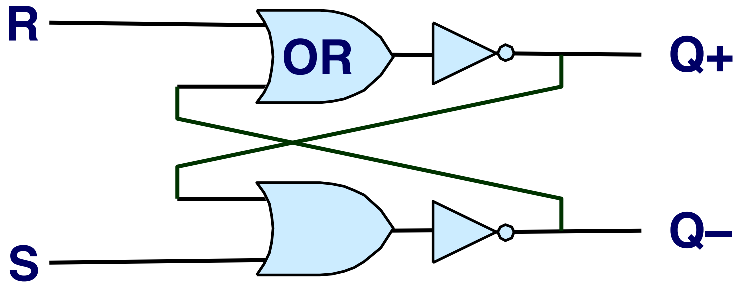
Storing and Accessing 1 Bit

Bistable Element

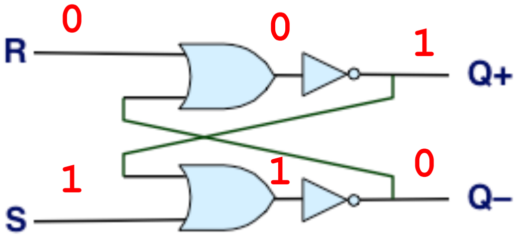


q = 0 or 1

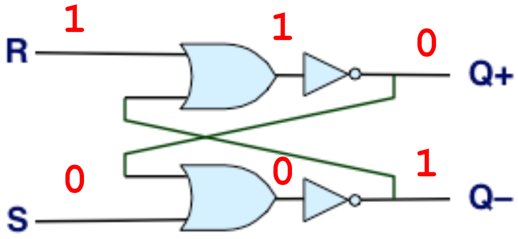
R-S Latch



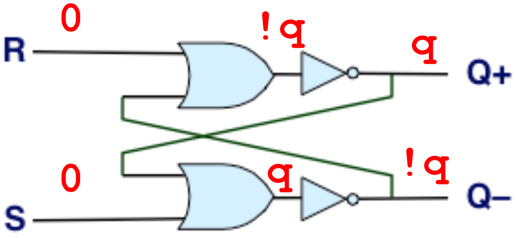
Setting Q+ to 1



Setting Q+ to 0

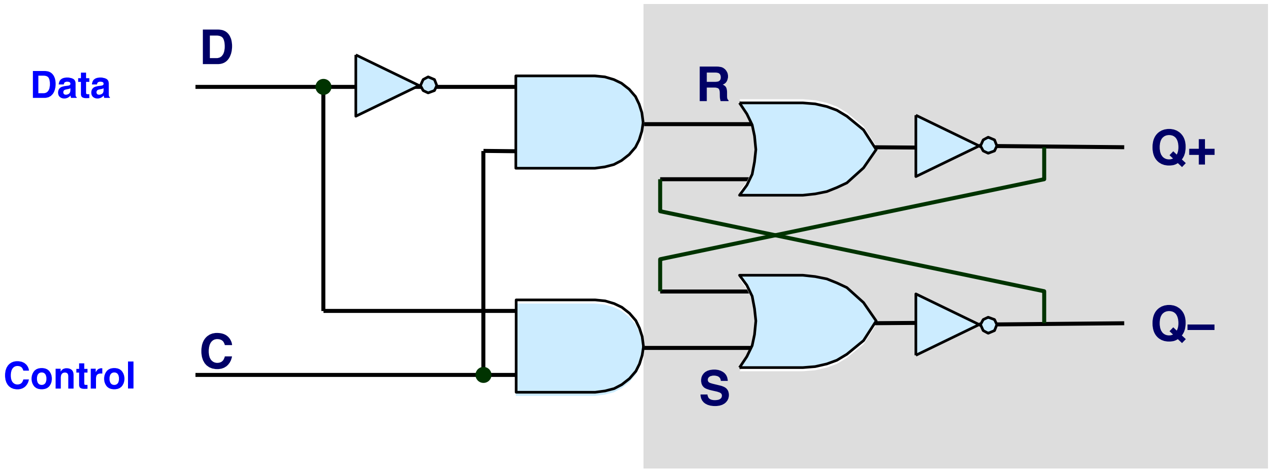


Q+ value unchanged i.e., stored!



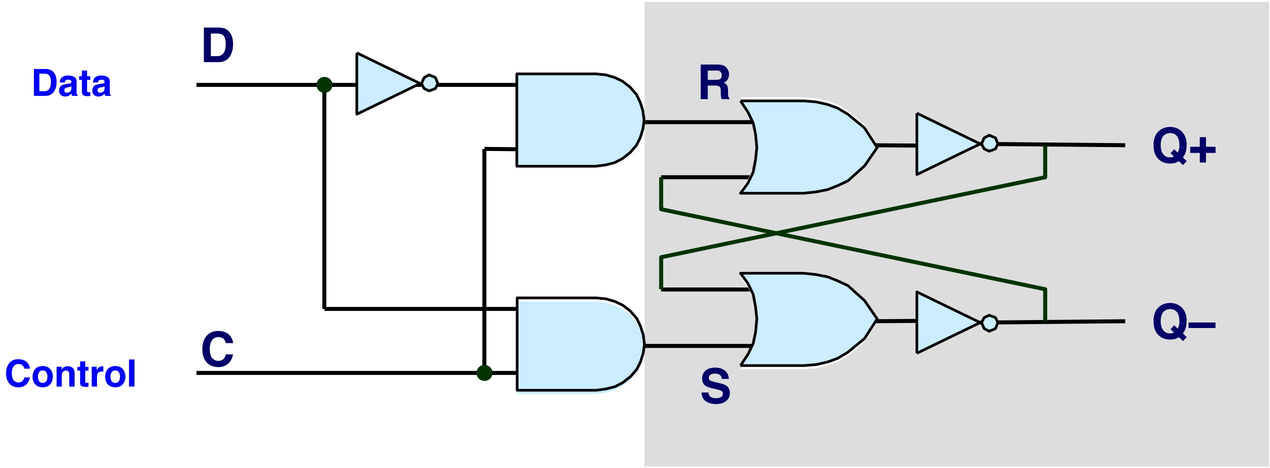
If R and S are different, Q+ is the same as S

A Better Way of Storing/Accessing 1 Bit

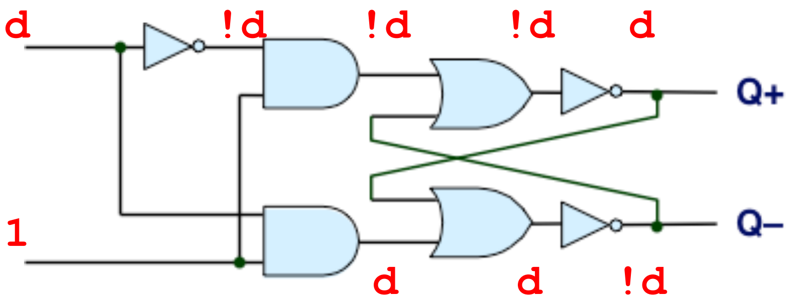


If R and S are different, Q+ is the same as S

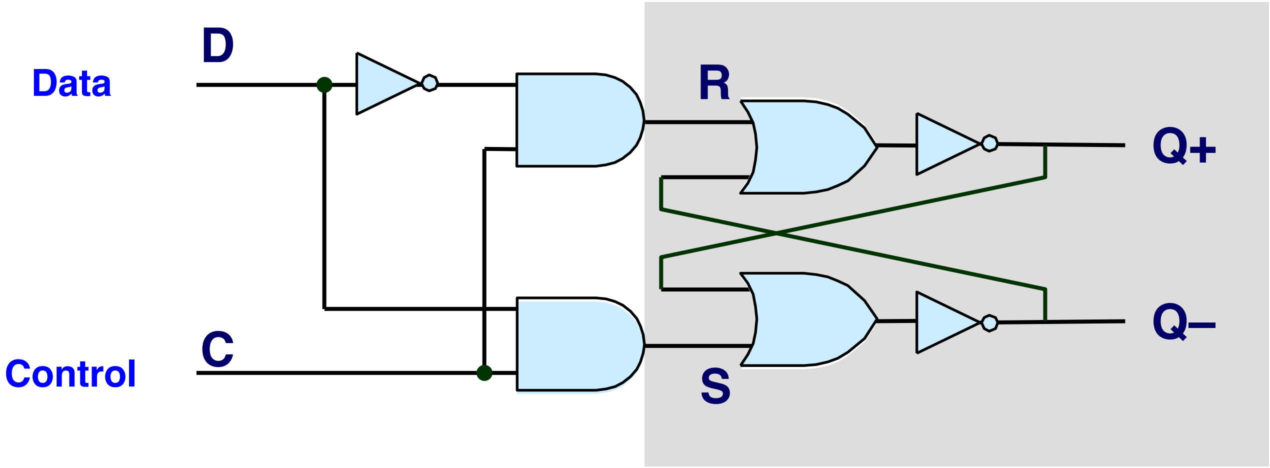
A Better Way of Storing/Accessing 1 Bit



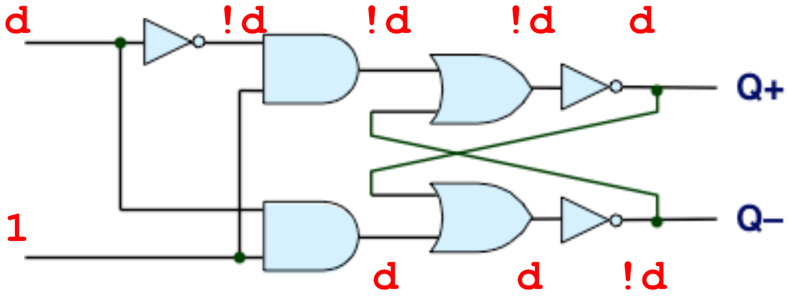
If R and S are different, Q+ is the same as S



A Better Way of Storing/Accessing 1 Bit

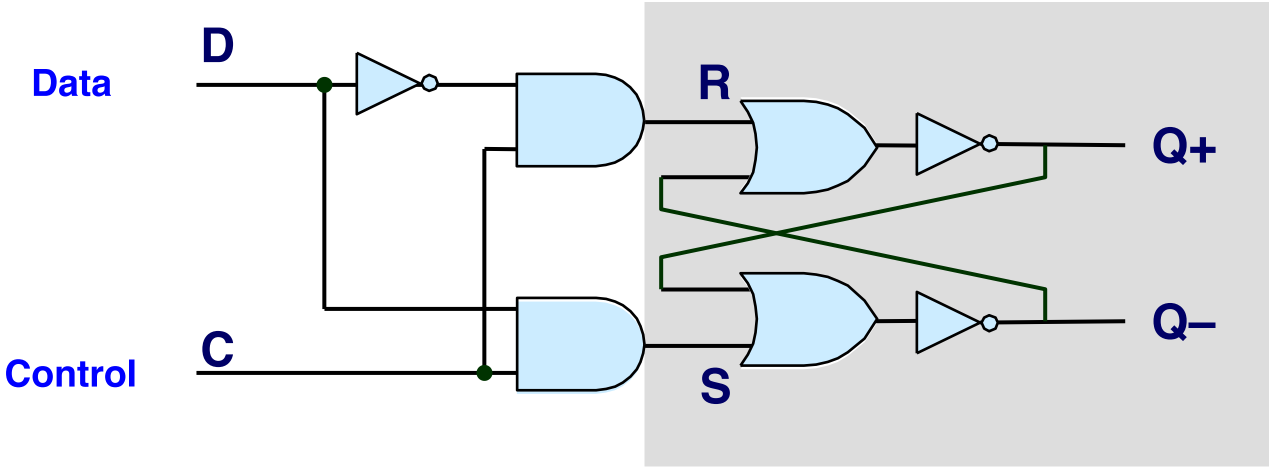


If R and S are different, Q+ is the same as S



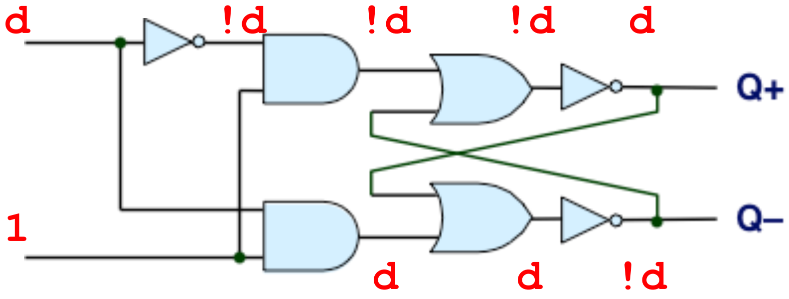
Q+ will continuously change as d changes

A Better Way of Storing/Accessing 1 Bit



If R and S are different, Q+ is the same as S

Storing Data (Latching)



Q+ will continuously
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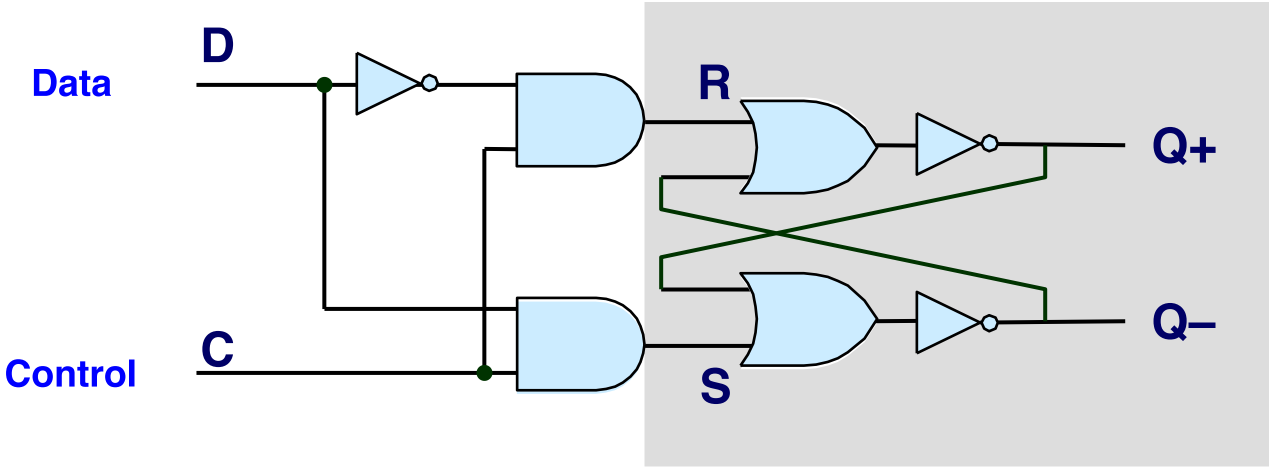
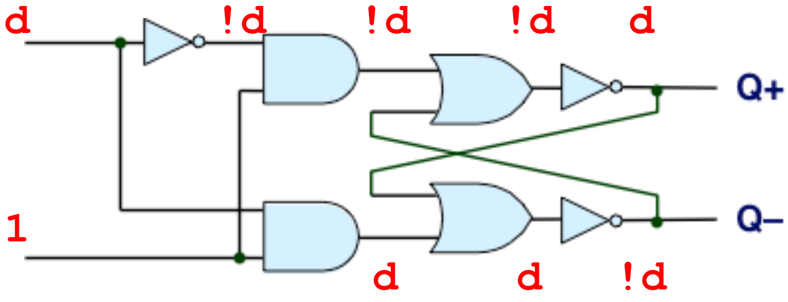
A Better Way of Storing/Accessing 1 Bit

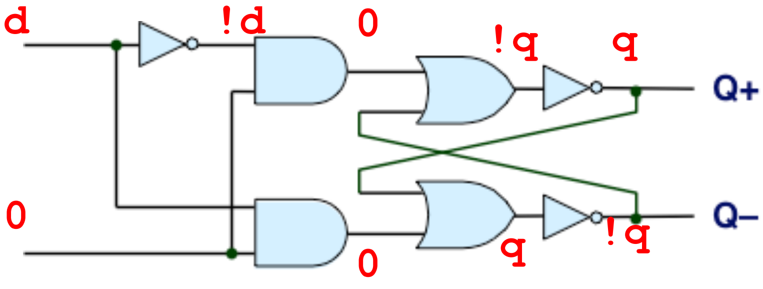


If R and S are different, Q+ is the same as S

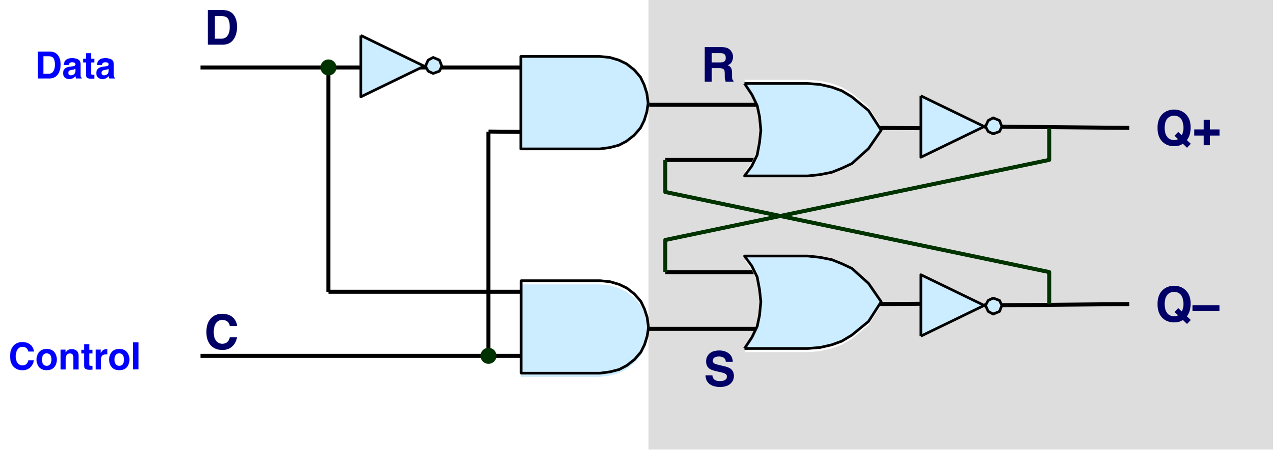
Storing Data (Latching)



Q+ will continuously change as d changes

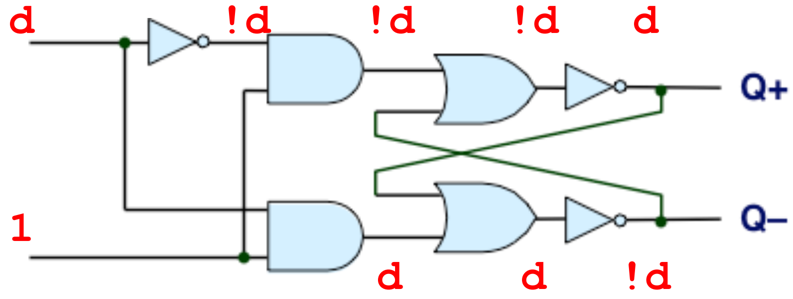


A Better Way of Storing/Accessing 1 Bit

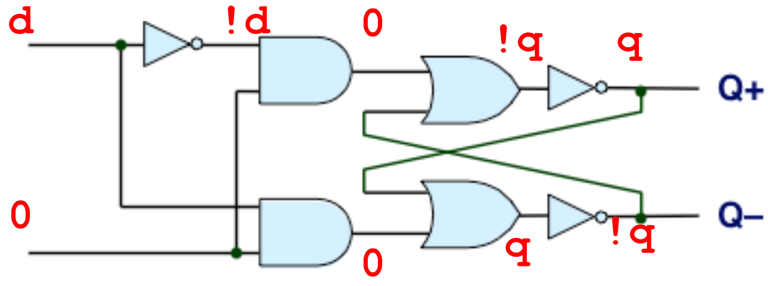


If R and S are different, Q+ is the same as S

Storing Data (Latching)

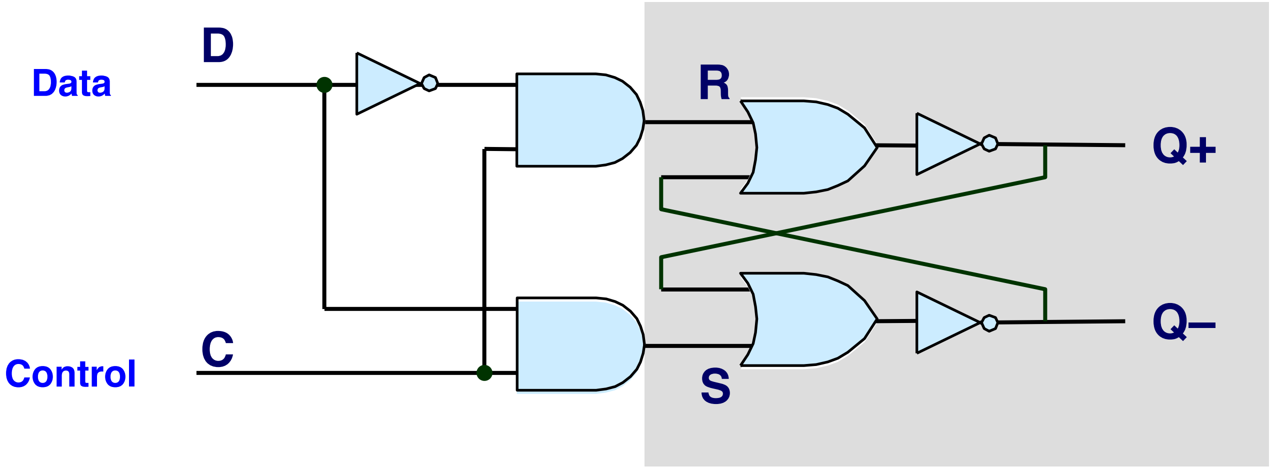


Q+ will continuously
change as d changes



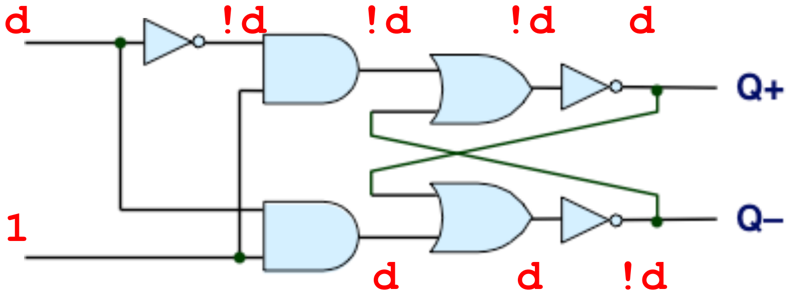
Q+ doesn’t change with d

A Better Way of Storing/Accessing 1 Bit



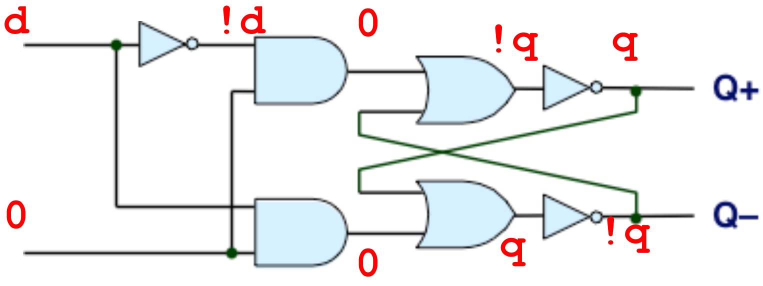
If R and S are different, Q+ is the same as S

Storing Data (Latching)



Q+ will continuously
change as d changes

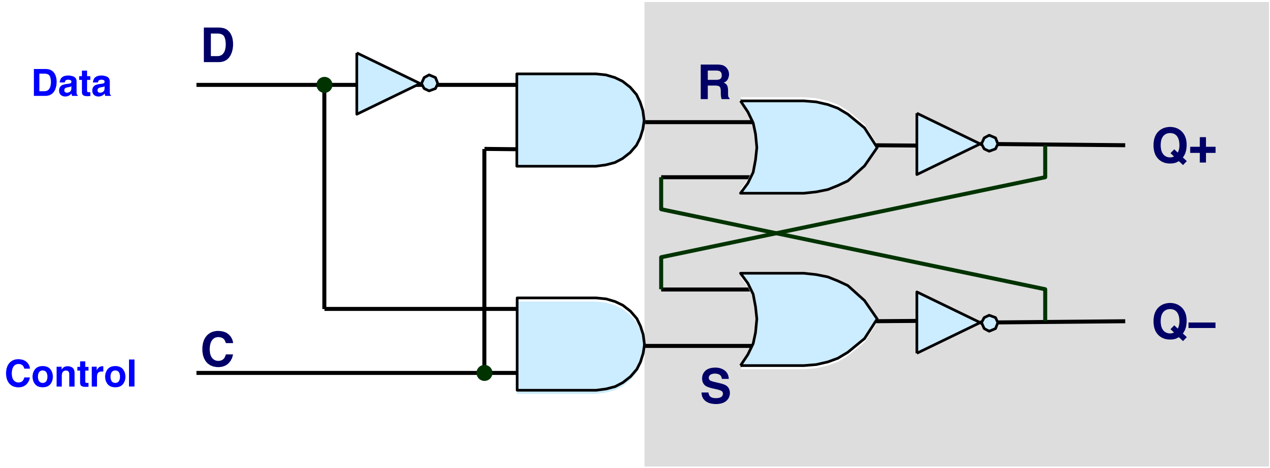
Holding Data



Q+ doesn't change with d

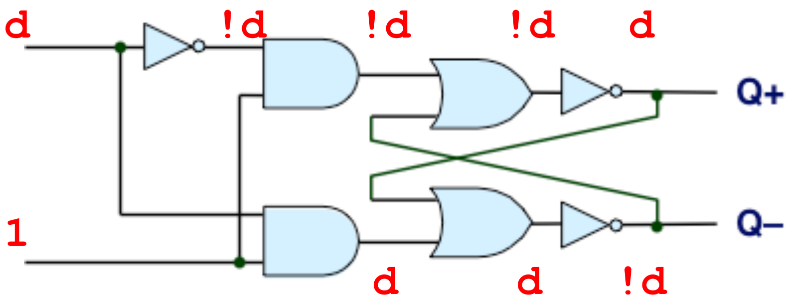
A Better Way of Storing/Accessing 1 Bit

D Latch



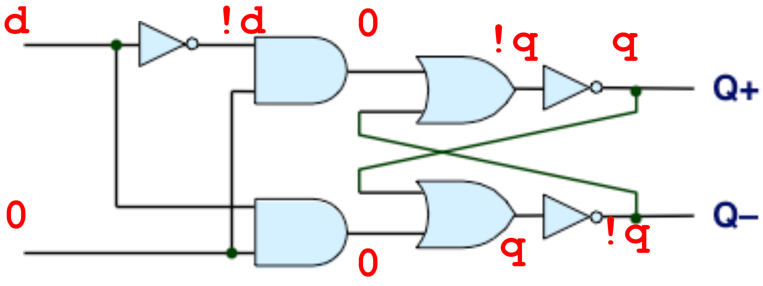
If R and S are different, Q+ is the same as S

Storing Data (Latching)



Q+ will continuously change as d changes

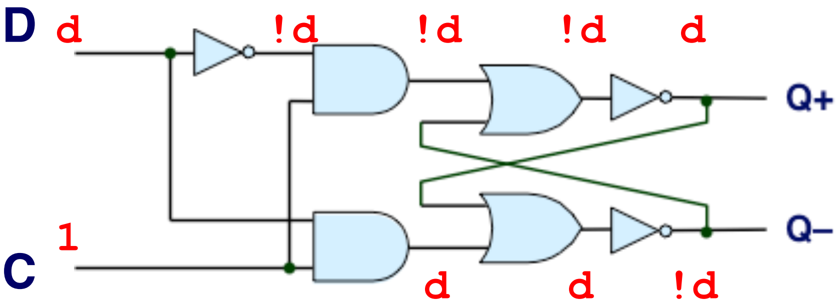
Holding Data



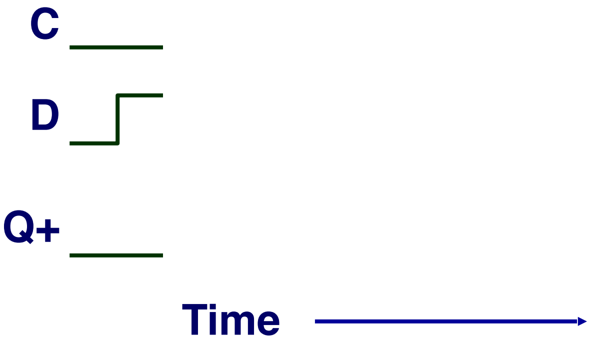
Q+ doesn't change with d

D-Latch is “Transparent”

Latching

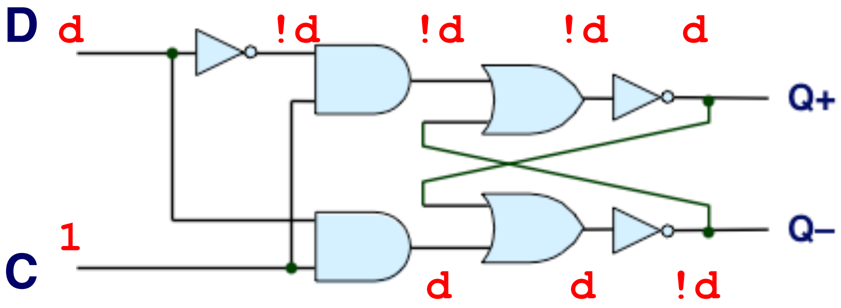


Changing D

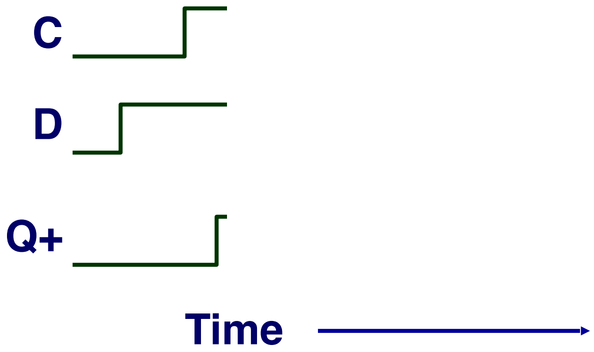


D-Latch is “Transparent”

Latching

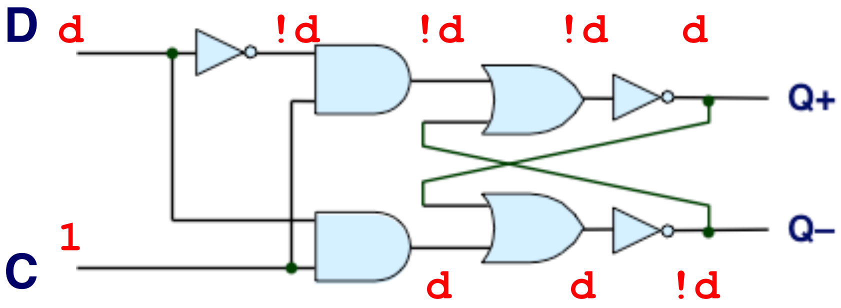


Changing D

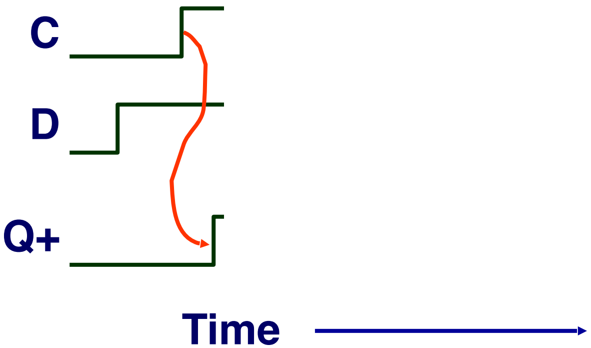


D-Latch is "Transparent"

Latching

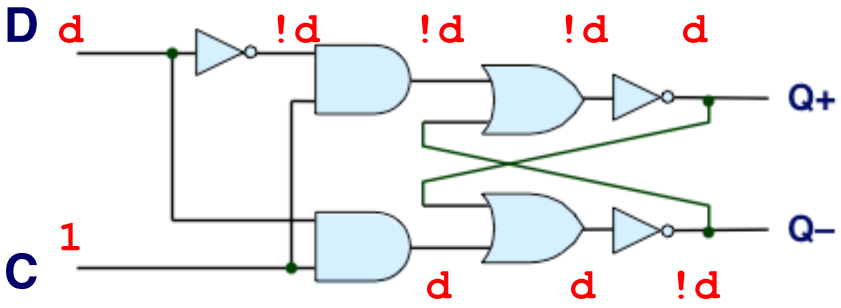


Changing D

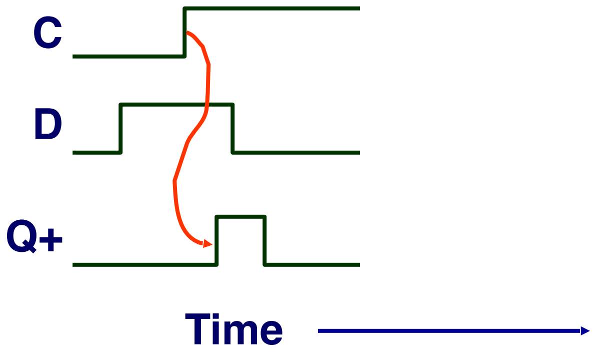


D-Latch is "Transparent"

Latching

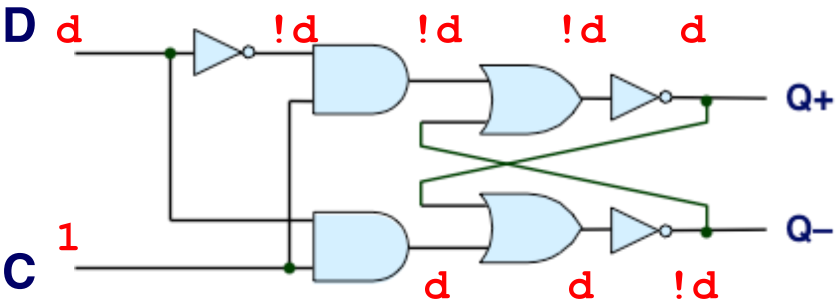


Changing D

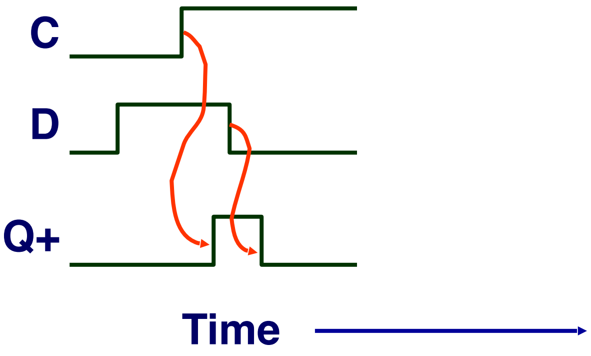


D-Latch is “Transparent”

Latching

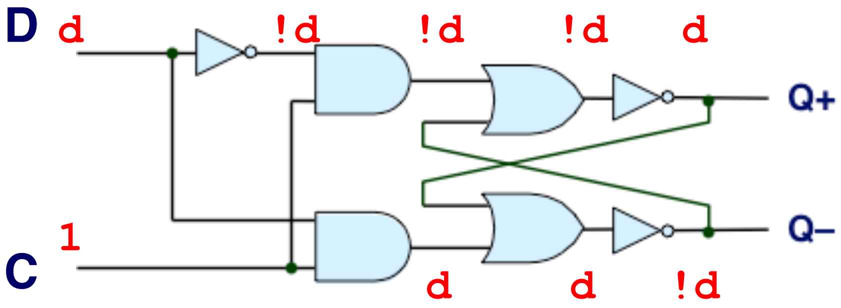


Changing D



D-Latch is “Transparent”

Latching



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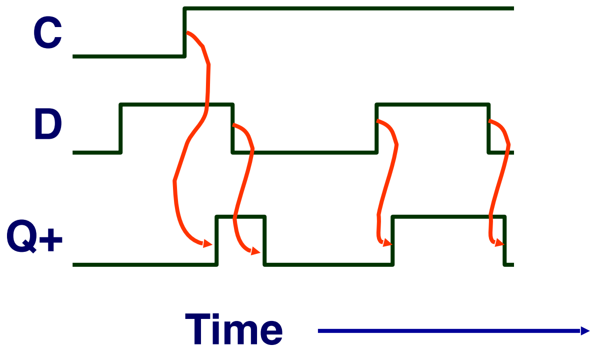

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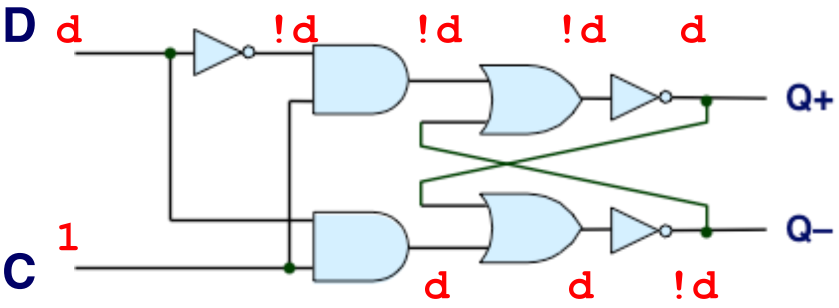

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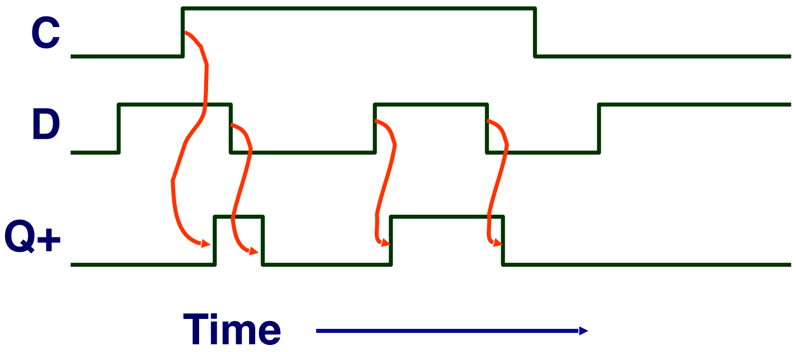

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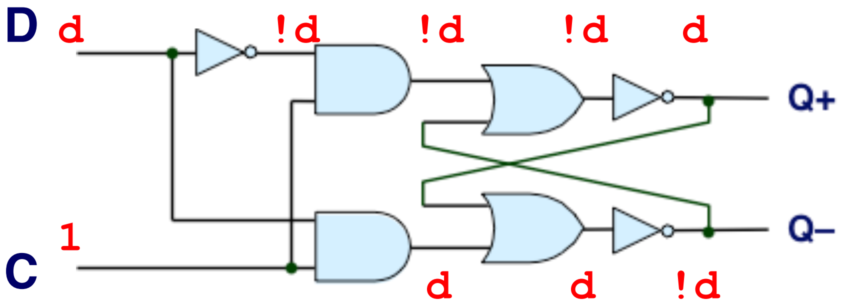

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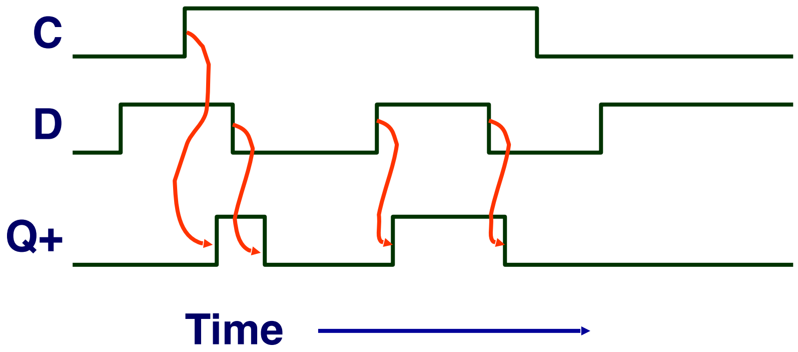

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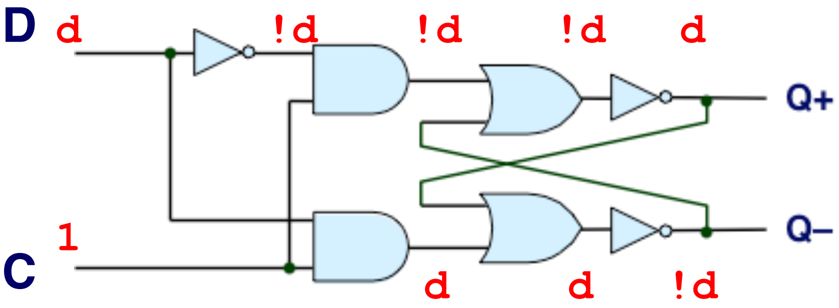

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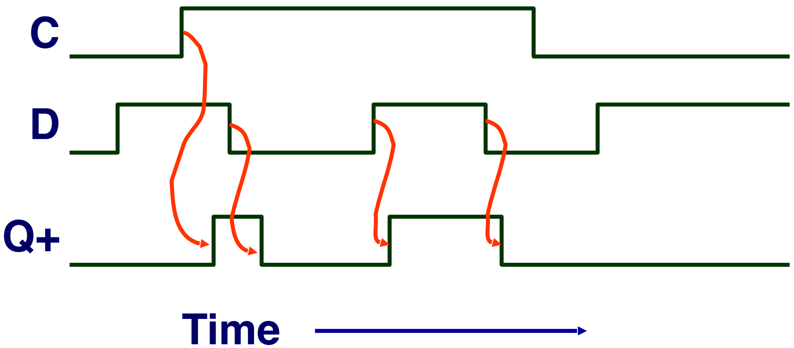

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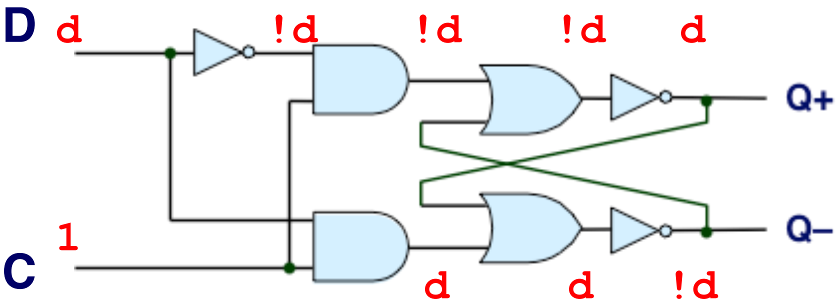

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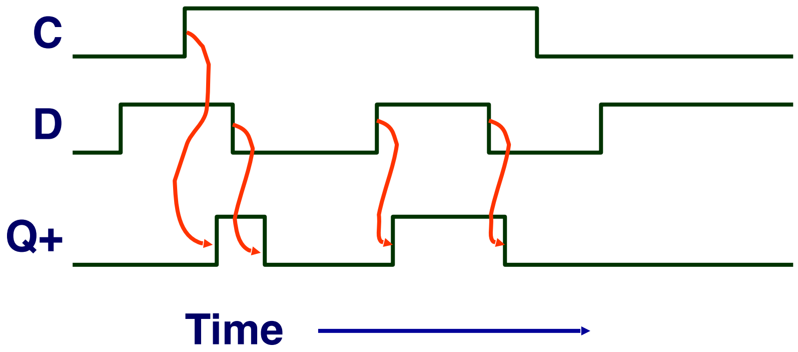

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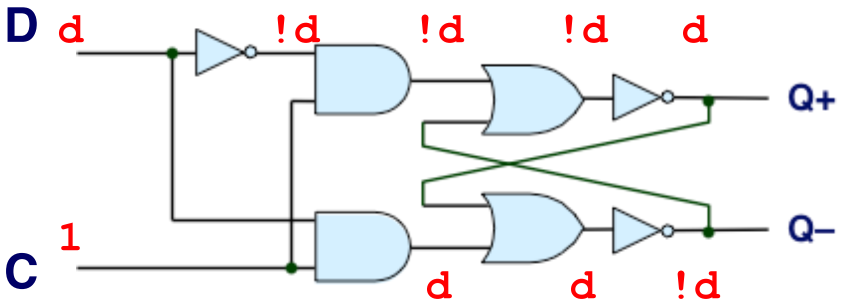

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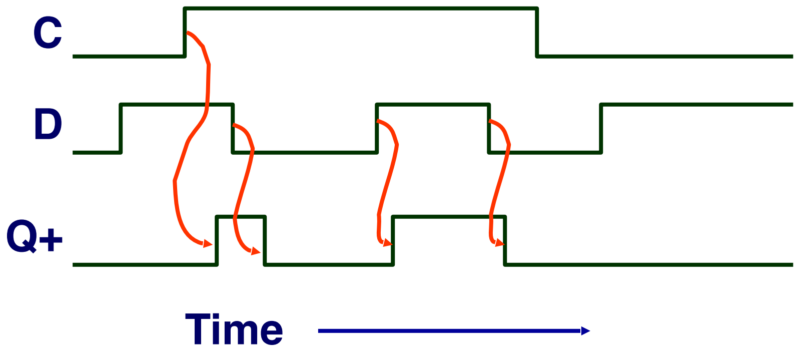

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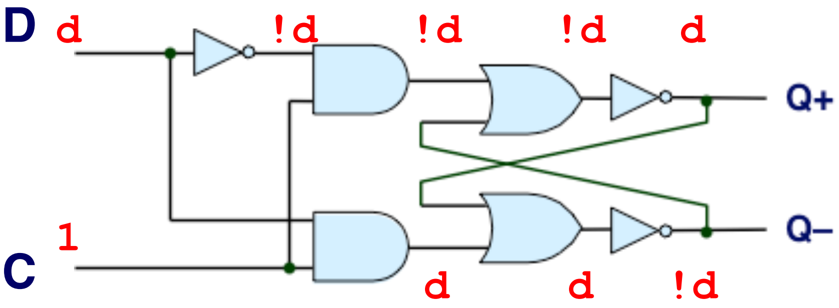

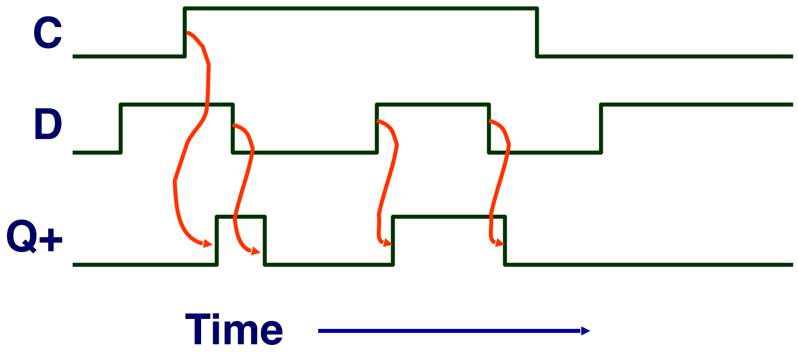

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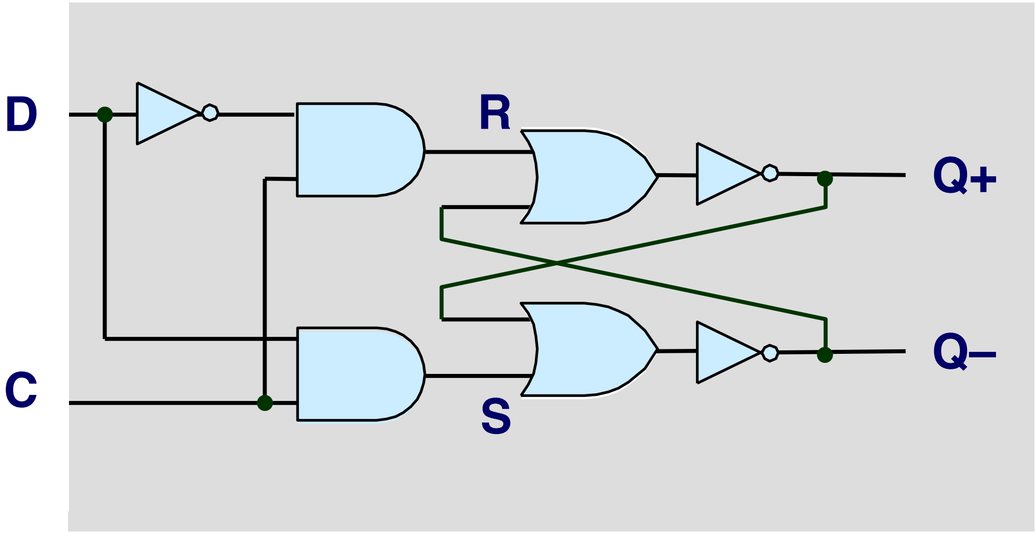
- D-latch is “*level-triggered*” b/c **Q** changes as the voltage level of **C** rises.

Edge-Triggered Latch (Flip-Flop)



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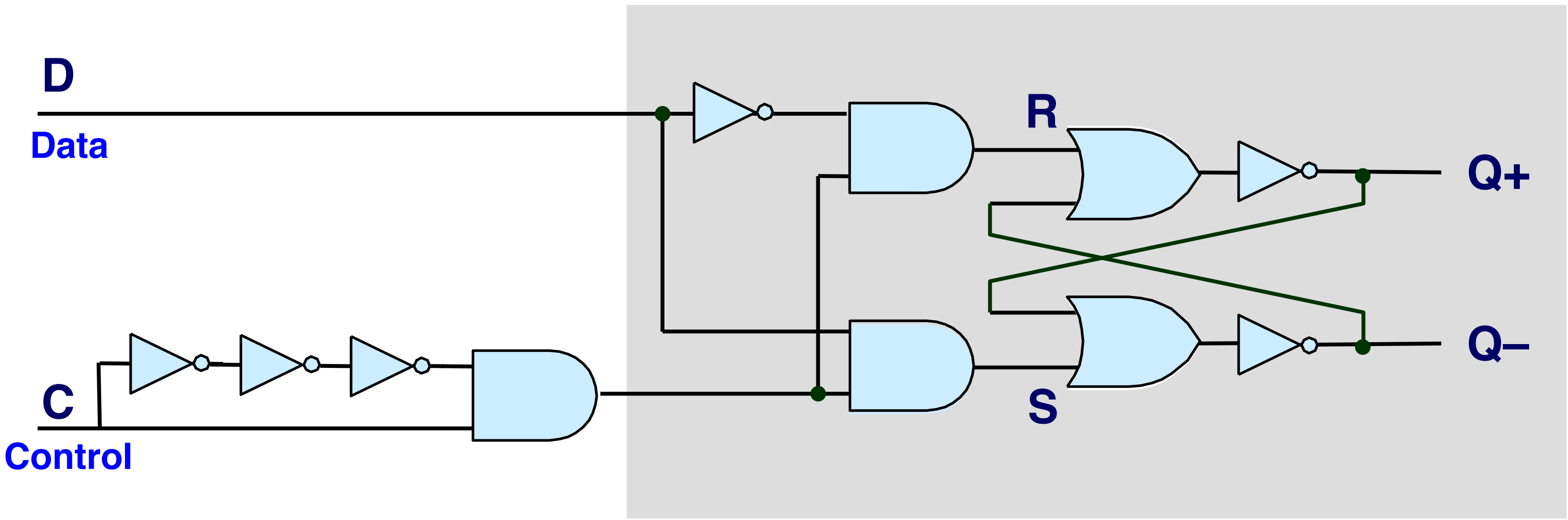

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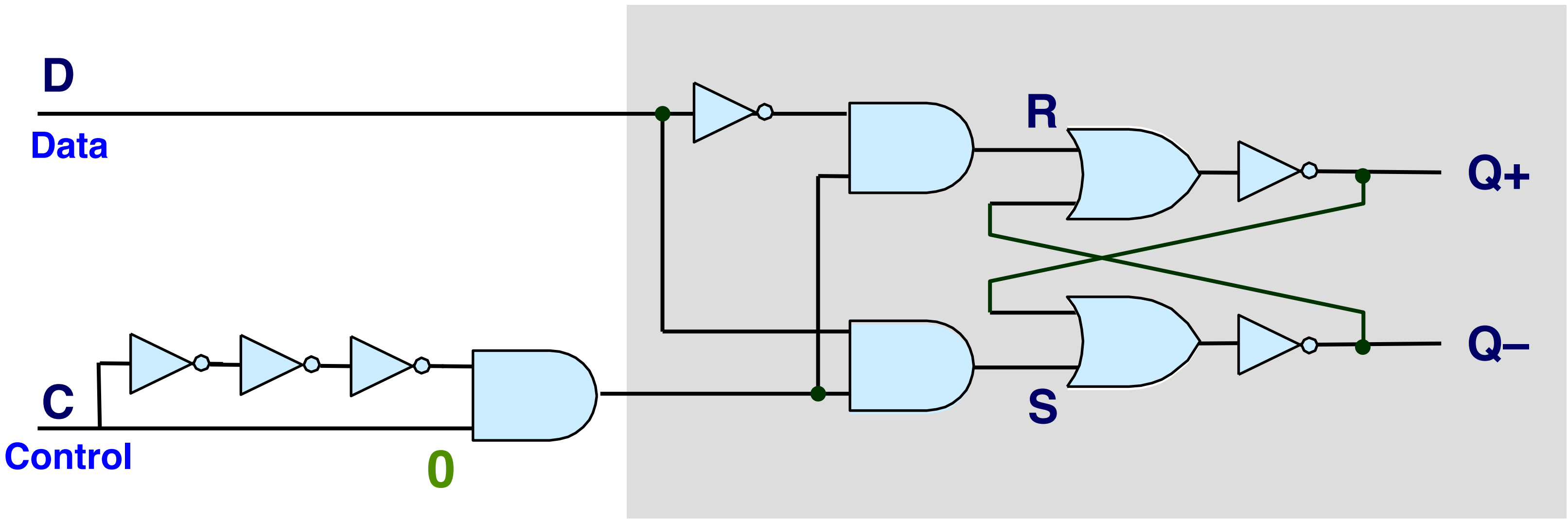

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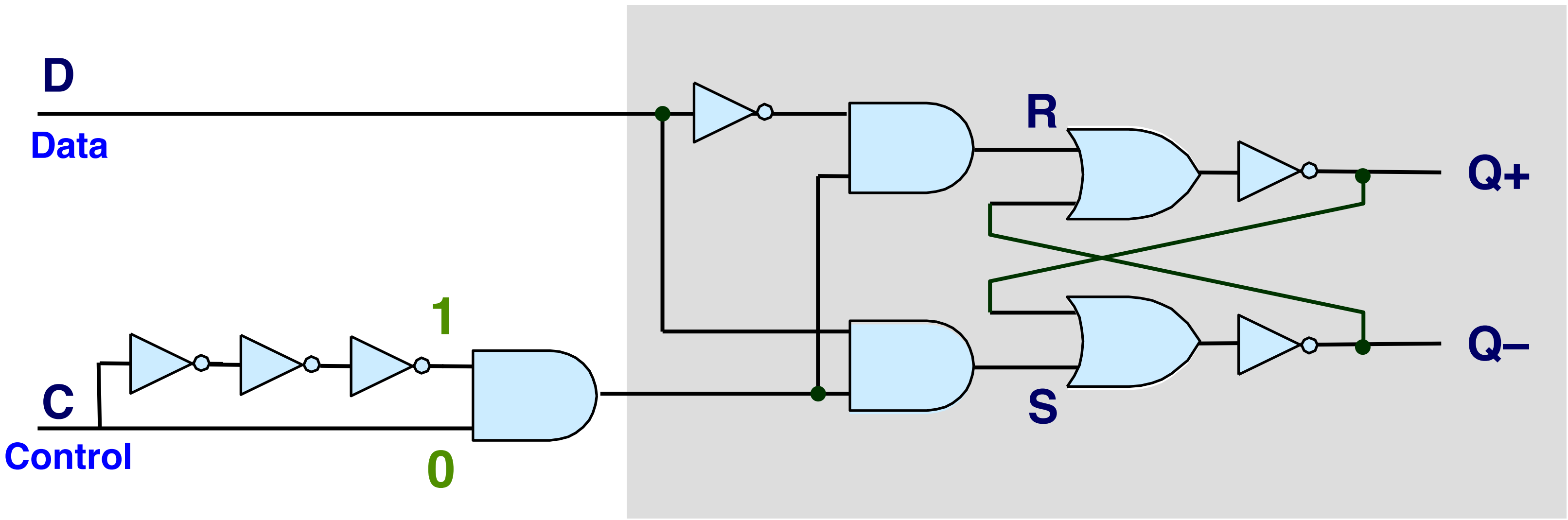

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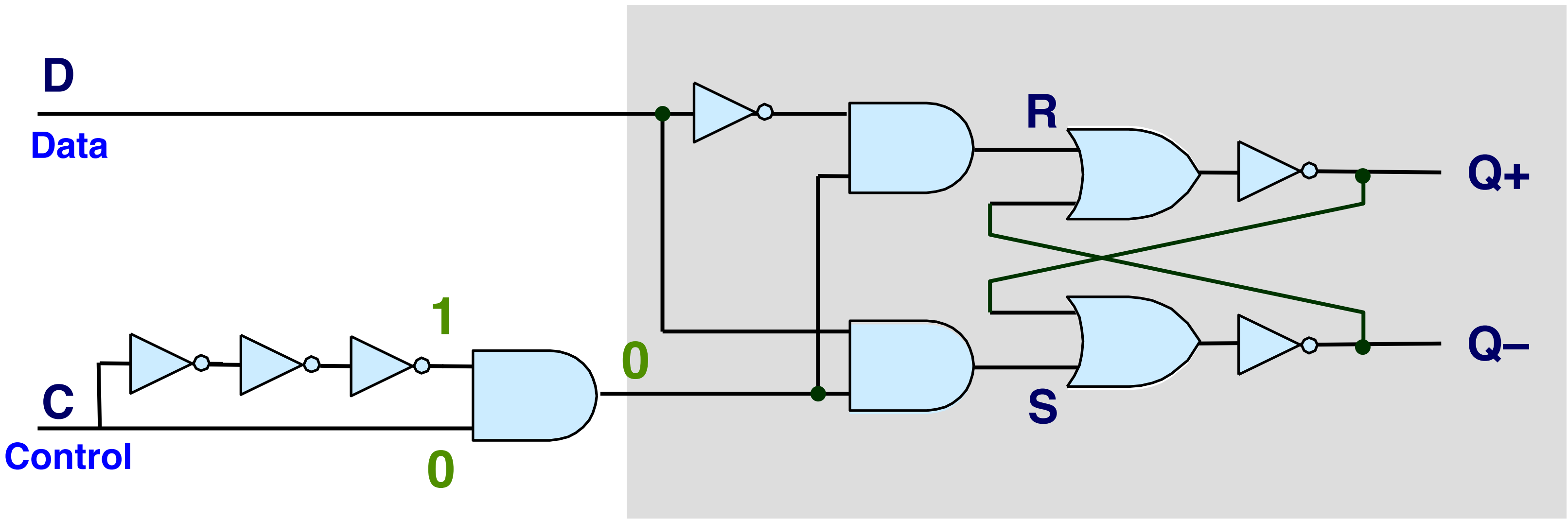

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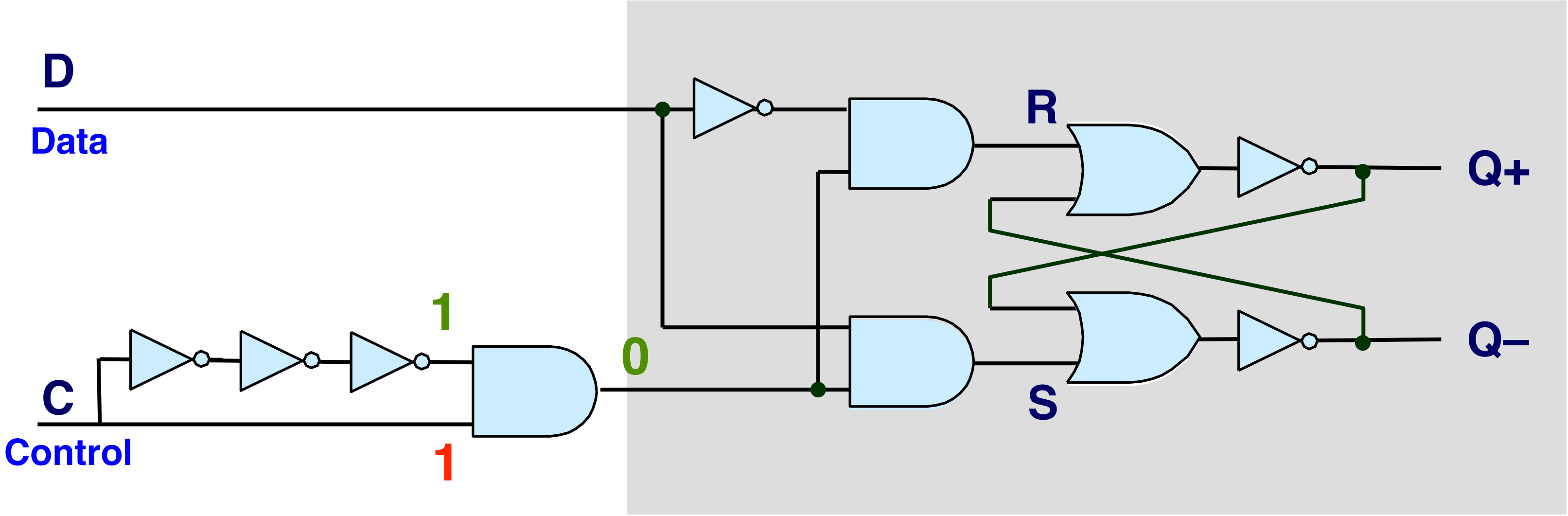

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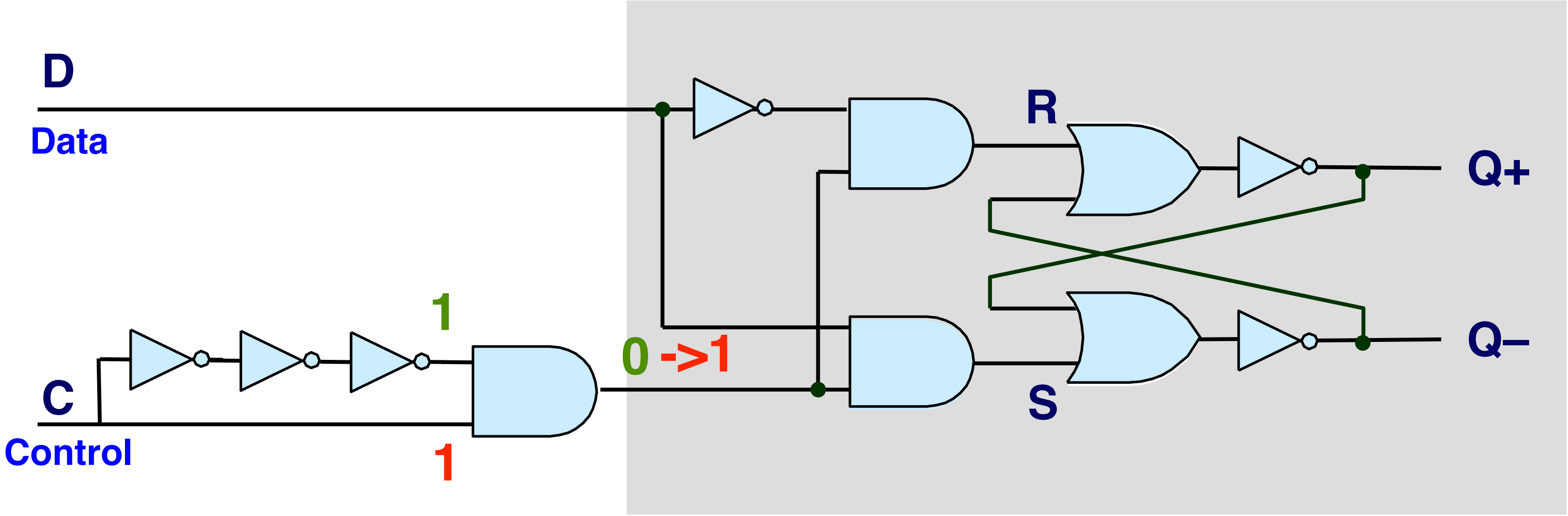

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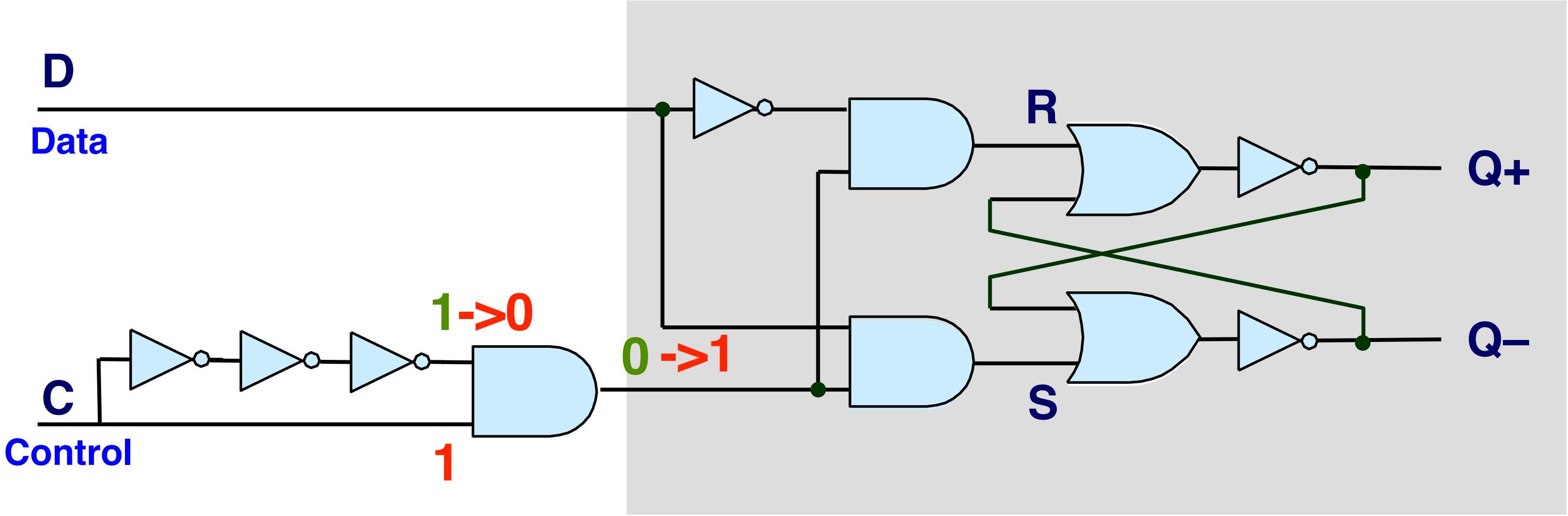

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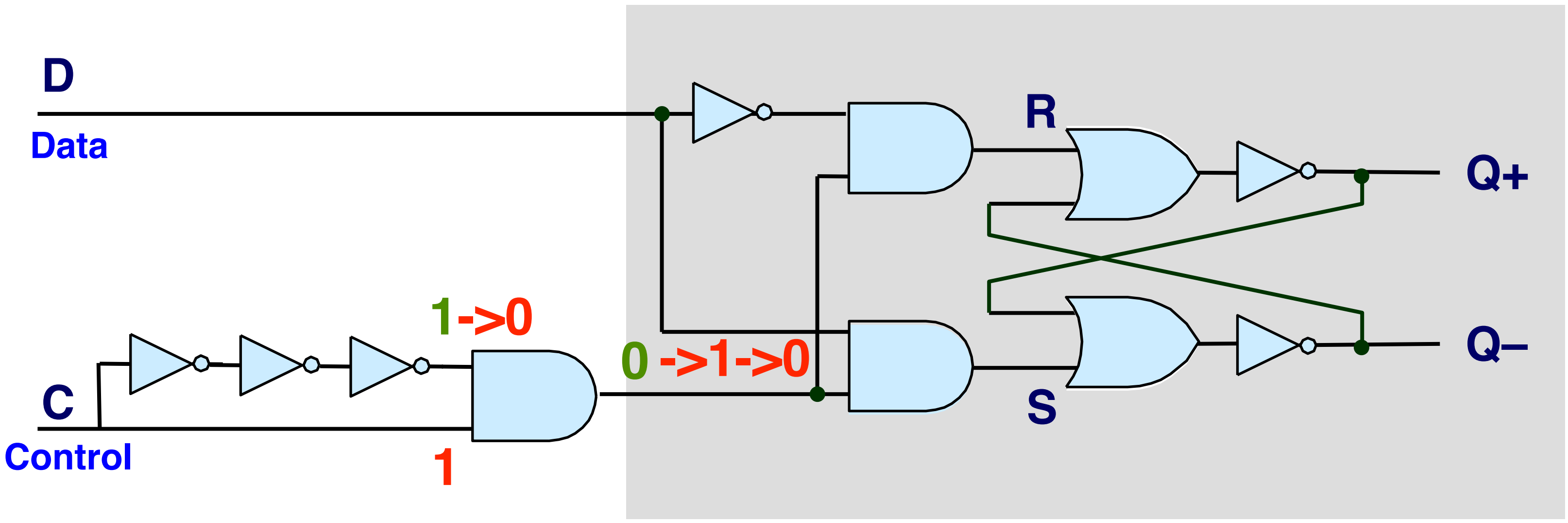

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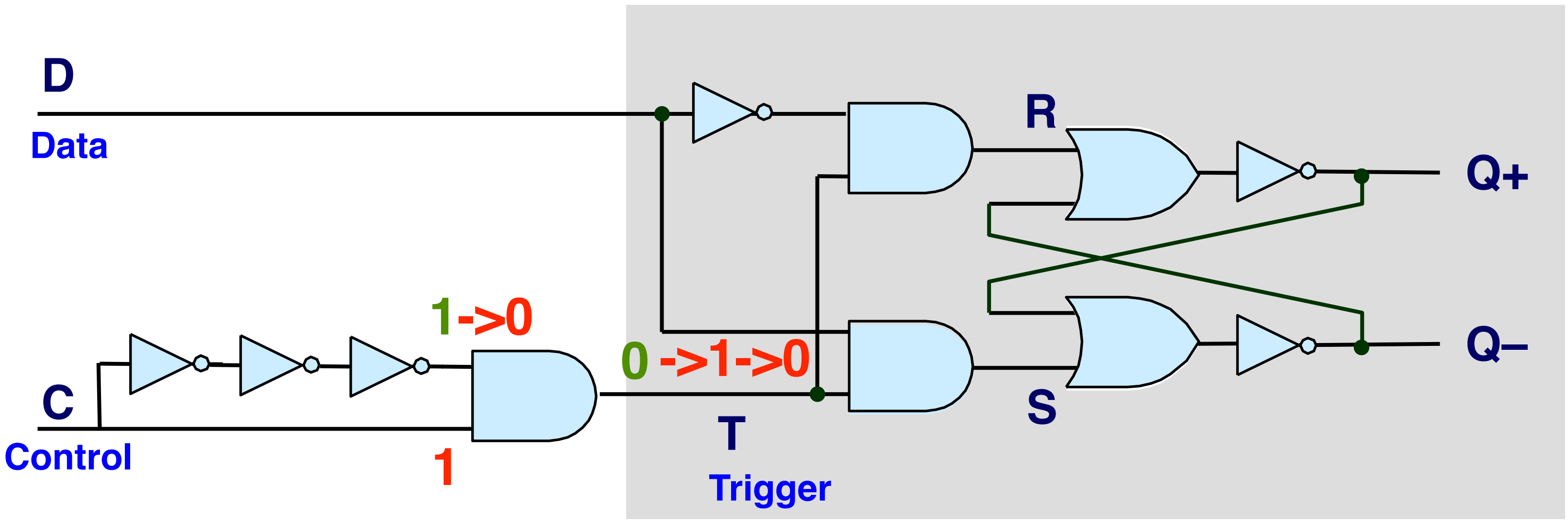

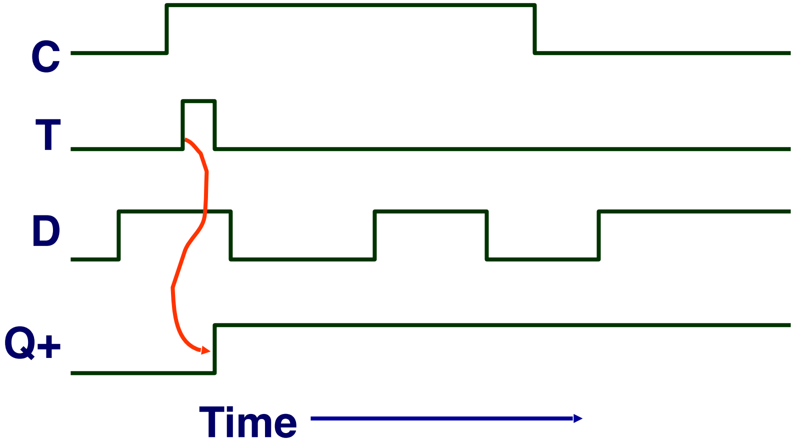

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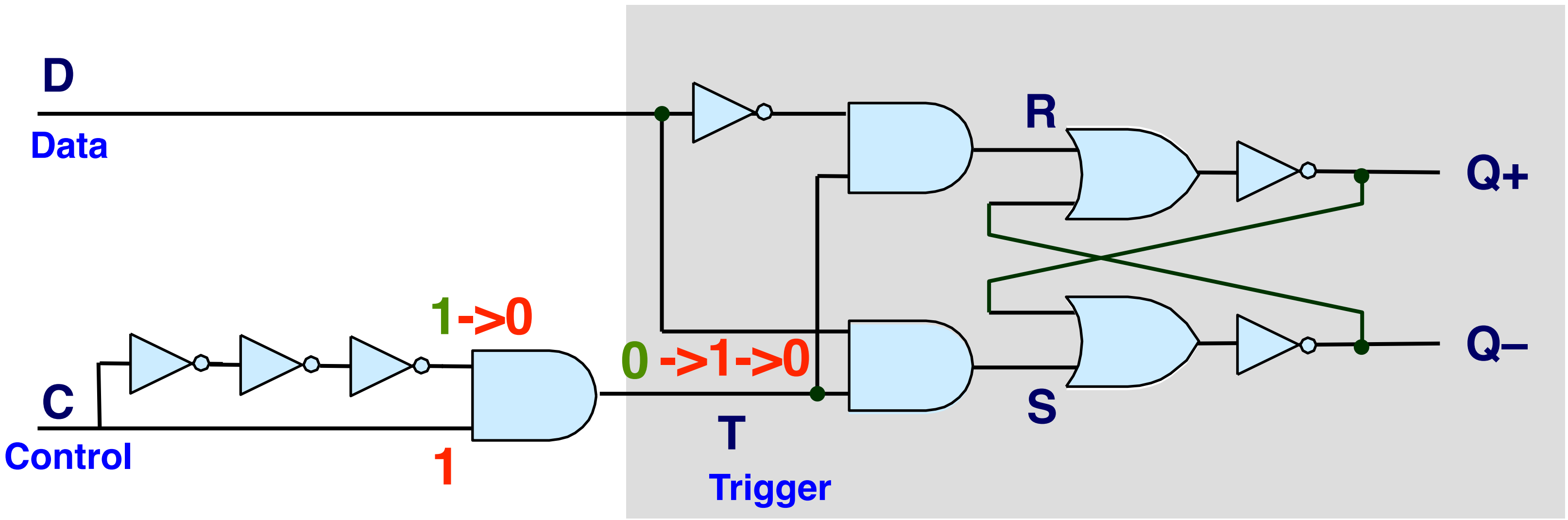

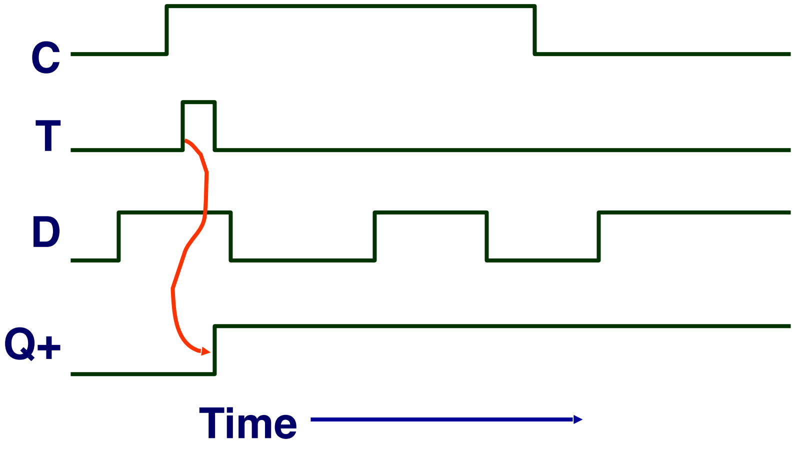

- Flip-flop: Only latches data for a brief period

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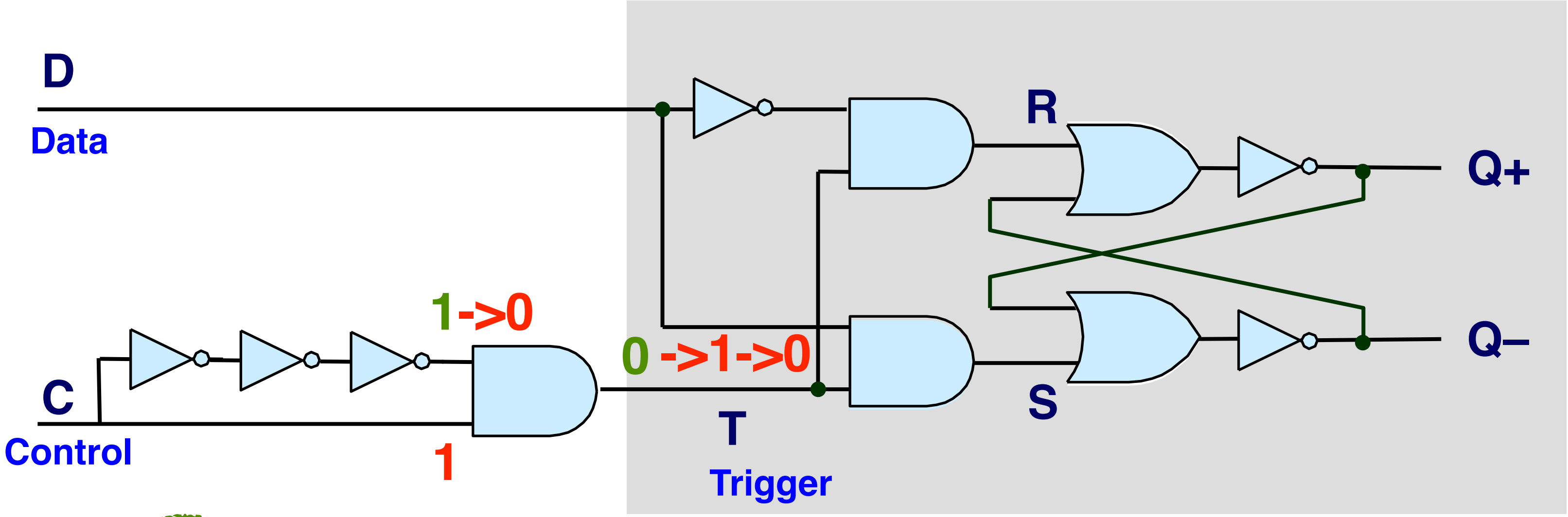

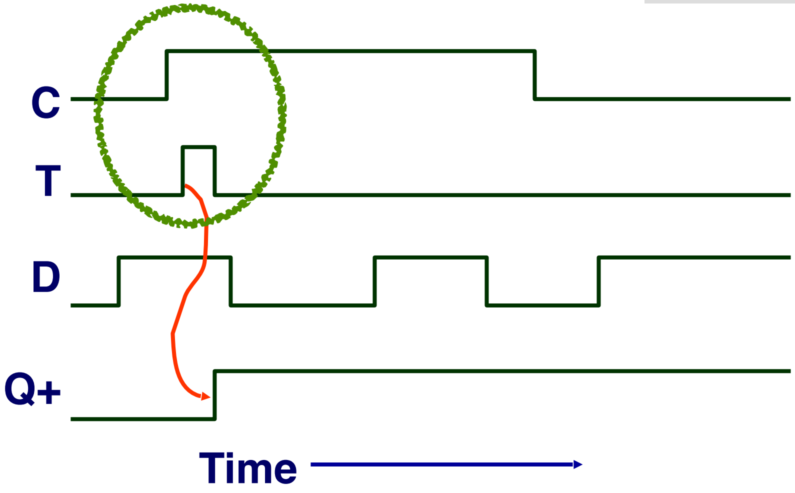

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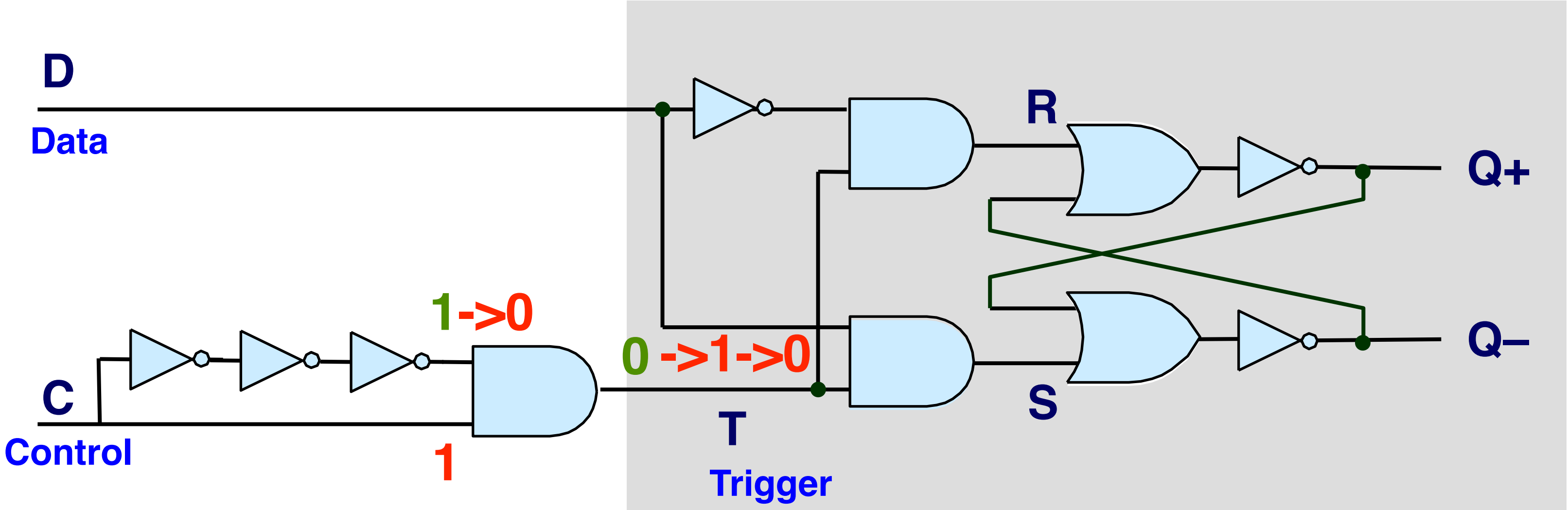
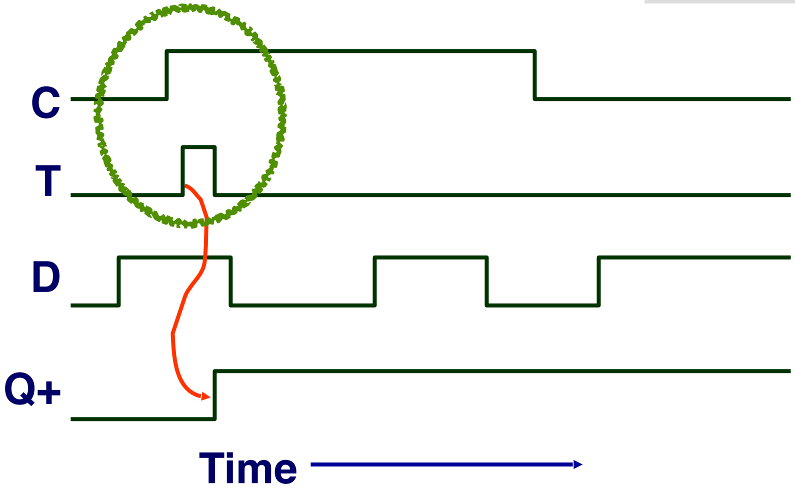
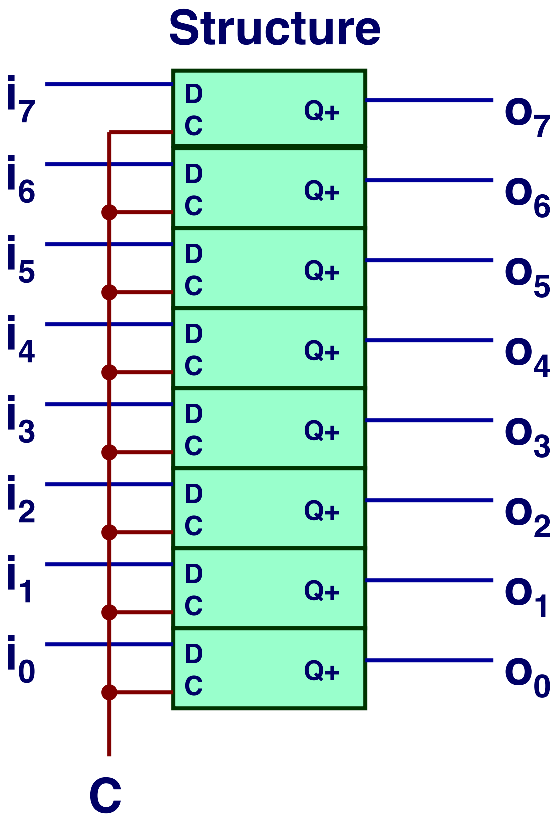




- Flip-flop: Only latches data for a brief period
- Value latched depends on data as C **rises** (i.e., 0–>1); usually called at the **rising edge** of C
- Output remains stable at all other times

Registers



- Stores several bits of data
- Collection of edge-triggered latches (D Flip-flops)
- Loads input on rising edge of the C signal

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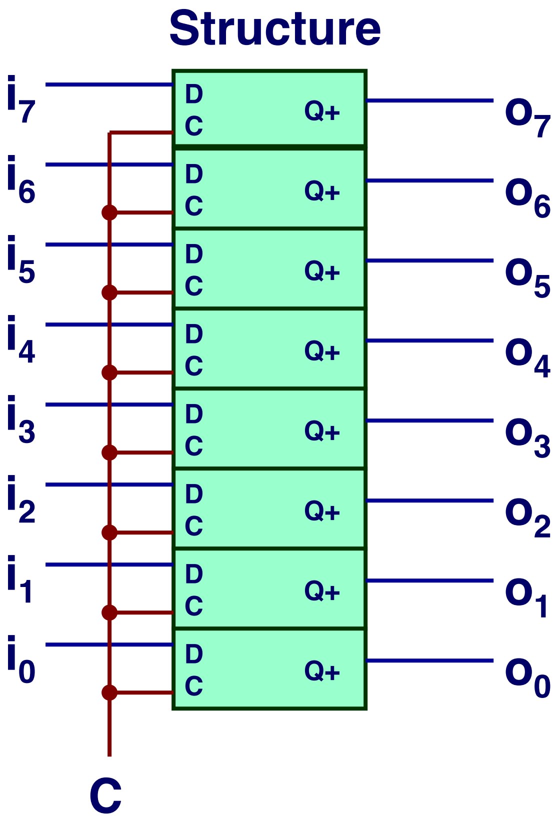

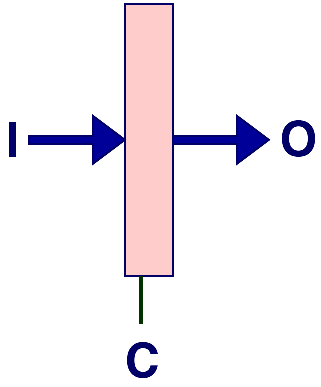

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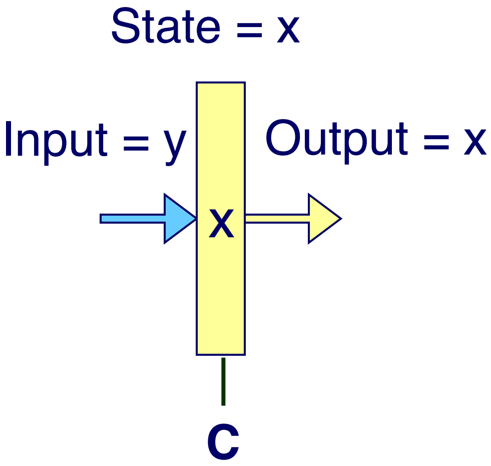
Register Operation



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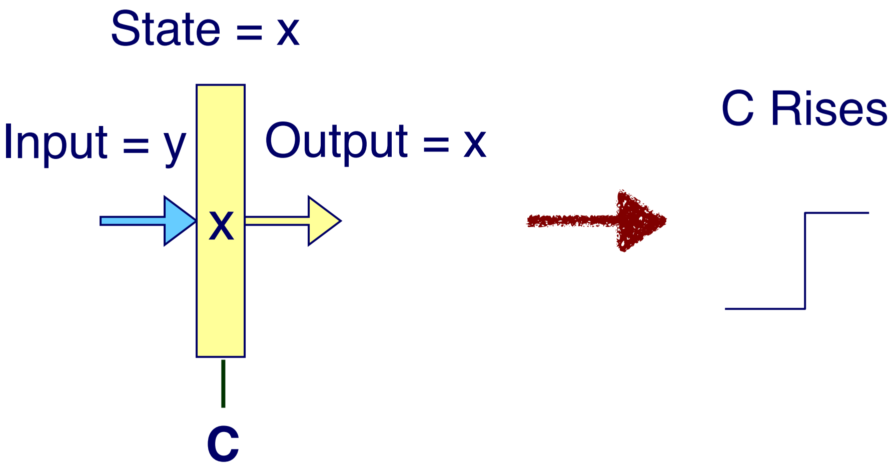


State = x

Input = y

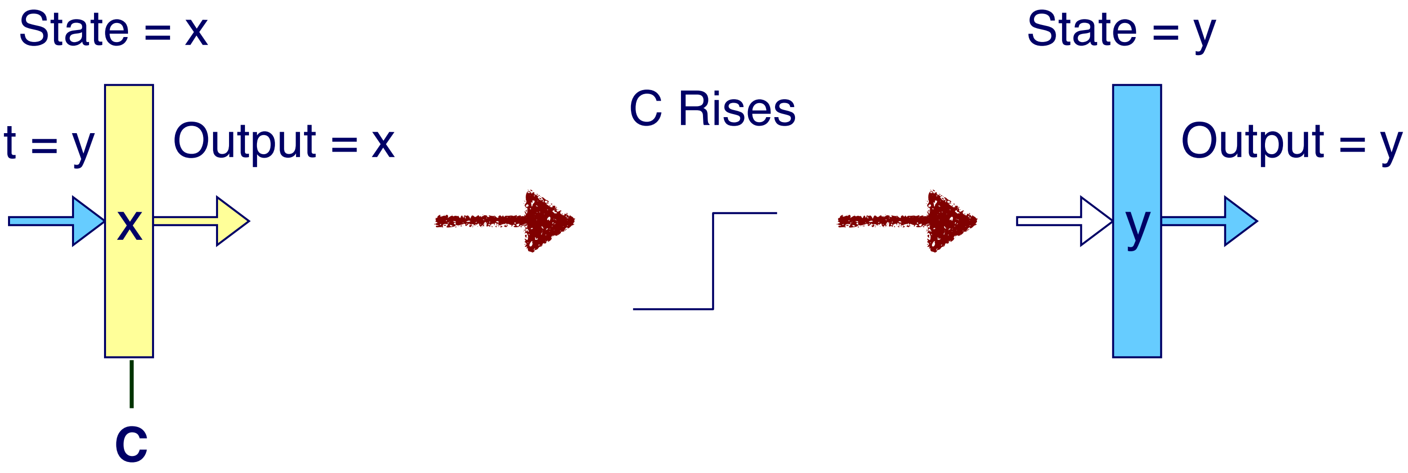
x

Output = x

C

C Rises

Register Operation



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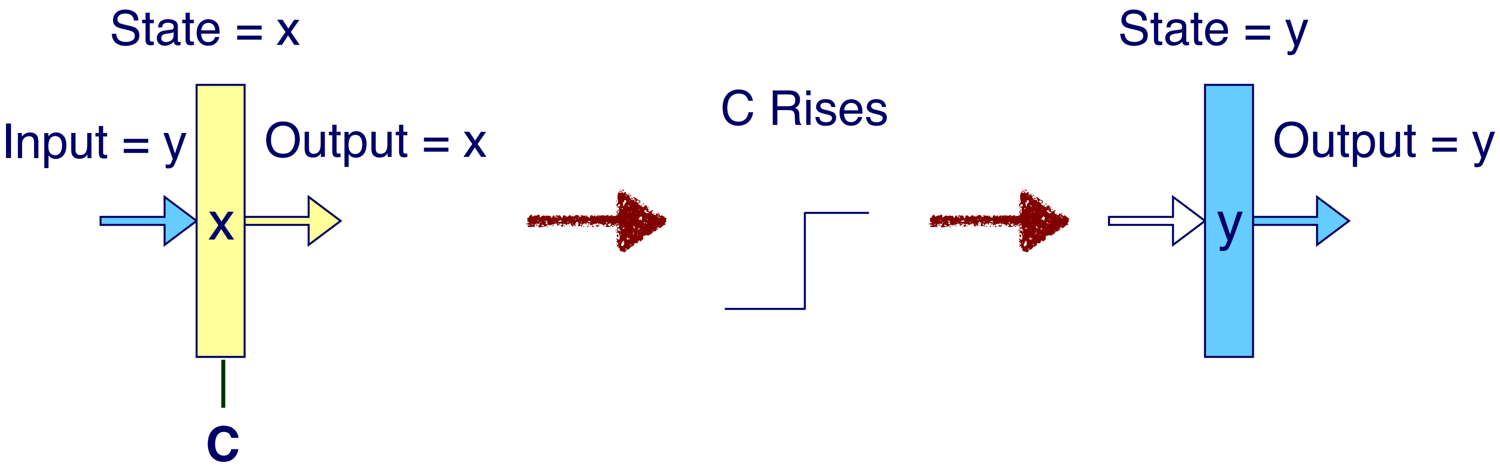

- Stores data bits
- For most of time acts as barrier between input and output
- As C rises, loads input
- So you'd better compute the input before the C signal rises if you want to store the input data to the register

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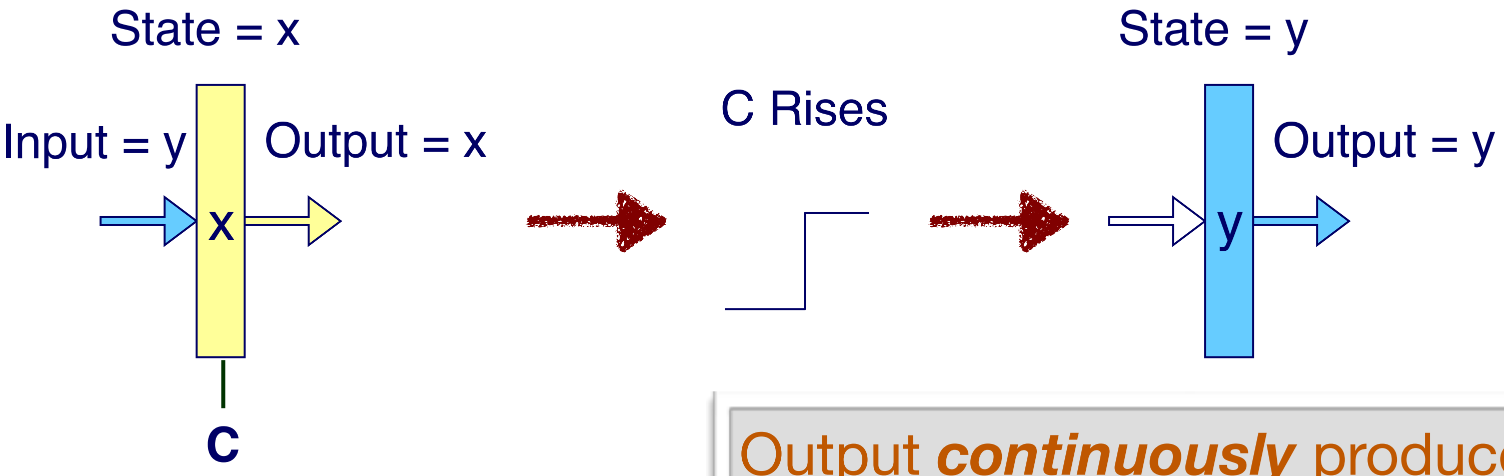

Output ***continuously*** produces y after the rising edge unless you cut off power.

- Stores data bits
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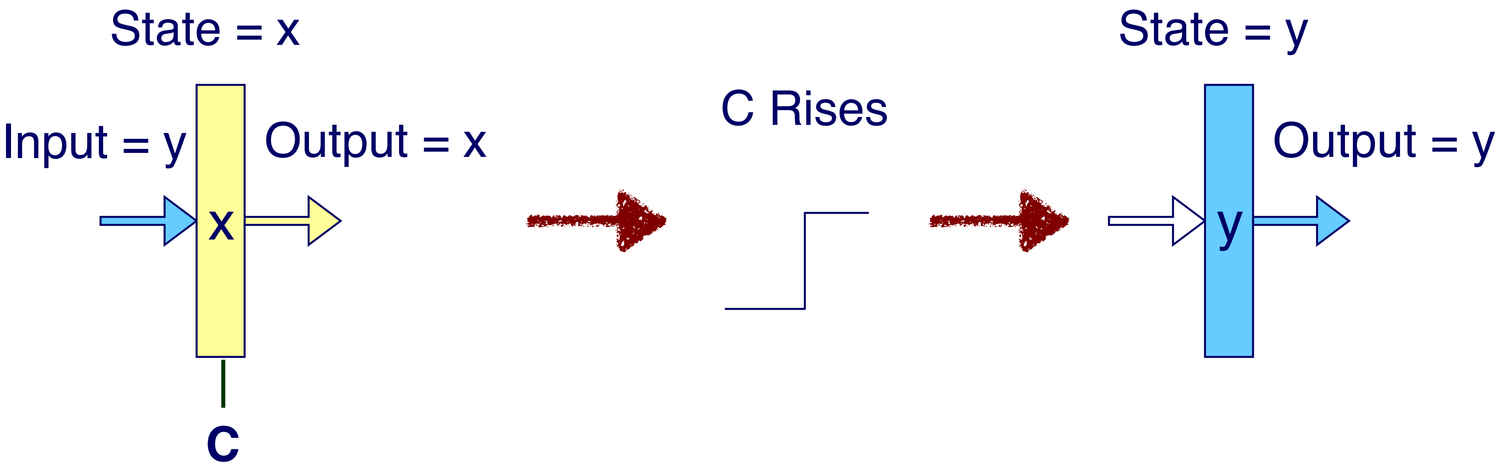
Clock Signal



- A special C: periodically oscillating between 0 and 1
- That’s called the **clock** signal. Generated by a crystal oscillator inside your computer

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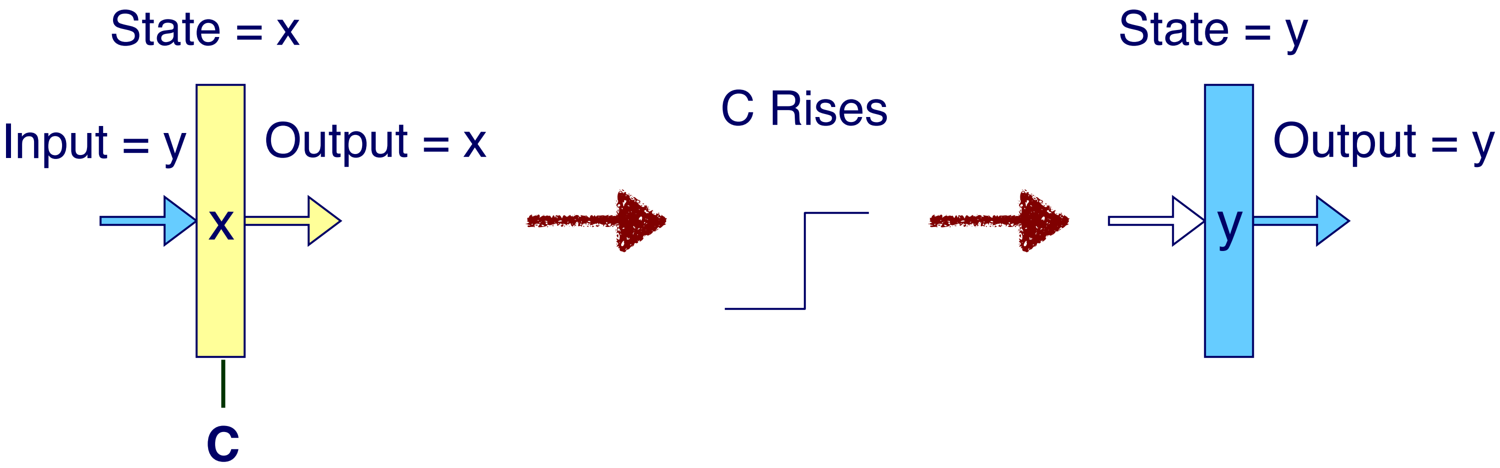

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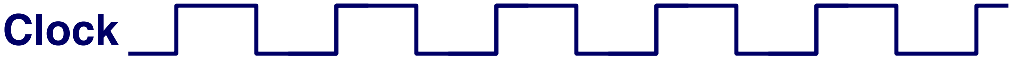

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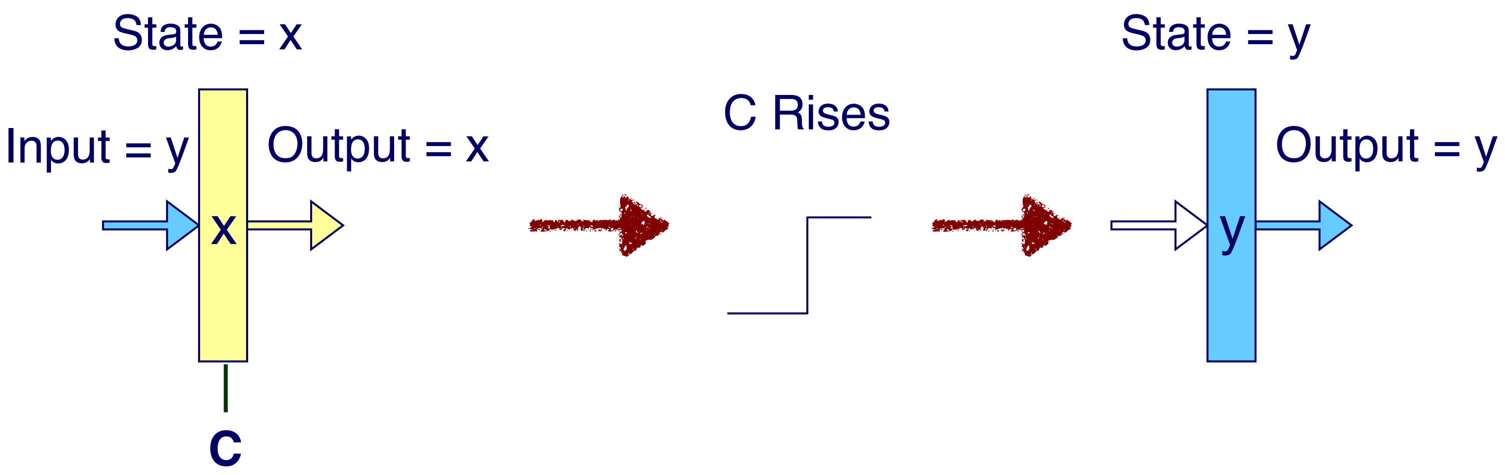

State = x

Input = y

x

Output = x

C

C Rises

State = y

y

Output = y

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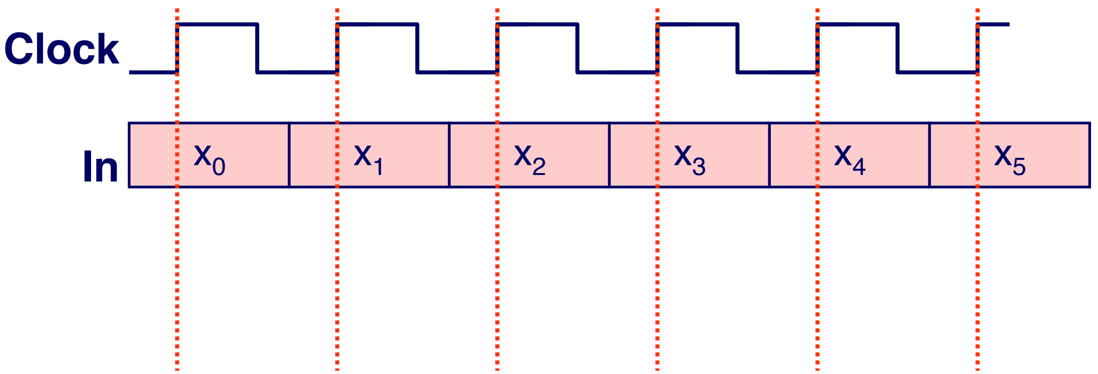
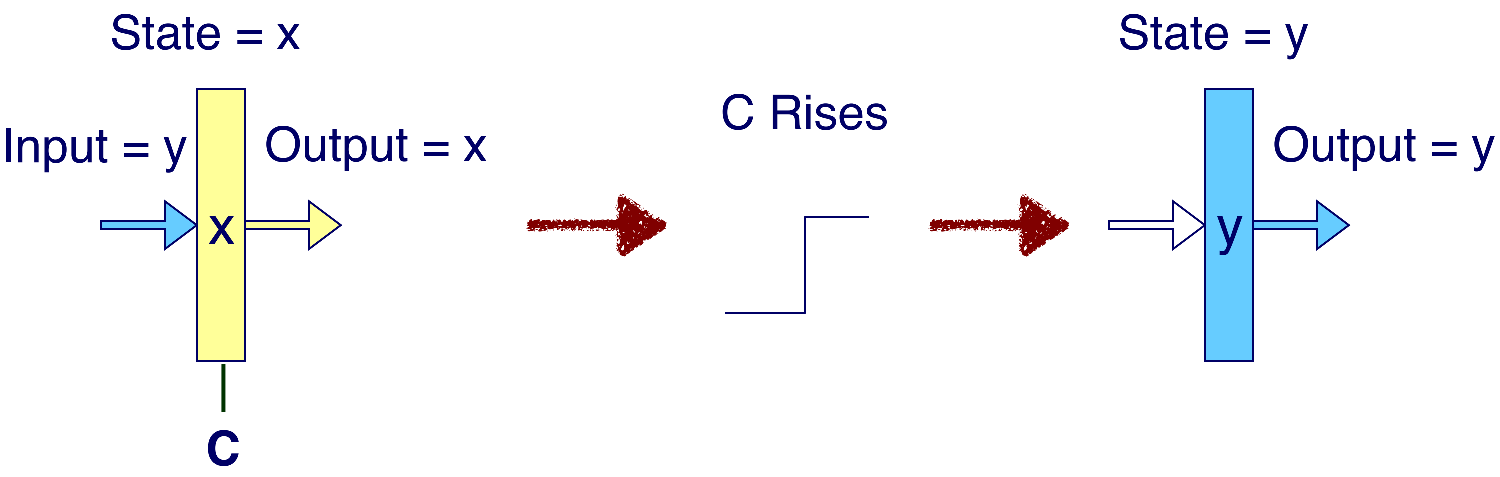


Clock

In

x_0 x_1 x_2 x_3 x_4 x_5

Clock Signal



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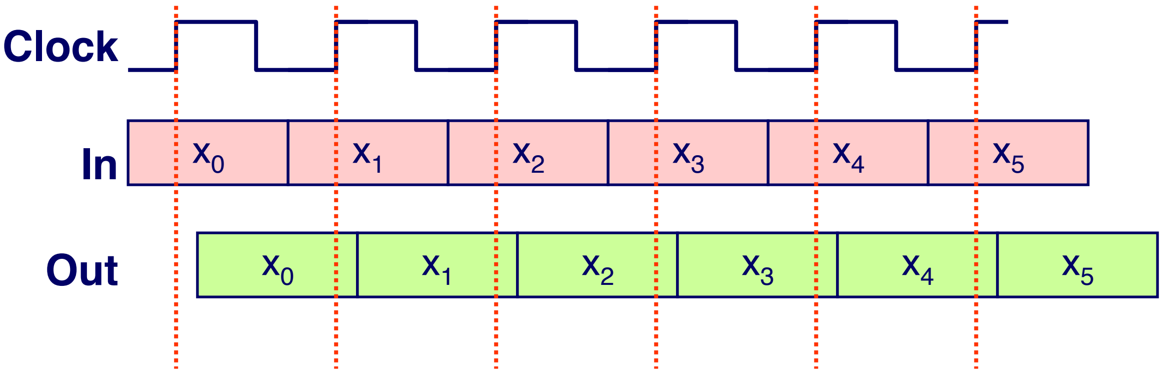

Clock Signal

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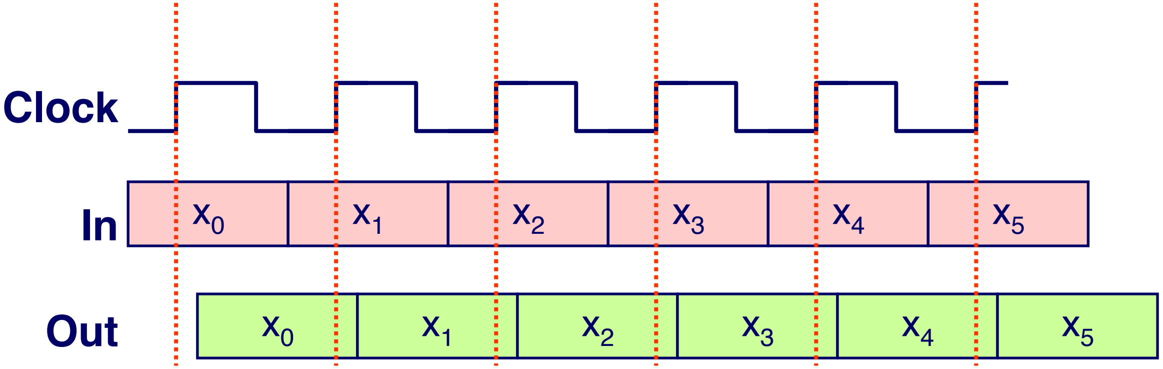

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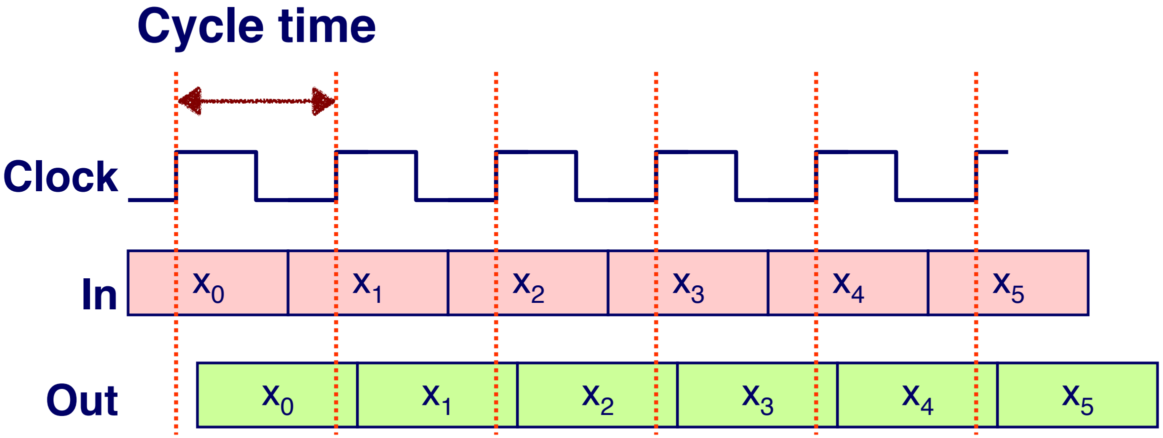

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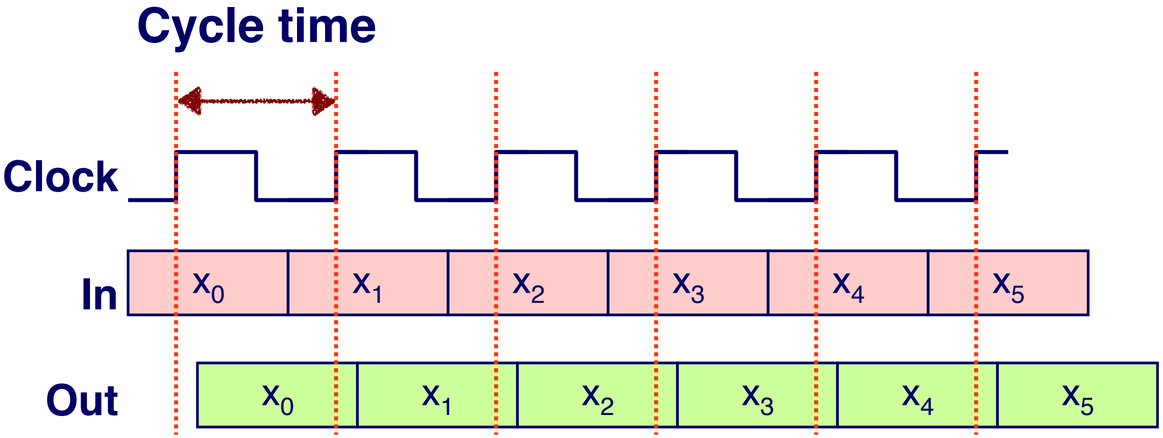

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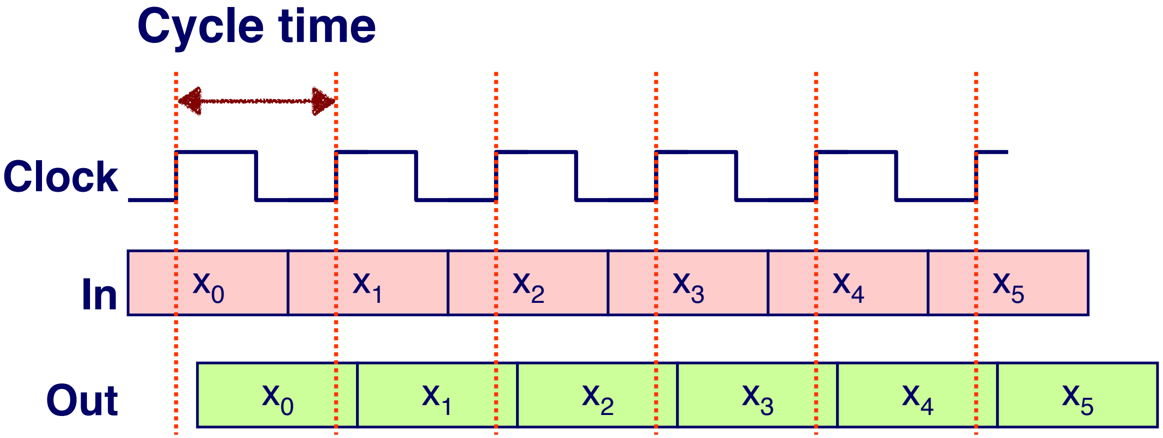

Clock Signal

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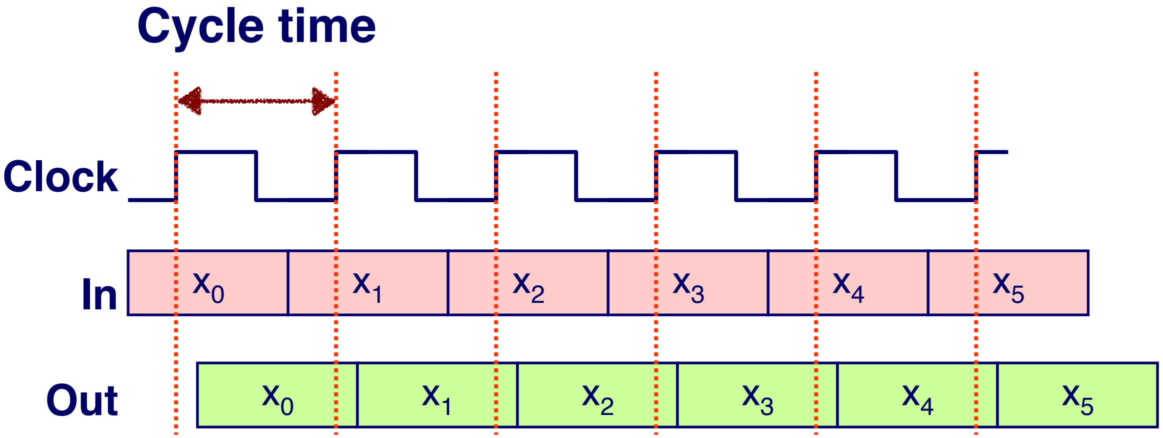
- 1 GHz CPU means the clock frequency is 1 GHz
  - The cycle time is 1/10^9 = 1 ns


Cycle time
Clock
In
x_0
x_1
x_2
x_3
x_4
x_5
Out
x_0
x_1
x_2
x_3
x_4
x_5