

CSC 252: Computer Organization

Spring 2021: Lecture 5

Instructor: Yuhao Zhu

Department of Computer Science
University of Rochester

Announcements

- Programming Assignment 1 is due tomorrow!
 - Details: <https://www.cs.rochester.edu/courses/252/spring2021/labs/assignment1.html>
 - Due on Feb. 17, 11:59 PM
 - You have 3 slip days

7	8	9	10	11	12	13
14	15	16	17	18	19	20
		Today	Due			

Announcements

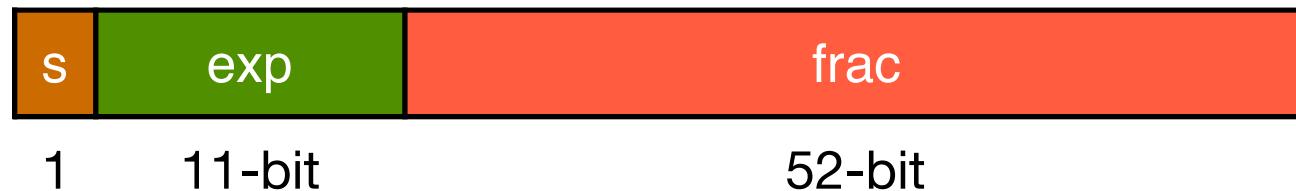
- Will release programming assignment 2 today.
- TAs are best positioned to answer your questions about programming assignments!!!
- Programming assignments do NOT repeat the lecture materials. They ask you to synthesize what you have learned from the lectures and work out something new.

IEEE 754 Floating Point Standard

- Single precision: 32 bits



- Double precision: 64 bits



- In C language

- `float` single precision
- `double` double precision

Floating Point in C

32-bit Machine

C Data Type	Bits	Max Value	Max Value (Decimal)
char	8	$2^7 - 1$	127
short	16	$2^{15} - 1$	32767
int	32	$2^{31} - 1$	2147483647
long	64	$2^{63} - 1$	$\sim 9.2 \times 10^{18}$
float	32	$(2 - 2^{-23}) \times 2^{127}$	$\sim 3.4 \times 10^{38}$
double	64	$(2 - 2^{-52}) \times 2^{1023}$	$\sim 1.8 \times 10^{308}$

Fixed point
(implicit binary point) {

SP floating point

DP floating point

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Fixed point
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SP floating point

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- To represent 2^{31} in fixed-point, you need at least 32 bits
 - Because fixed-point is a *weighted positional* representation
- In floating-point, we directly encode the exponent
 - Floating point is based on scientific notation
 - Encoding 31 only needs 7 bits in the exp field

Floating Point Conversions/Casting in C

- **double/float → int**

- Truncates fractional part
- Like rounding toward zero
- Not defined when out of range or NaN

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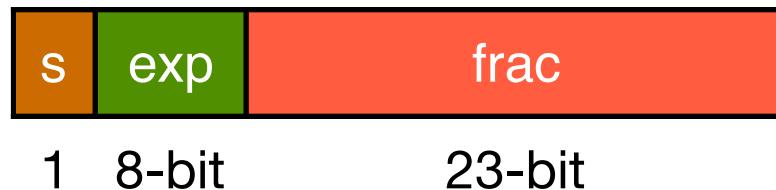
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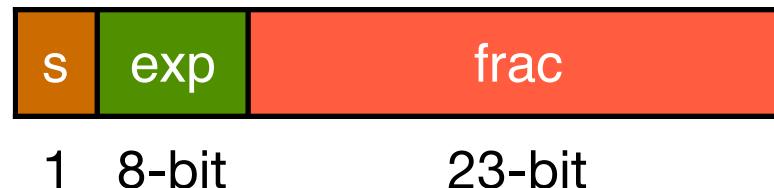
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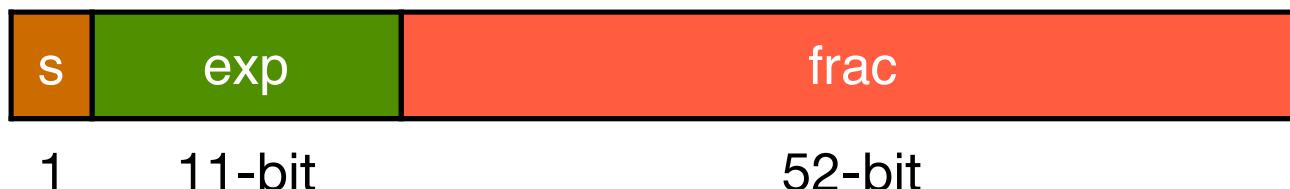
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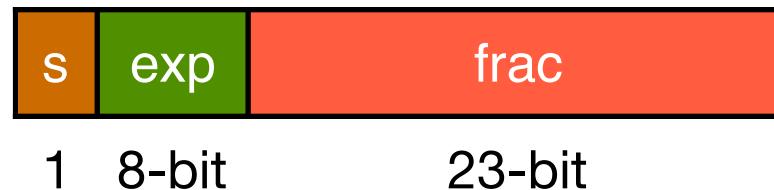
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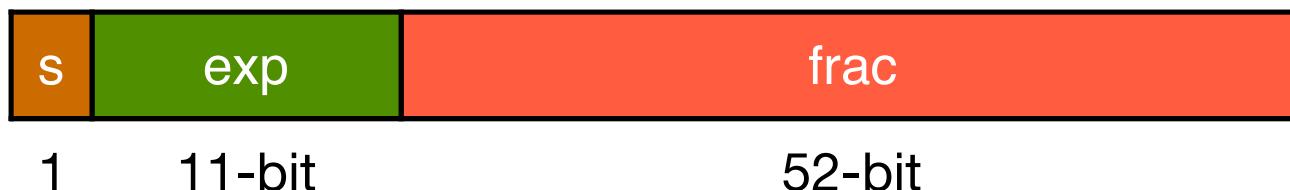
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- Exact conversion

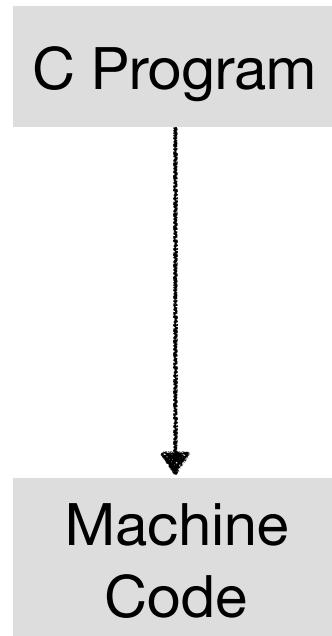


So far in 252...

C Program

int, float
if, else
+, -, >>

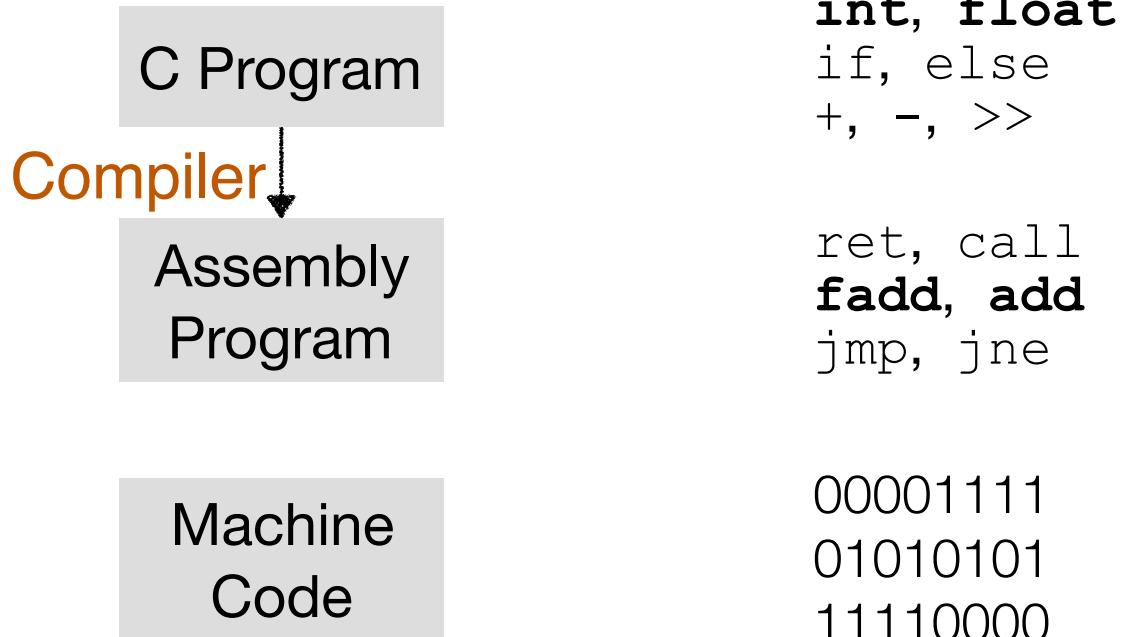
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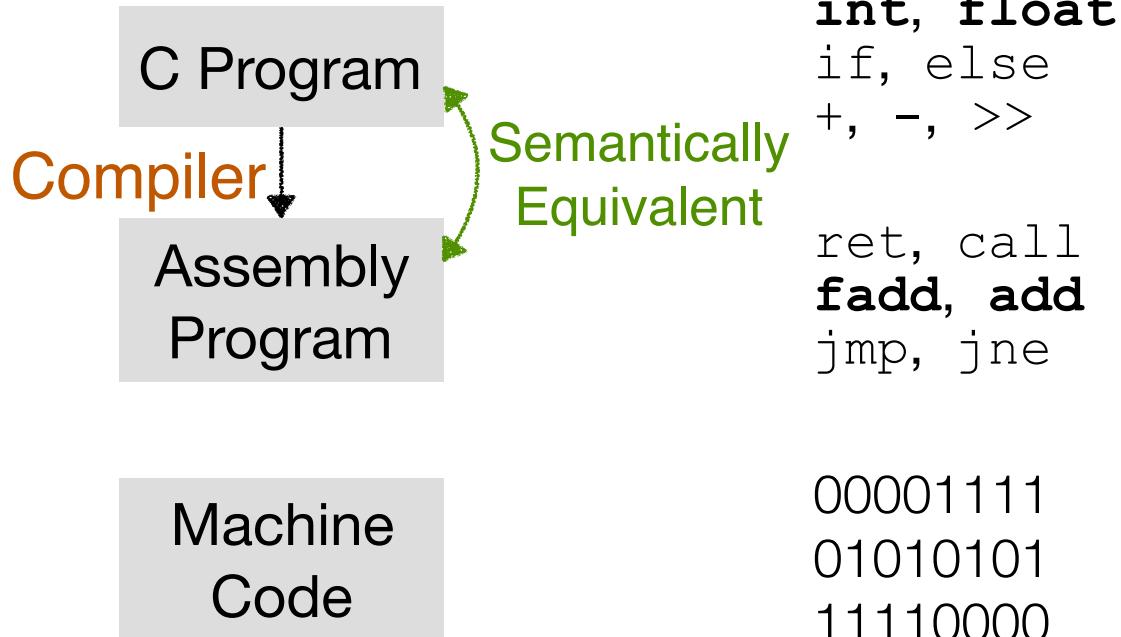
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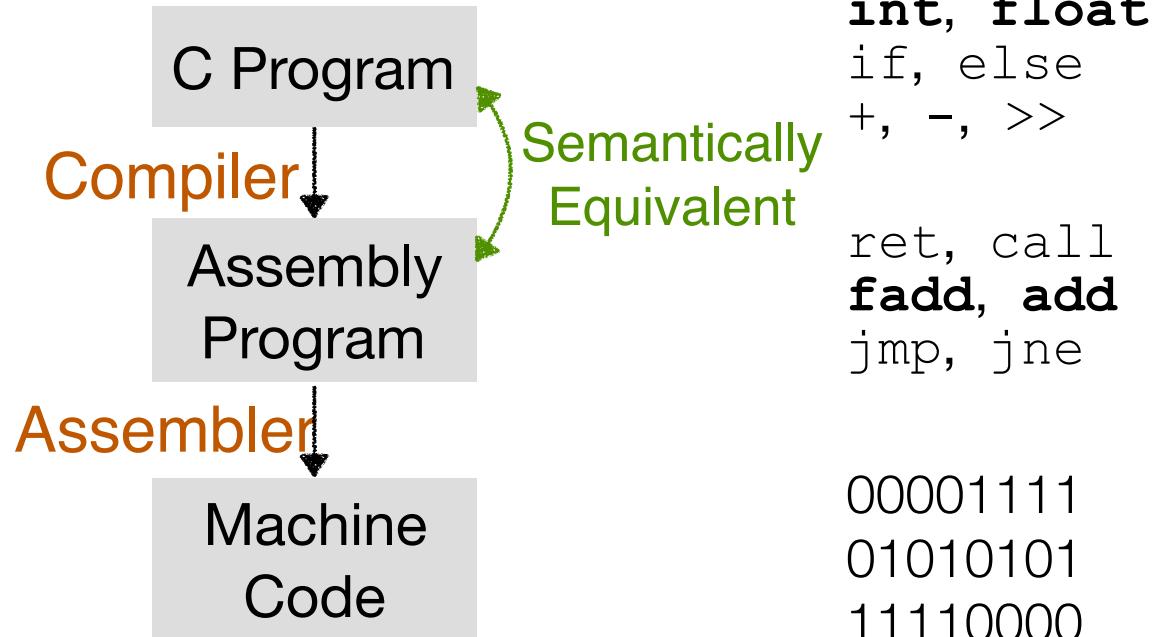
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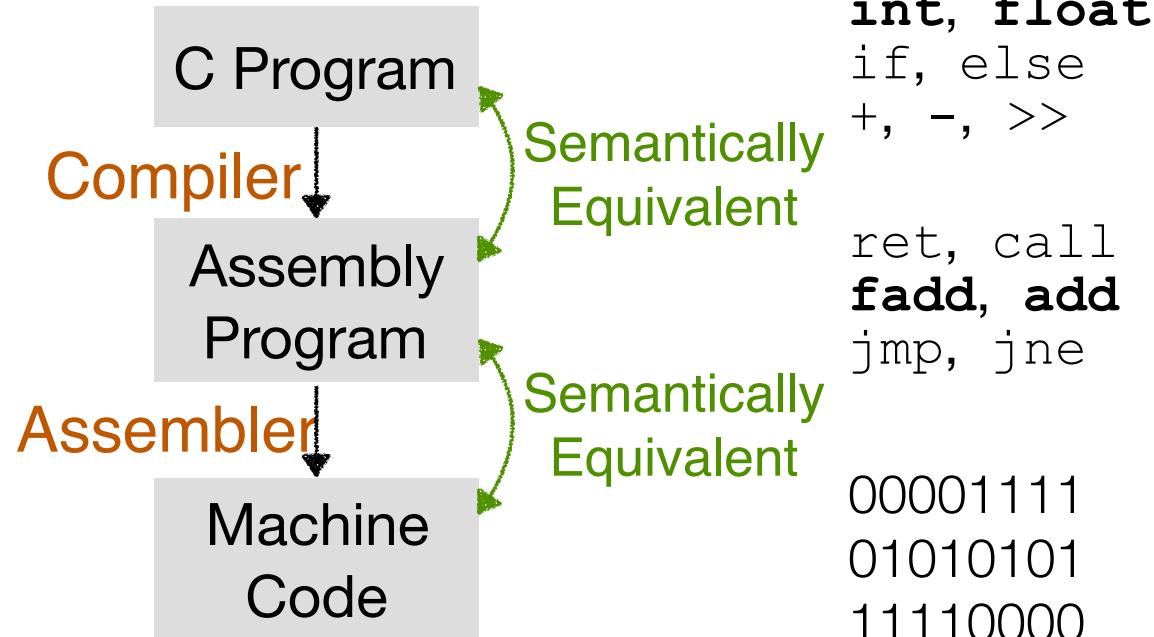
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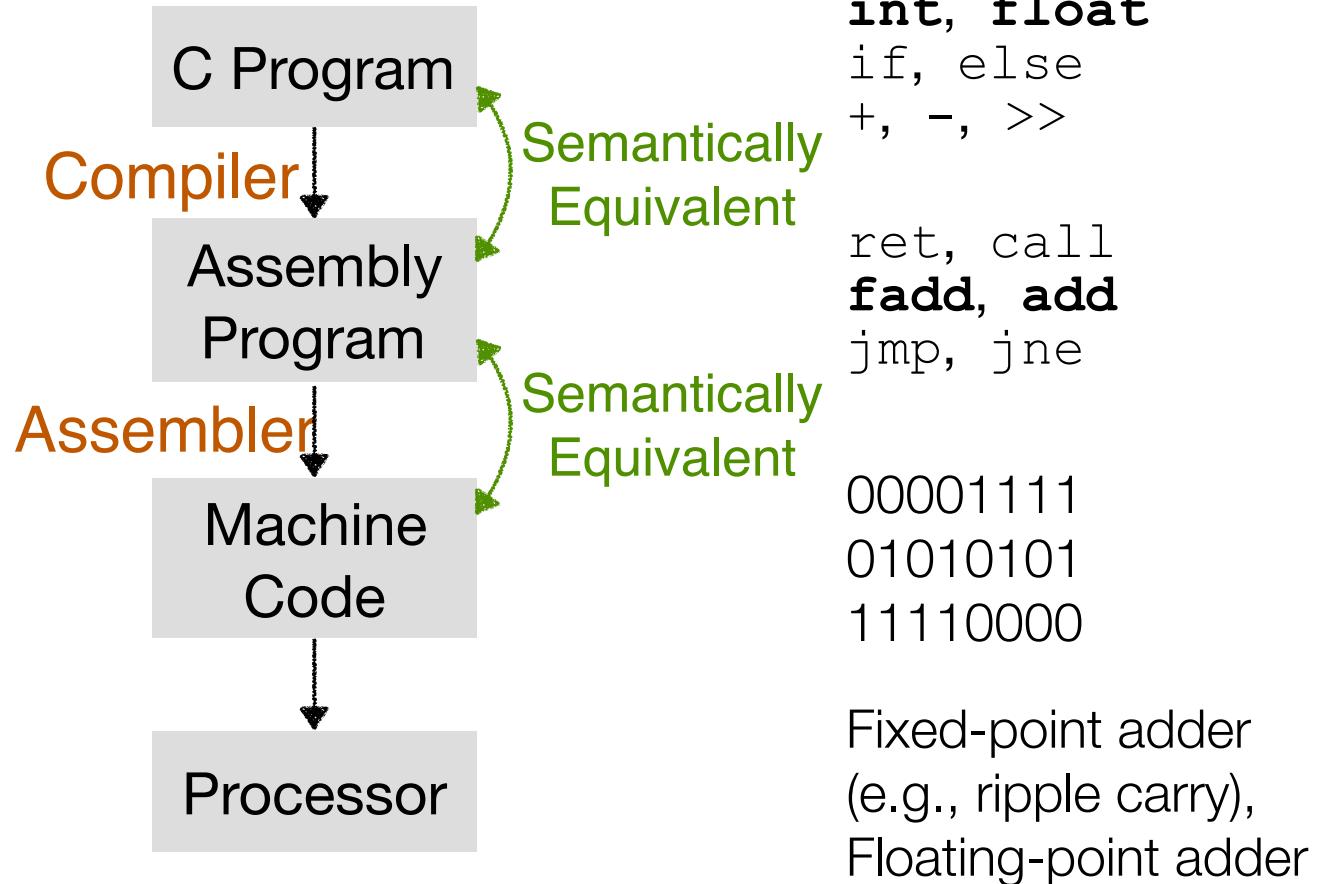
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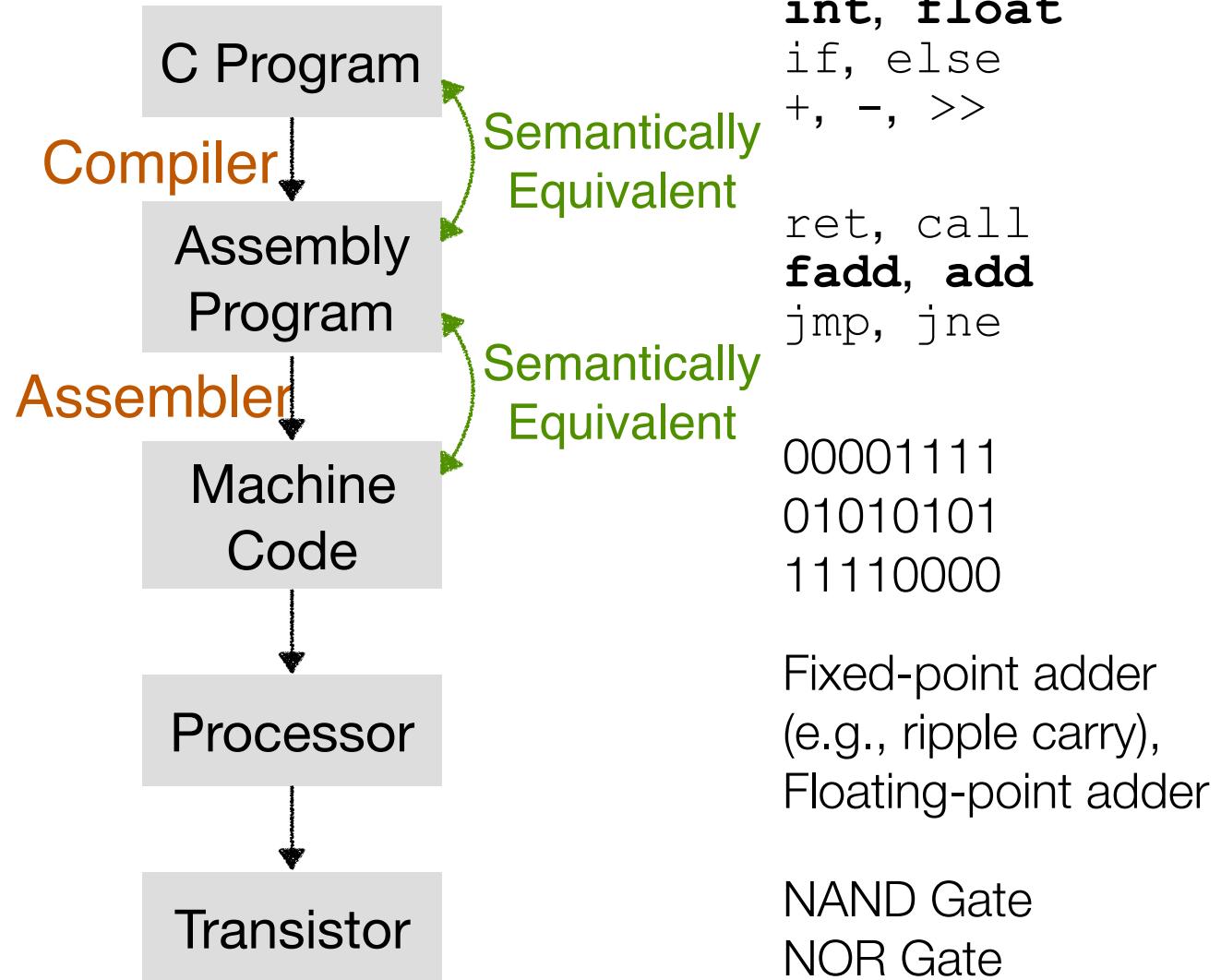
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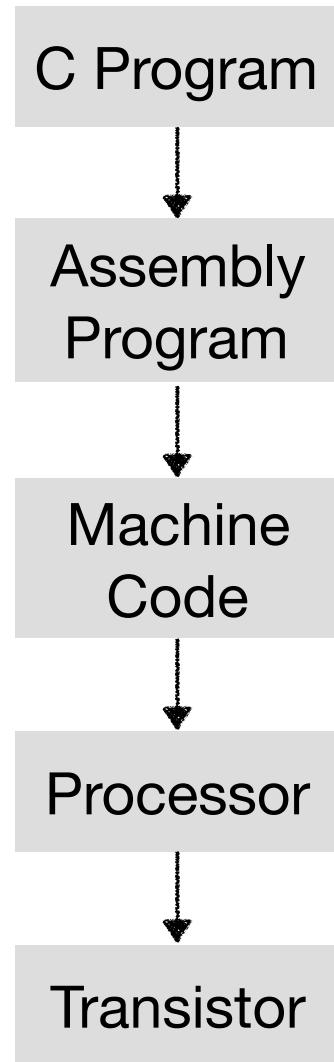


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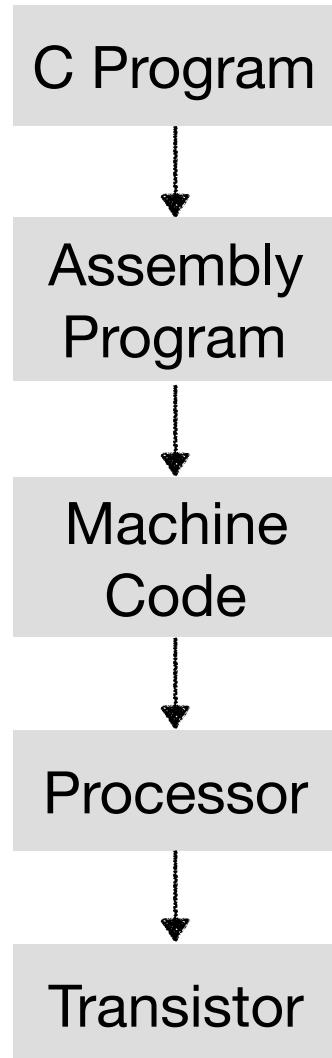
High-Level
Language



So far in 252...

High-Level Language

Instruction Set Architecture (ISA)

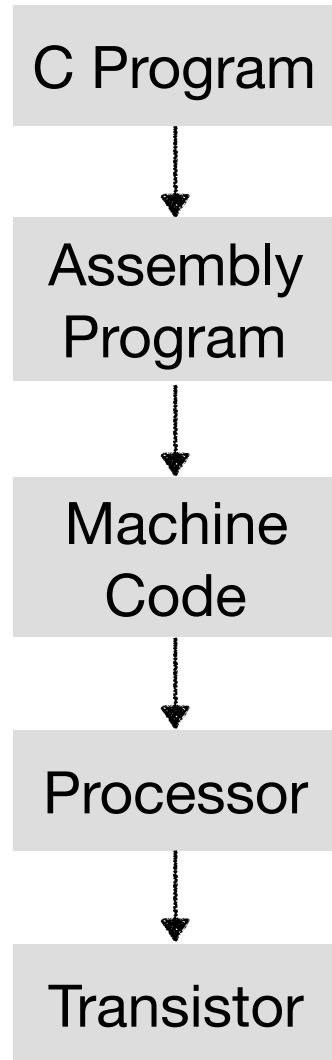


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 - Provide all info for someone wants to write assembly/machine code
 - “Contract” between assembly/machine code and processor

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High-Level Language

Instruction Set Architecture (ISA)



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- Processors execute machine code (binary). Assembly program is merely a text representation of machine code

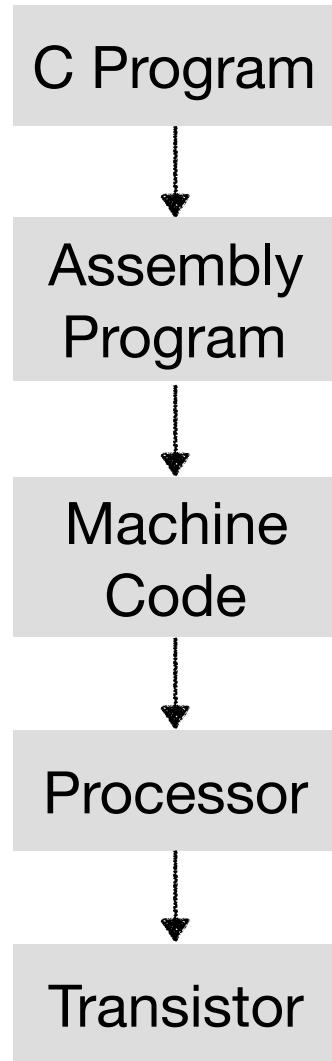
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High-Level Language

Instruction Set Architecture (ISA)

Microarchitecture

Circuit



- **ISA:** Software programmers' view of a computer
 - Provide all info for someone wants to write assembly/machine code
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- Processors execute machine code (binary). Assembly program is merely a text representation of machine code
- **Microarchitecture:** Hardware implementation of the ISA (with the help of circuit technologies)

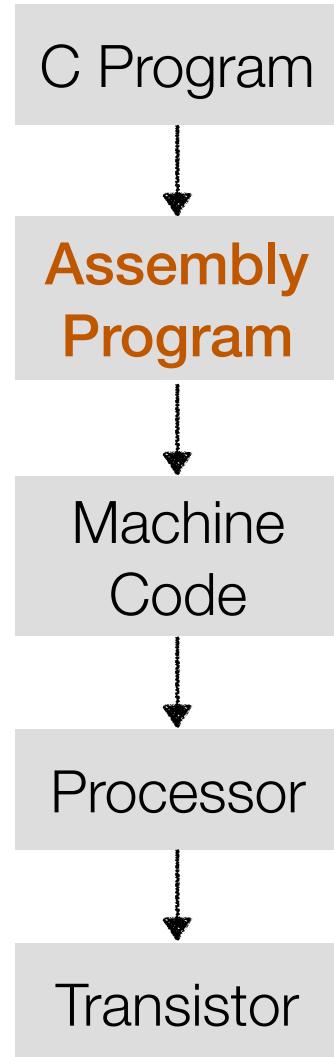
This Module (4 Lectures)

High-Level
Language

Instruction Set
Architecture
(ISA)

Microarchitecture

Circuit



- Assembly Programming
 - Explain how various C constructs are implemented in assembly code
 - Effectively translating from C to assembly program manually
 - Helps us understand how compilers work
 - Helps us understand how assemblers work
- Microarchitecture is the topic of the next module

Today: Assembly Programming I: Basics

- Different ISAs and history behind them
- C, assembly, machine code
- Move operations (and addressing modes)

Instruction Set Architecture

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 - x86, ARM, Power/PowerPC, Sparc, MIPS, IA64, z
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 - Intel and AMD have different microarchitectures for x86
- ISA is lucrative business: ARM's Business Model
 - Patent the ISA, and then license the ISA
 - Every implementer pays a royalty to ARM
 - Apple/Samsung pays ARM whenever they sell a smartphone

The ARM Diaries, Part 1: How ARM's Business Model Works: <https://www.anandtech.com/show/7112/the-arm-diaries-part-1-how-arms-business-model-works>

Intel x86 ISA

- Dominate laptop/desktop/cloud market

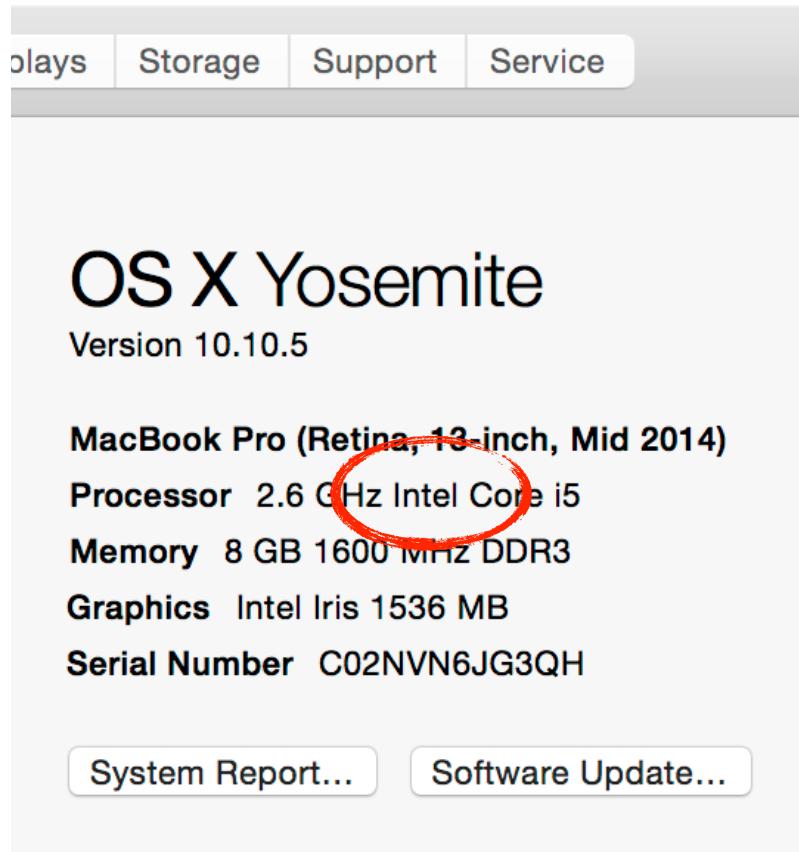
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Intel x86 ISA Evolution (Milestones)

- Evolutionary design: Added more features as time goes on

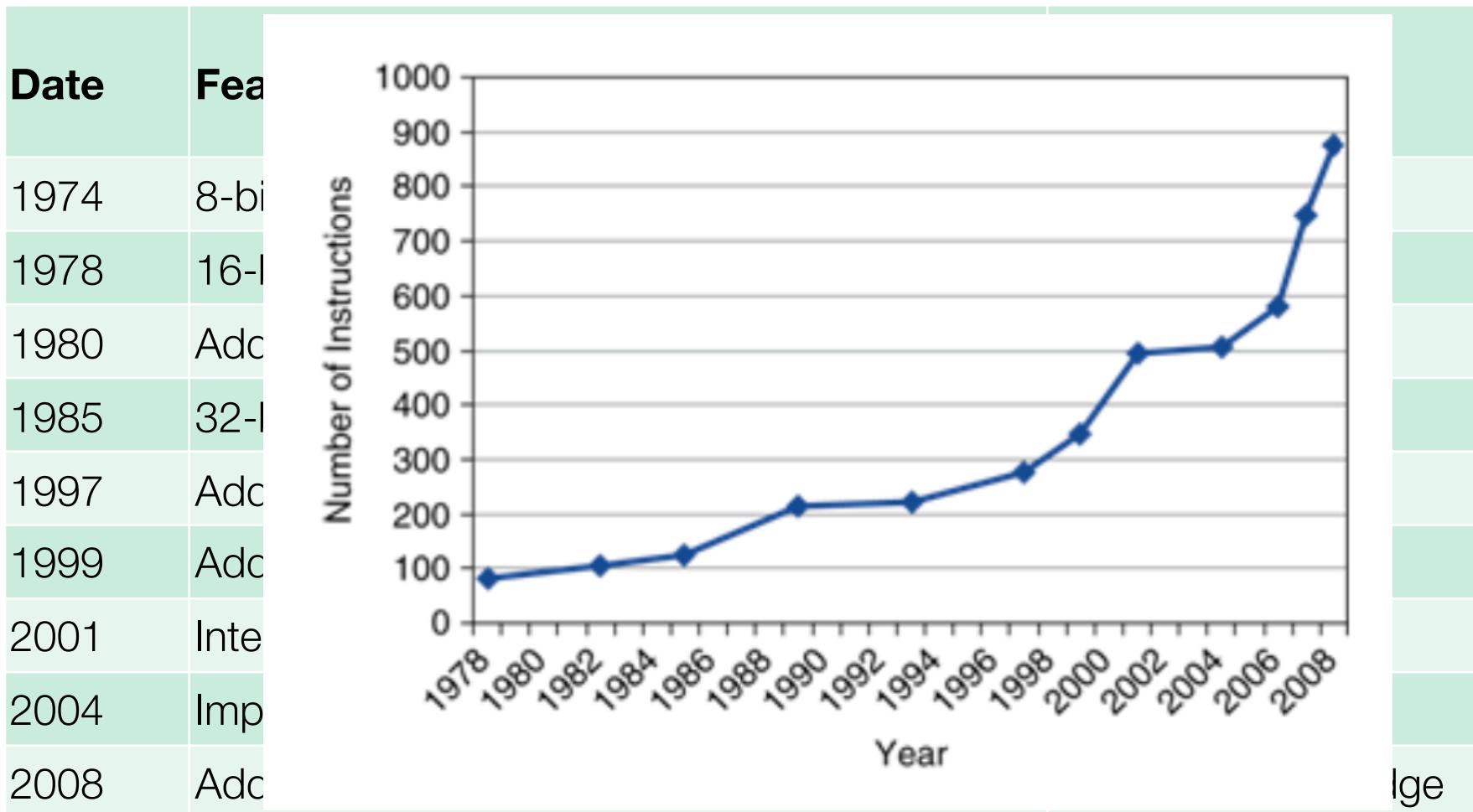
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Date	Feature	Notable Implementation
1974	8-bit ISA	8080
1978	16-bit ISA (Basis for IBM PC & DOS)	8086
1980	Add Floating Point instructions	8087
1985	32-bit ISA (Refer to as IA32)	386
1997	Add Multi-Media eXtension (MMX)	Pentium/MMX
1999	Add Streaming SIMD Extension (SSE)	Pentium III
2001	Intel's first attempt at 64-bit ISA (IA64, failed)	Itanium
2004	Implement AMD's 64-bit ISA (x86-64, AMD64)	Pentium 4E
2008	Add Advanced Vector Extension (AVE)	Core i7 Sandy Bridge

Intel x86 ISA Evolution (Milestones)

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Backward Compatibility

- Binary executable generated for an older processor can execute on a newer processor
- Allows legacy code to be executed on newer machines
 - Buy new machines without changing the software
- x86 is backward compatible up until 8086 (16-bit ISA)
 - i.e., an 8086 binary executable can be executed on any of today's x86 machines
- Great for users, nasty for processor implementers
 - Every instruction you put into the ISA, you are stuck with it *FOREVER*

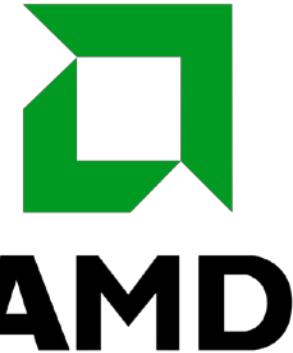
x86 Clones: Advanced Micro Devices (AMD)

- Historically

- AMD build processors for x86 ISA
- A little bit slower, a lot cheaper

- Then

- Recruited top circuit designers from Digital Equipment Corp. and other downward trending companies
- Developed x86-64, their own 64-bit x86 extension to IA32
- Built first 1 GHz CPU
- Intel felt hard to admit mistake or that AMD was better
- 2004: Intel Announces EM64T extension to IA32
 - Almost identical to x86-64!
 - Today's 64-bit x86 ISA is basically AMD's original proposal



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Our Coverage

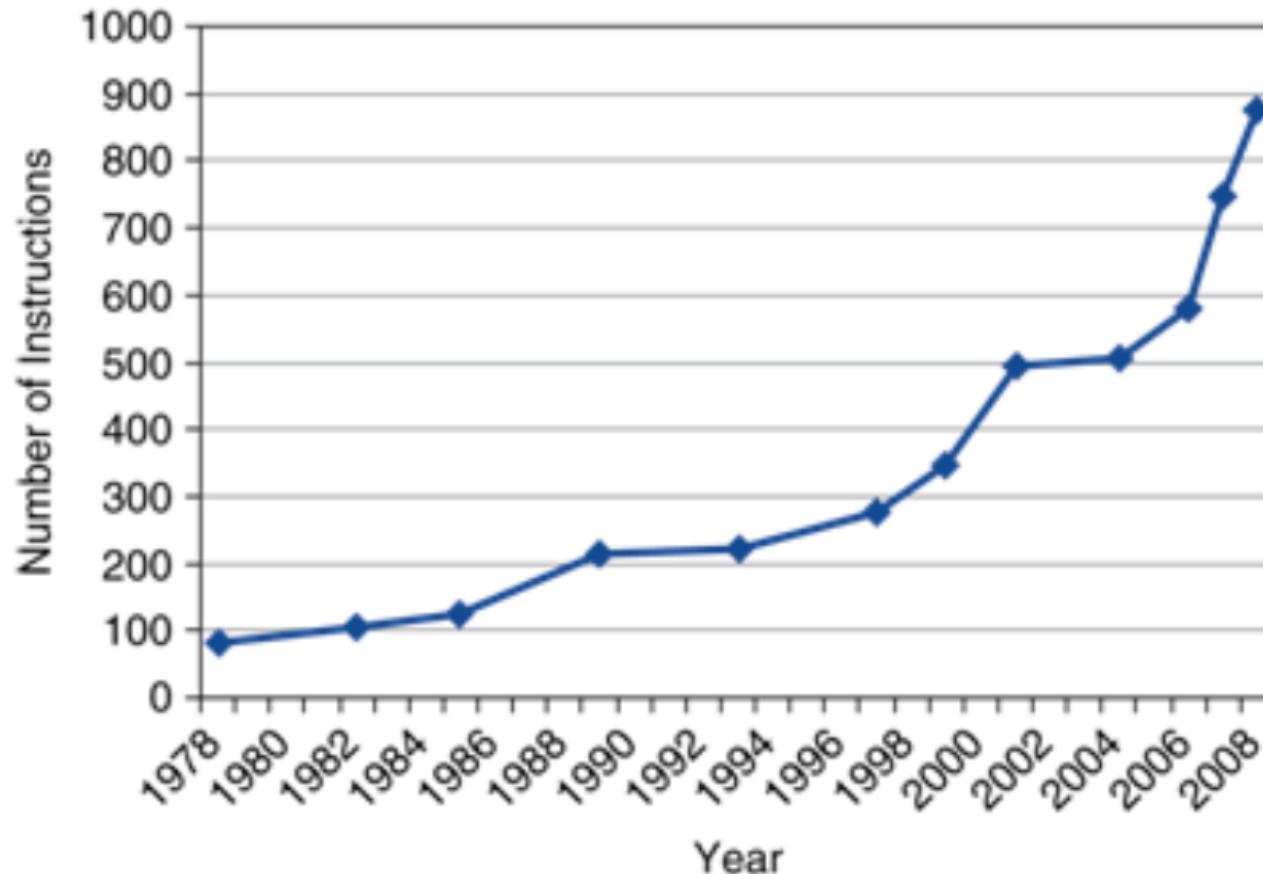
- IA32
 - The traditional x86
 - 2nd edition of the textbook
- x86-64
 - The standard
 - CSUG machine
 - 3rd edition of the textbook
 - Our focus

Moore's Law

- More instructions typically require more transistors to implement

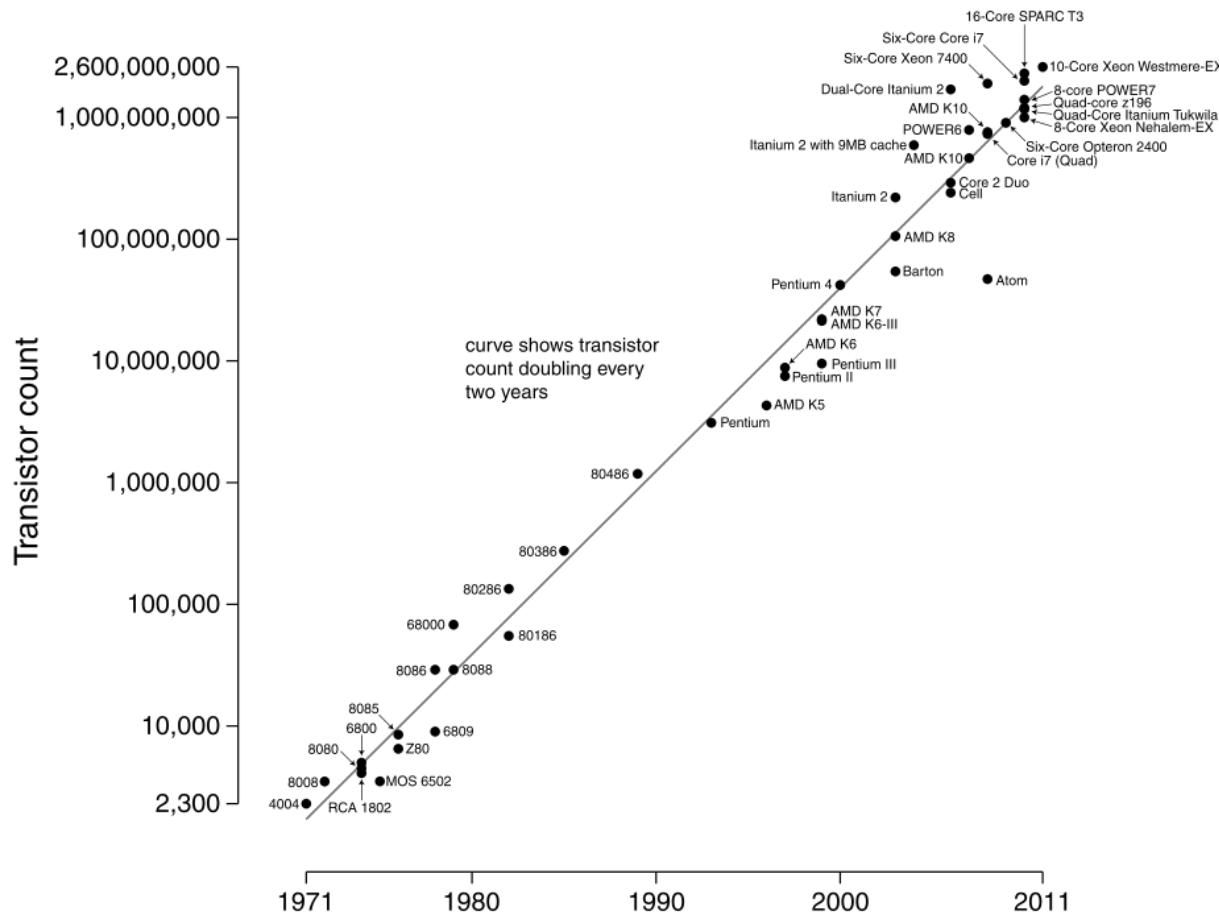
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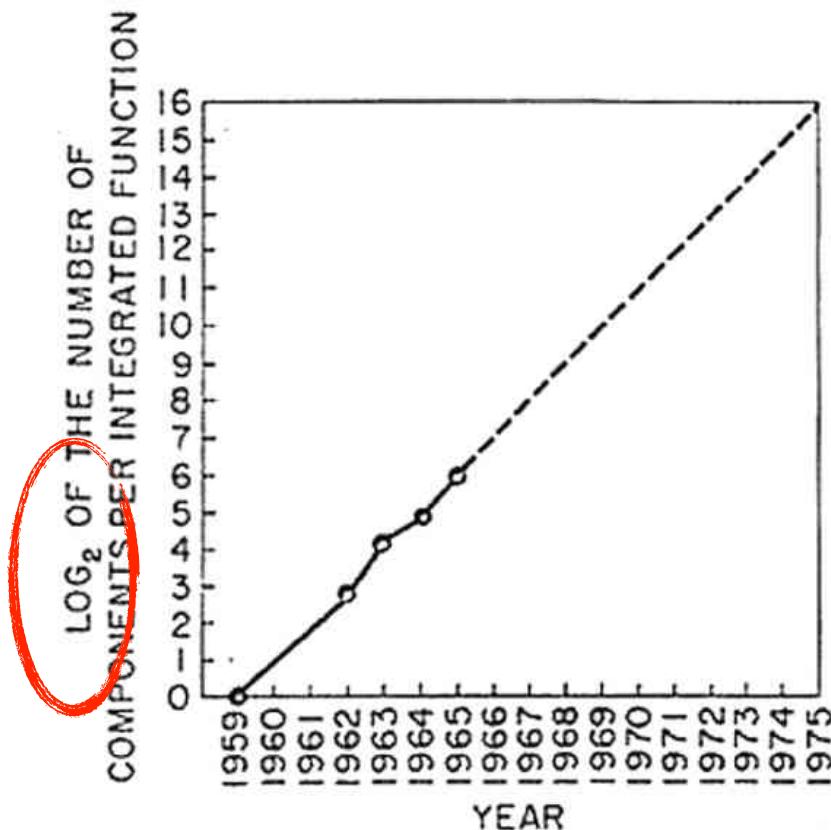
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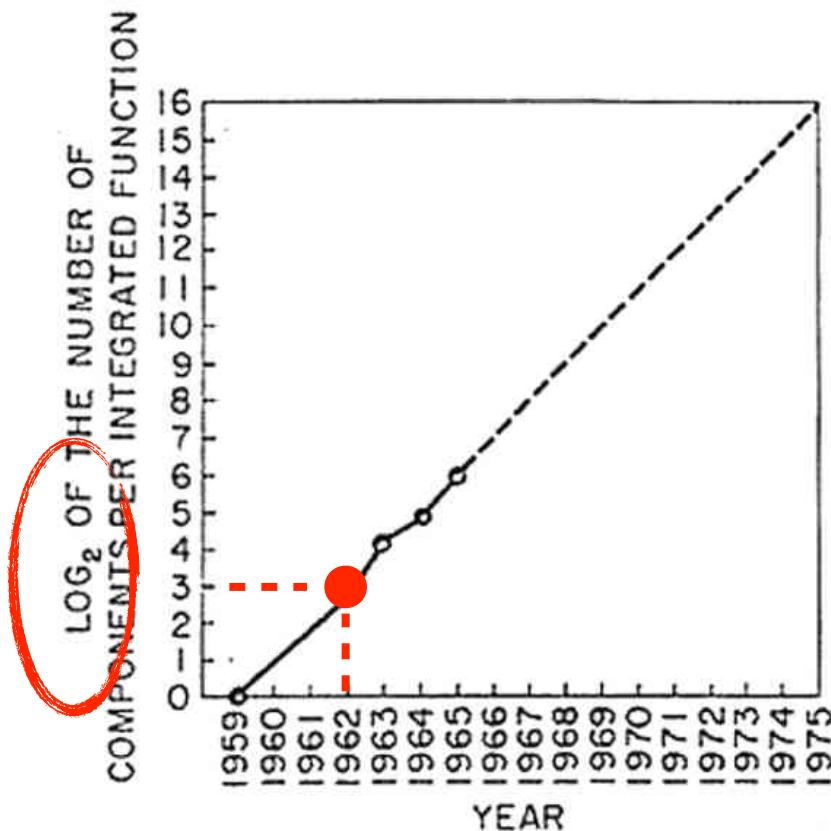
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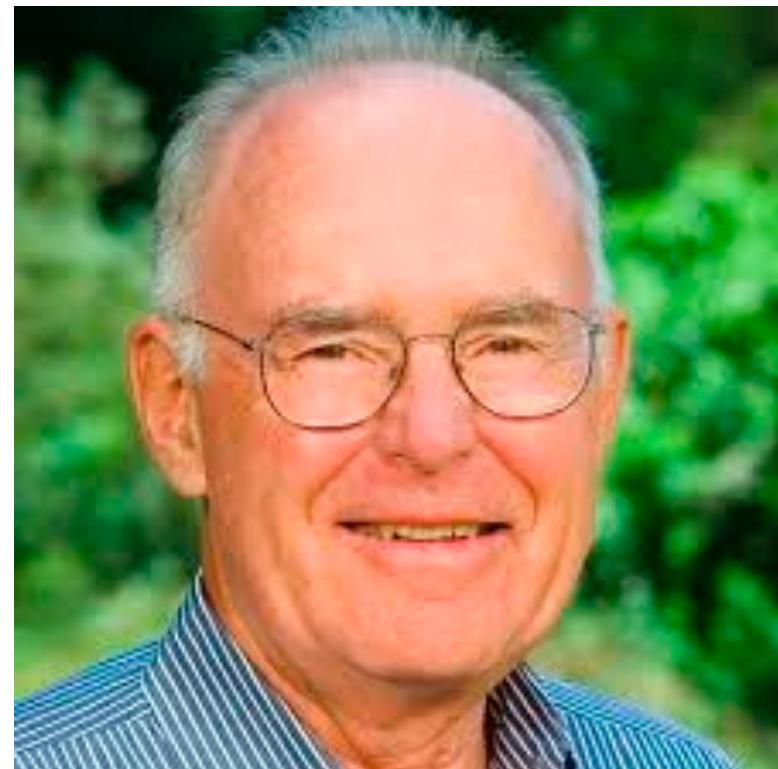
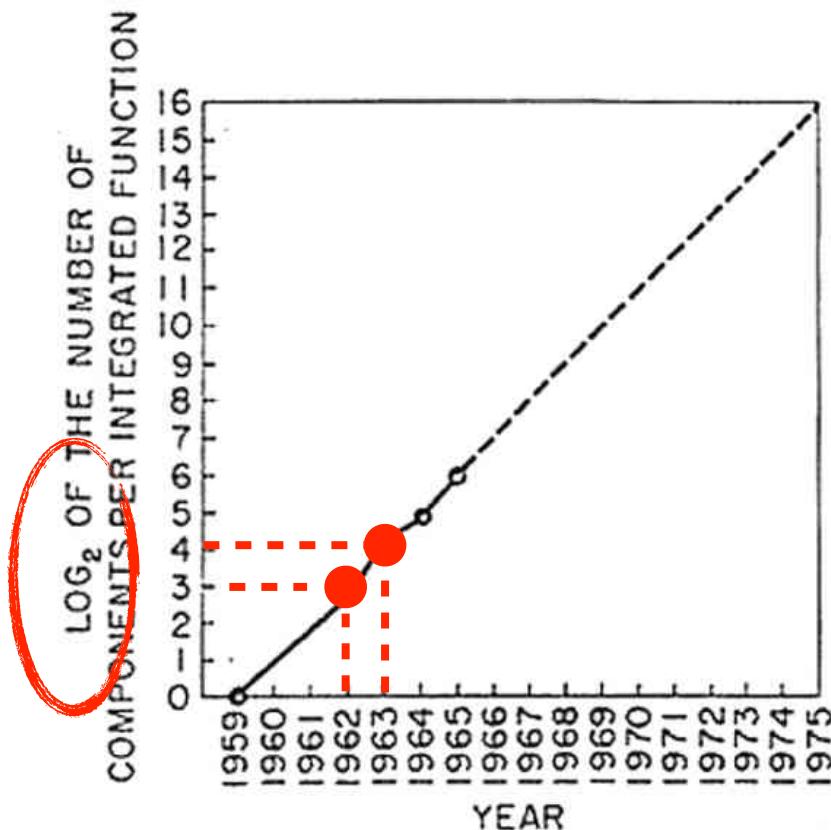
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- Gordon Moore in 1965 predicted that the number of transistors doubles every year
- In 1975 he revised the prediction to doubling every 2 years
- Today's widely-known Moore's Law: number of transistors double about every 18 months
 - Moore never used the number 18...

Moore's Law

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Moore's Law

ars

TECHNICA

BIZ & IT

TECH

SCIENCE

POLICY

CARS

GAMING & CULTURE

TECH —

Transistors will stop shrinking in 2021, but Moore's law will live on

Final semiconductor industry roadmap says the future is 3D packaging and cooling.

The first problem has been known about for a long while. Basically, starting at around the 65nm node in 2006, the economic gains from moving to smaller transistors have been slowly dribbling away. Previously, moving to a smaller node meant you could cram tons more chips onto a single silicon wafer, at a reasonably small price increase. With recent nodes like 22 or 14nm, though, there are so many additional steps required that it costs a lot more to manufacture a completed wafer—not to mention additional costs for things like package-on-package (PoP) and through-silicon vias (TSV) packaging.

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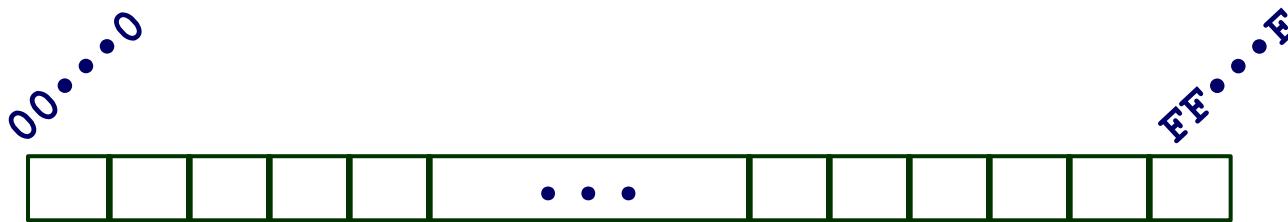
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- Memory, C, assembly, machine code
- Move operations (and addressing modes)

Byte-Oriented Memory Organization



- Programs refer to data by address
 - Conceptually, envision it as a very large array of bytes: **byte-addressable**
 - An address is like an index into that array
 - and, a pointer variable stores an address

How Does Pointer Work in C???

```
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char b = 3;  
char* c;  
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0x11

...

0x16

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- The ‘&’ operator (address-of operator) returns the memory address of a variable.
- The ‘*’ operator returns the content stored at the memory location pointed by the pointer variable (dereferencing)

C Variable	Memory Content	Memory Address
a	4	0x10
b	3	0x11
	...	
c	0x10	0x16
	...	

How Does Pointer Work in C???

```
char a = 4;  
char b = 3;  
char* c;  
c = &a;  
→ b += (*c);
```

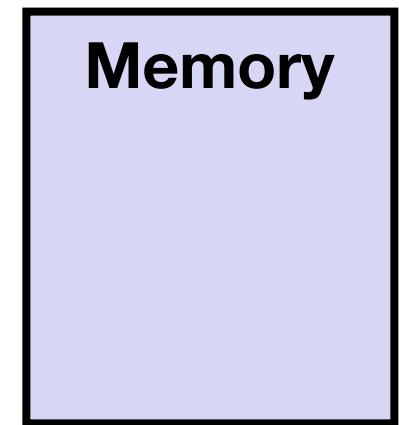
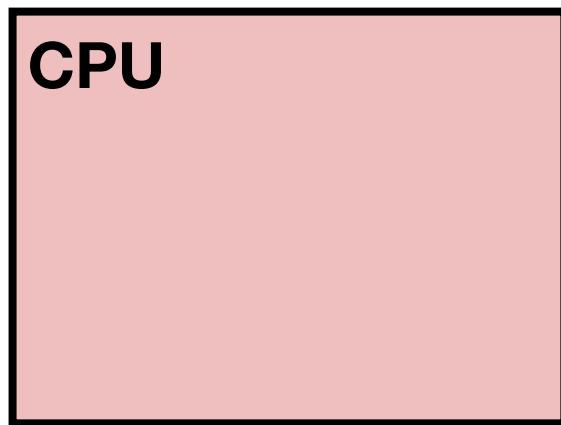
- The content of a pointer variable is memory address.
- The ‘&’ operator (address-of operator) returns the memory address of a variable.
- The ‘*’ operator returns the content stored at the memory location pointed by the pointer variable (dereferencing)

C Variable	Memory Content	Memory Address
a	4	0x10
b	7	0x11
	...	
c	0x10	0x16
	...	

Assembly Code's View of Computer: ISA

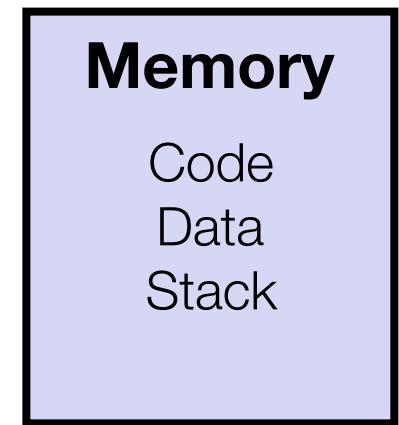
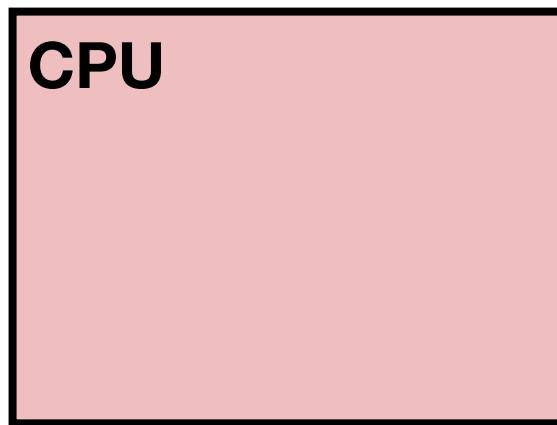
Assembly Code's View of Computer: ISA

Assembly
Programmer's
Perspective
of a Computer



Assembly Code's View of Computer: ISA

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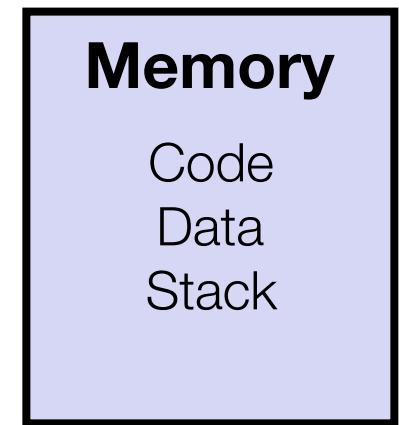
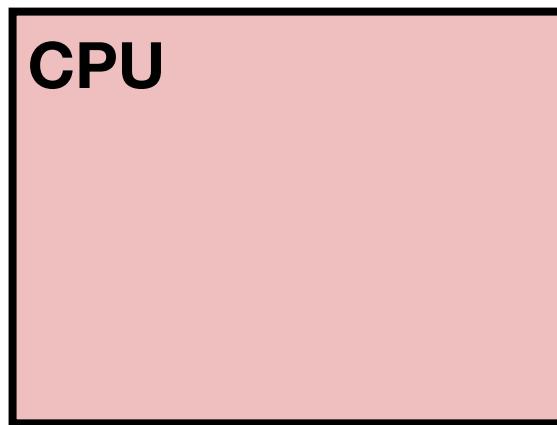


- (Byte Addressable) Memory

- Code: instructions
- Data
- Stack to support function call

Assembly Code's View of Computer: ISA

Assembly
Programmer's
Perspective
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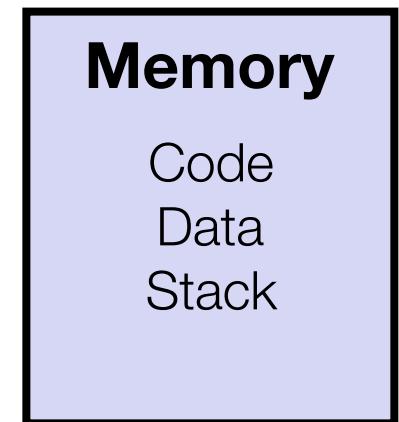
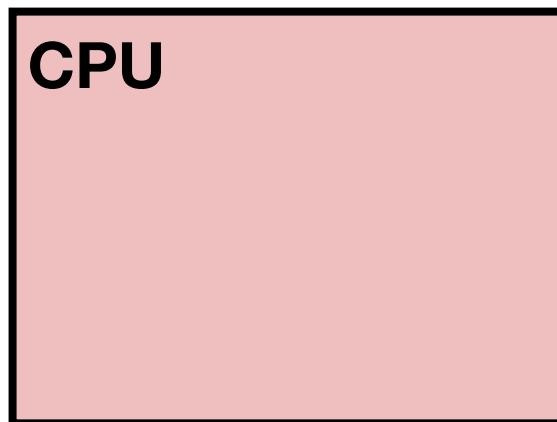
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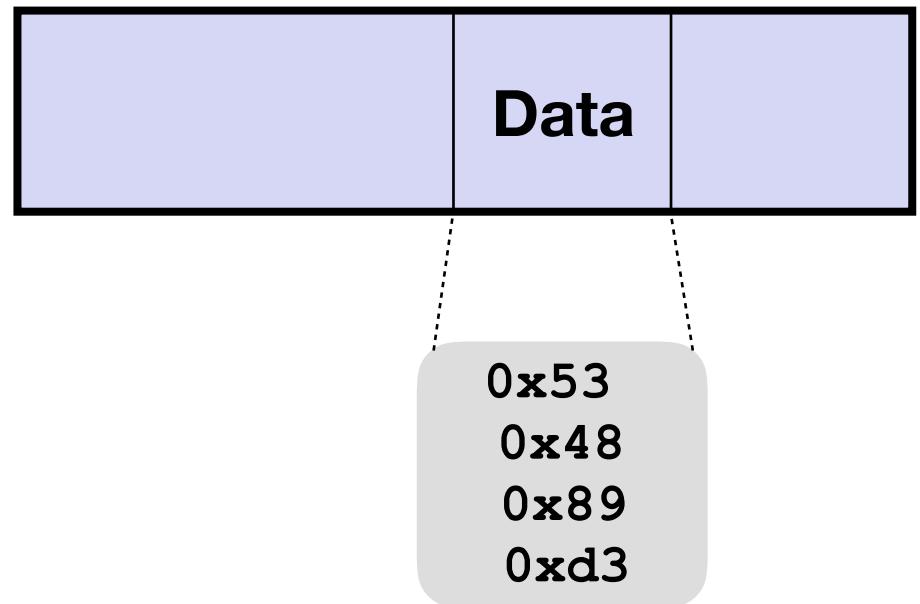
Assembly Code's View of Computer: ISA

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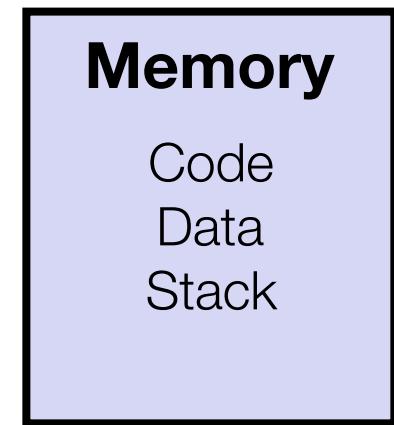
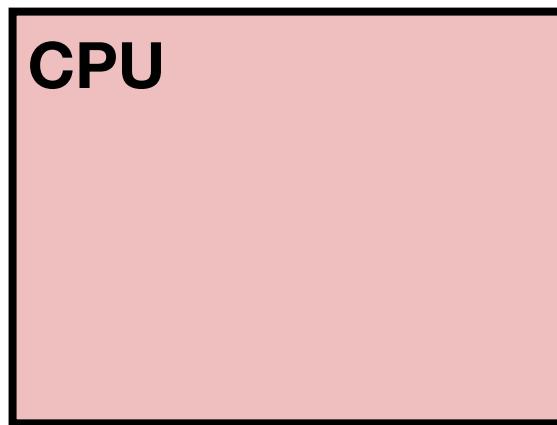
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Assembly Code's View of Computer: ISA

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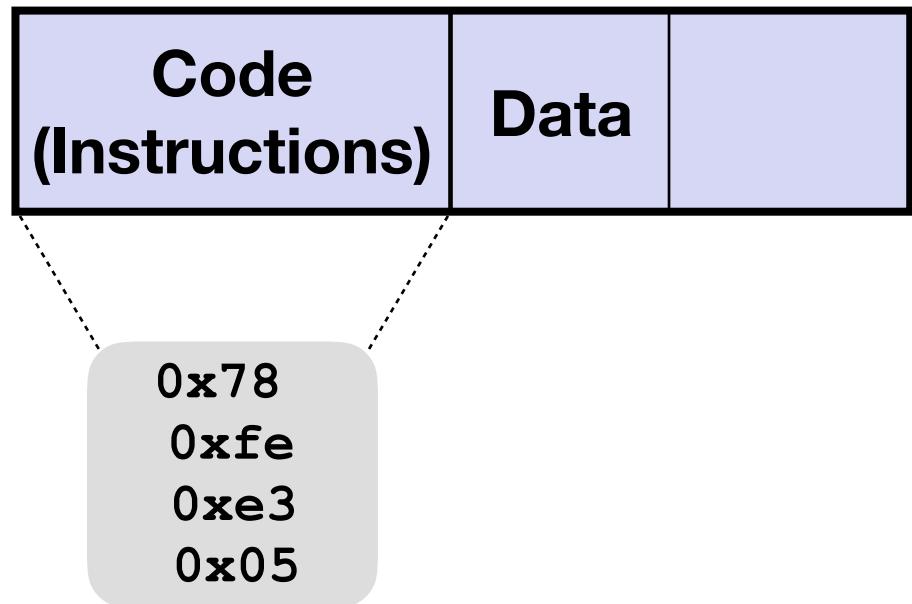


- (Byte Addressable) Memory

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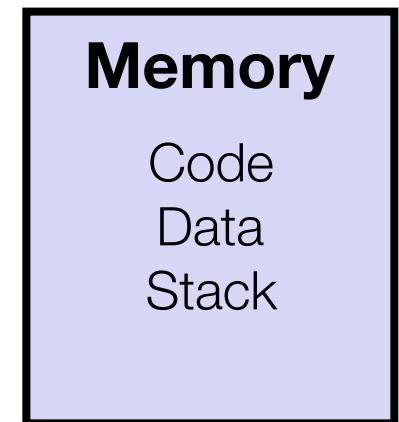
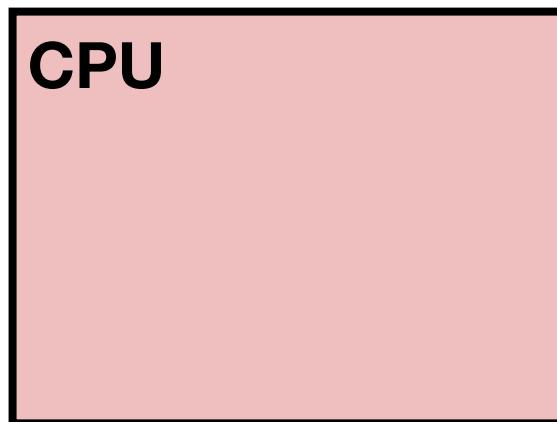
Instruction is the fundamental unit of work.

All instructions are coded as bits (just like data!)



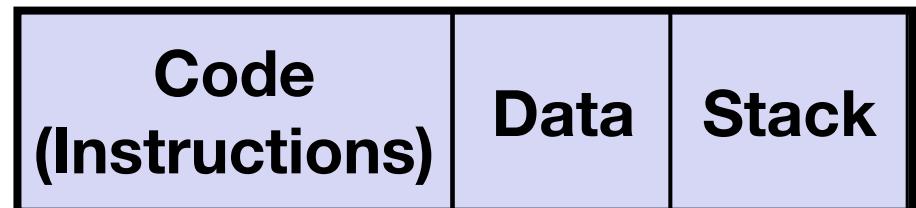
Assembly Code's View of Computer: ISA

Assembly
Programmer's
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- (Byte Addressable) Memory

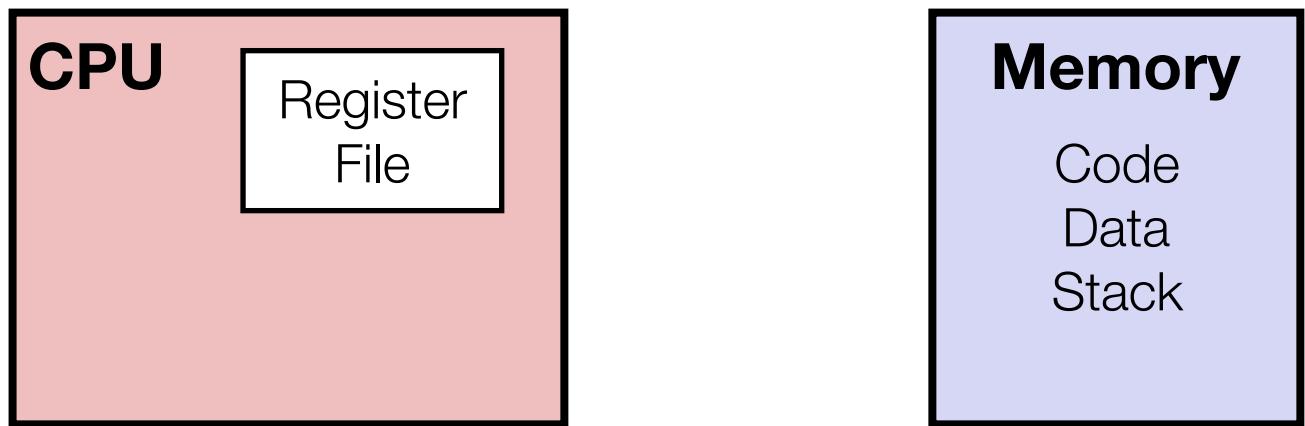
- Code: instructions
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0x53
0x48
0x89
0xd3

Assembly Code's View of Computer: ISA

Assembly
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- (Byte Addressable) Memory
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x86-64 Integer Register File

← 8 Bytes →

%rax

%rbx

%rcx

%rdx

%rsi

%rdi

%rsp

%rbp

%r8

%r9

%r10

%r11

%r12

%r13

%r14

%r15

x86-64 Integer Register File

- Lower-half of each register can be independently addressed (until 1 bytes)

x86-64 Integer Register File

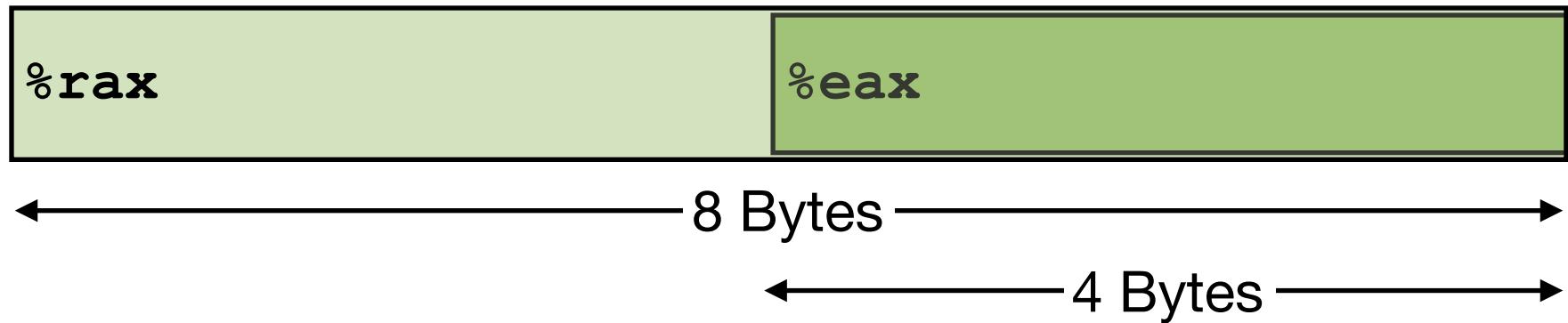
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`%rax`

8 Bytes

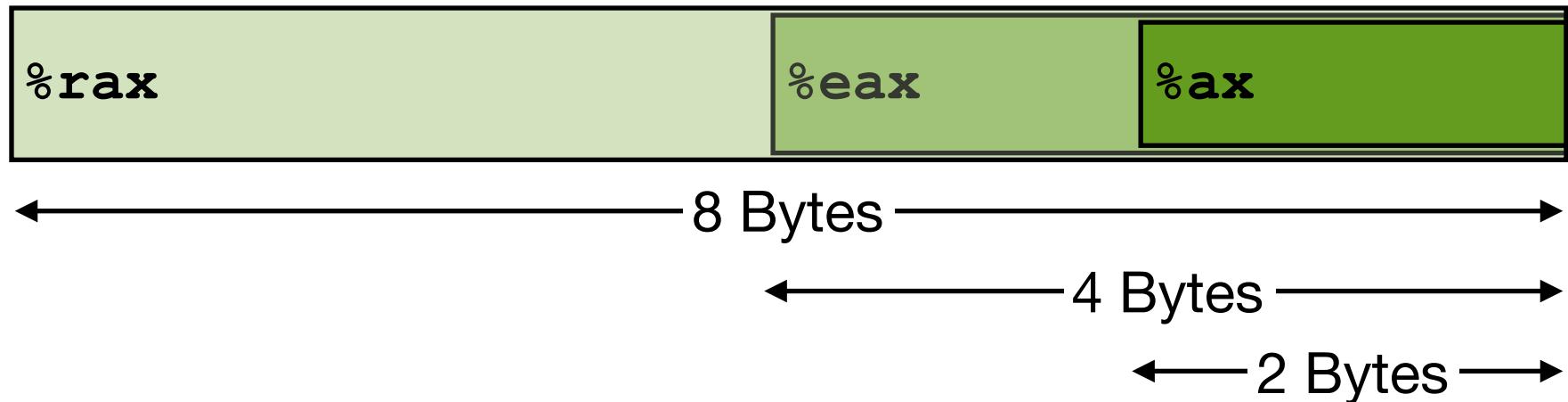
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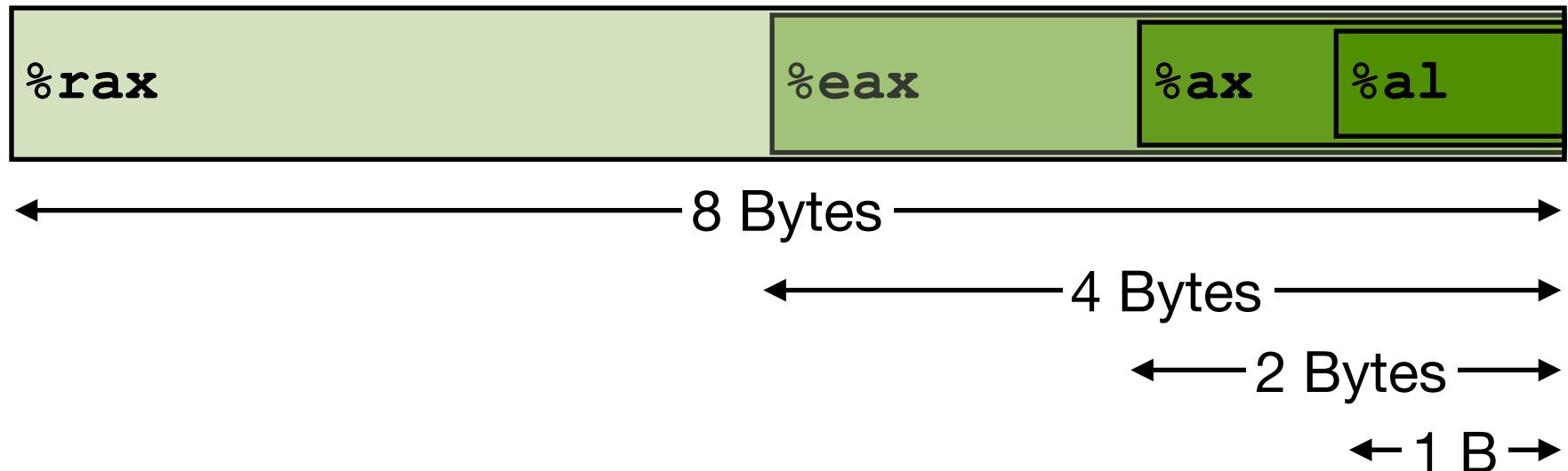
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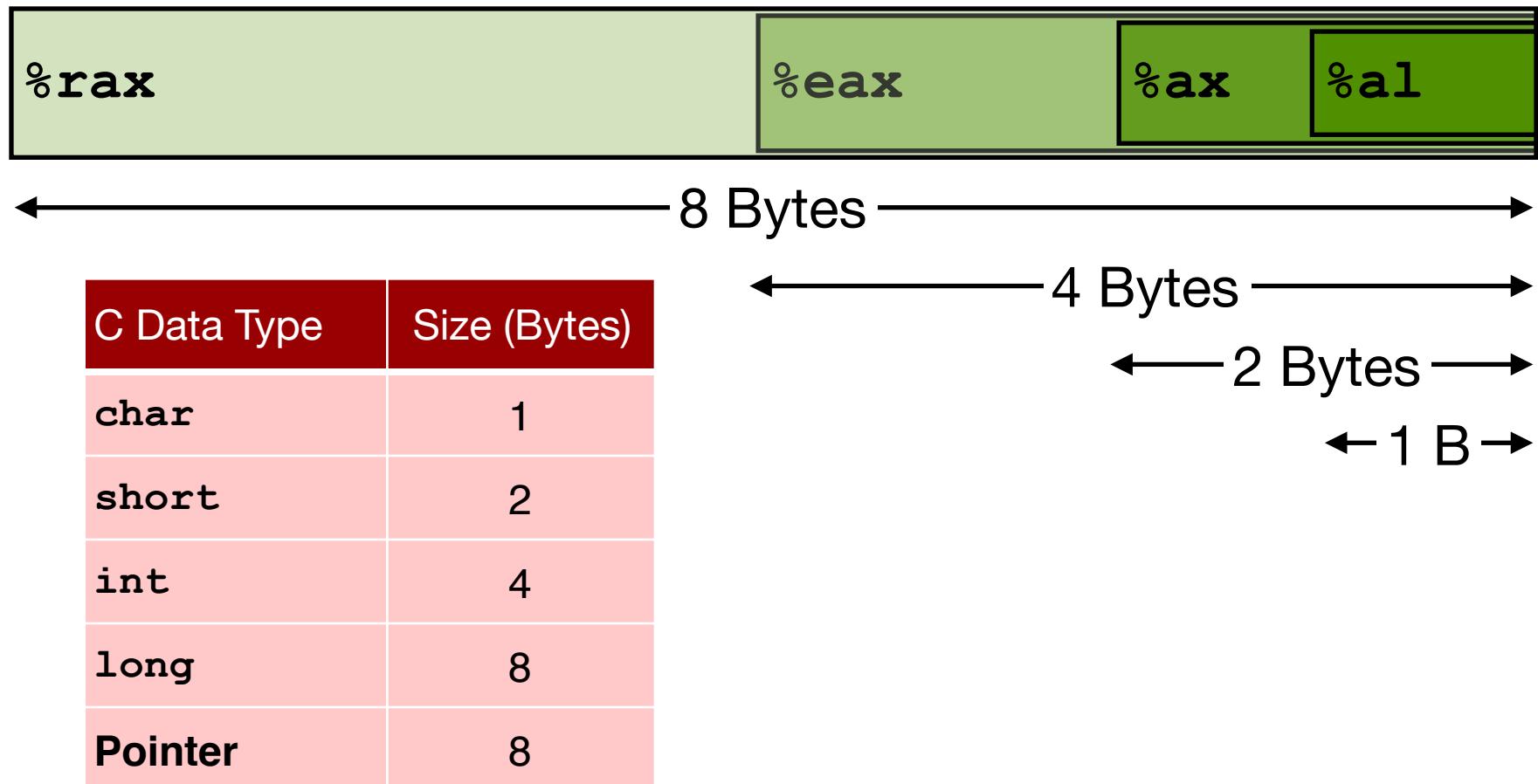
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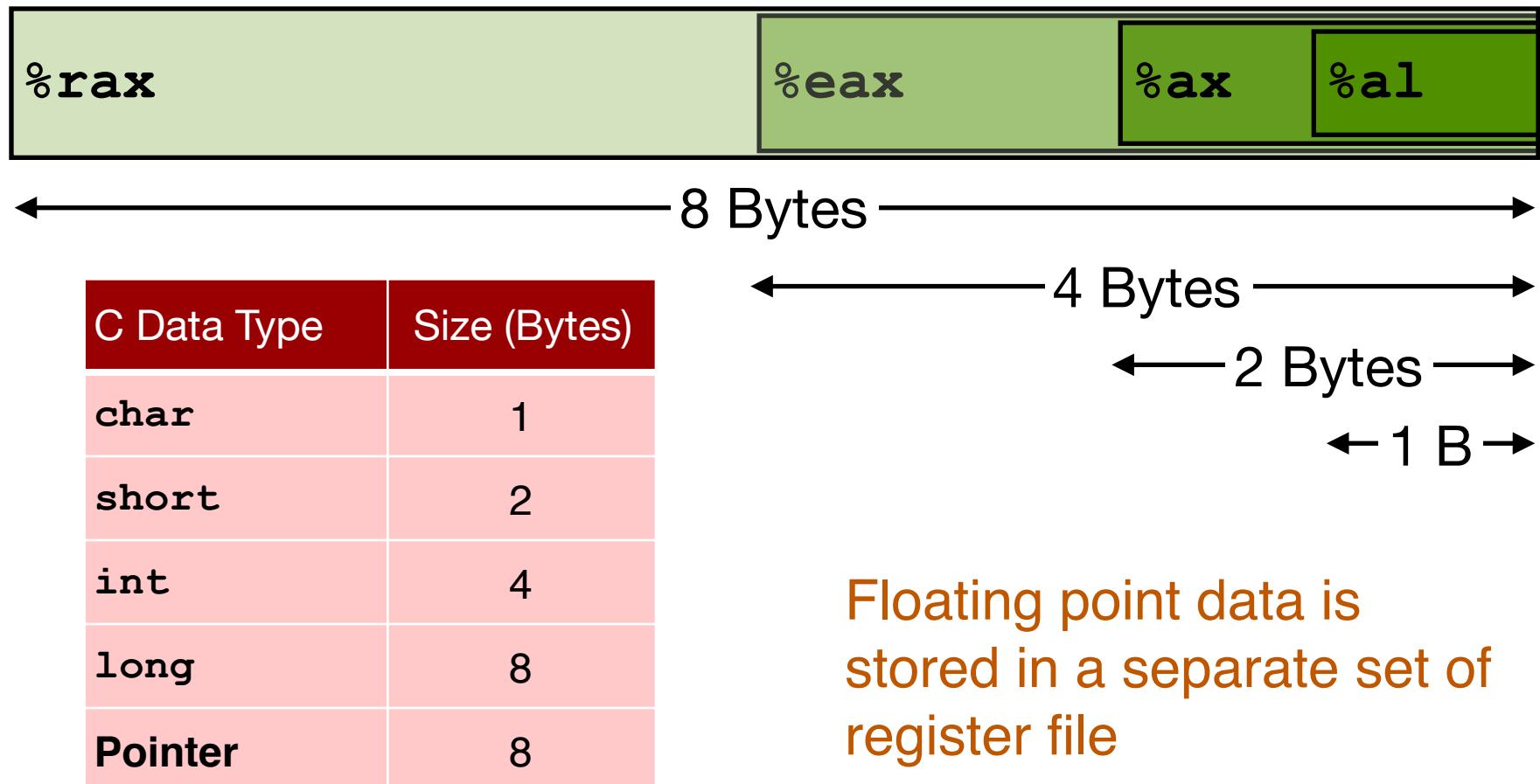
x86-64 Integer Register File

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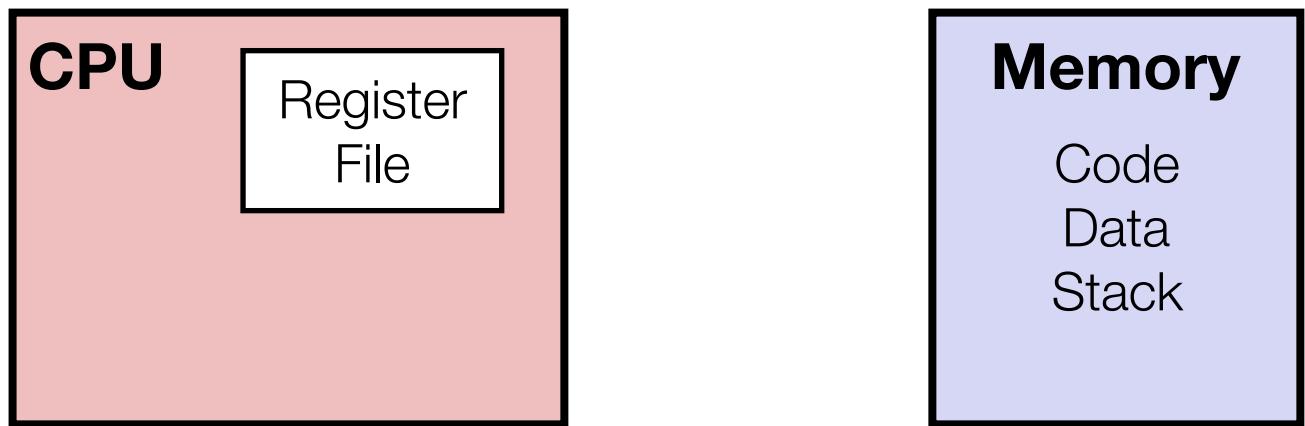
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Assembly Code's View of Computer: ISA

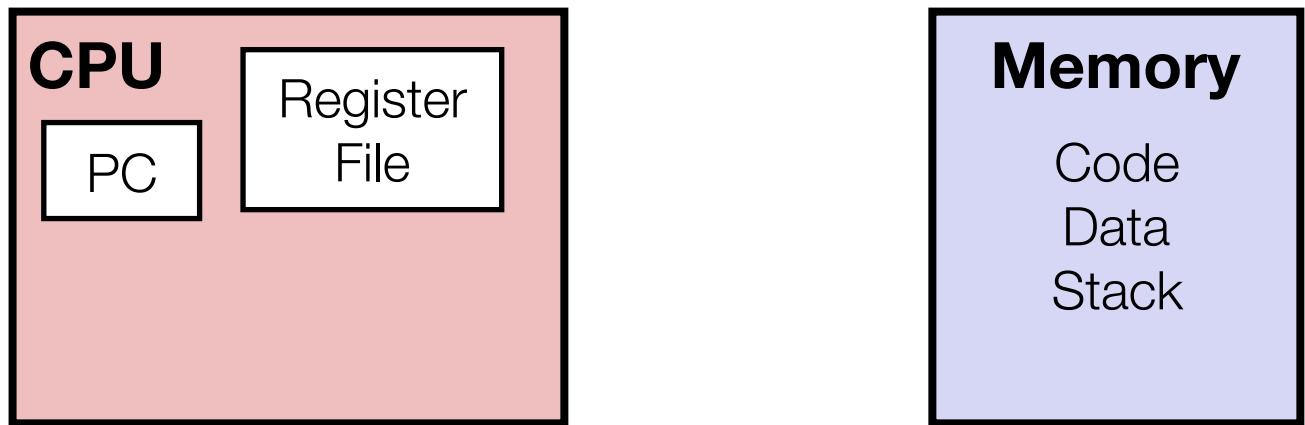
Assembly
Programmer's
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- (Byte Addressable) Memory
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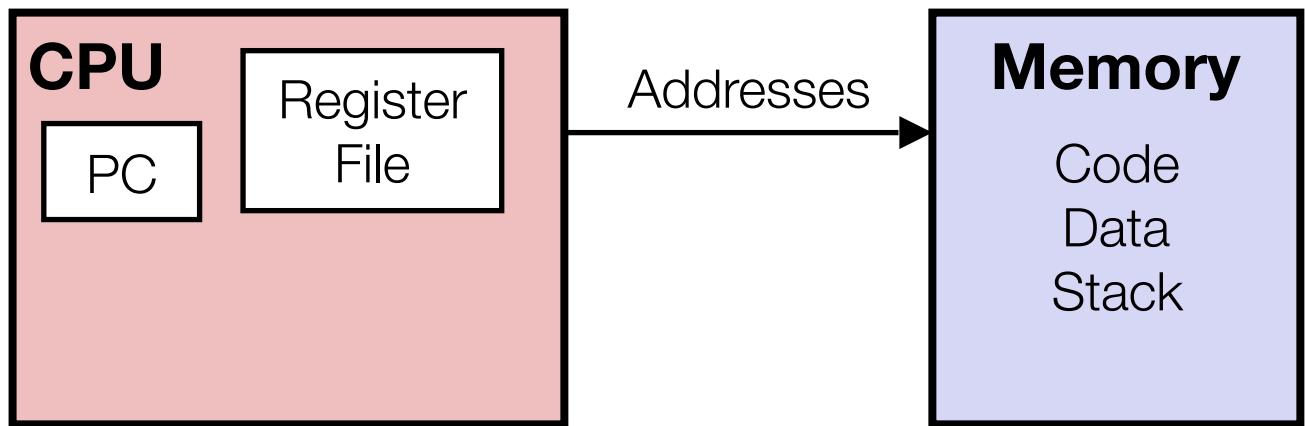
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 - A special register containing address of next instruction
 - Called “RIP” in x86-64

Assembly Code's View of Computer: ISA

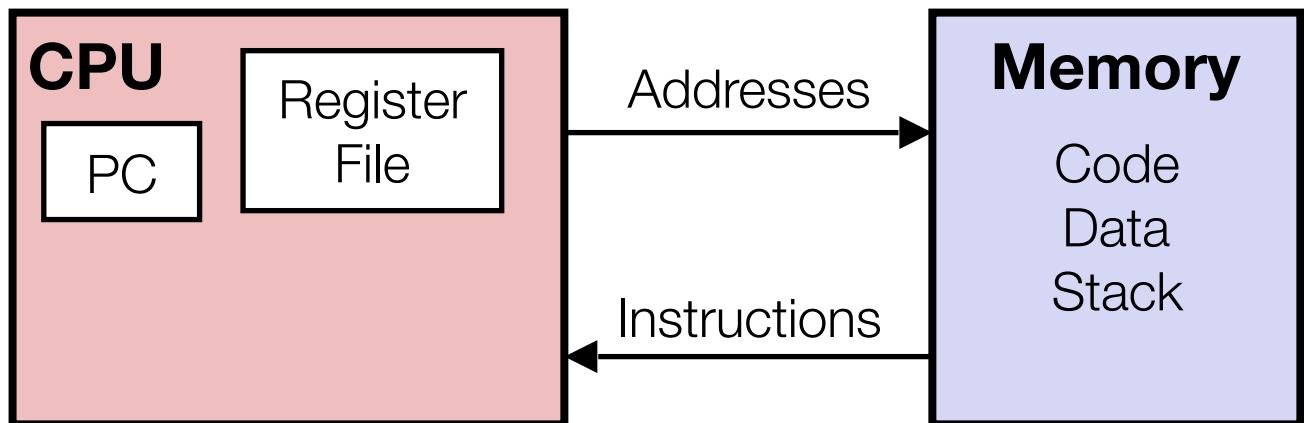
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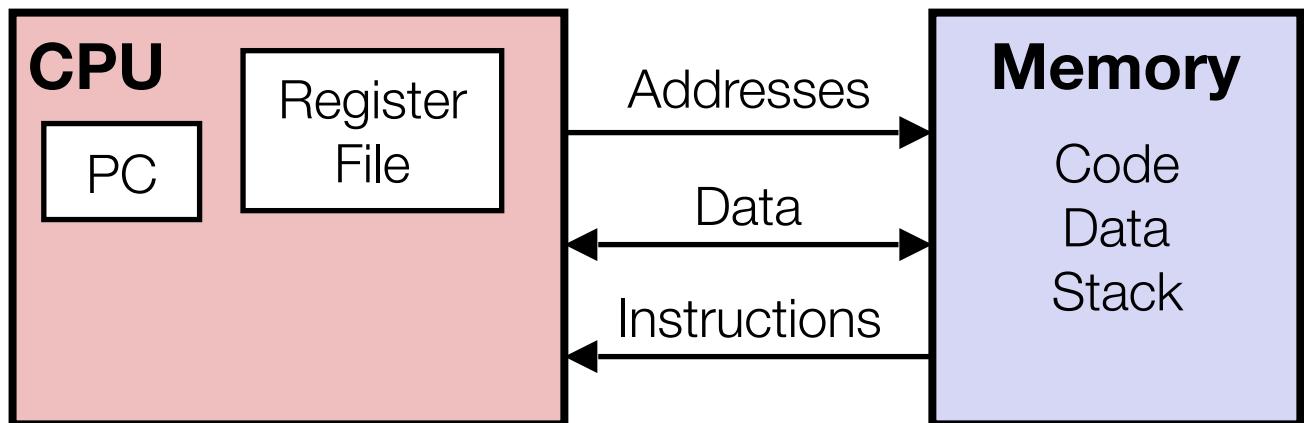
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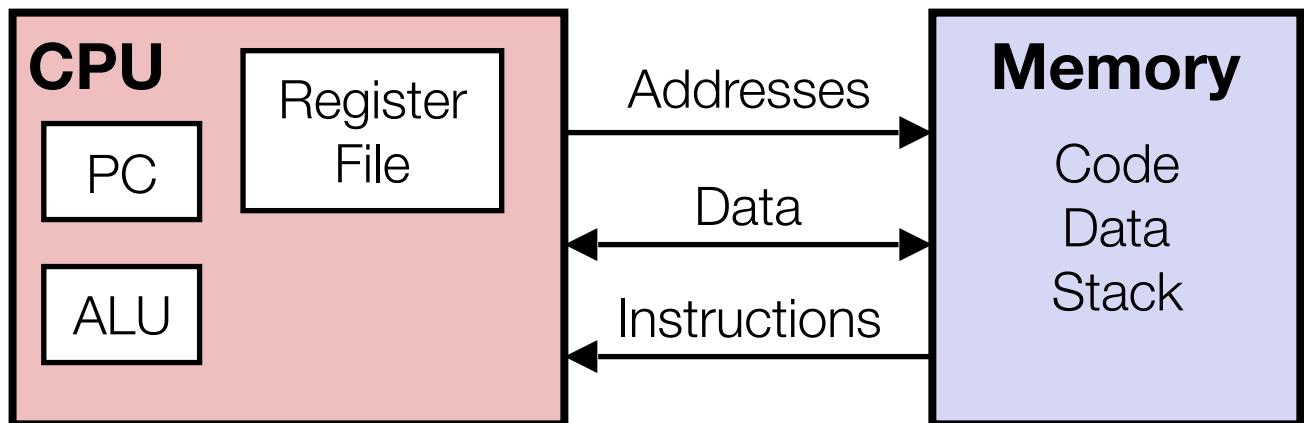
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Assembly Code's View of Computer: ISA

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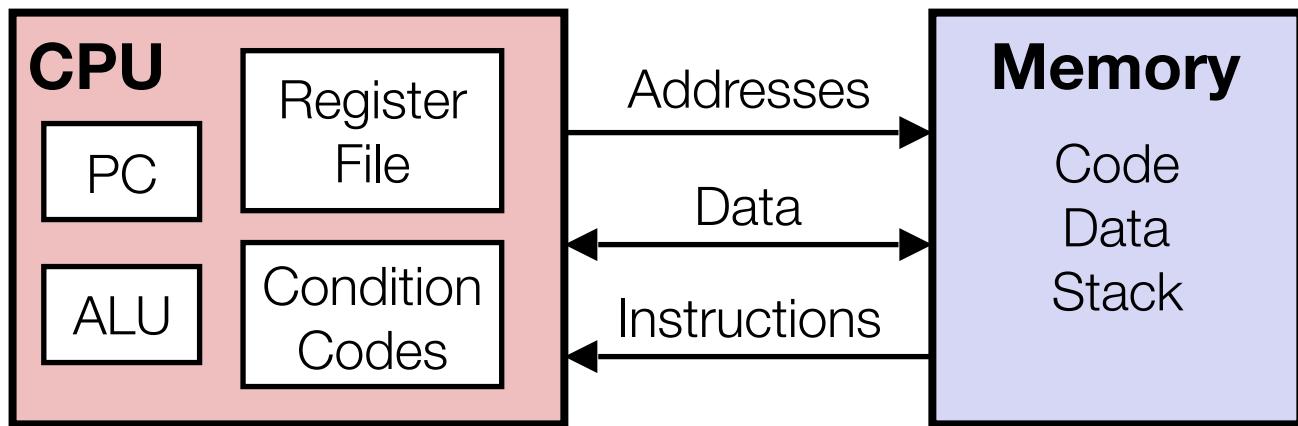


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- Arithmetic logic unit (ALU)
 - Where computation happens

Assembly Code's View of Computer: ISA

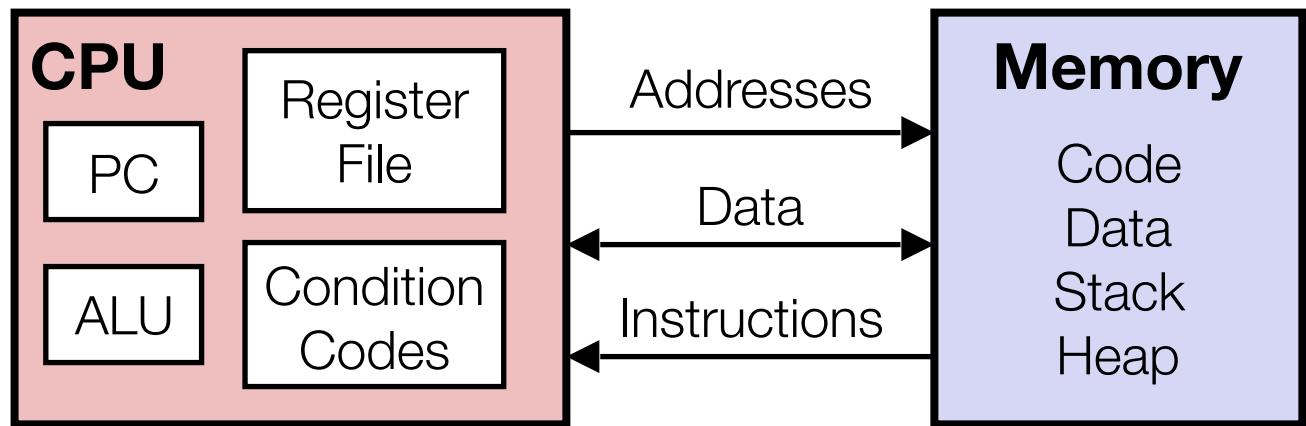
Assembly
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- Arithmetic logic unit (ALU)
 - Where computation happens
- Condition codes
 - Store status information about most recent arithmetic or logical operation
 - Used for conditional branch

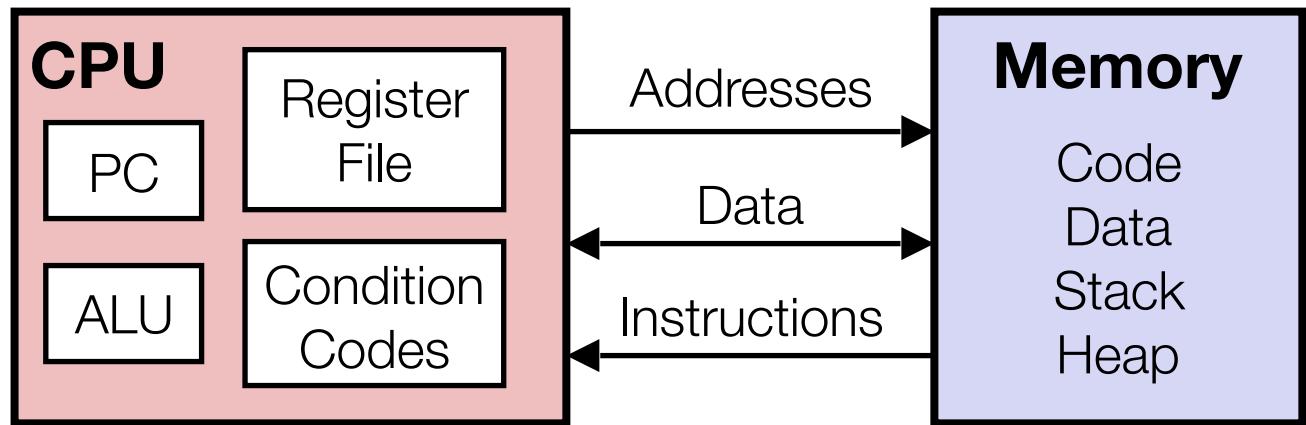
Assembly Program Instructions

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Assembly Program Instructions

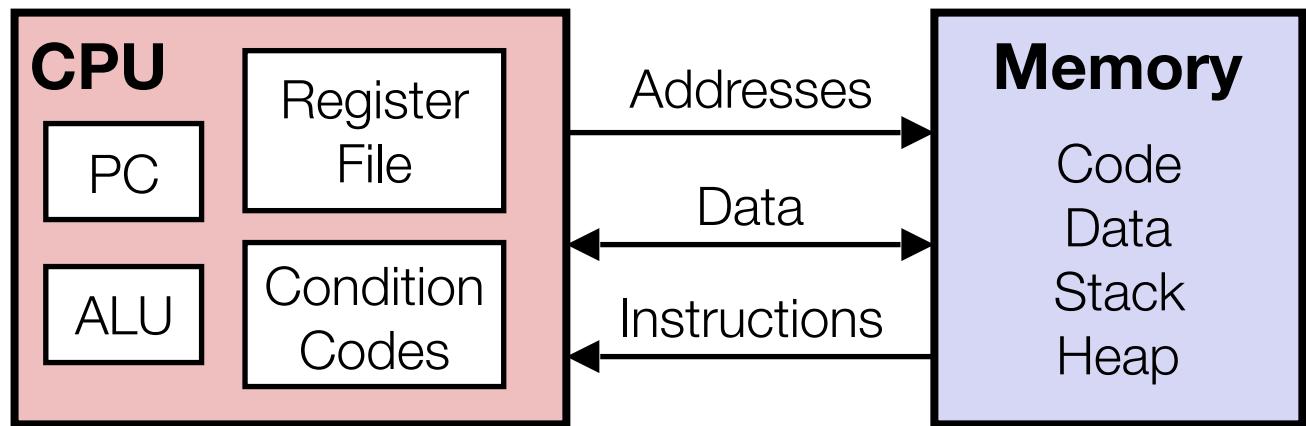
Assembly
Programmer's
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- *Compute Instruction*: Perform arithmetics on register or memory data
 - `addq %eax, %ebx`
 - C constructs: +, -, >>, etc.

Assembly Program Instructions

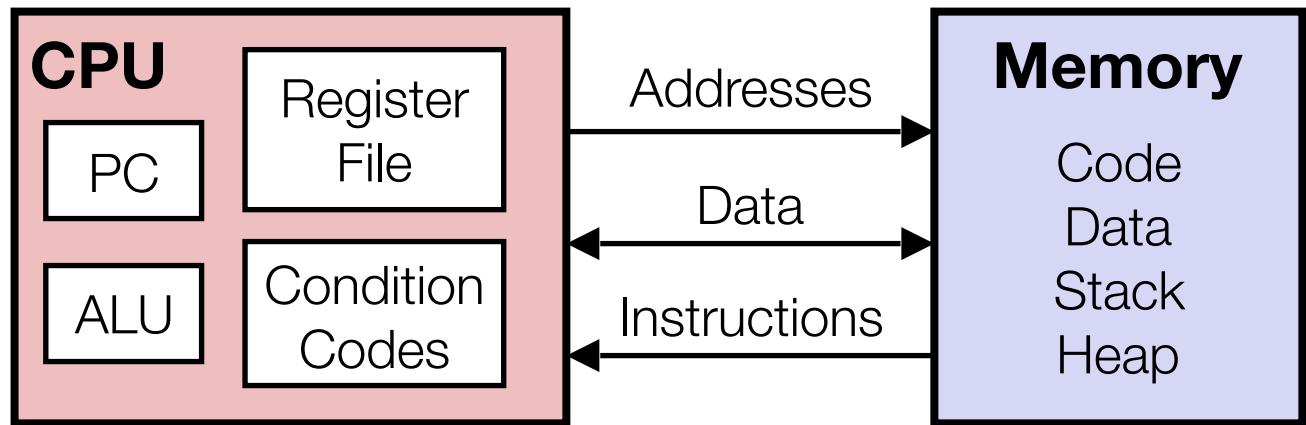
Assembly
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- *Data Movement Instruction*: Transfer data between memory and register
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Assembly Program Instructions

Assembly
Programmer's
Perspective
of a Computer



- **Compute Instruction:** Perform arithmetics on register or memory data
 - `addq %eax, %ebx`
 - C constructs: +, -, >>, etc.
- **Data Movement Instruction:** Transfer data between memory and register
 - `movq %eax, (%ebx)`
- **Control Instruction:** Alter the sequence of instructions (by changing PC)
 - `jmp, call`
 - C constructs: `if-else`, `do-while`, function call, etc.

Turning C into Object Code

C Code (sum.c)

```
long plus(long x, long y);

void sumstore(long x, long y,
              long *dest)
{
    long t = plus(x, y);
    *dest = t;
}
```

Turning C into Object Code

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Generated x86-64 Assembly

```
sumstore:
    pushq   %rbx
    movq    %rdx, %rbx
    call    plus
    movq    %rax, (%rbx)
    popq   %rbx
    ret
```

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Obtain (on CSUG machine) with command

```
gcc -Og -S sum.c -o sum.s
```

Turning C into Object Code

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Turning C into Object Code

Generated x86-64 Assembly

Binary Code for **sumstore**

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    pushq  %rbx  
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```

Memory

0x53
0x48
0x89
0xd3
0xe8
0xf2
0xff
0xff
0xff
0x48
0x89
0x03
0x5b
0xc3

Turning C into Object Code

Generated x86-64 Assembly

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    ret
```

Address Memory

0x0400595	0x53
	0x48
	0x89
	0xd3
	0xe8
	0xf2
	0xff
	0xff
	0xff
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Turning C into Object Code

Generated x86-64 Assembly

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Obtain (on CSUG machine) with command

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gcc -c sum.s -o sum.o
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Turning C into Object Code

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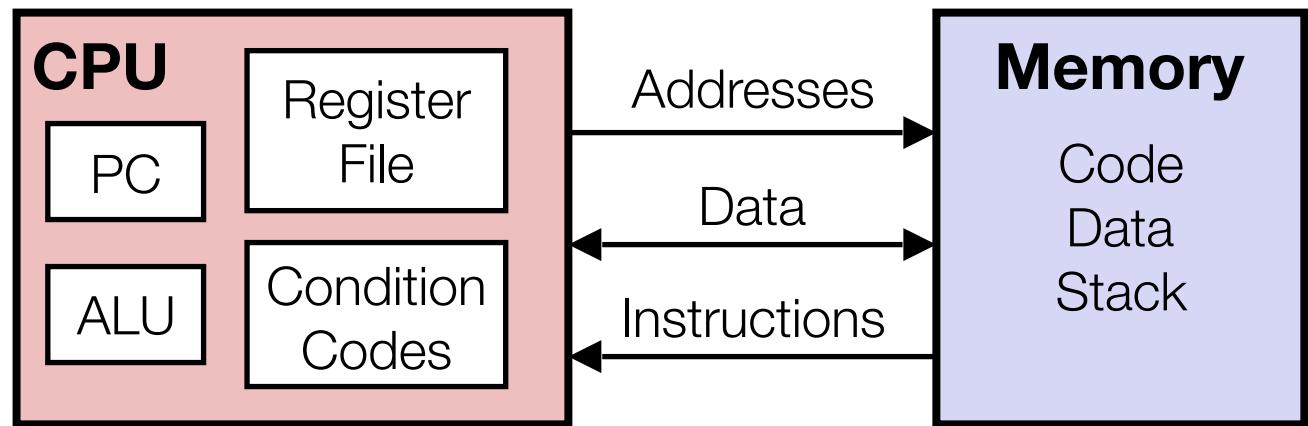
```
gcc -c sum.s -o sum.o
```

- Total of 14 bytes
- Instructions have variable lengths: e.g., 1, 3, or 5 bytes
- Code starts at memory address 0x0400595

Address	Memory
0x0400595	0x53
	0x48
	0x89
	0xd3
	0xe8
	0xff
	0xff
	0xff
	0x48
	0x89
	0x03
	0x5b
	0xc3

Instruction Processing Sequence

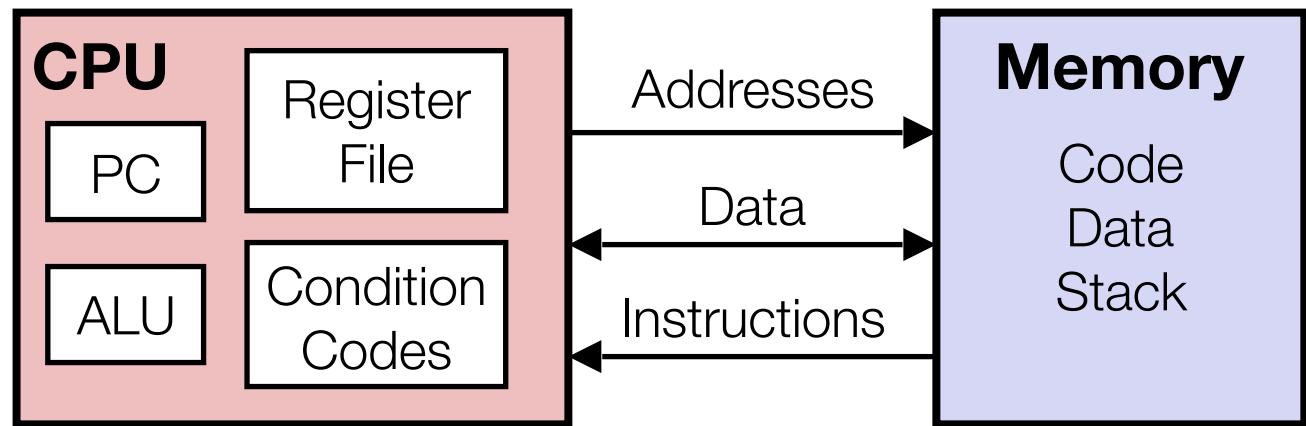
Assembly
Programmer's
Perspective
of a Computer



Fetch Instruction
(According to PC)

Instruction Processing Sequence

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Programmer's
Perspective
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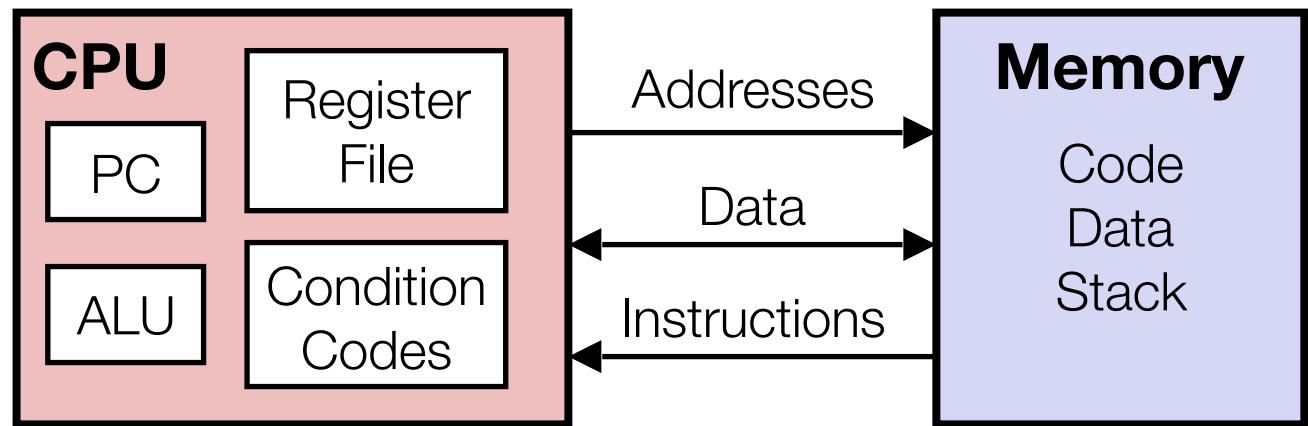


Fetch Instruction
(According to PC)

0x4801d8

Instruction Processing Sequence

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Programmer's
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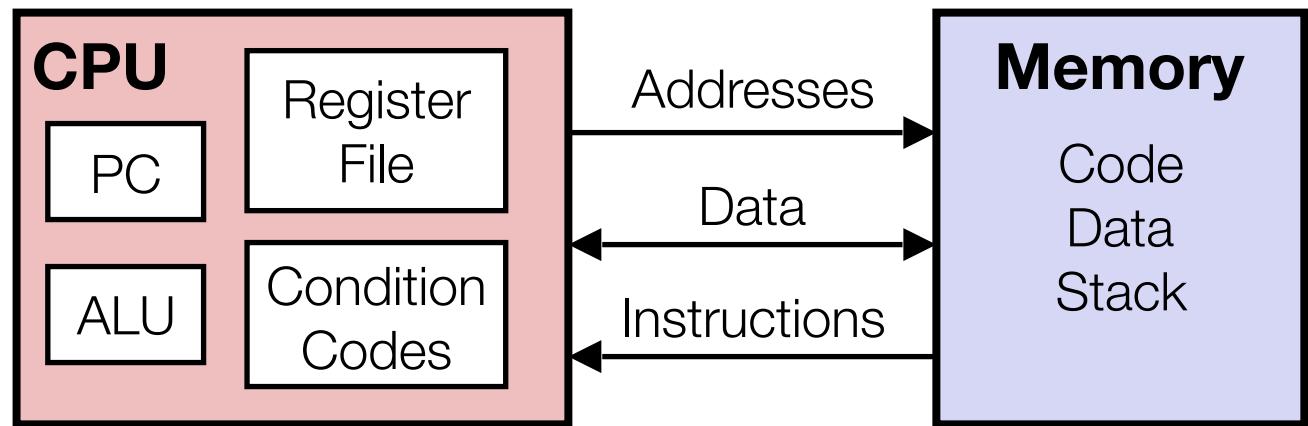


Fetch Instruction
(According to PC) → Decode
Instruction

addq %rax, (%rbx)

Instruction Processing Sequence

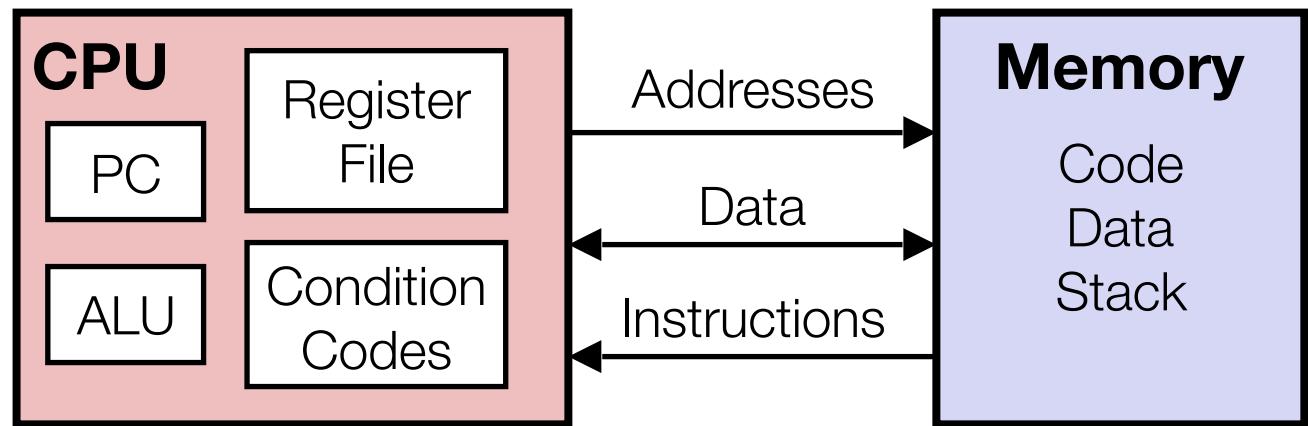
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Fetch Instruction
(According to PC) → Decode Instruction → Fetch Operands

Instruction Processing Sequence

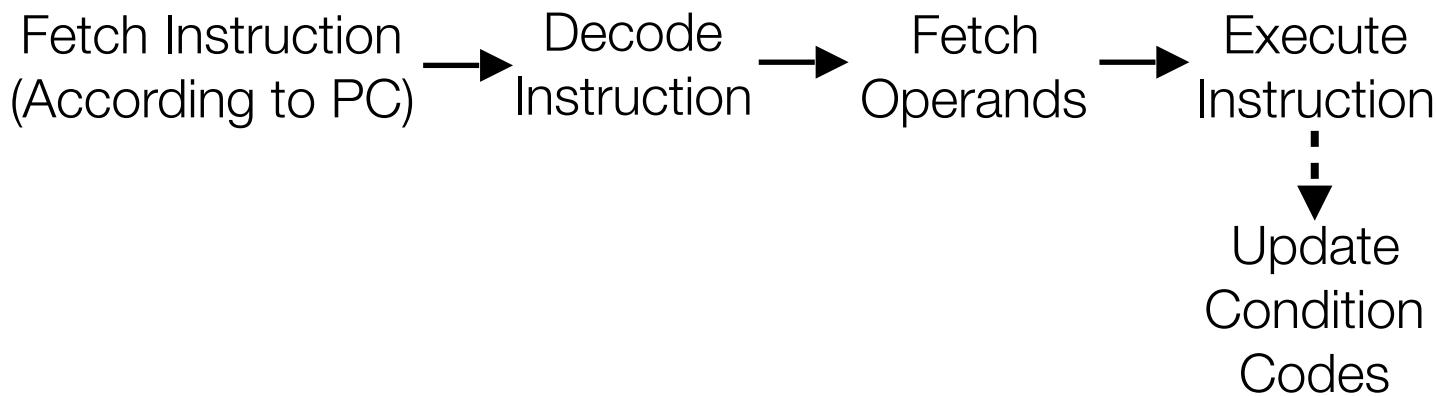
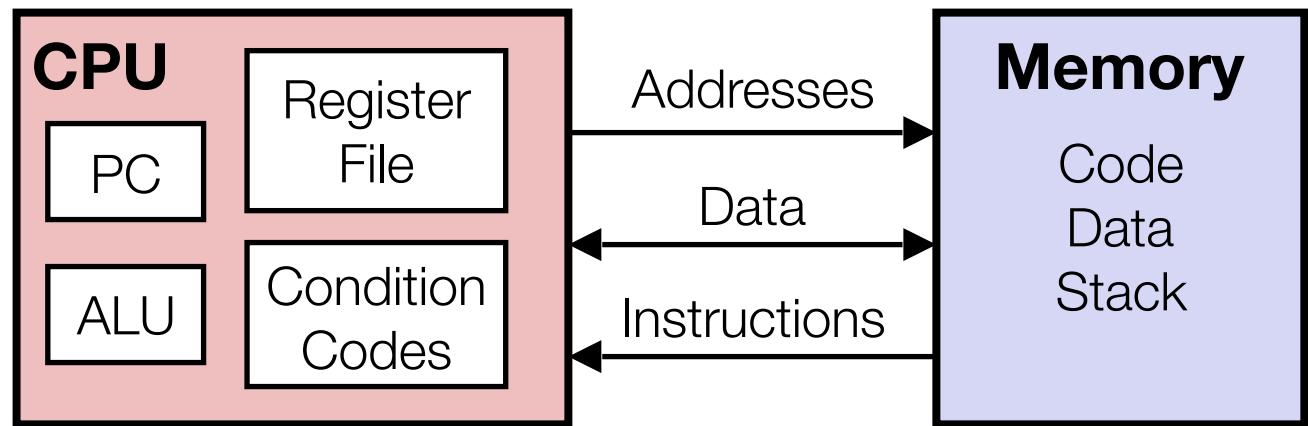
Assembly
Programmer's
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Fetch Instruction
(According to PC) → Decode Instruction → Fetch Operands → Execute Instruction

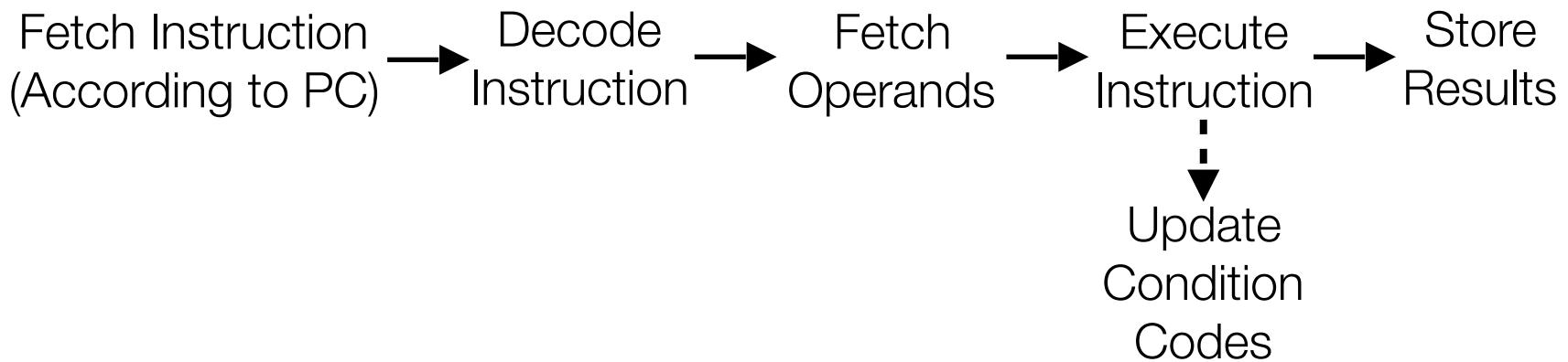
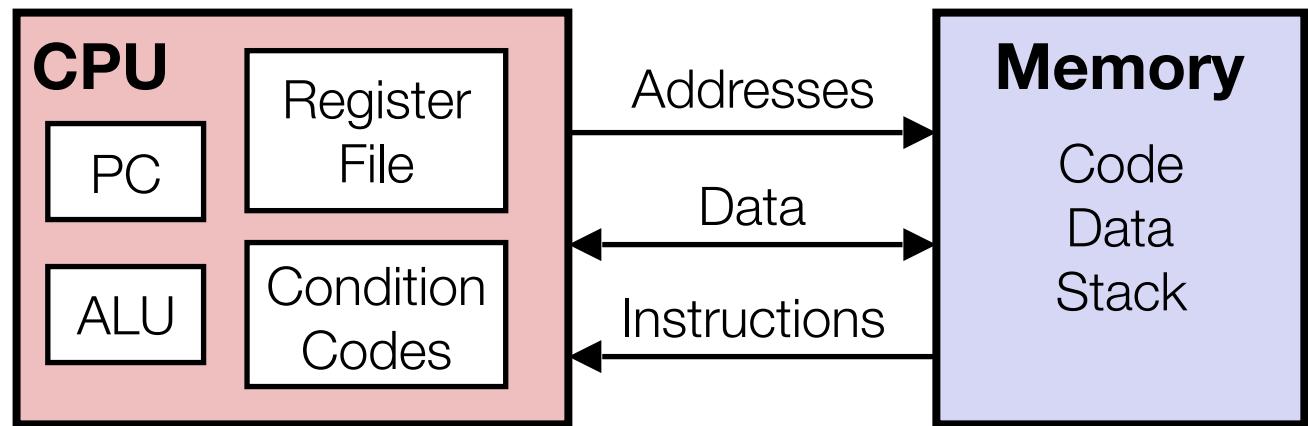
Instruction Processing Sequence

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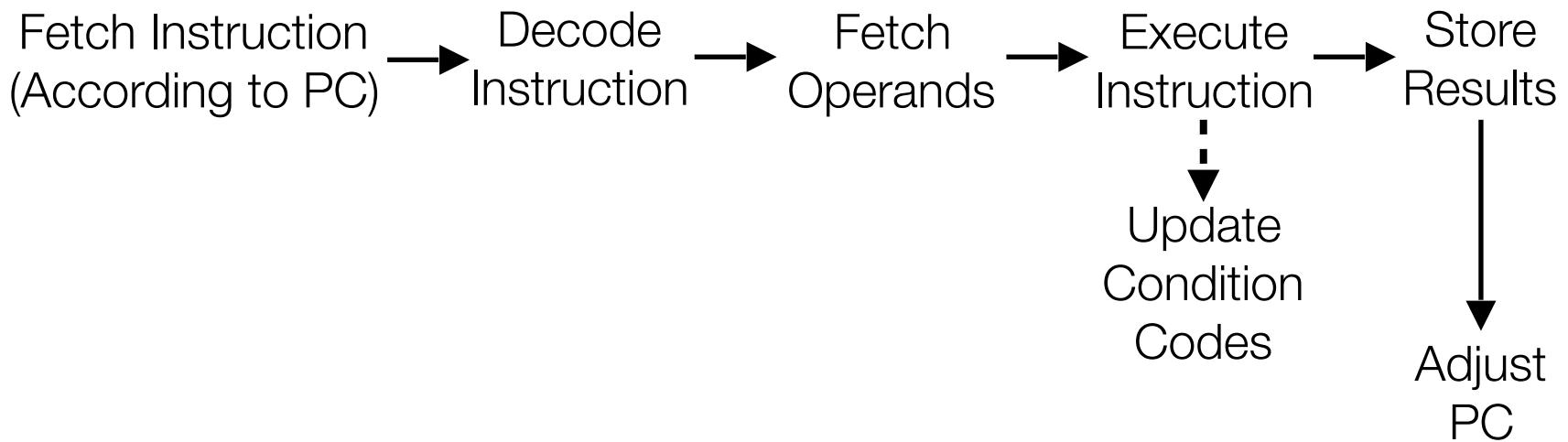
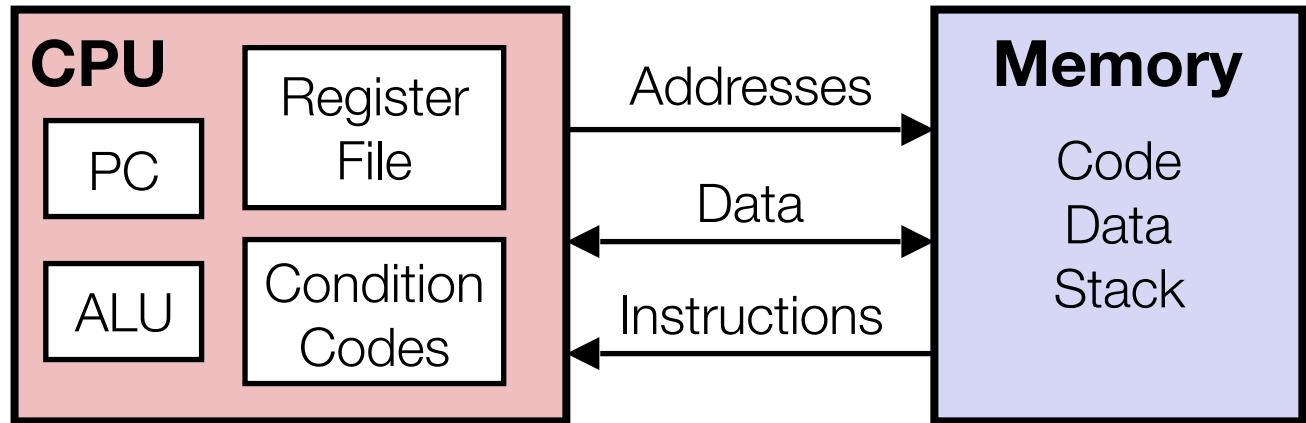
Instruction Processing Sequence

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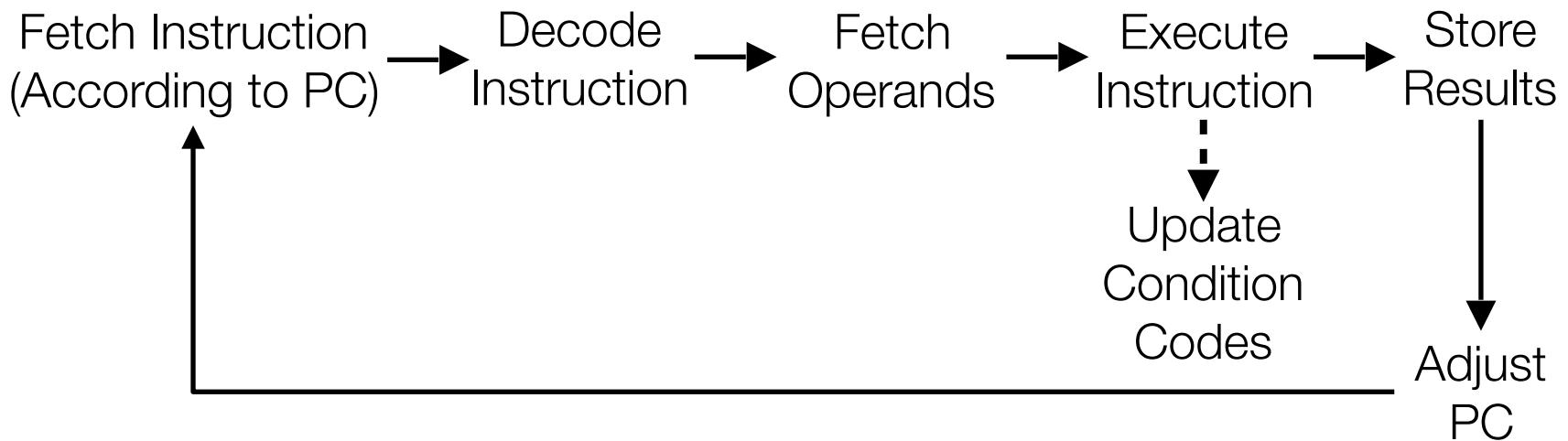
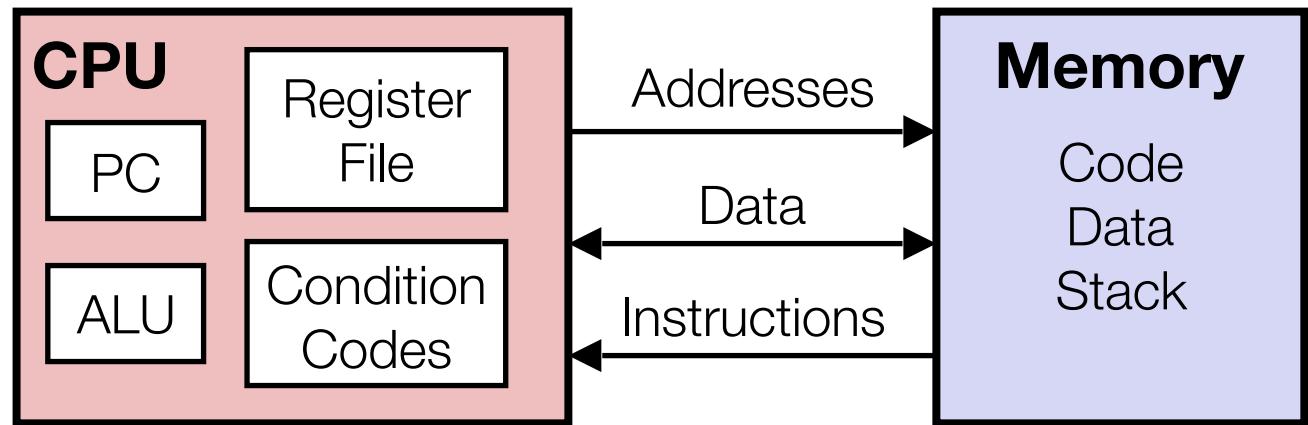
Instruction Processing Sequence

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Instruction Processing Sequence

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Machine Instruction Example (A Teaser)

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```
long t;  
long *d;  
t += *d;
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- C Code
 - Add value **t** with value in memory location whose address is **d** and store the result back to **t**

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addq %rax, (%rbx)
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- Assembly Instruction

- Operator: Add two 8-byte values
 - Quad words in x86-64 parlance

- Operands:

- t: Register **%rax**

- dest: Register **%rbx**

- *dest: Memory M[%rbx]

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Operand(s)

```
addq %rax, (%rbx)
```

- C Code

- Add value **t** with value in memory location whose address is **d** and store the result back to **t**

- Assembly Instruction

- Operator: Add two 8-byte values
 - Quad words in x86-64 parlance
 - Operands:

- t: Register **%rax**

- dest: Register **%rbx**

- *dest: Memory M[%rbx]

Machine Instruction Example (A Teaser)

```
long t;  
long *d;  
t += *d;
```

addq %rax, (%rbx)



- C Code

- Add value `t` with value in memory location whose address is `d` and store the result back to `t`

- Assembly Instruction

- Operator: Add two 8-byte values
 - Quad words in x86-64 parlance
- Operands:

`t:` Register `%rax`

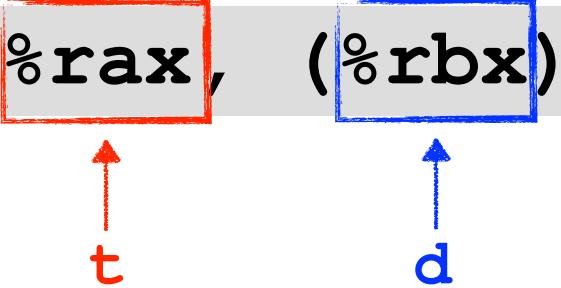
`dest:` Register `%rbx`

`*dest:` Memory $M[\%rbx]$

Machine Instruction Example (A Teaser)

```
long t;  
long *d;  
t += *d;
```

addq **%rax**, (%**rbx**)



- C Code

- Add value **t** with value in memory location whose address is **d** and store the result back to **t**

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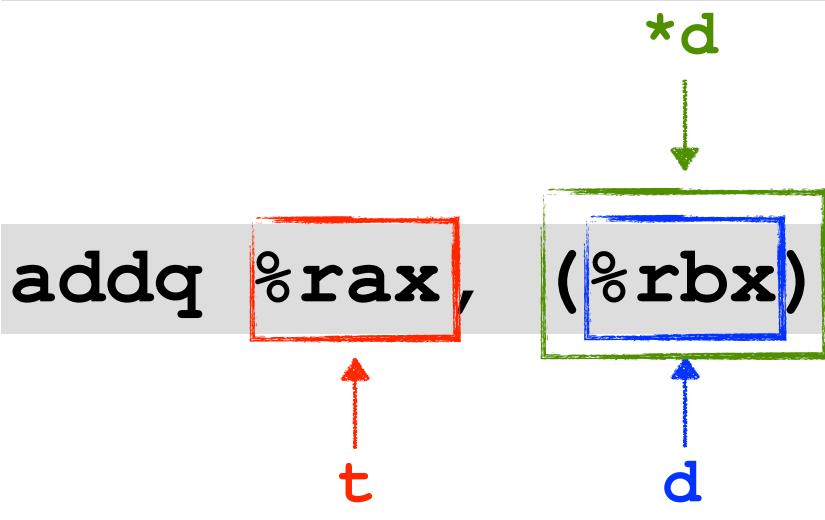
t: Register **%rax**

dest: Register **%rbx**

*dest: Memory M[%**rbx**]

Machine Instruction Example (A Teaser)

```
long t;  
long *d;  
t += *d;
```



- C Code

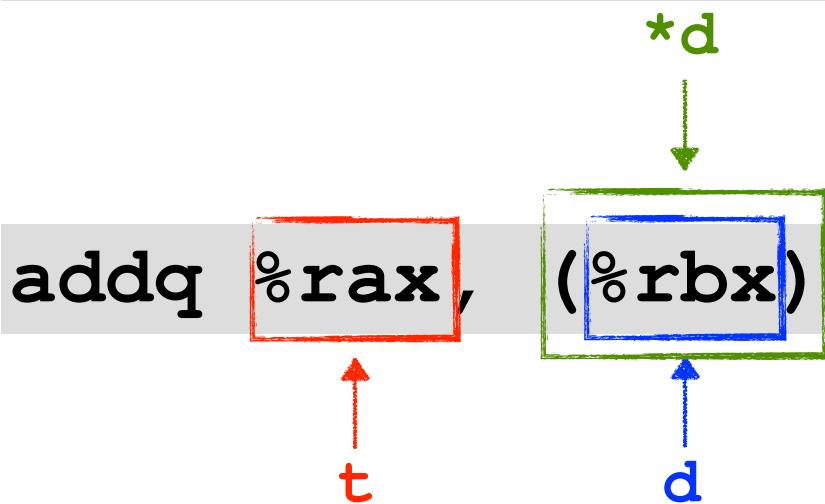
- Add value `t` with value in memory location whose address is `d` and store the result back to `t`

- Assembly Instruction

- Operator: Add two 8-byte values
 - Quad words in x86-64 parlance
- Operands:
 - `t`: Register `%rax`
 - `dest`: Register `%rbx`
 - `*dest`: Memory $M[\%rbx]$

Machine Instruction Example (A Teaser)

```
long t;  
long *d;  
t += *d;
```



`0xf0059e:`

`0x 48 01 d8`

- C Code

- Add value `t` with value in memory location whose address is `d` and store the result back to `t`

- Assembly Instruction

- Operator: Add two 8-byte values
 - Quad words in x86-64 parlance
- Operands:
 - `t`: Register `%rax`
 - `dest`: Register `%rbx`
 - `*dest`: Memory $M[\%rbx]$

- Object Code

- 3-byte instruction
- Stored at address `0xf0059e`