CSC 252: Computer Organization
Spring 2023: Lecture 11

Instructor: Yuhao Zhu

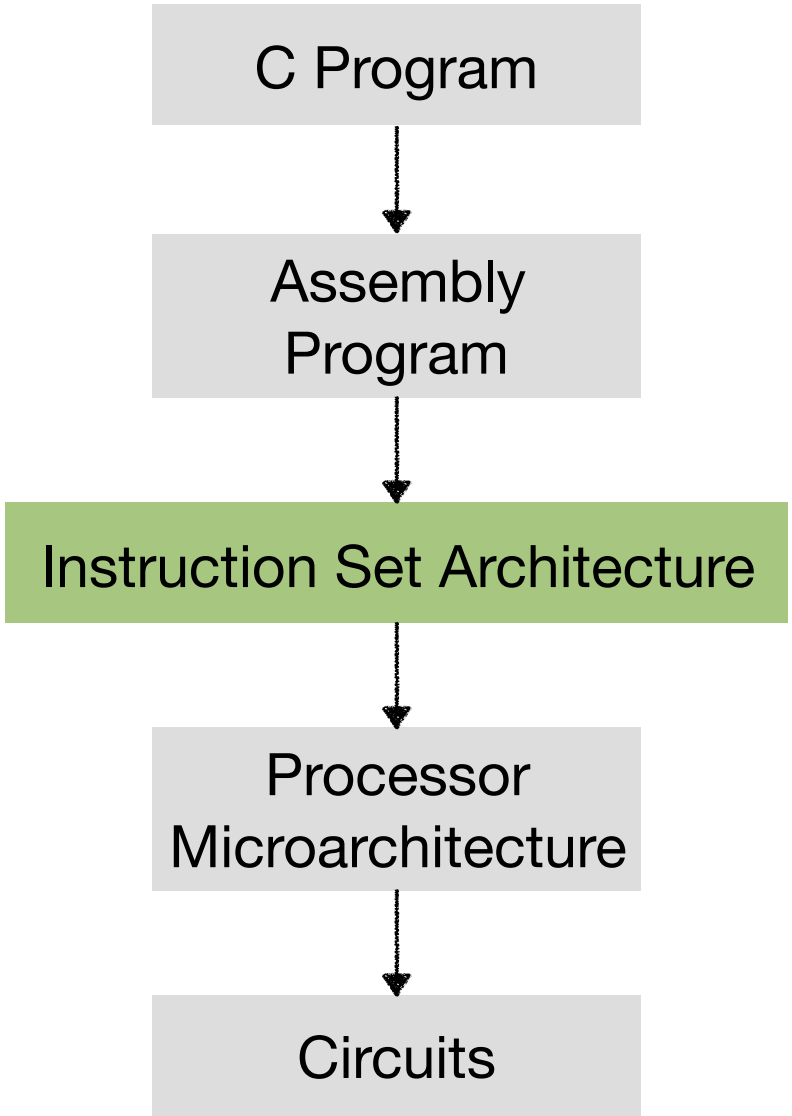
Department of Computer Science
University of Rochester

Announcement

- Programming assignment 3 out.

12	13	14	15 **Today**	16	17	18
19	20	21	22	23	24	25
26	27	28	Mar 1 **Due**	2	3	4

So far in 252…


C Program
Assembly Program
Instruction Set Architecture
Processor Microarchitecture
Circuits

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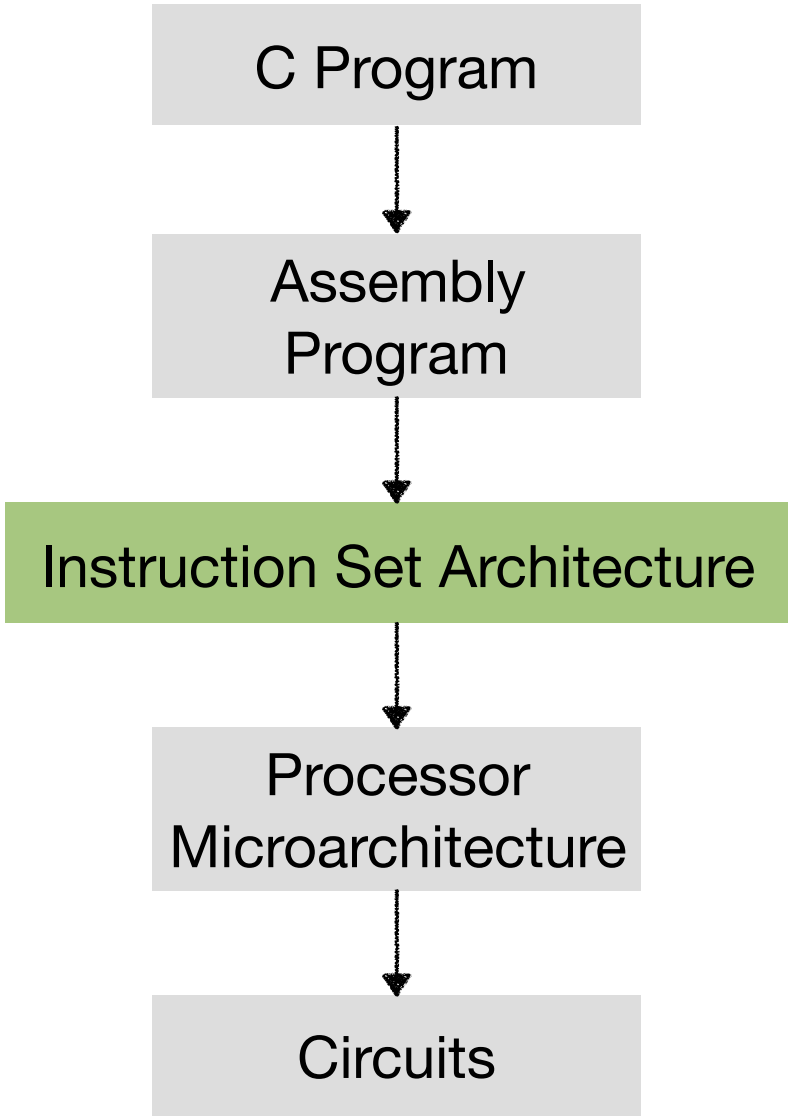


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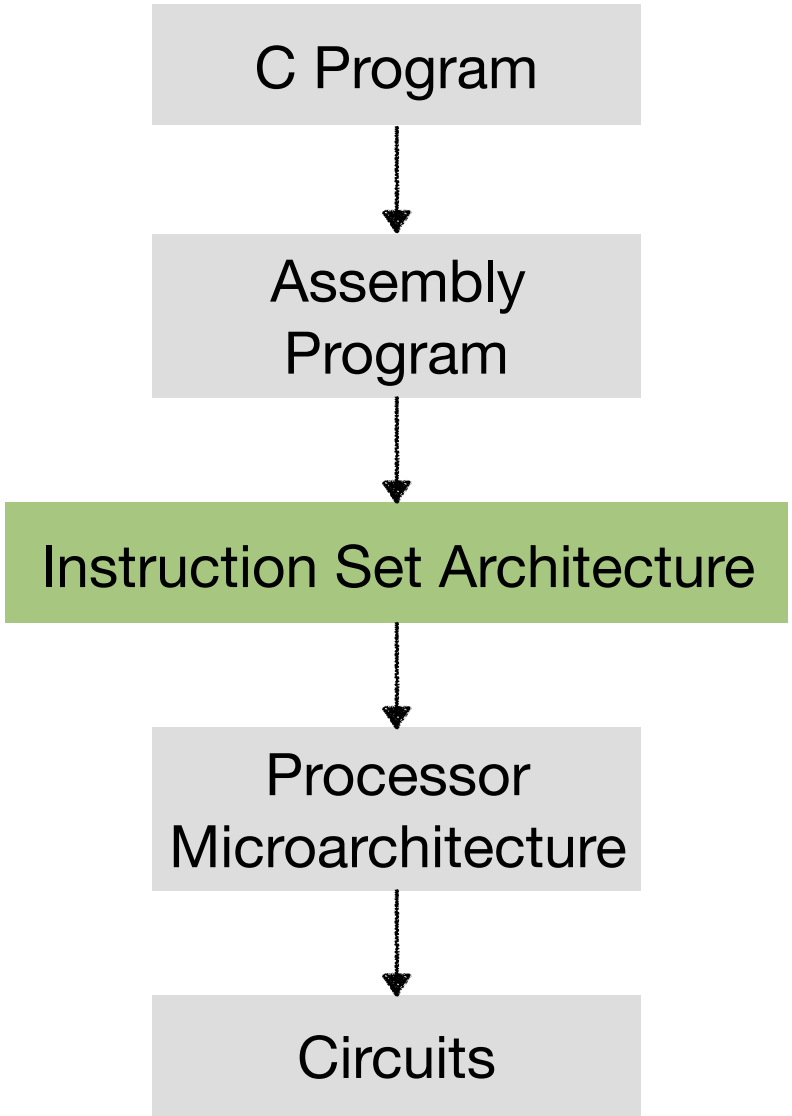


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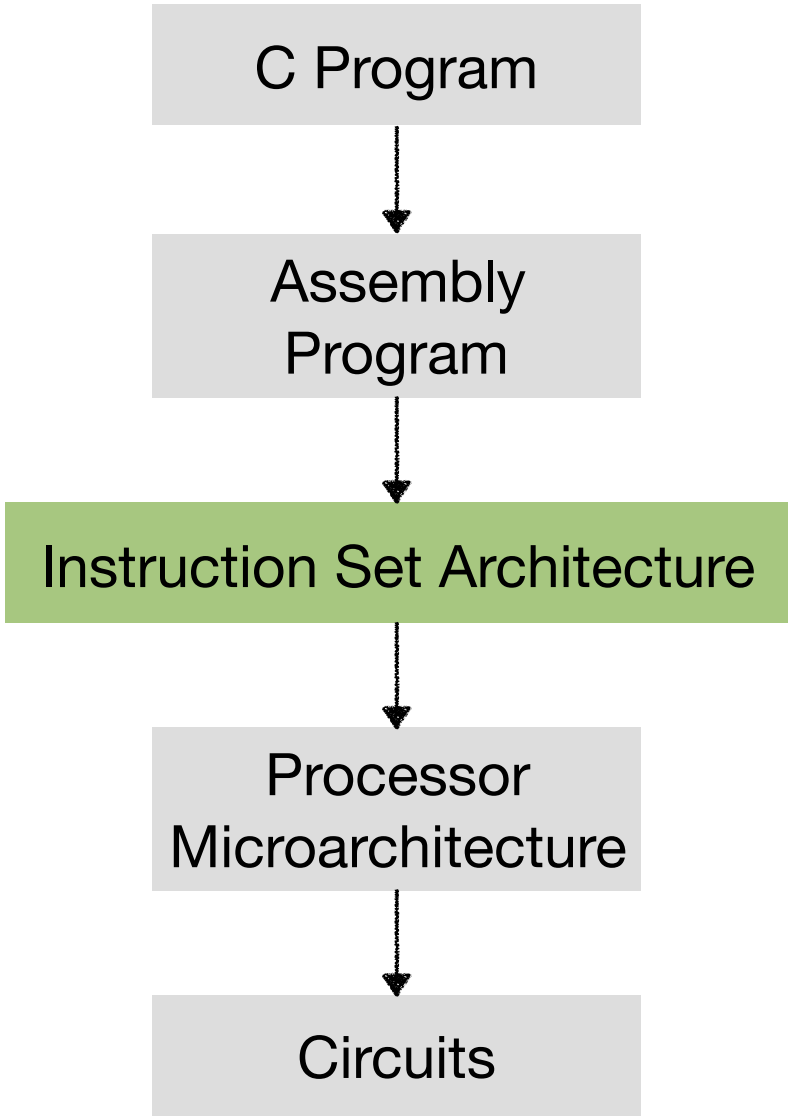


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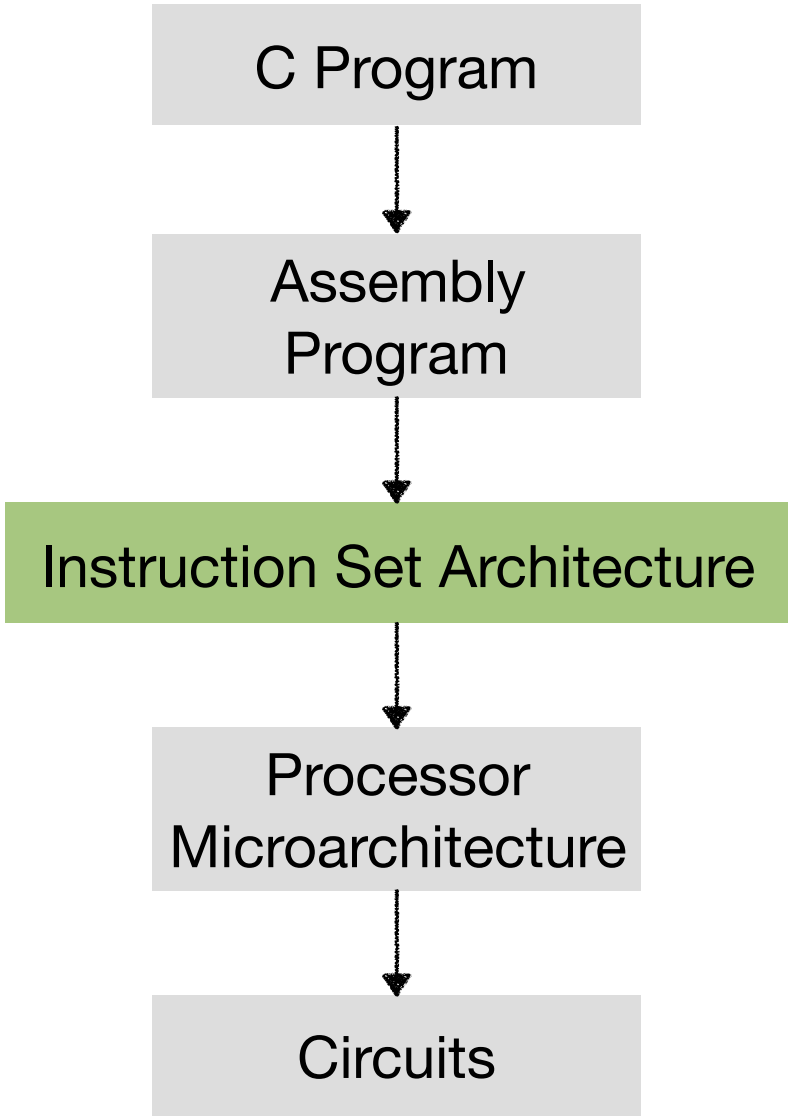


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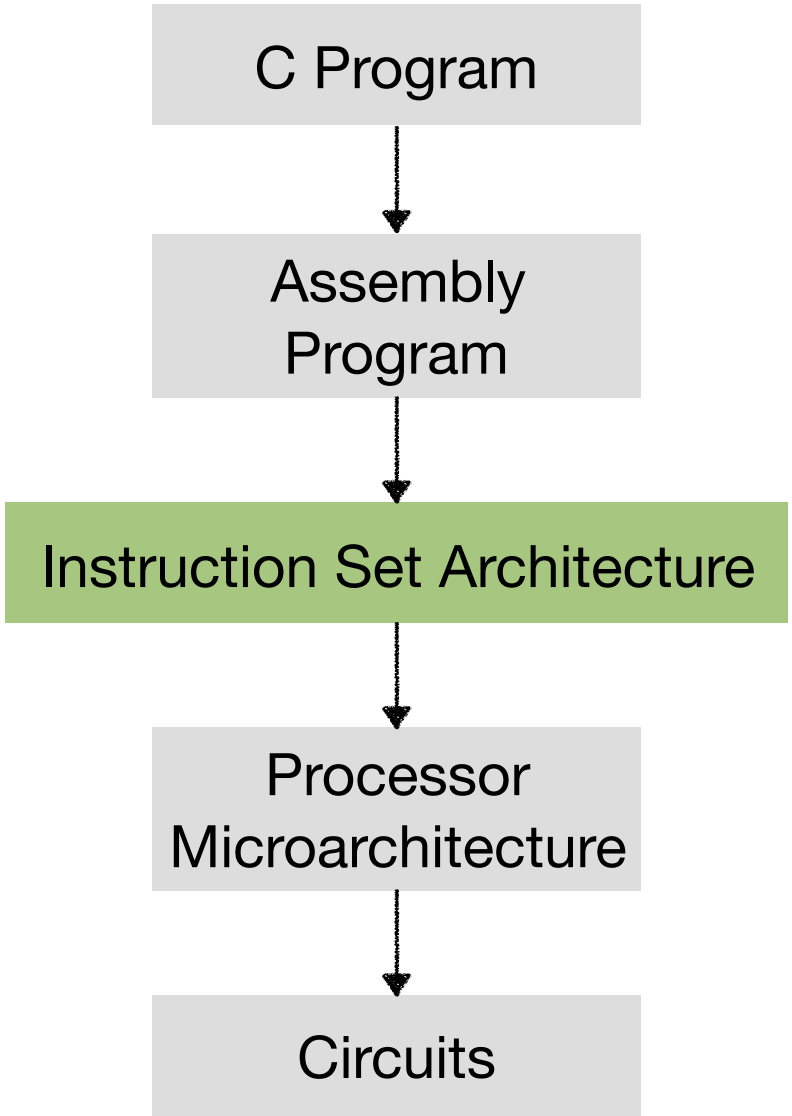


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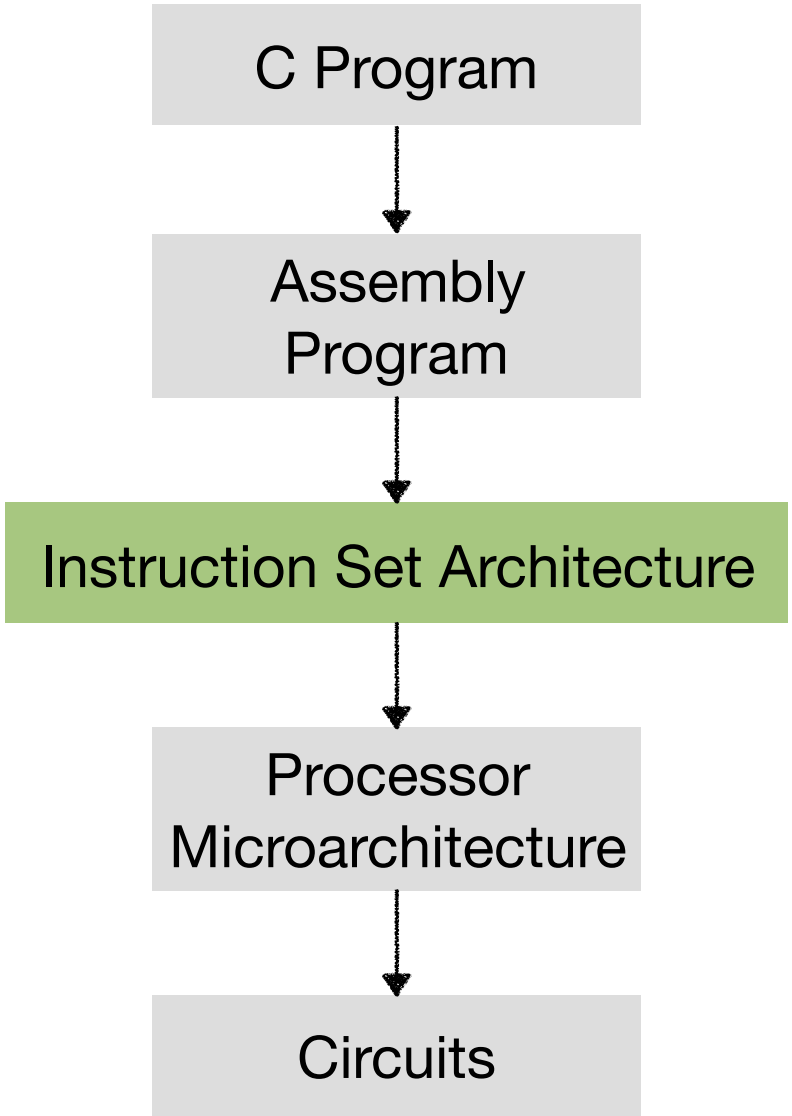

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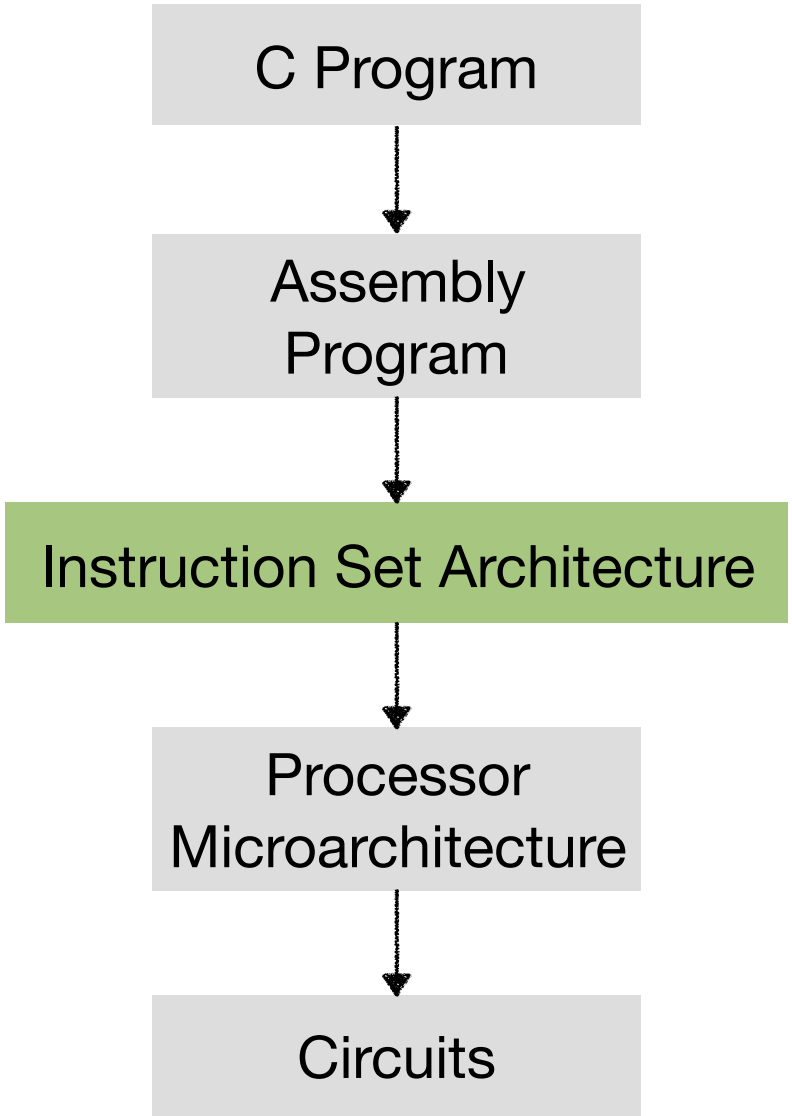

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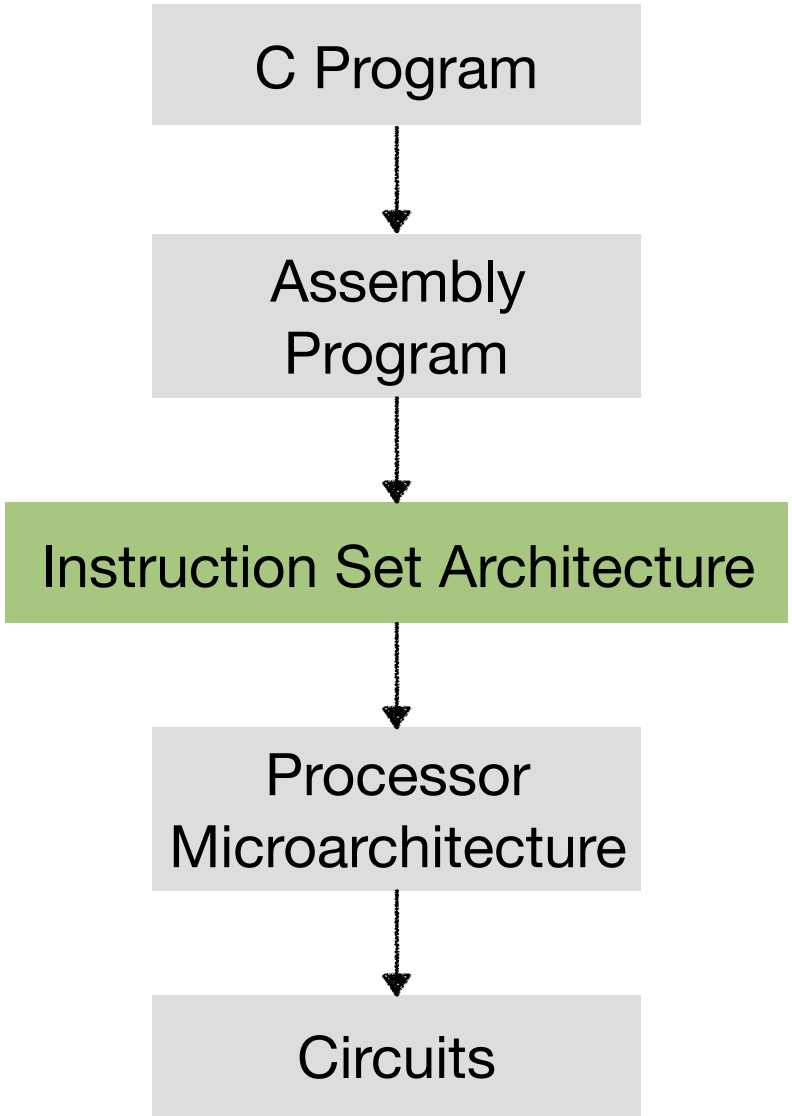

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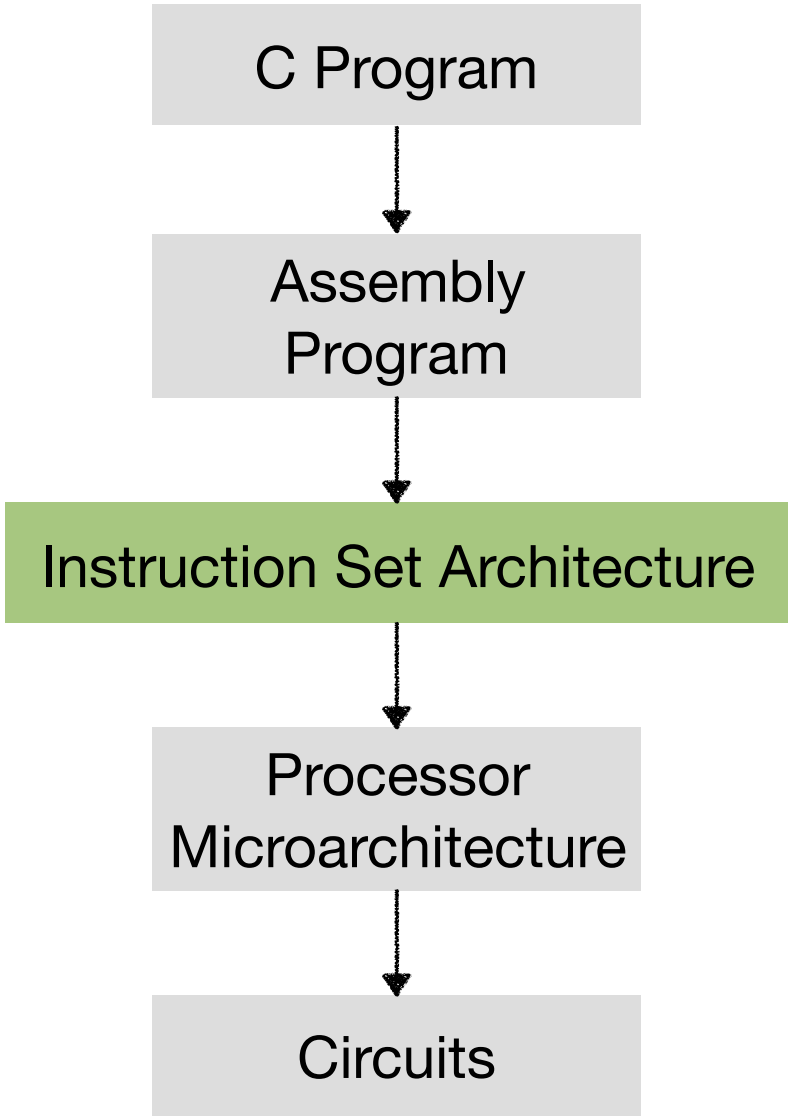

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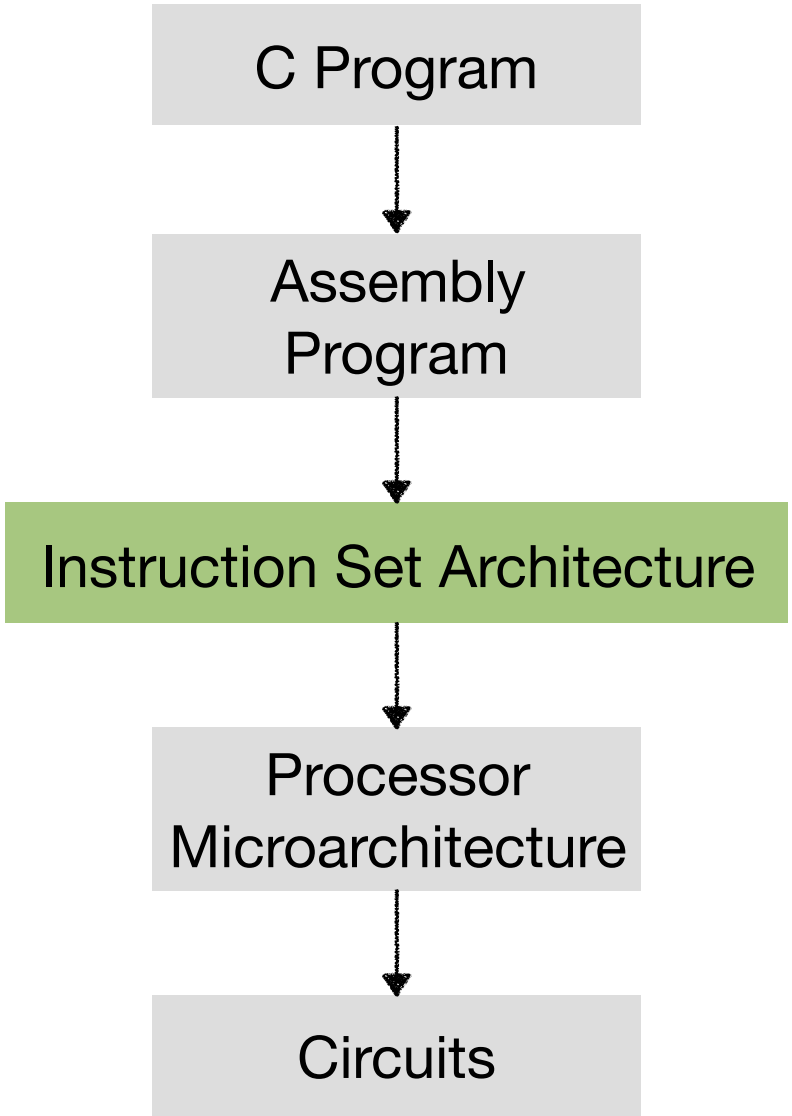

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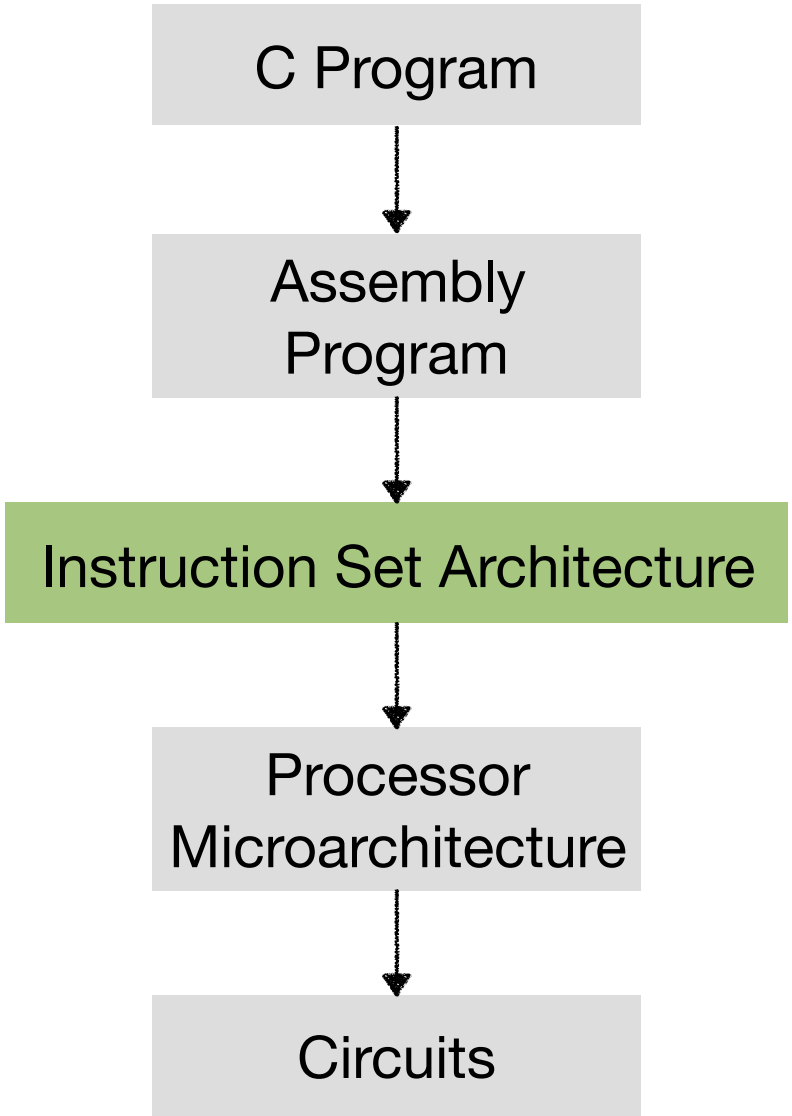

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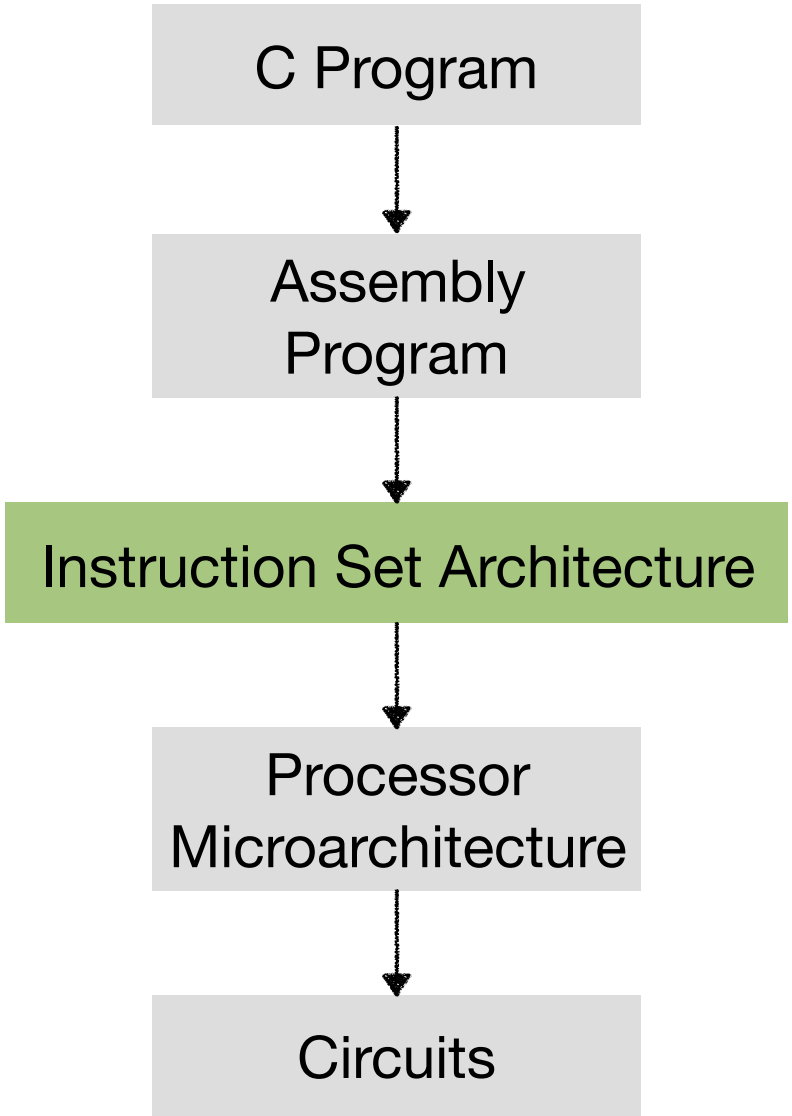

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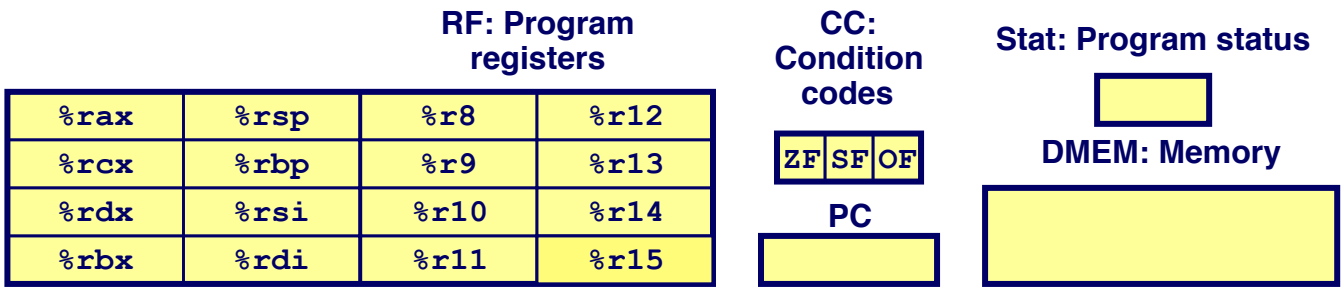
  - What hardware needs to be built to run assembly programs?
  - How to run programs as fast (energy-efficient) as possible?

(Simplified) x86 Processor State



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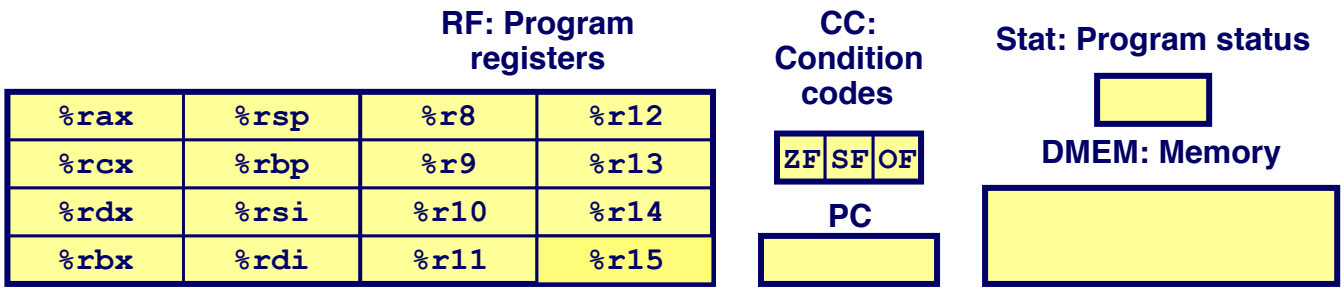

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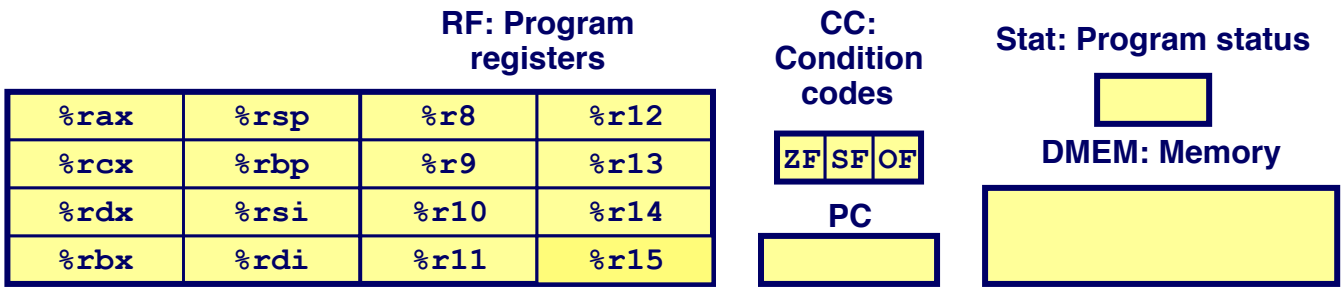

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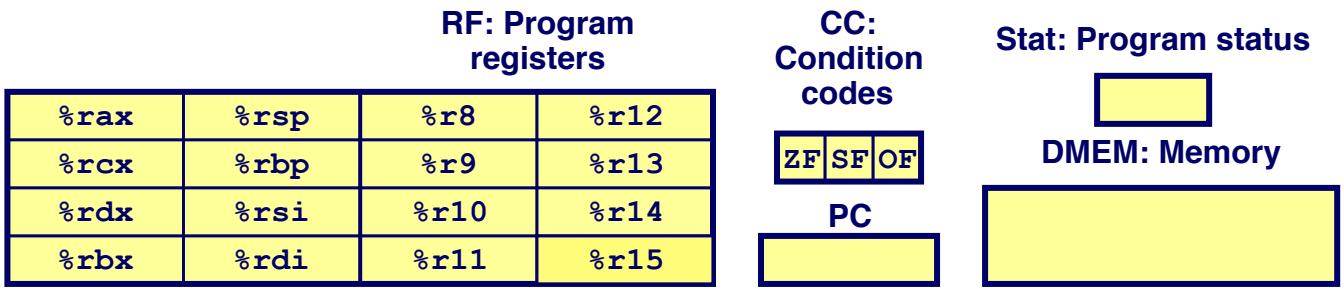

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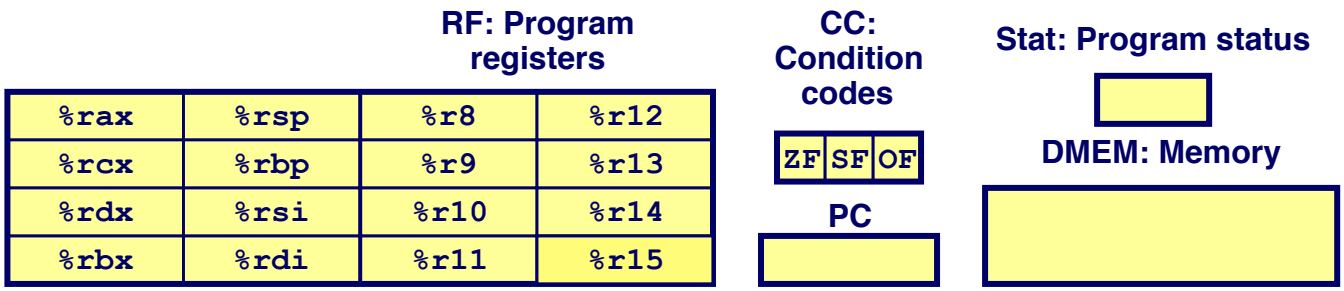

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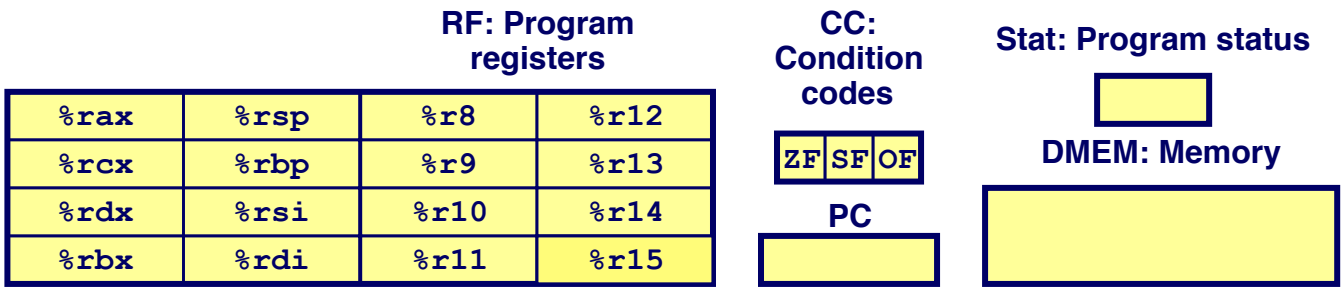

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- Memory
  - Byte-addressable storage array
  - Words stored in little-endian byte order

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- Abstraction protects software and hardware
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- Alternatives: Application-Specific Integrated Circuits (ASIC)
  - No instructions, (largely) not programmable, fixed-functioned, so no instruction fetch, decoding, etc.
  - So could be implemented extremely efficiently.
  - Examples: video/audio codec, (conventional) image signal processors, (conventional) IP packet router

Today: Instruction Encoding

- How to translate assembly instructions to binary
  - Essentially how an assembler works
- Using the Y86-64 ISA: Simplified version of x86-64

How are Instructions Encoded in Binary?

- Remember that instructions are stored in memory **as bits** (just like data)
- Each instruction is fetched (according to the address specified in the PC), decoded, and executed by the CPU
- The ISA defines the format of an instruction (syntax) and its meaning (semantics)
- Idea: encode the two major fields, opcode and operand, separately in bits.
  - The OPCODE field says what the instruction does (e.g. ADD)
  - The OPERAND field(s) say where to find inputs and outputs

Y86-64 Instructions

```
halt

nop

cmovXX rA, rB

irmovq V, rB

rmmovq rA, D(rB)

mrmovq D(rB), rA

OPq rA, rB

jXX Dest

call Dest

ret

pushq rA

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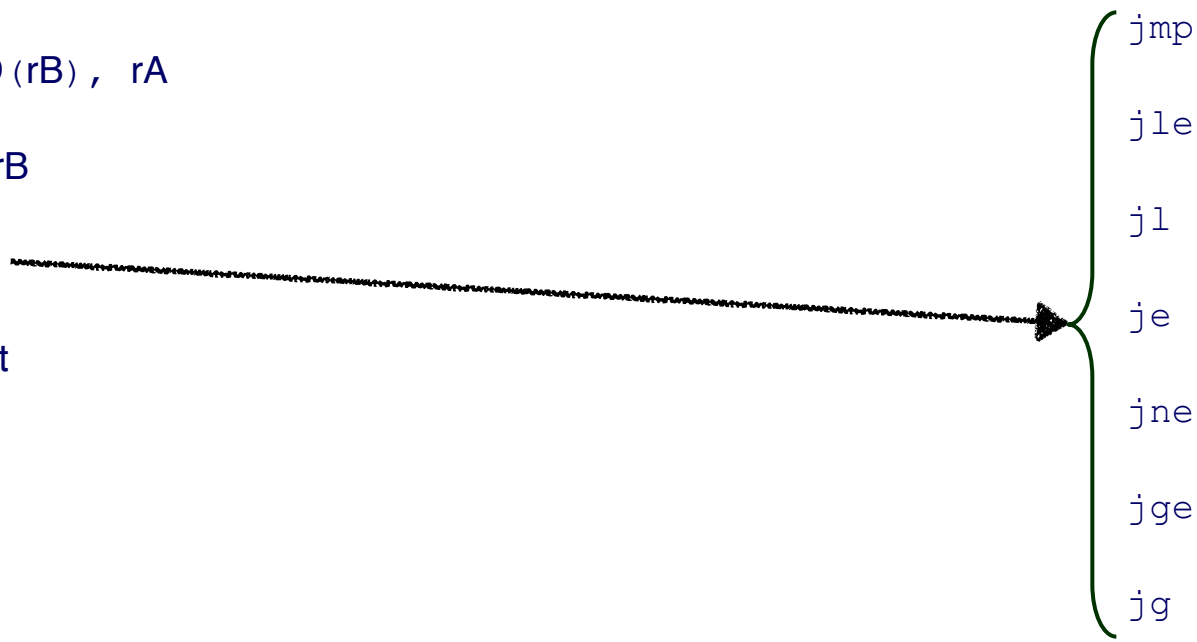

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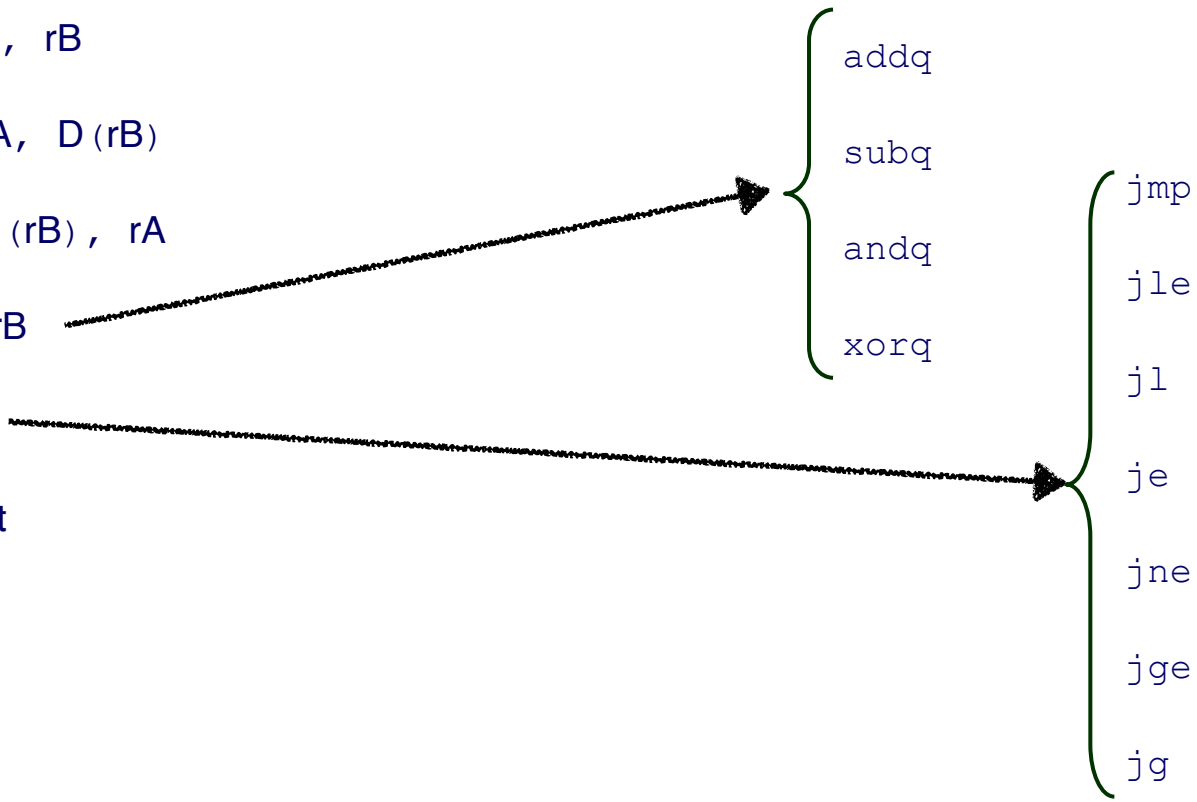

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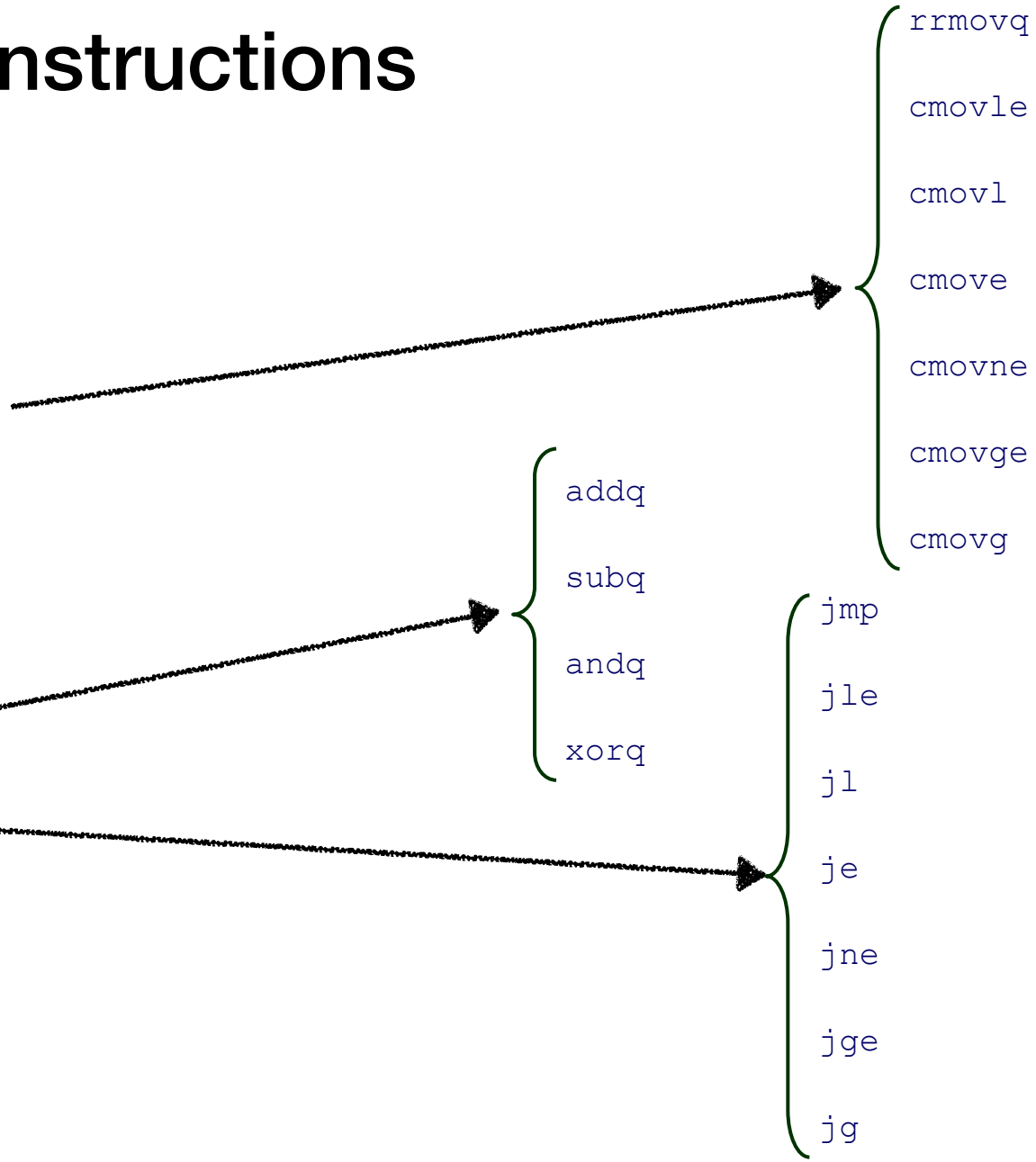
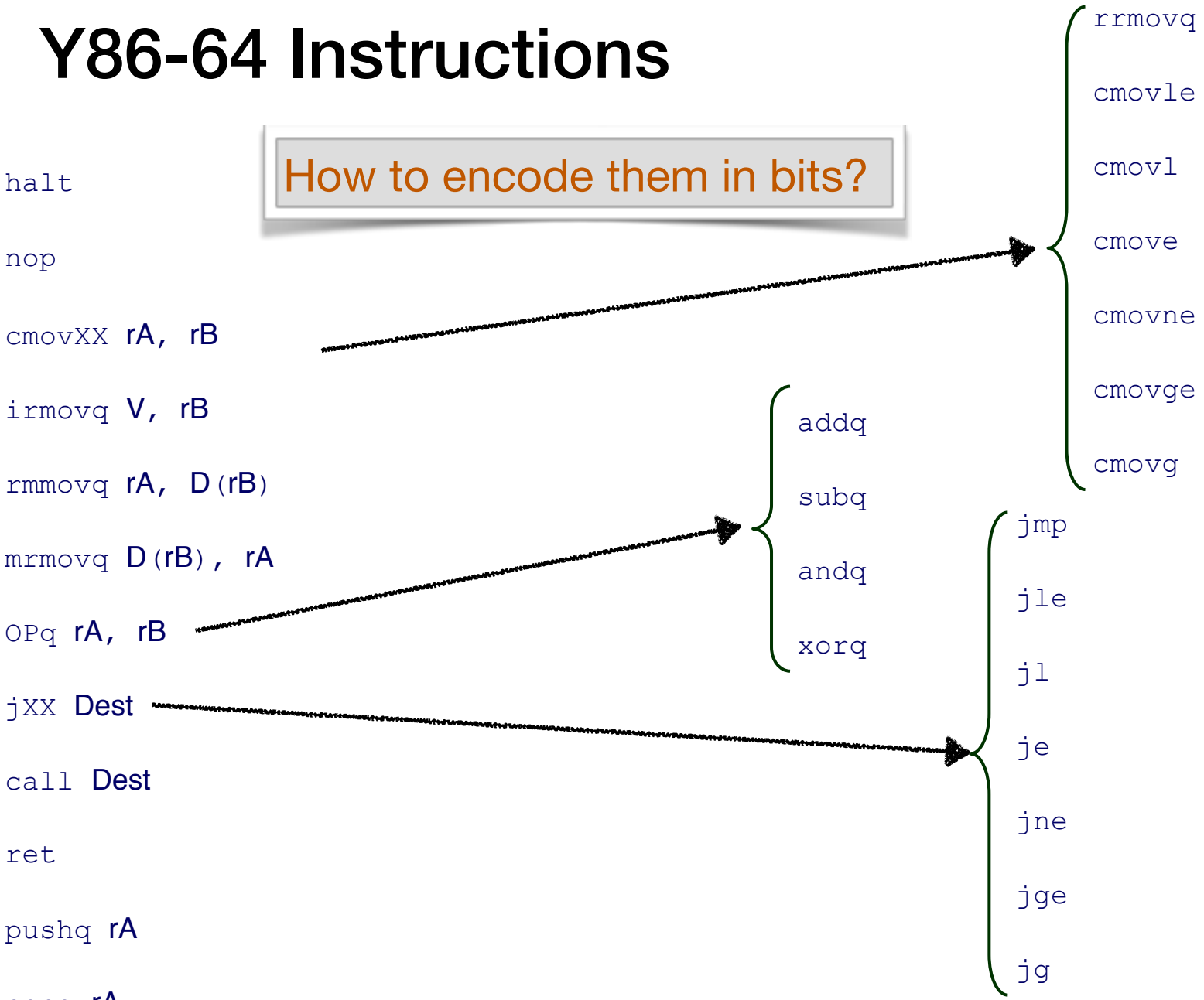


Y86-64 Instructions

How to encode them in bits?



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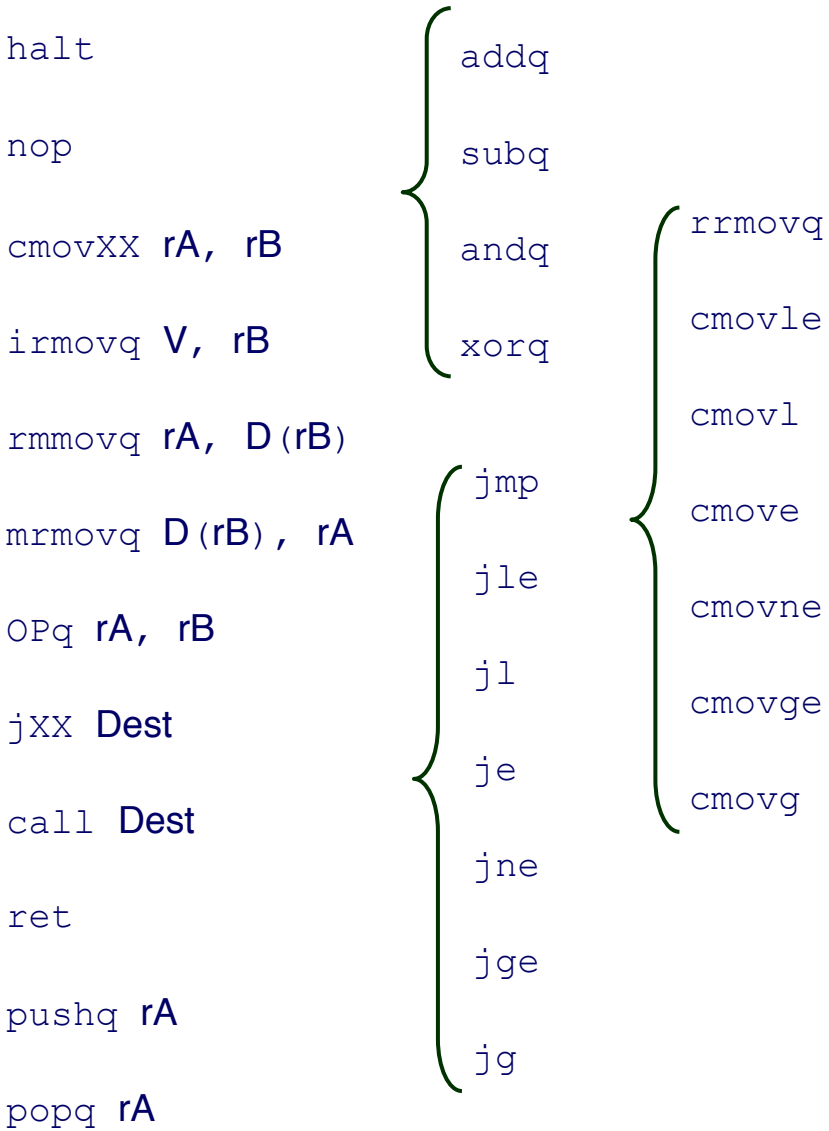

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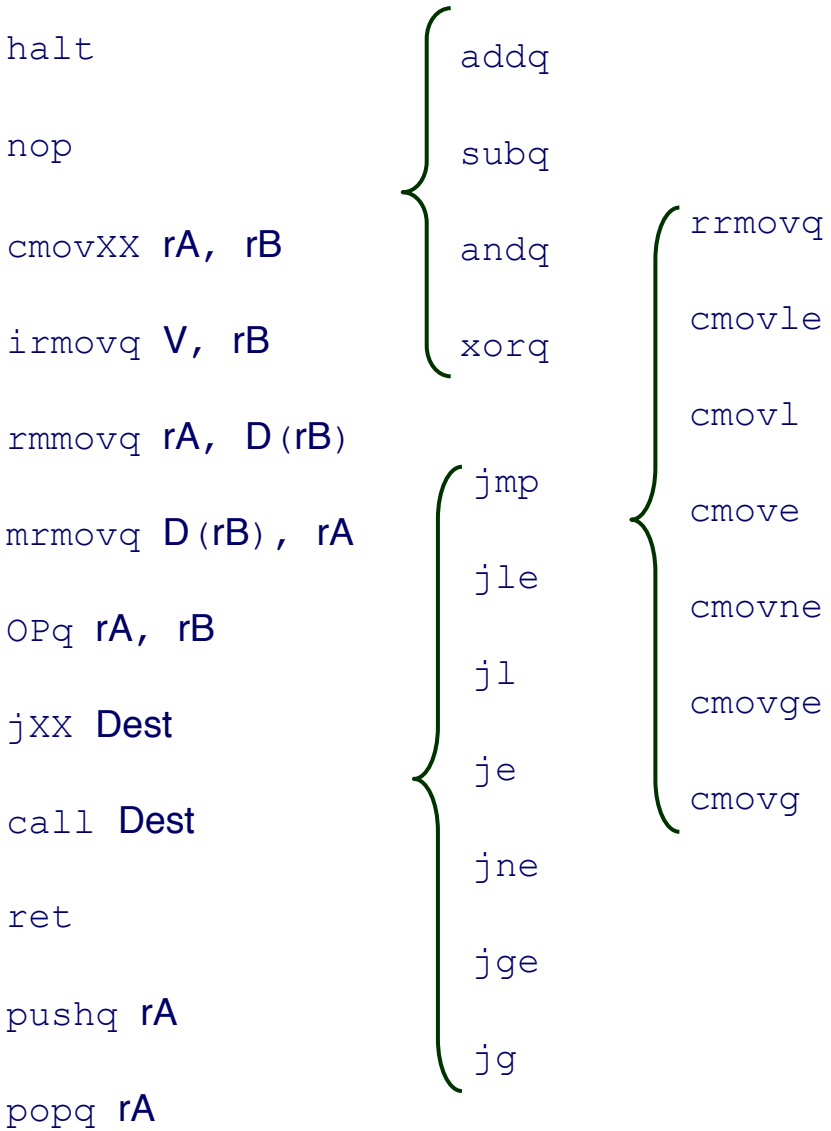

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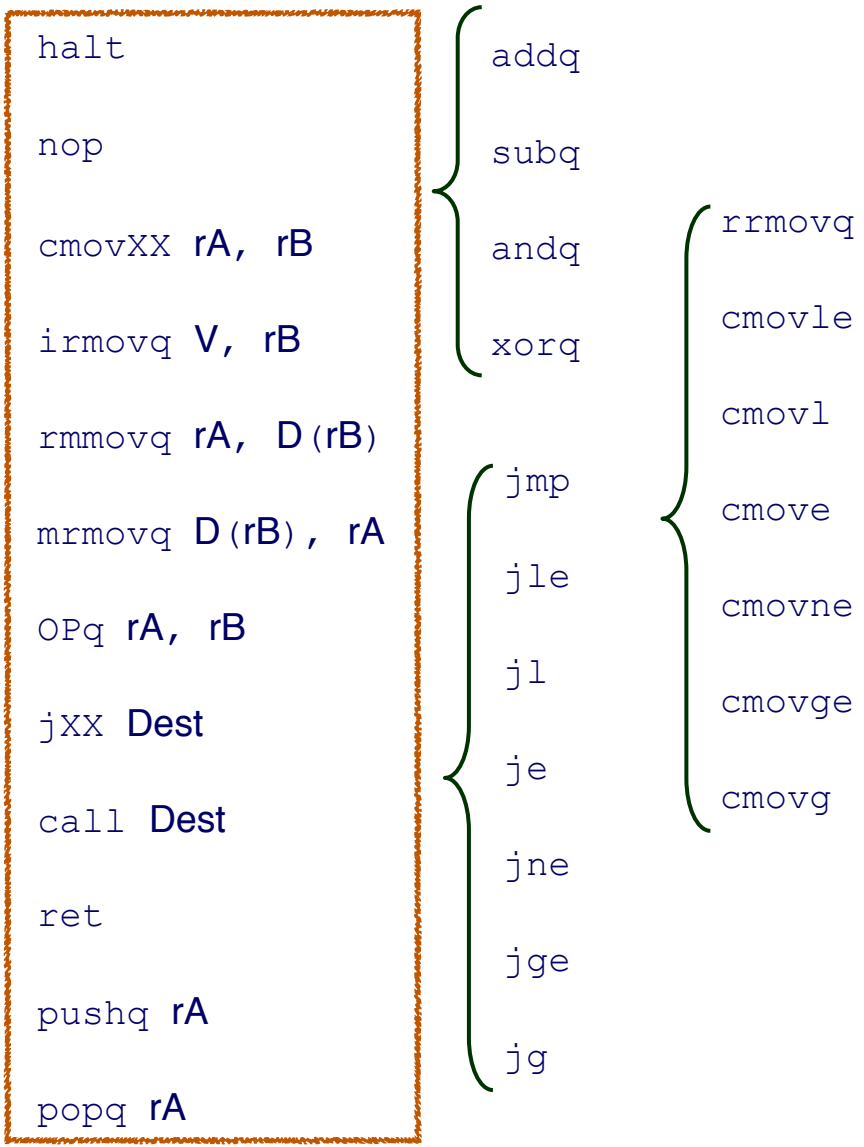

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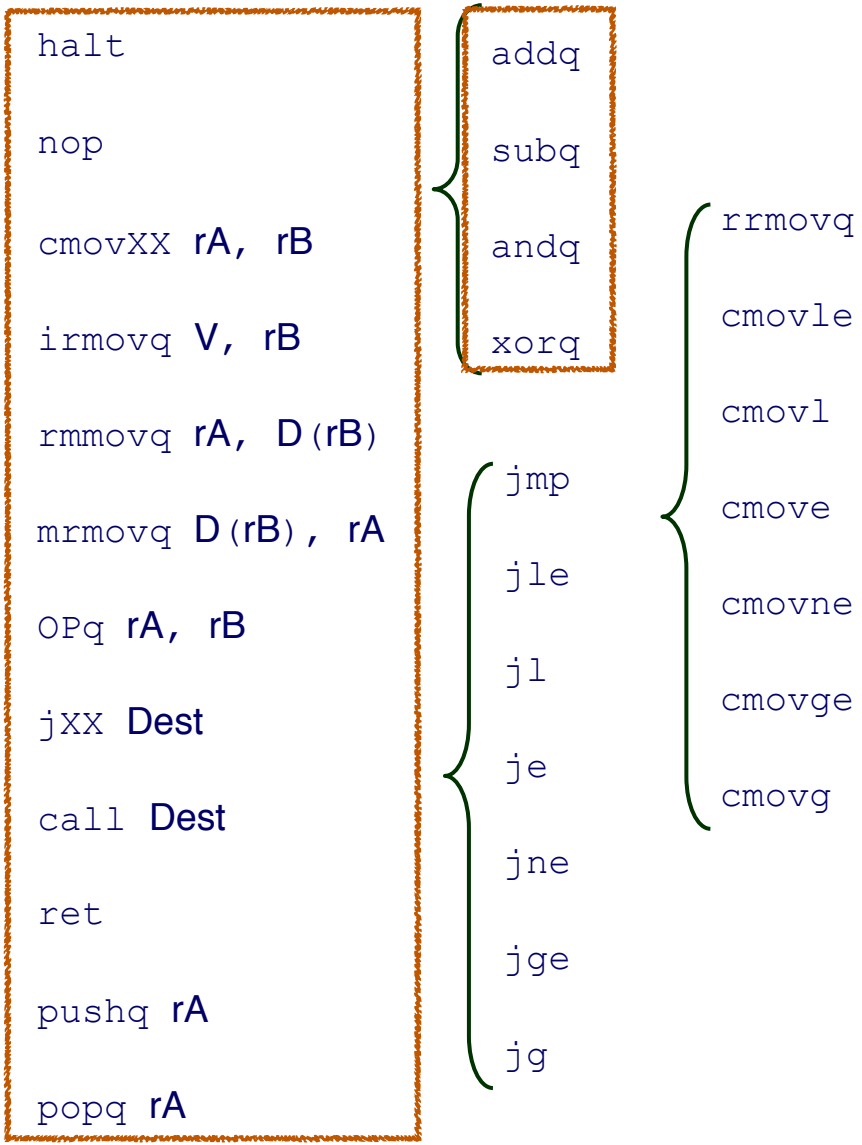

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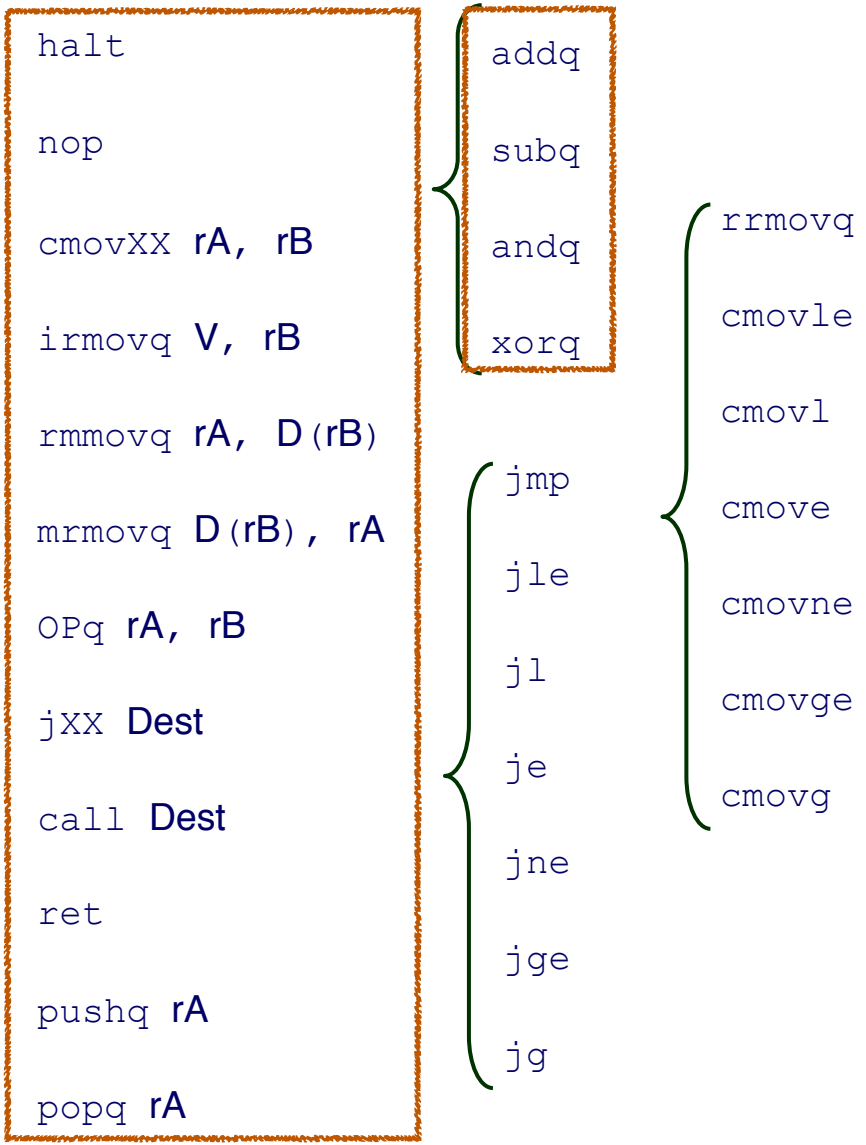

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- Which one is better???

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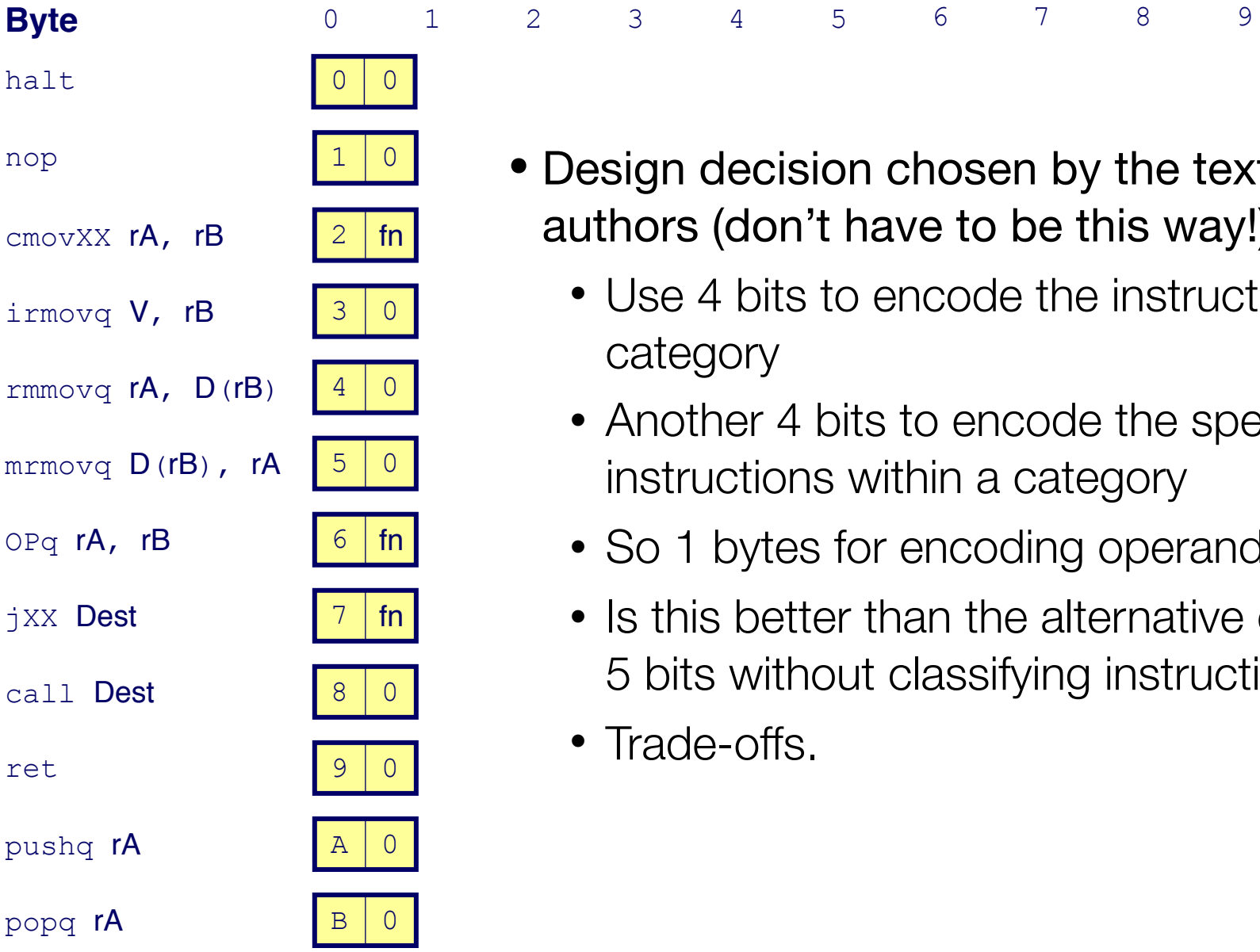

- Design decision chosen by the textbook authors (don't have to be this way!)
  - Use 4 bits to encode the instruction category
  - Another 4 bits to encode the specific instructions within a category
  - So 1 bytes for encoding operand
  - Is this better than the alternative of using 5 bits without classifying instructions?
  - Trade-offs.

Encoding Registers

Each register has 4-bit ID

- Same encoding as in x86-64
- Register ID 15 (`0xF`) indicates “no register”

%rax	0	%r8	8
%rcx	1	%r9	9
%rdx	2	%r10	A
%rbx	3	%r11	B
%rsp	4	%r12	C
%rbp	5	%r13	D
%rsi	6	%r14	E
%rdi	7	No Register	F

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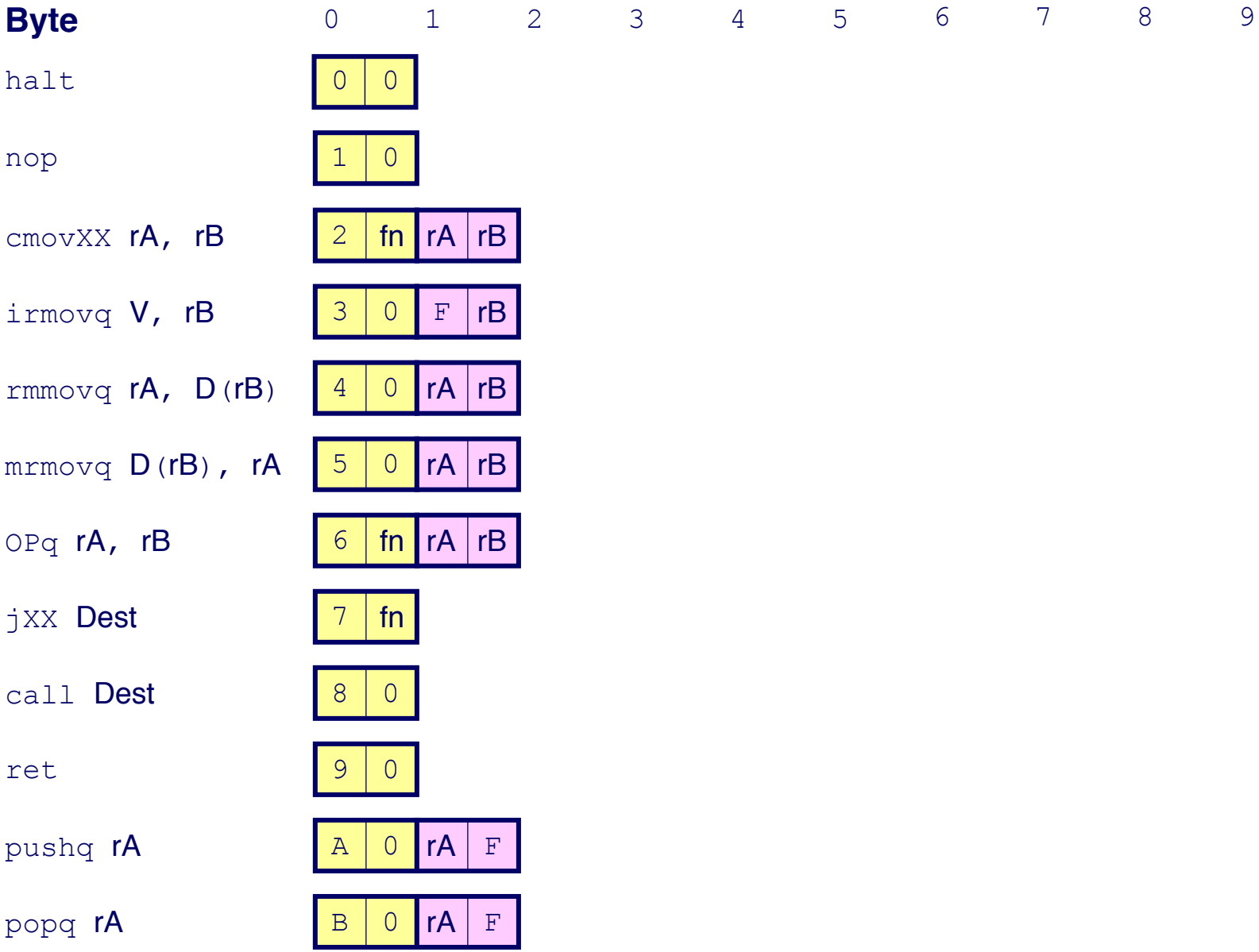

Instruction Example

Addition Instruction

- Add value in register rA to that in register rB
  - Store result in register rB
- Set condition codes based on result
- e.g., `addq %rax,%rsi` Encoding: `60 06`
- Two-byte encoding
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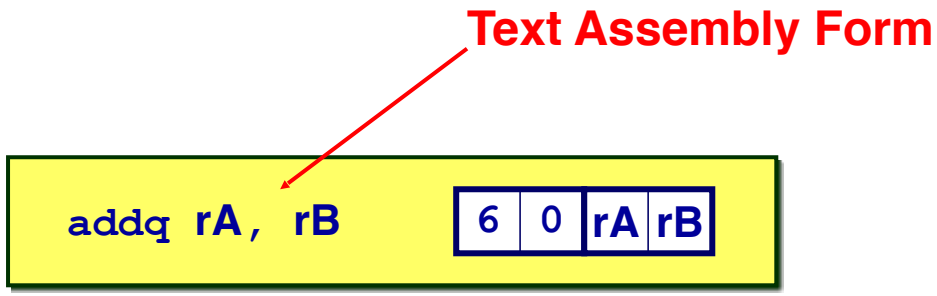

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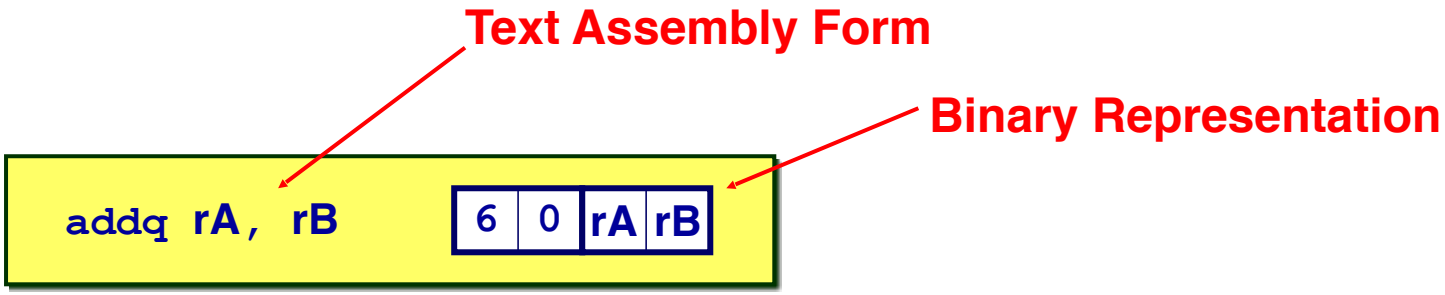

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Arithmetic and Logical Operations

Add

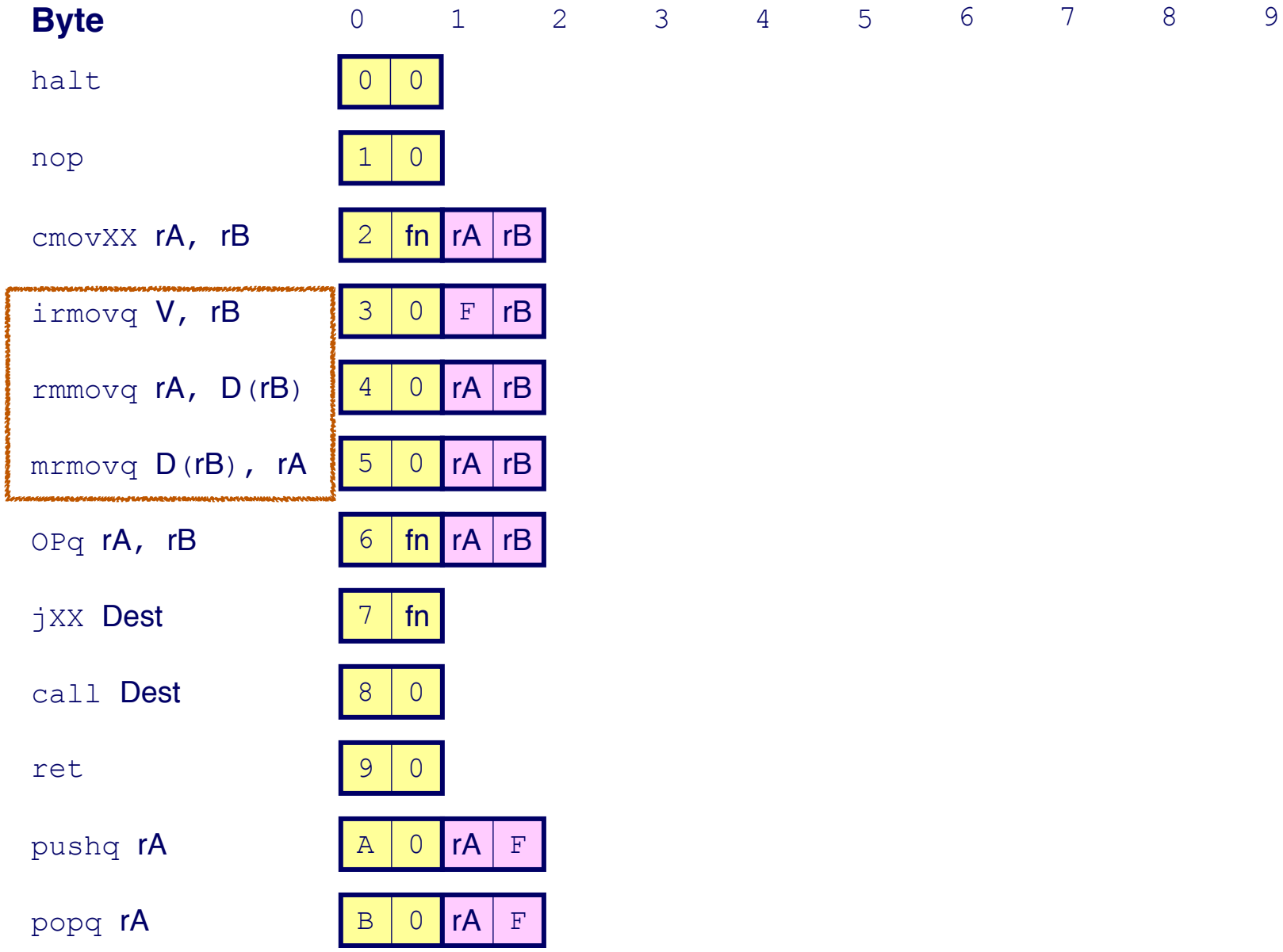
Subtract (rA from rB)

And

Exclusive-Or

- Referred to generically as "`OPq`"
- Encodings differ only by "function code"
  - Low-order 4 bytes in first instruction word
- Set condition codes as side effect

Move Instructions



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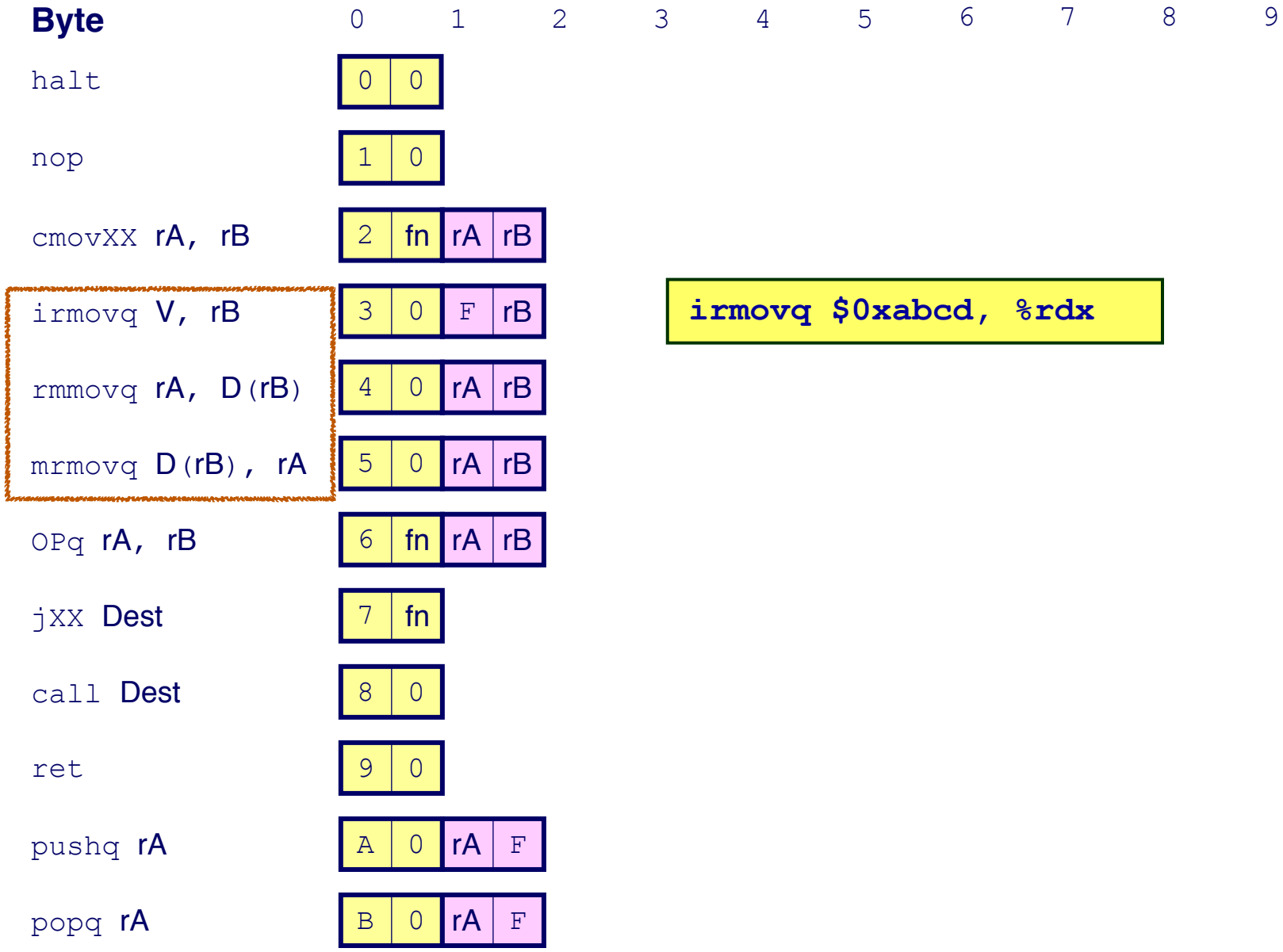

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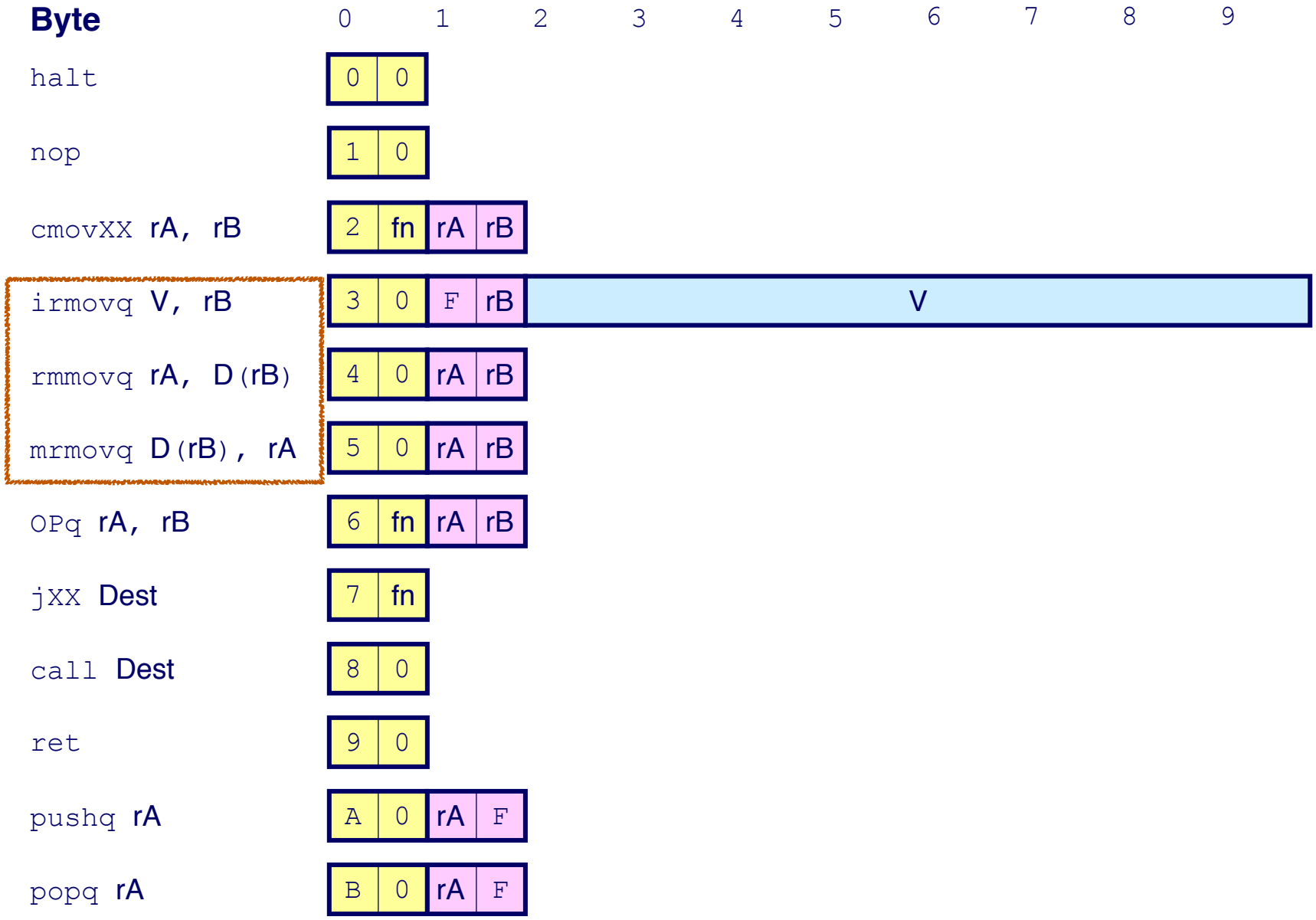

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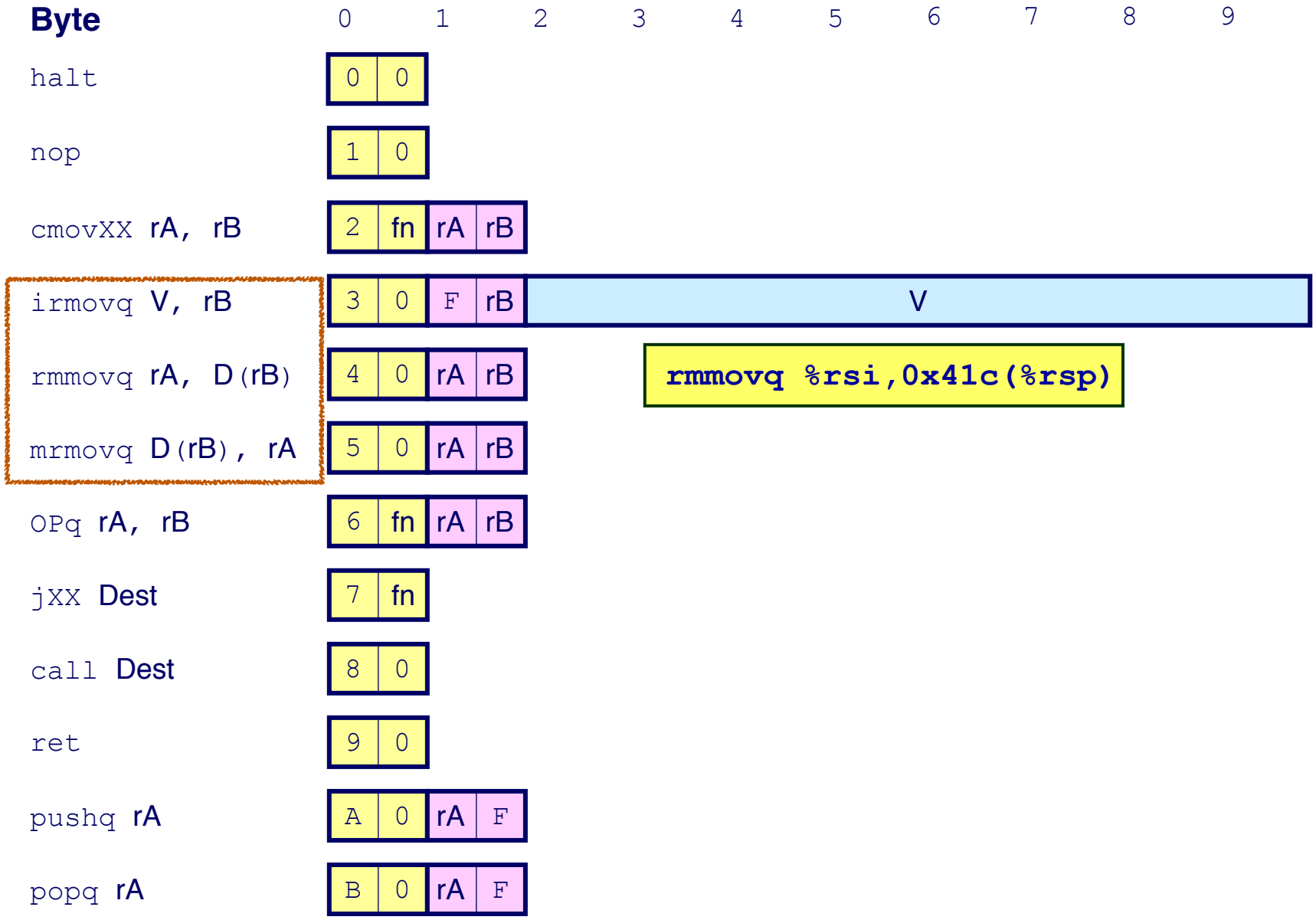

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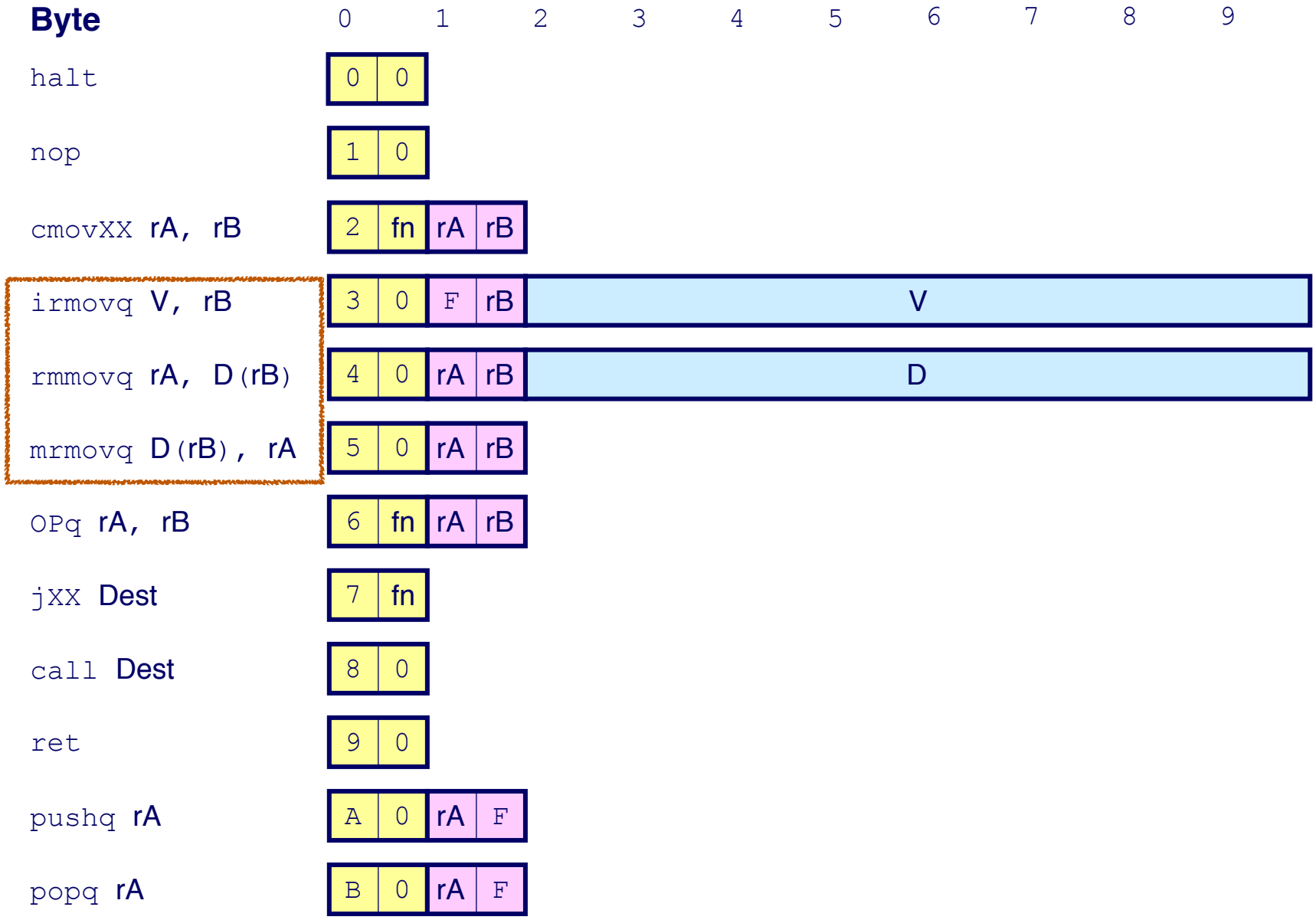

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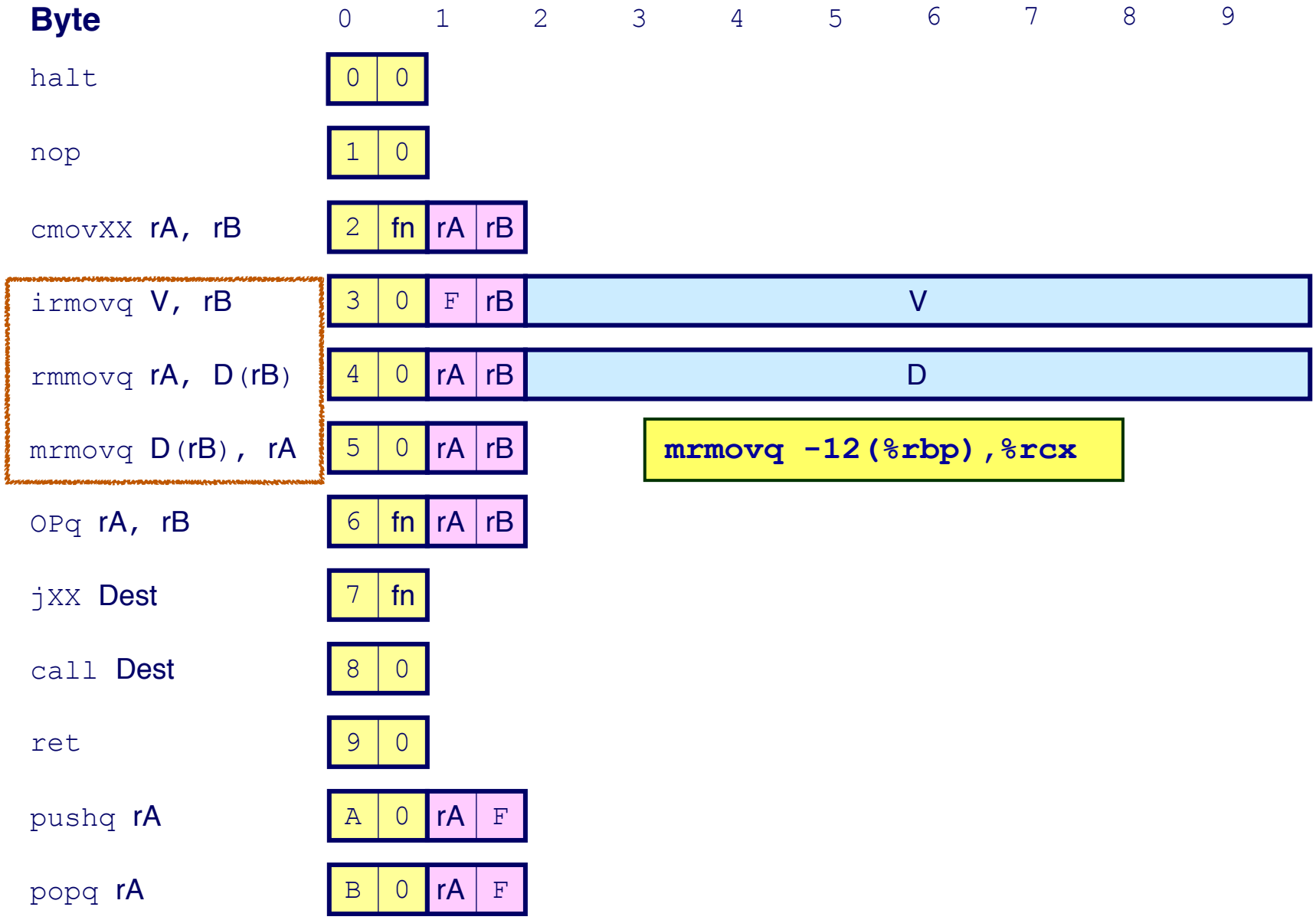

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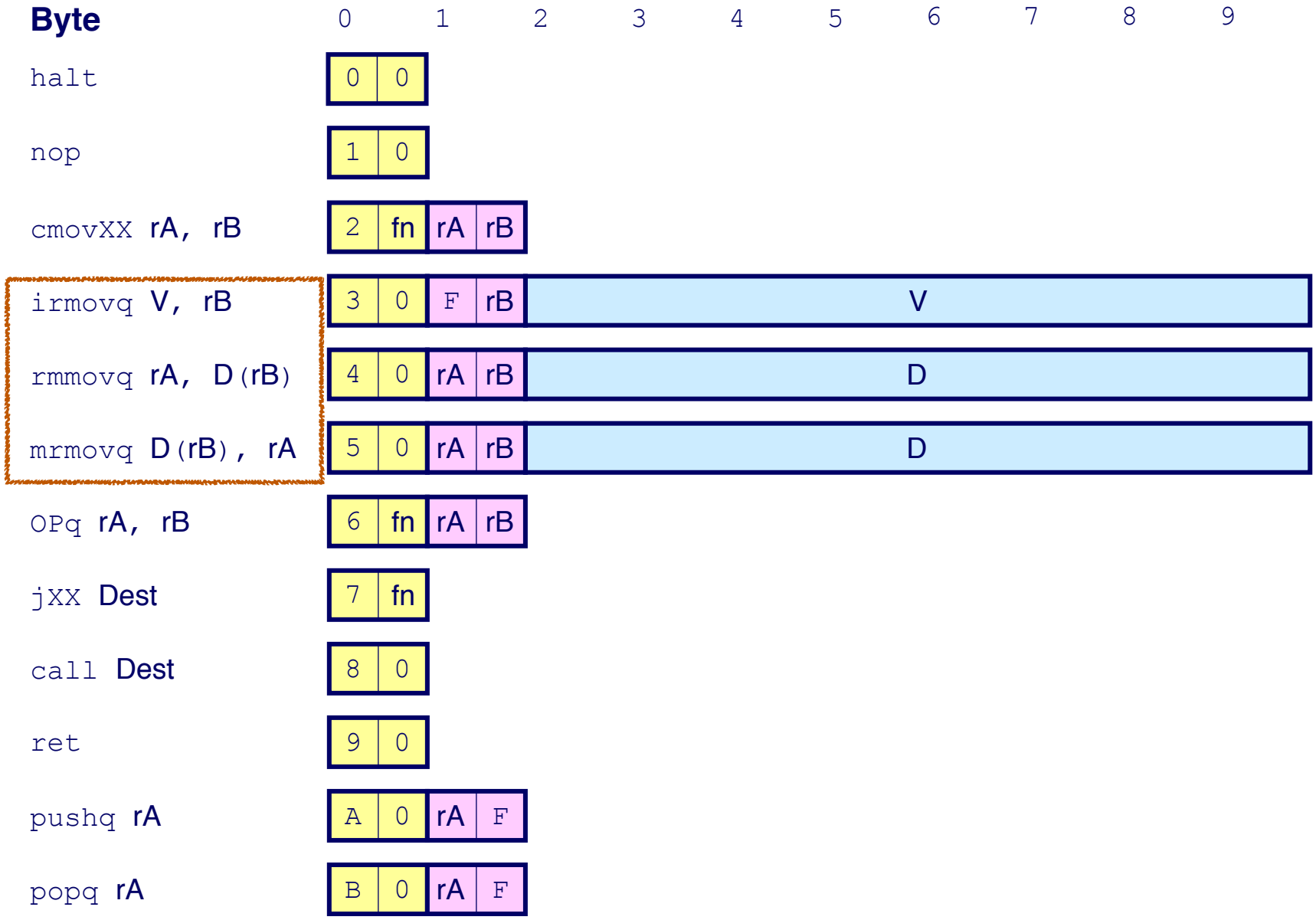

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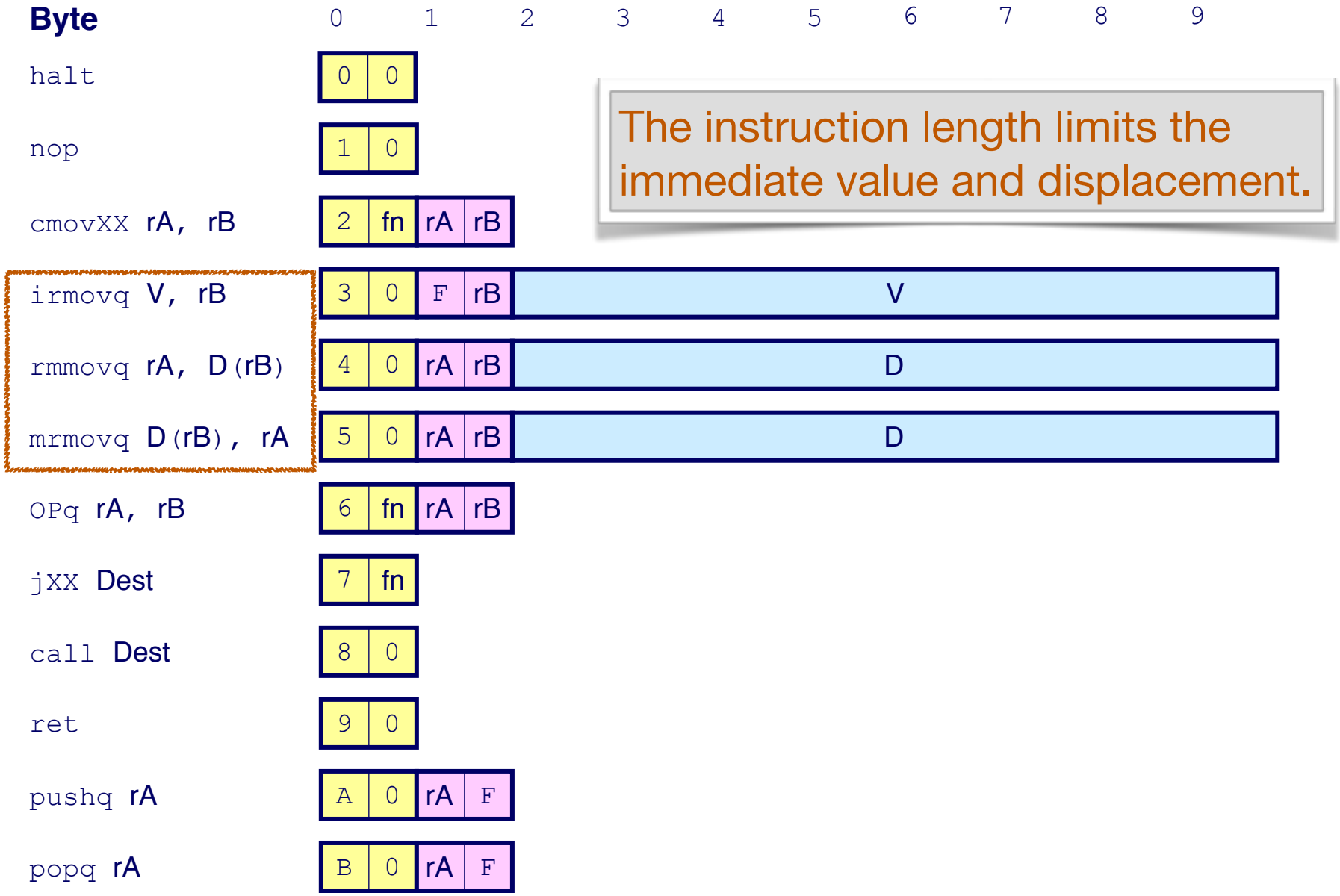


The instruction length limits the immediate value and displacement.

Move Instruction Examples

Y86-64

```
irmovq $0xabcd, %rdx
```

Encoding: `30 82 cd ab 00 00 00 00 00 00`

```
rrmovq %rsp, %rbx
```

Encoding: `20 43`

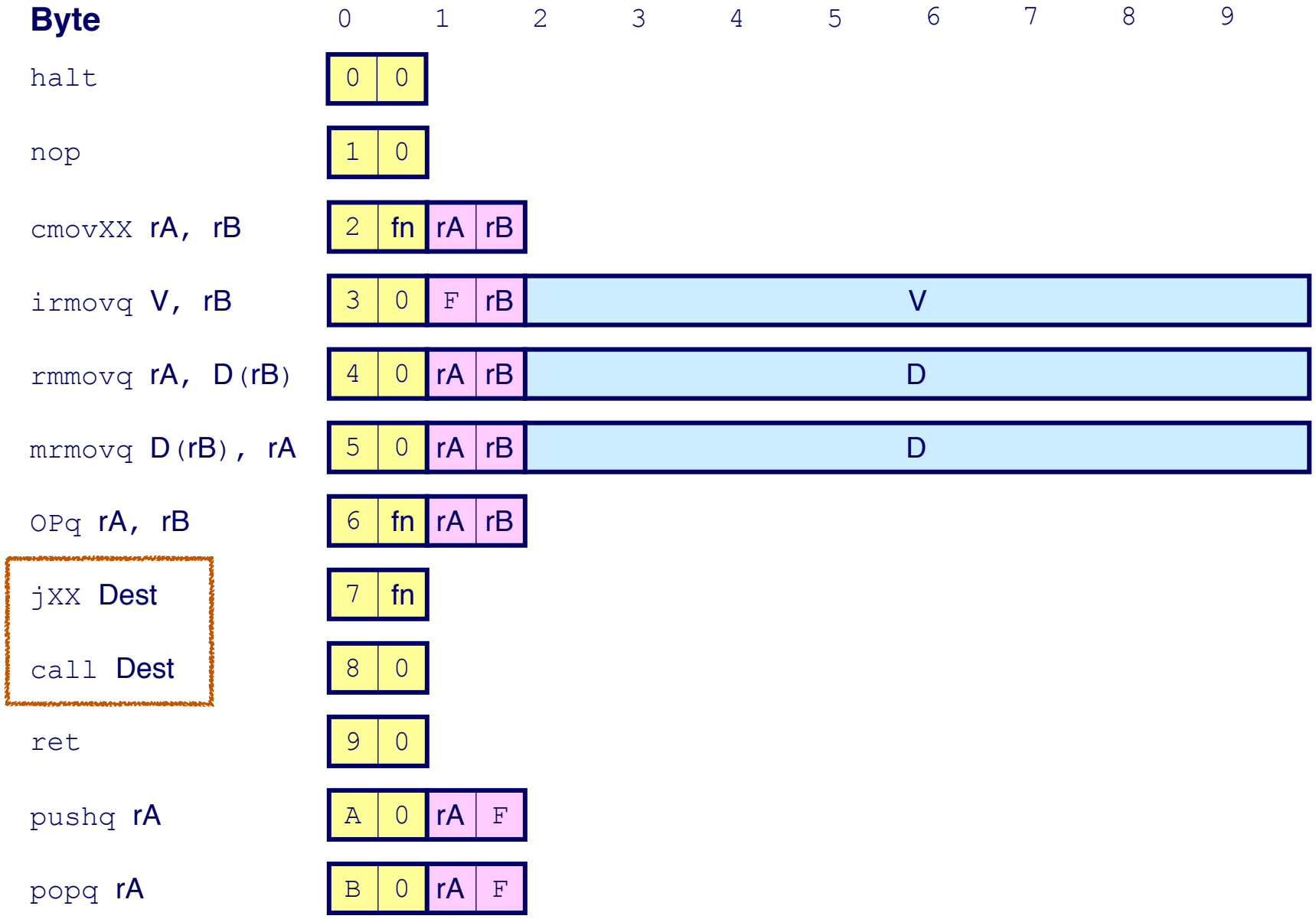
```
mrmovq -12(%rbp),%rcx
```

Encoding: `50 15 f4 ff ff ff ff ff ff ff`

```
rmmovq %rsi,0x41c(%rsp)
```

Encoding: `40 64 1c 04 00 00 00 00 00 00`

Jump/Call Instructions



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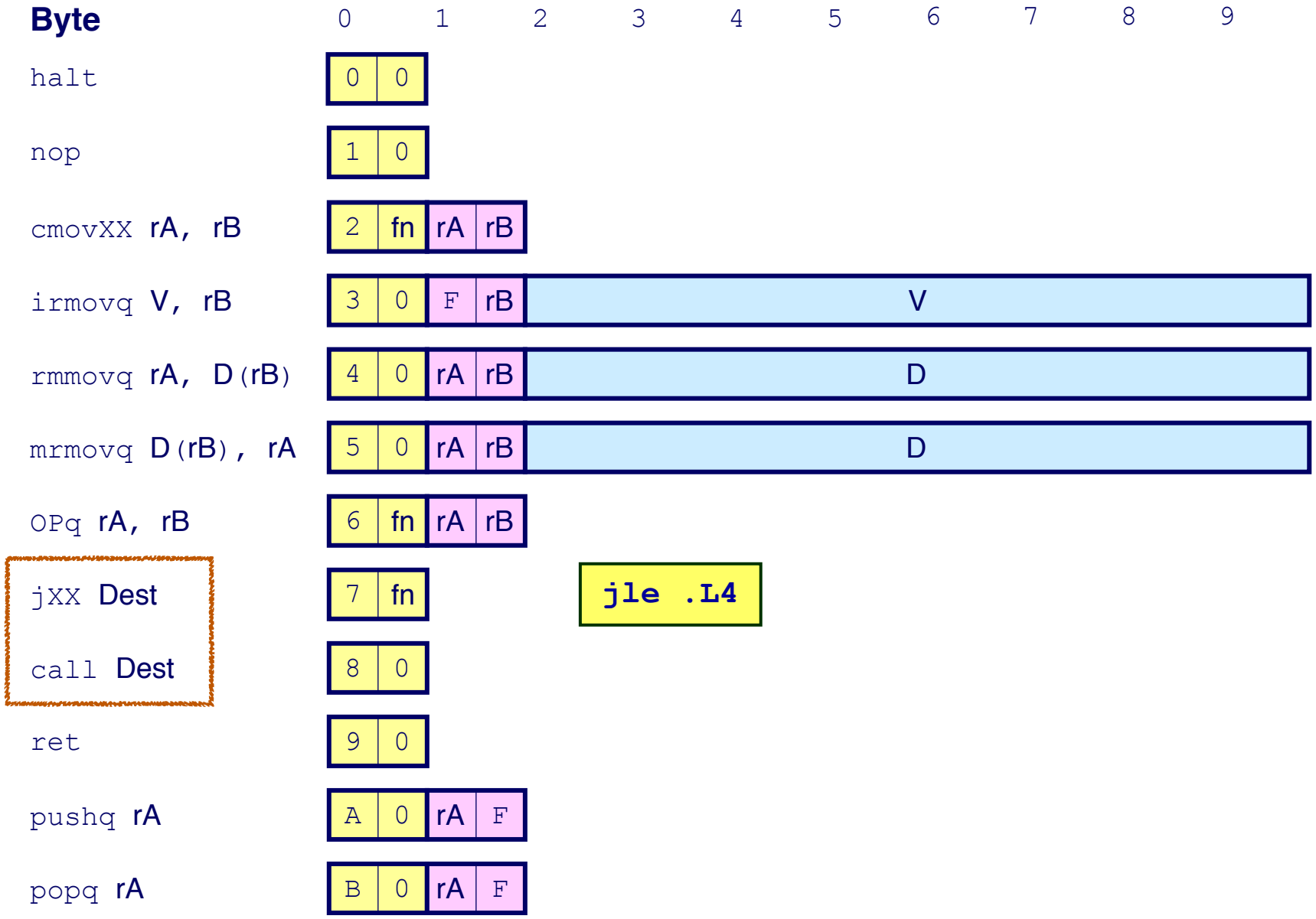

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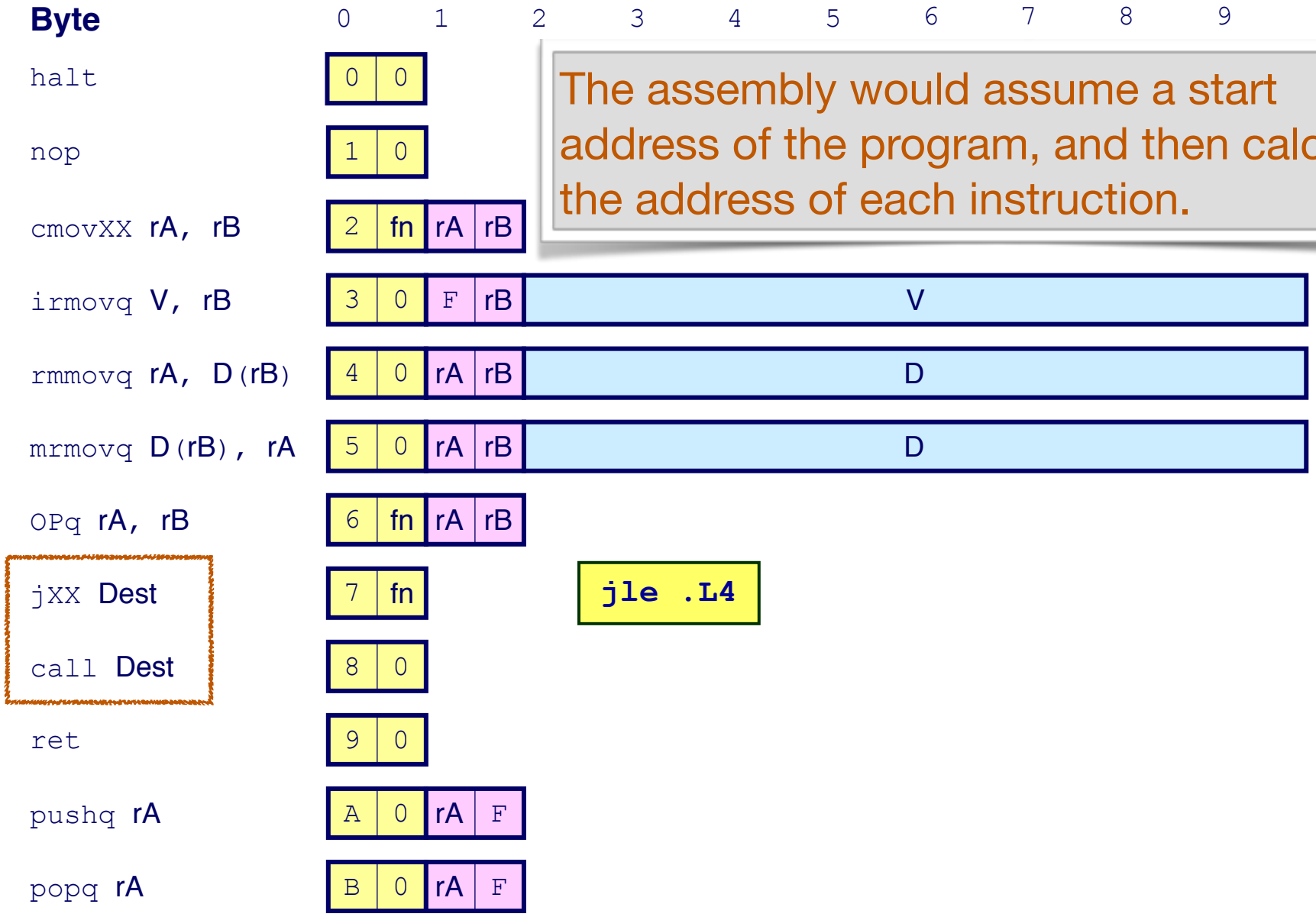

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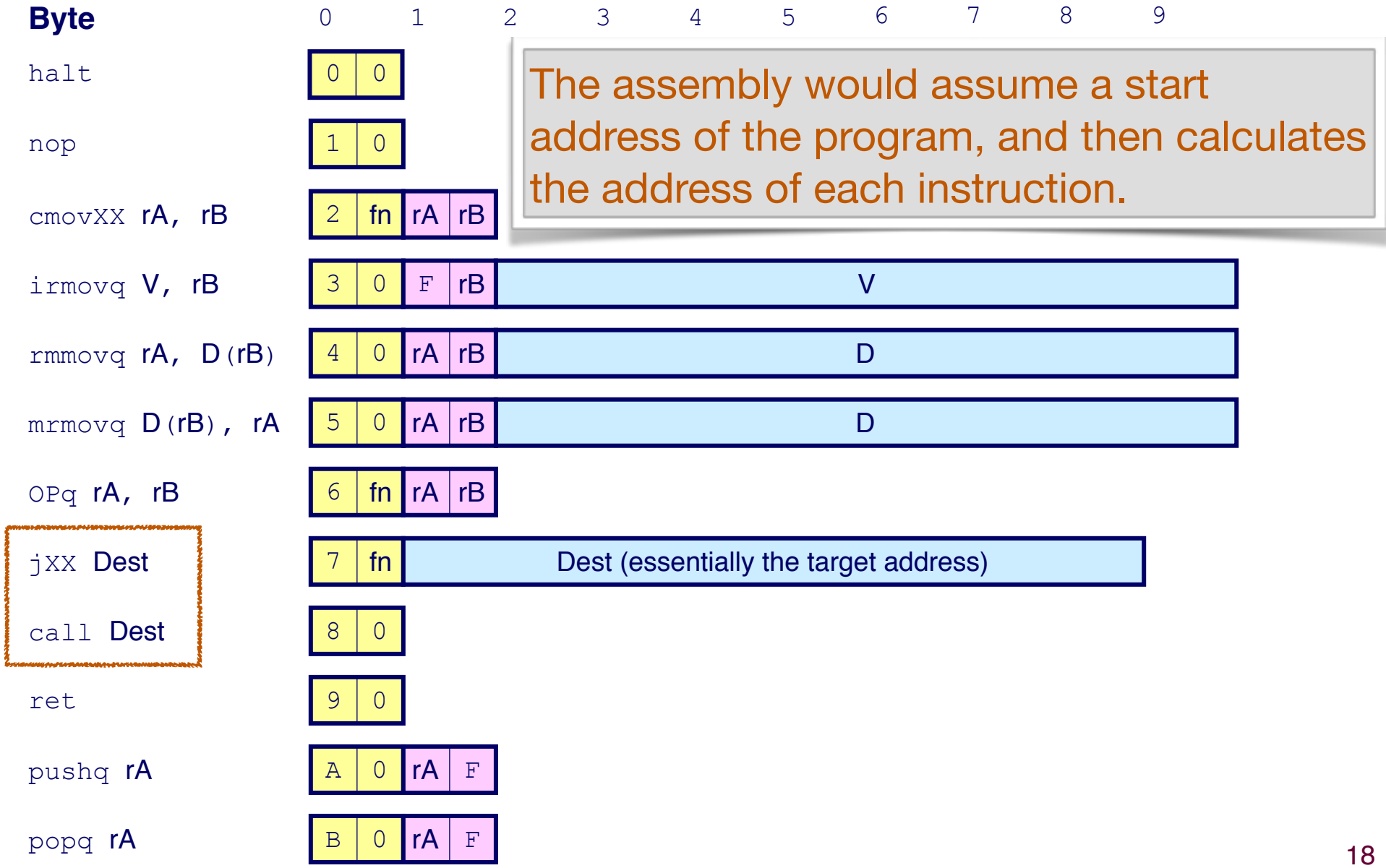

The assembly would assume a start address of the program, and then calculates the address of each instruction.

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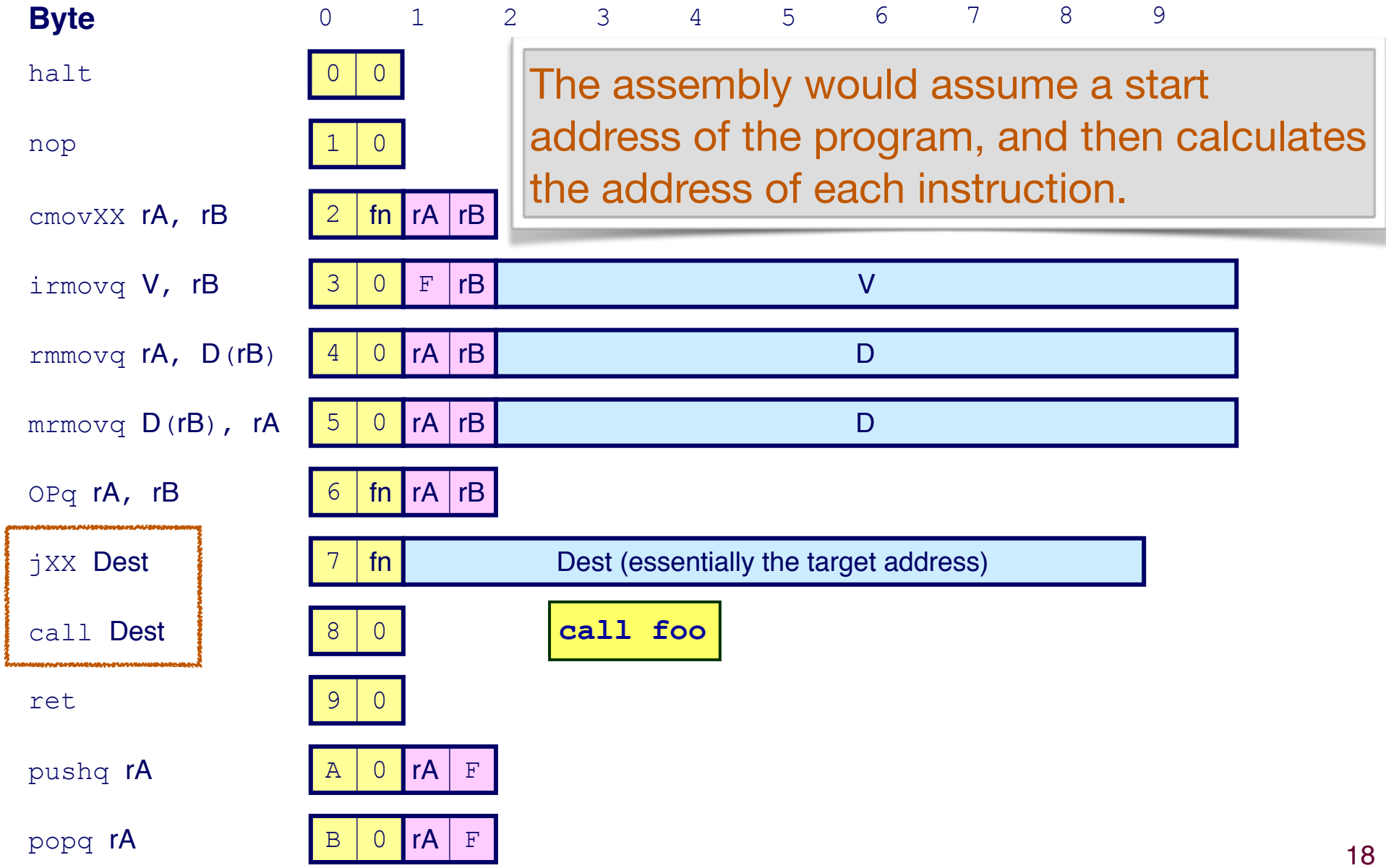

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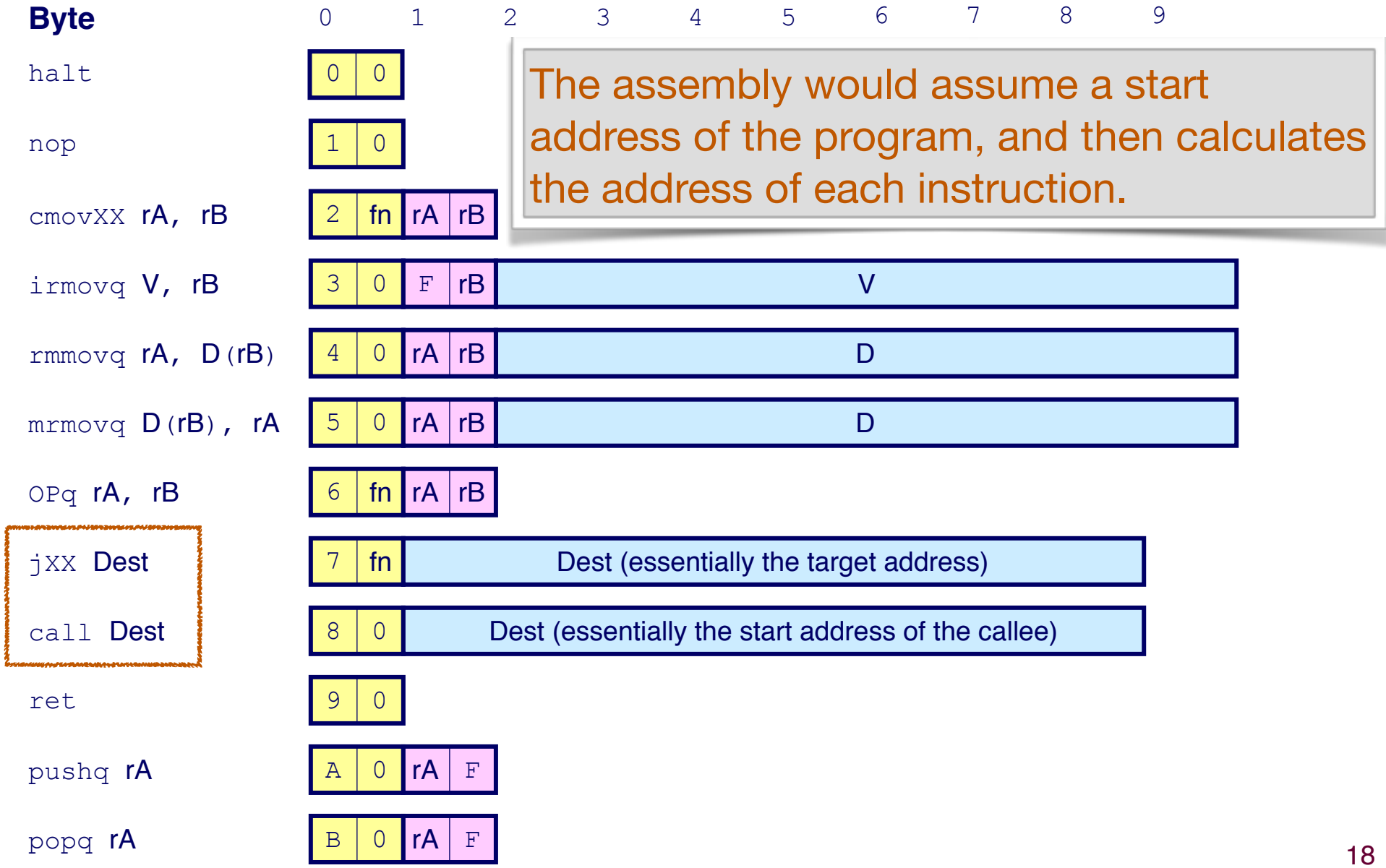

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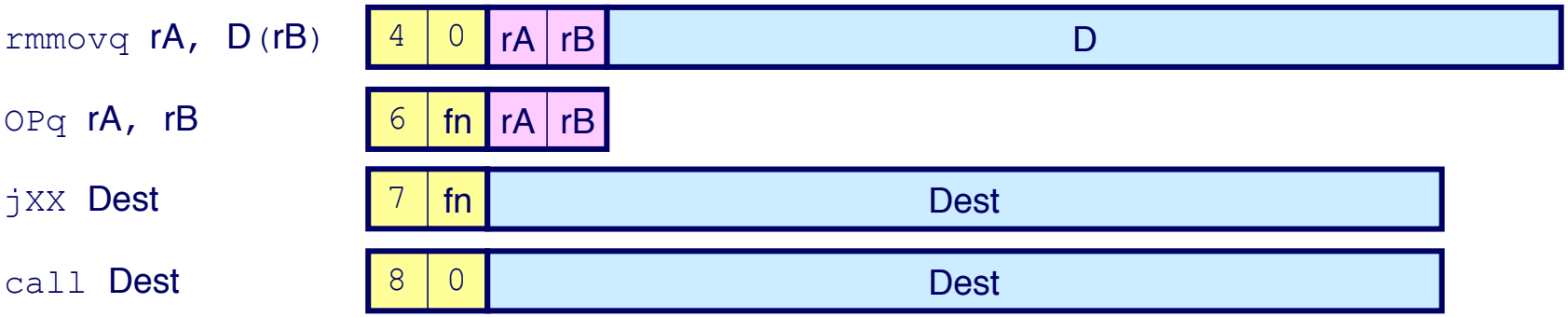

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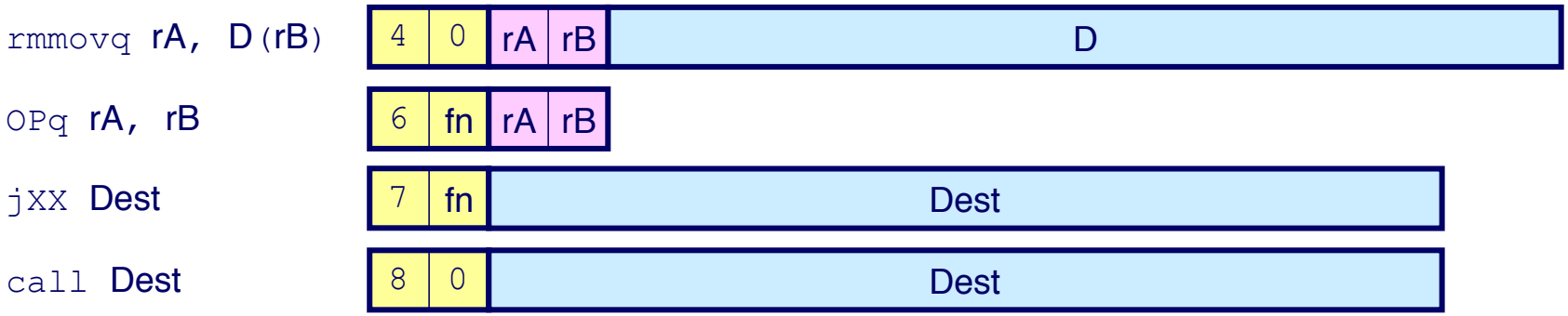


```
0x100    <foo>   rmmovq %rsi,0x41c(%rsp)
                 ... ...
                 ret
                 addq %rax,%rsi
                 call <foo>
                 jmp .L0
                 ... ...
         .L0     irmovq $0xabcd, %rdx
```

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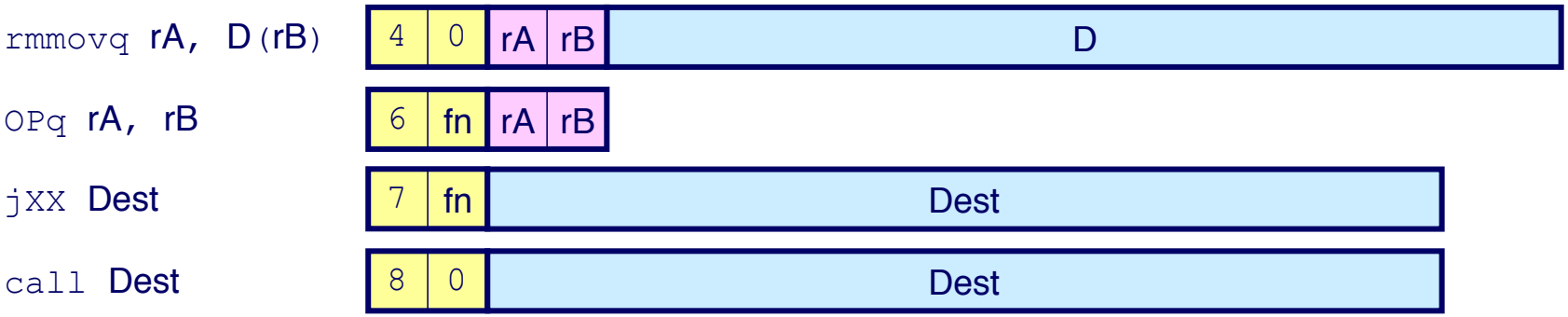


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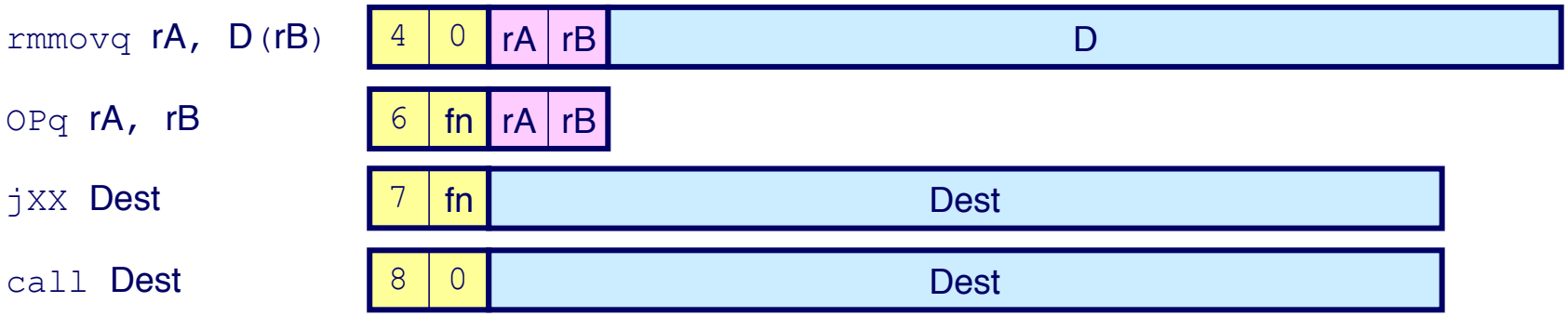


```
0x100    <foo>   rmmovq %rsi,0x41c(%rsp)    40 64 1c 04 00 00 00 00 00 00
                 ... ...
                 ret                       90
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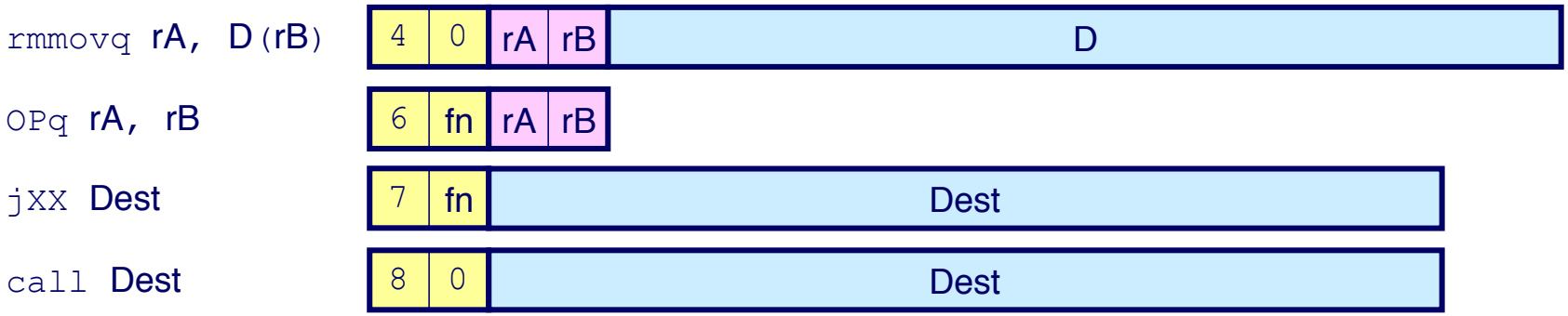


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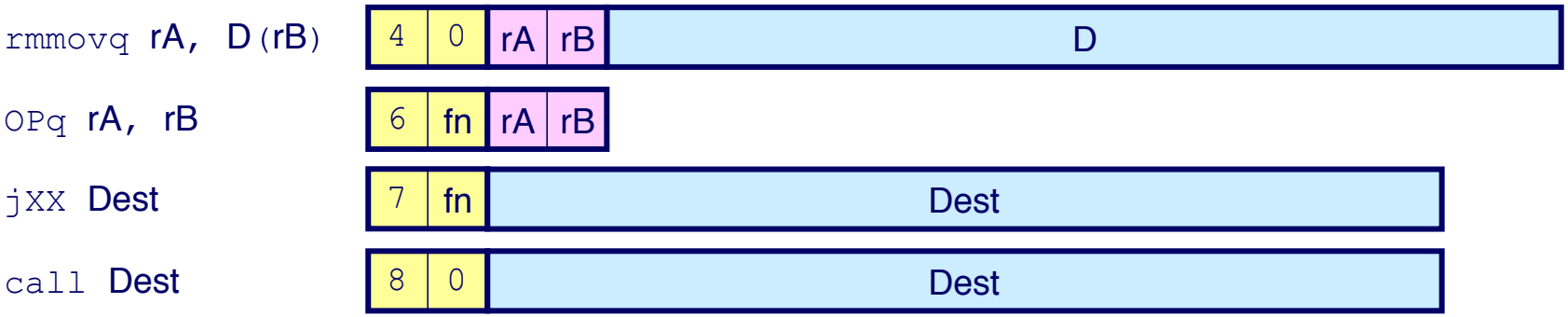


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                 ... ...
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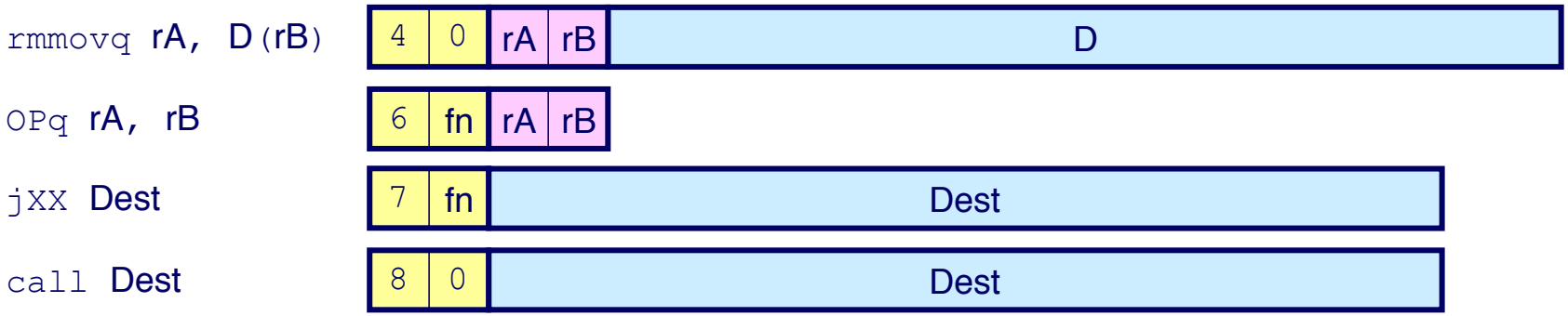


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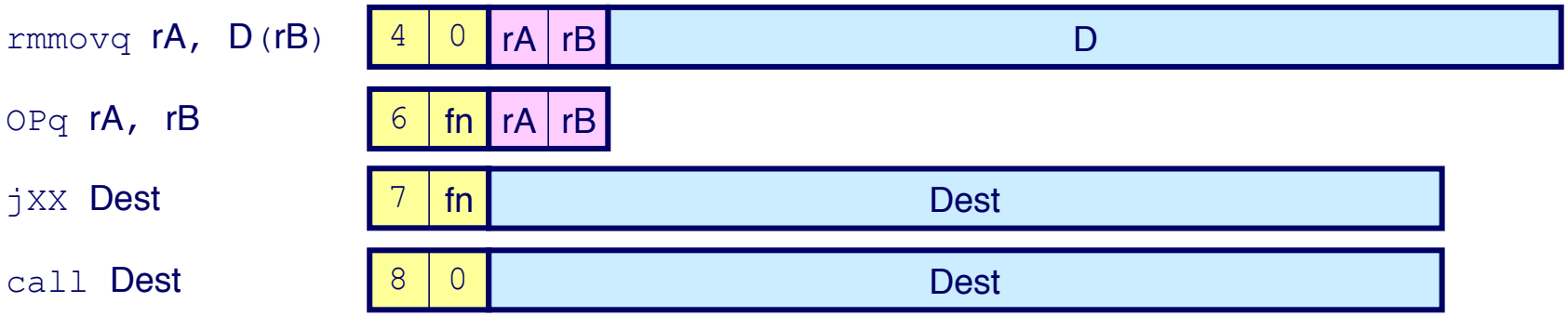


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```

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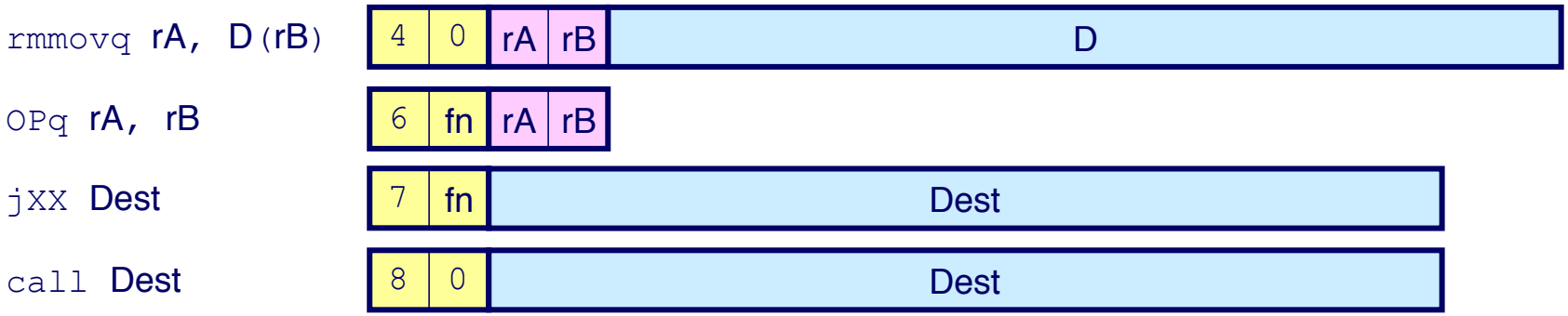


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```

0x100 + the lengths of all instructions in-between

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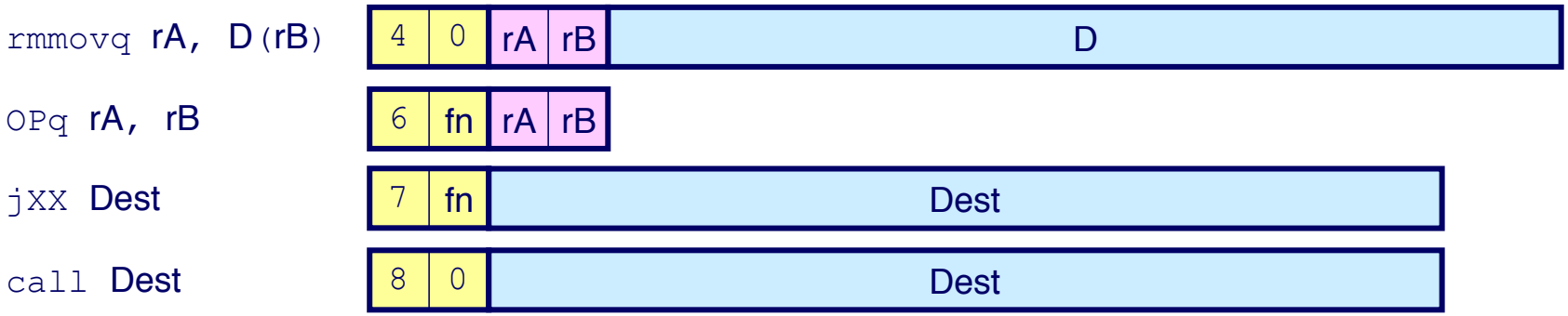


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```

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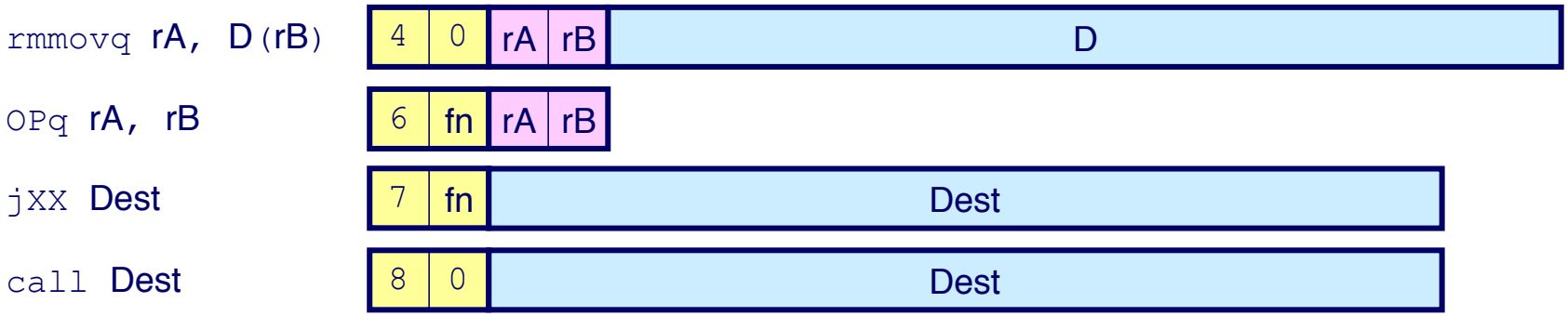


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                 ... ...
0x200    .L0     irmovq $0xabcd, %rdx       30 f2 cd ab 00 00 00 00 00 00
```
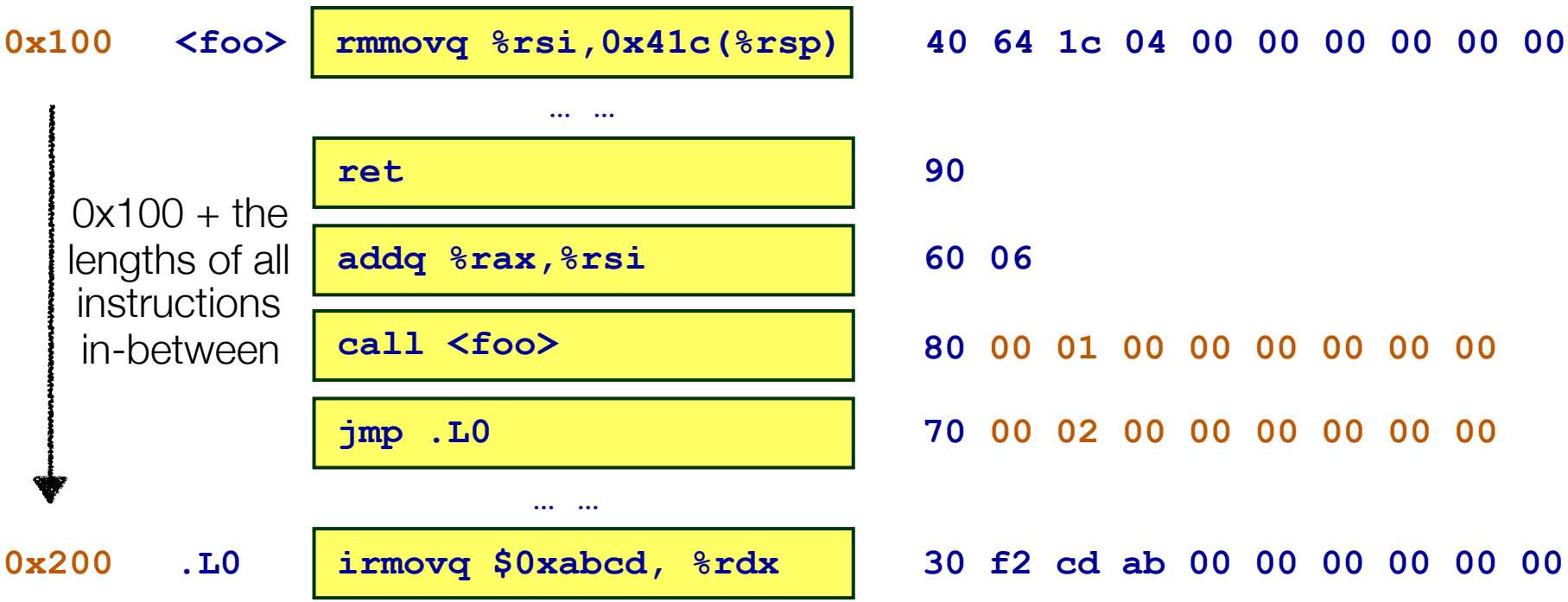

0x100 + the lengths of all instructions in-between

How Does An Assembler Work?

- The assembler is a program that translates assembly code to binary code
- The OS tells the assembler the start address of the code (sort of…)
- Translate the assembly program line by line
- Need to build a “label map” that maps each label to its address



Jump Instructions

Jump Unconditionally

Jump When Less or Equal

Jump When Less

Jump When Equal

Jump When Not Equal

Jump When Greater or Equal

Jump When Greater

Subroutine Call and Return

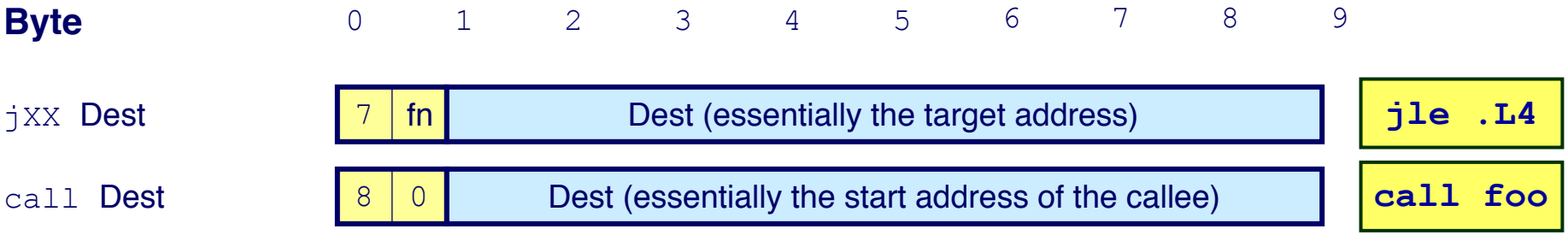
`call` Dest

- Push address of next instruction onto stack
- Start executing instructions at Dest
- Like x86-64

`ret`

- Pop value from stack
- Use as address for next instruction
- Like x86-64

One More Complication…



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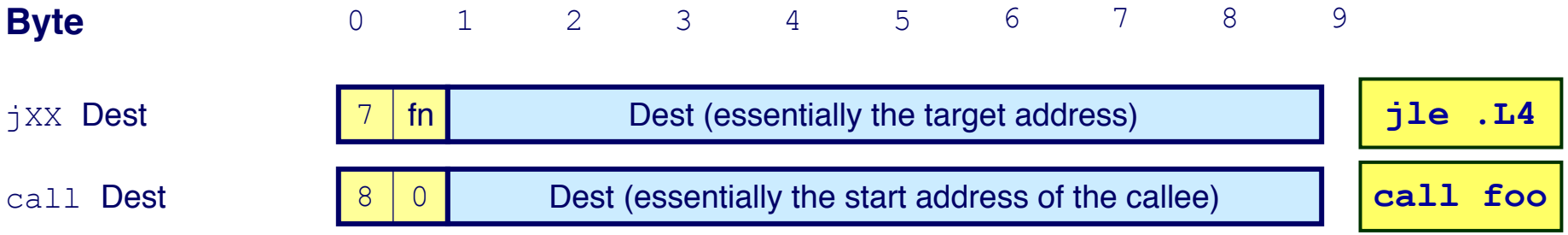

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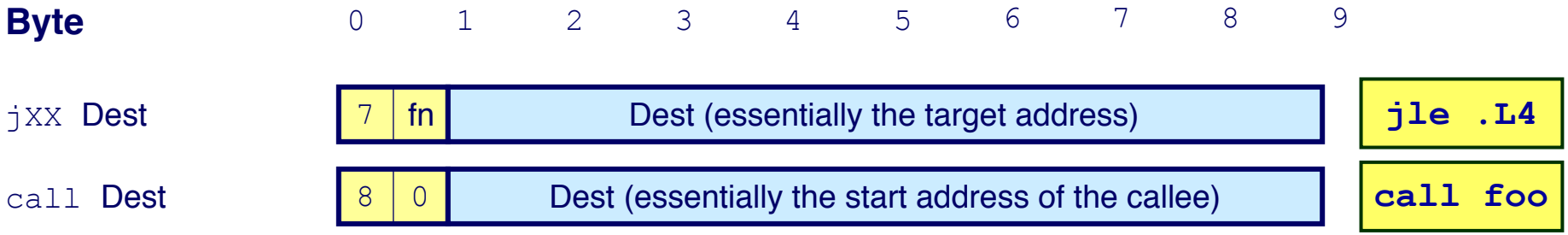

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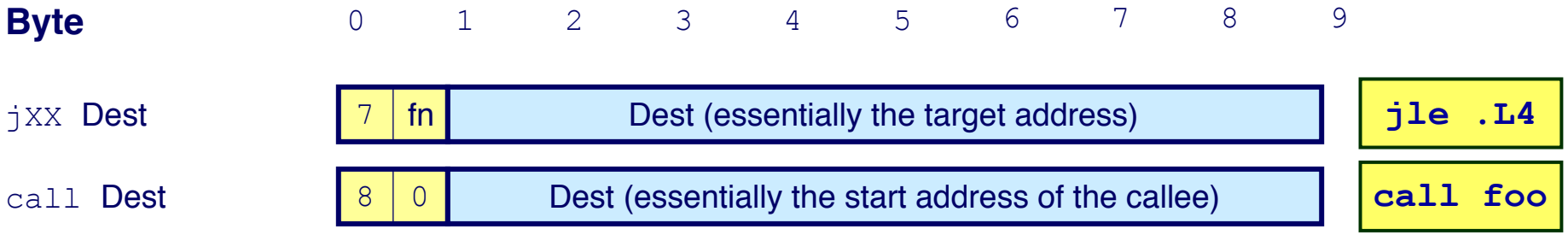

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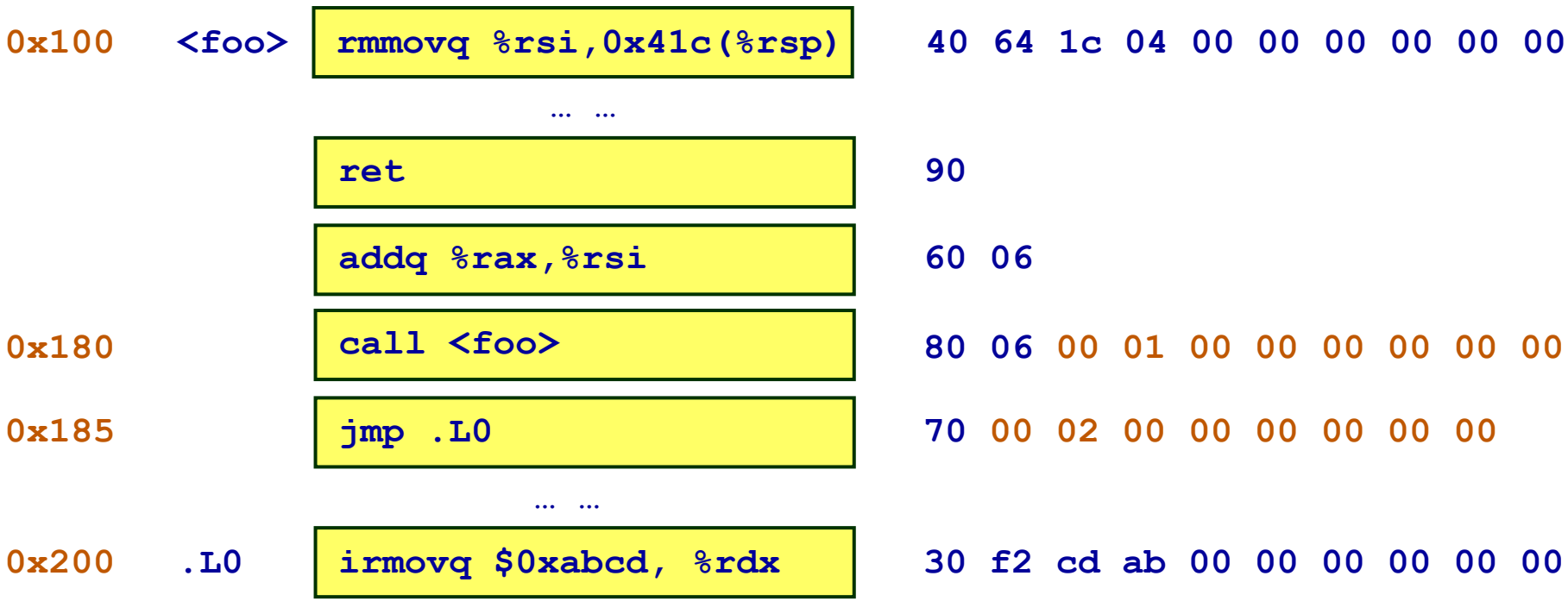
- One alternative: use a super long instruction encoding format.
  - Simple to encode, but space inefficient (waste bits for jumps to short addr.)
- Another alternative: encode the relative address, not the absolute address
  - E.g., encode (.L4 - current address) in Dest

Using Relative Addresses for Jumps

- What if the ISA encoding uses relative address for jump and call?



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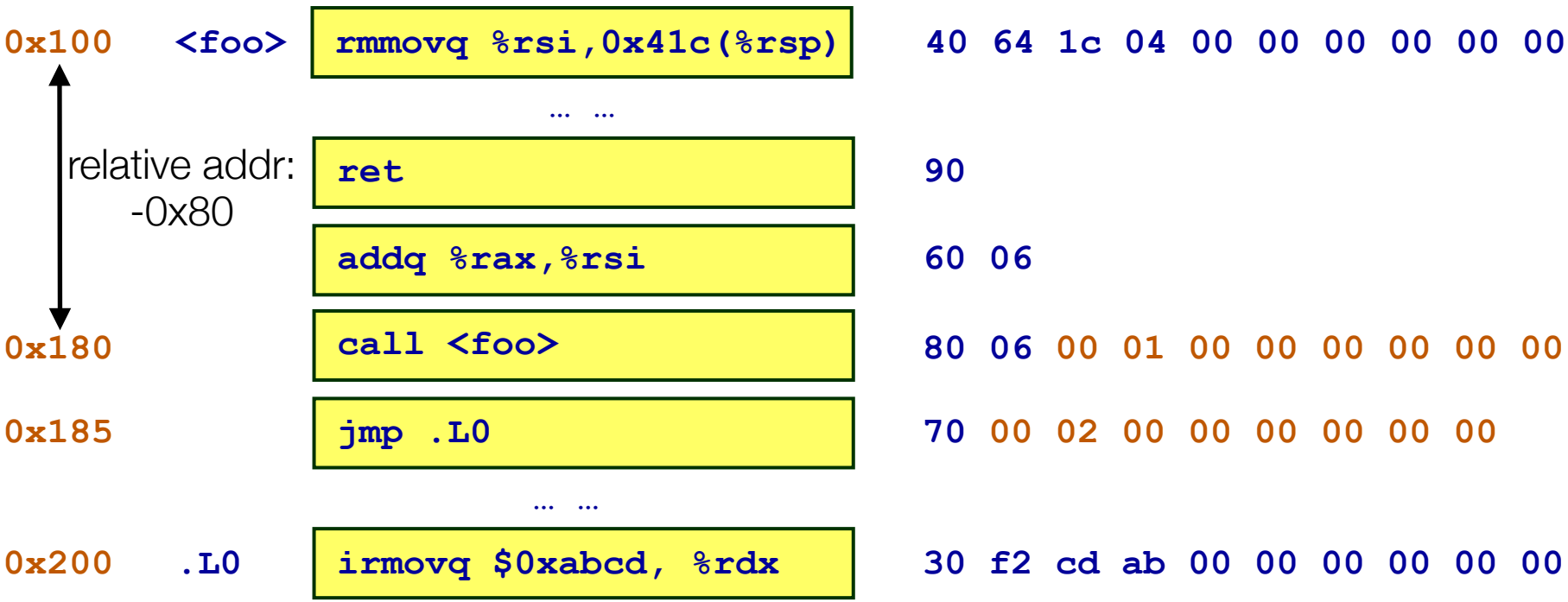

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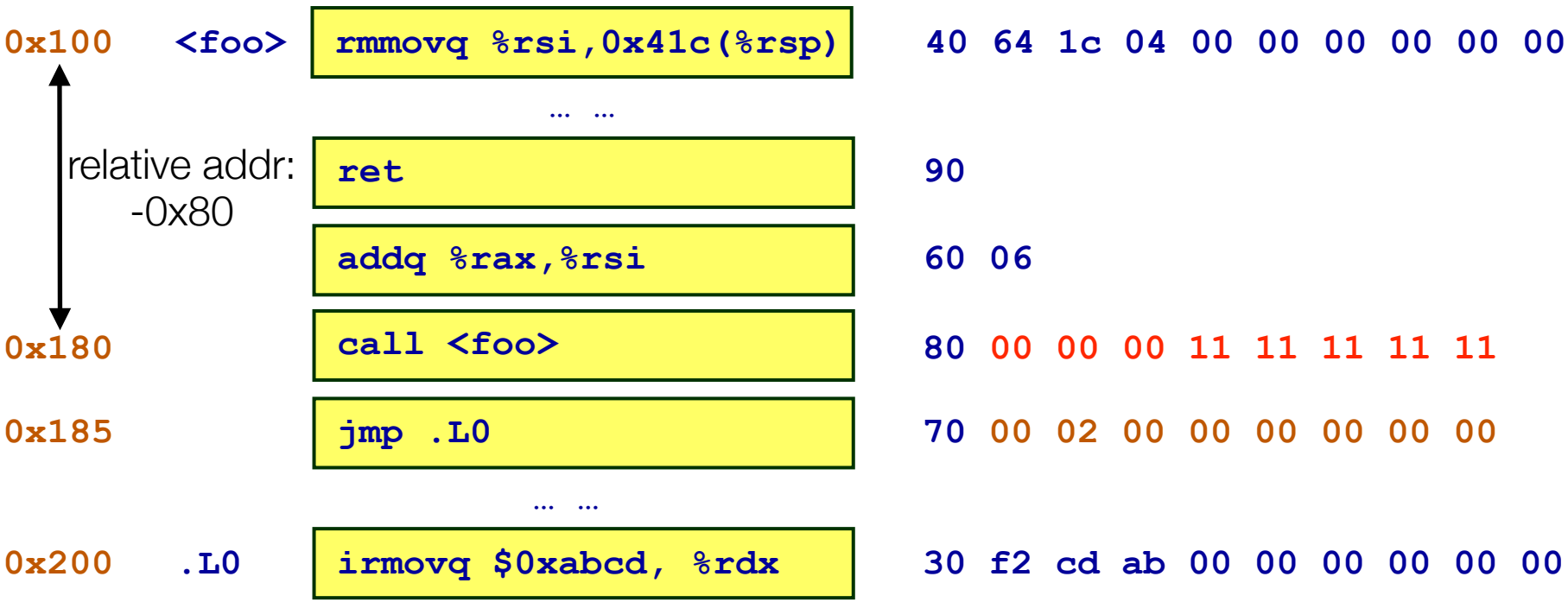

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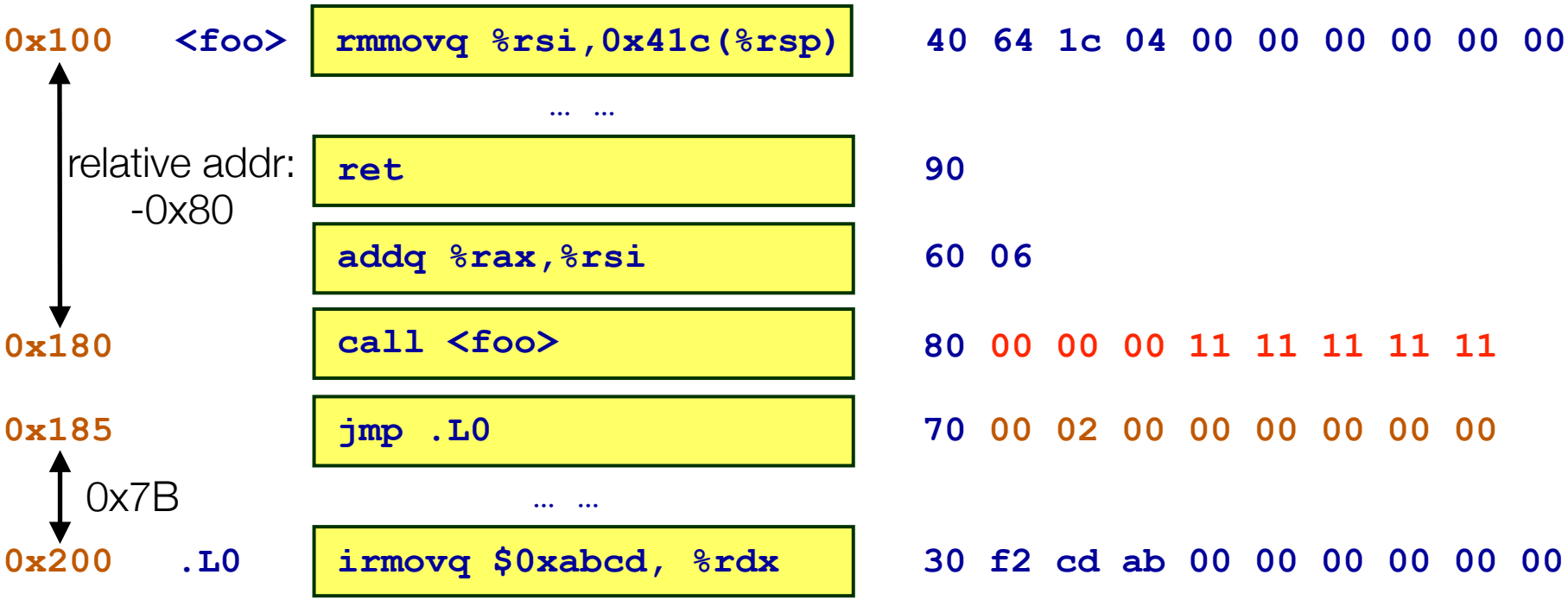

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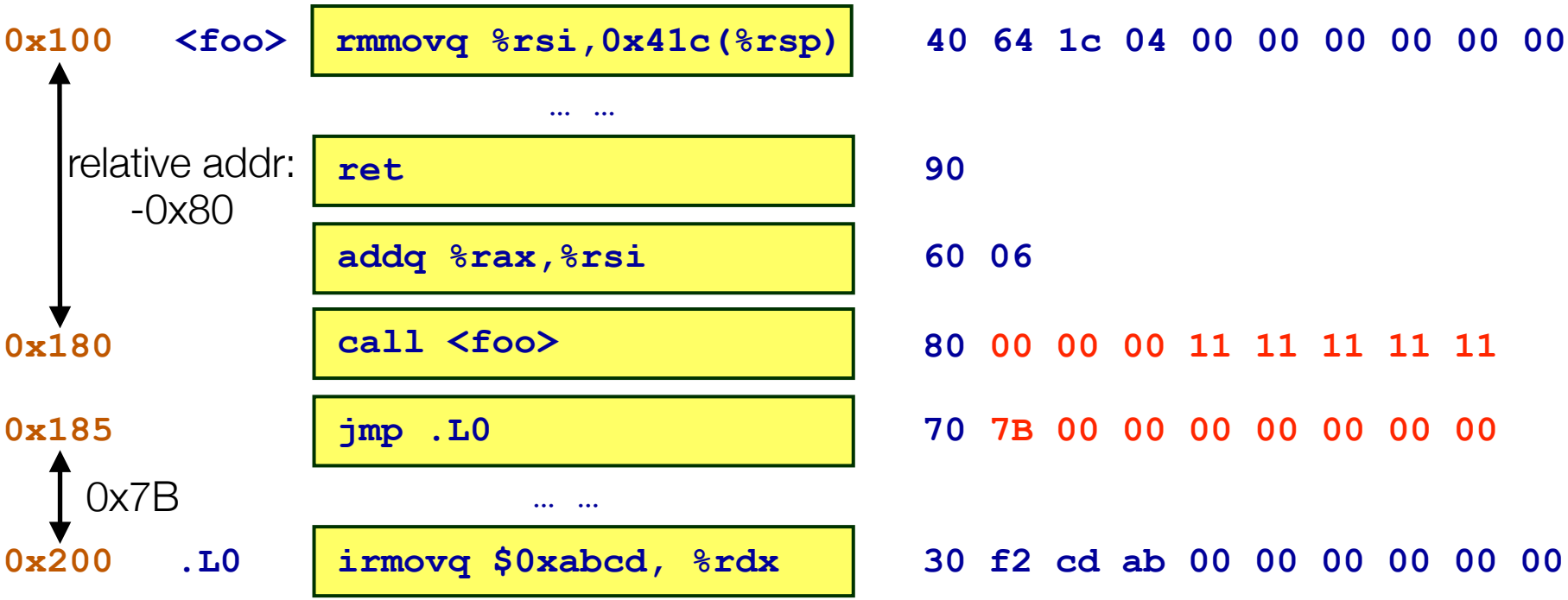

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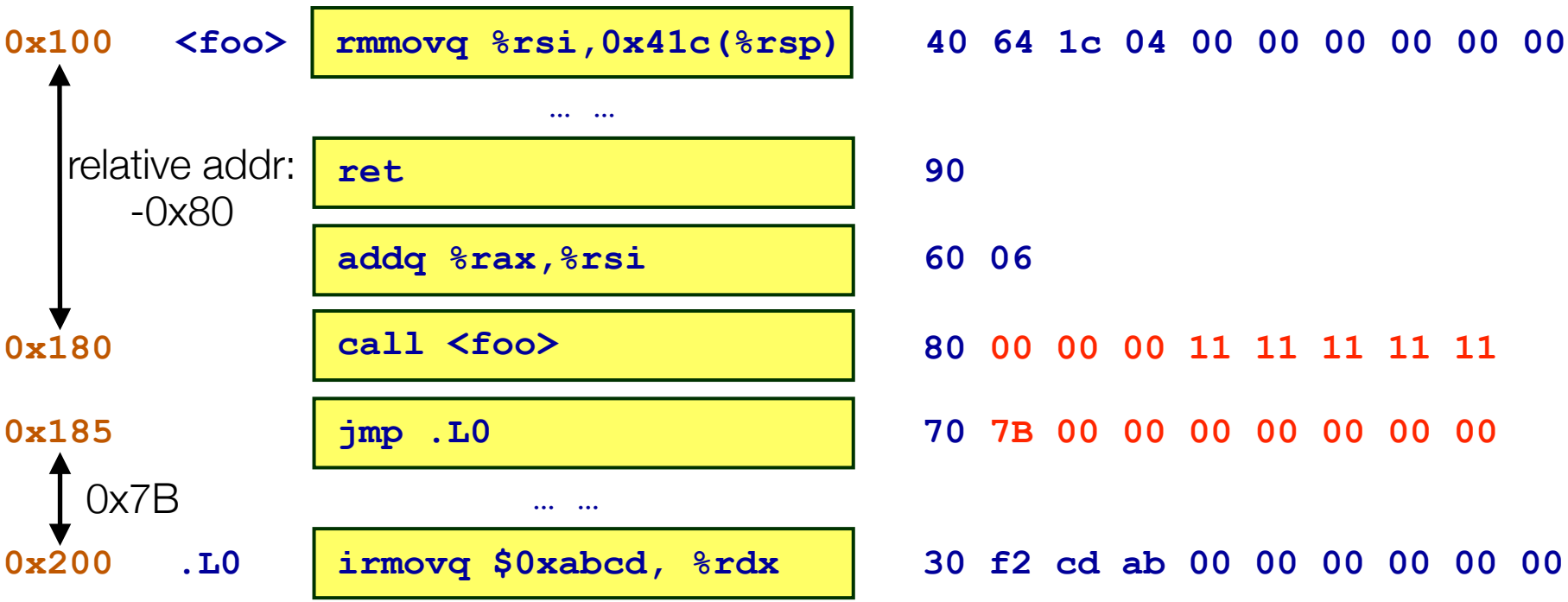

Using Relative Addresses for Jumps

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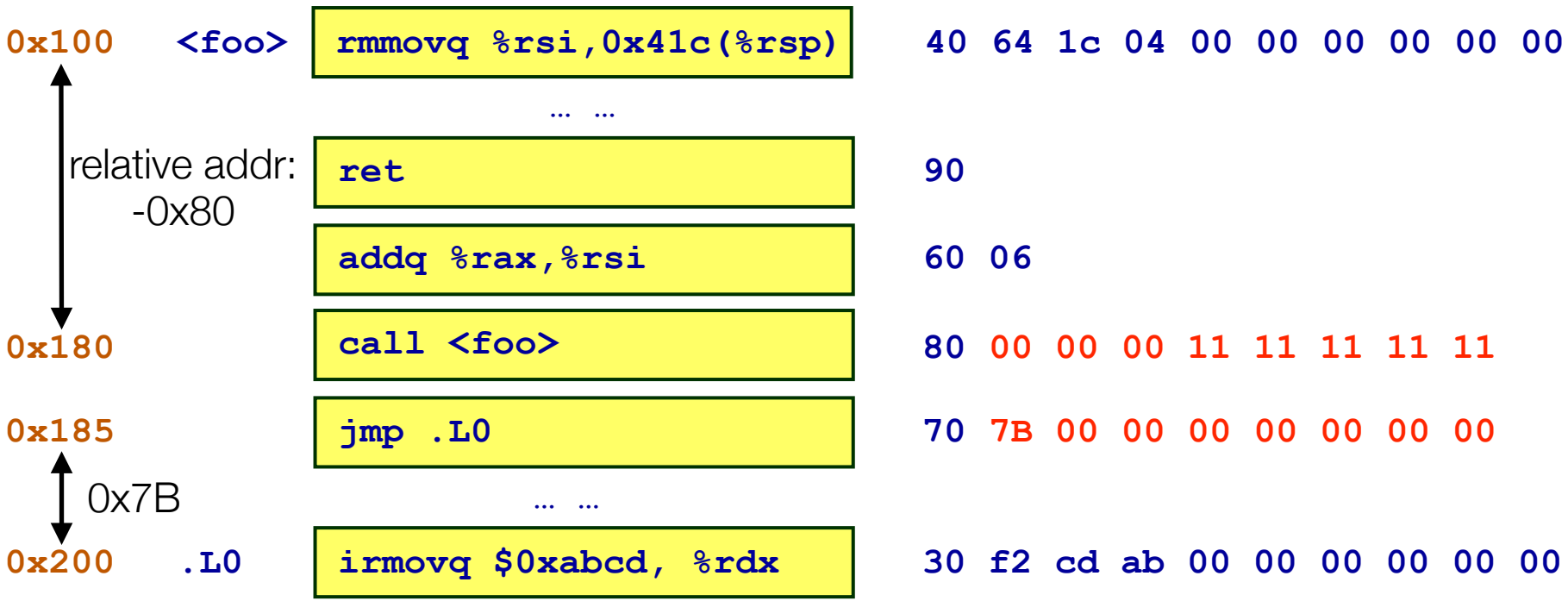
- This code is called Position-Independent Code (PIC)



Miscellaneous Instructions

- Don’t do anything

- Stop executing instructions
- Usually can’t be executed in the user mode, only by the OS
- Encoding ensures that program hitting memory initialized to zero will halt

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  - Can have arbitrary number of instructions: easy to add new inst.

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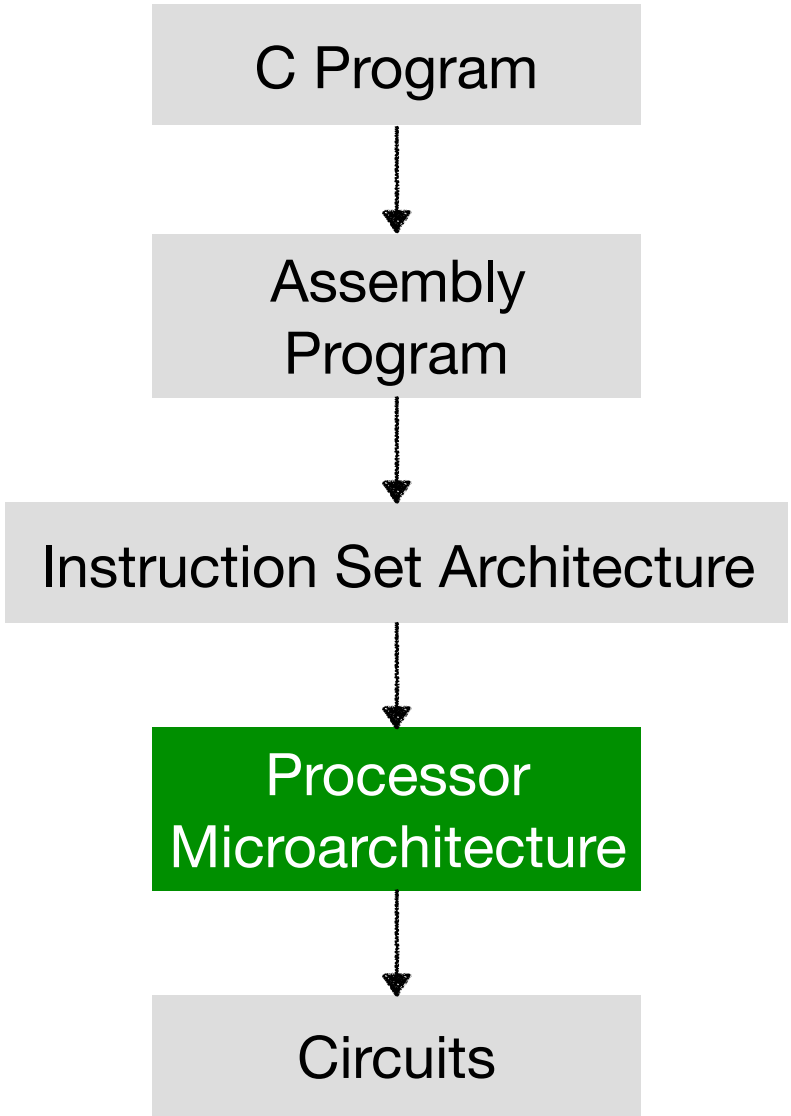
- A good writeup showing some of the complexity involved: http://www.c-jump.com/CIS77/CPU/x86/lecture.html

So far in 252…

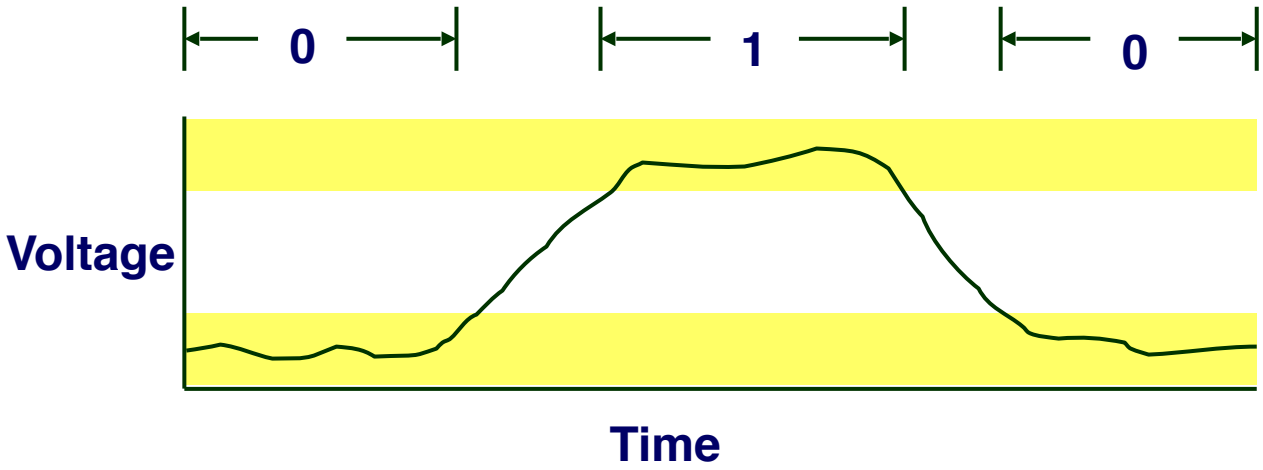

C Program
Assembly Program
Instruction Set Architecture
Processor Microarchitecture
Circuits

Today: Circuits Basics

- Basics
- Circuits for computations
- Circuits for storing data

Overview of Circuit-Level Design

- Fundamental Hardware Requirements
  - Communication: How to get values from one place to another. Mainly three electrical **wires**.
  - Computation: **transistors**. Combinational logic.
  - Storage: **transistors**. Sequential logic.
- Circuit design is often abstracted as logic design



Today: Circuits Basics

- Transistors
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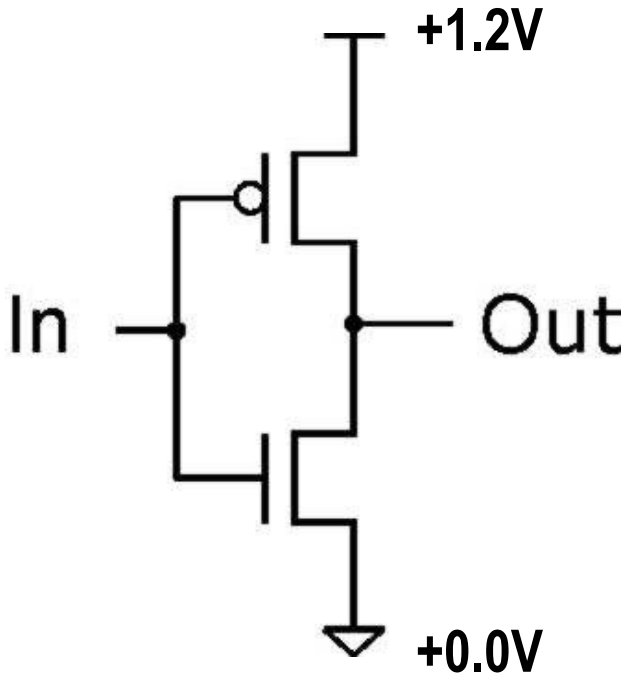
Inverter (NOT Gate)



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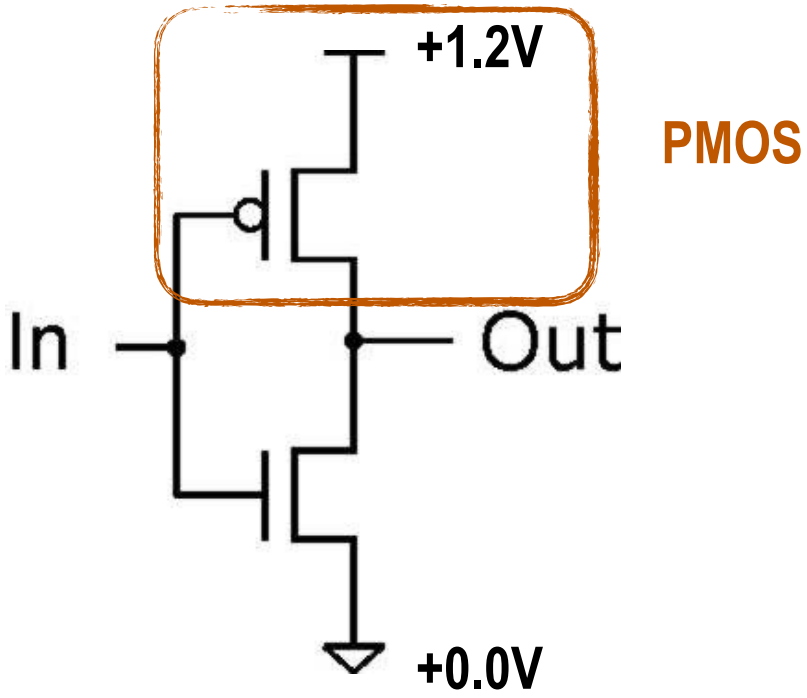

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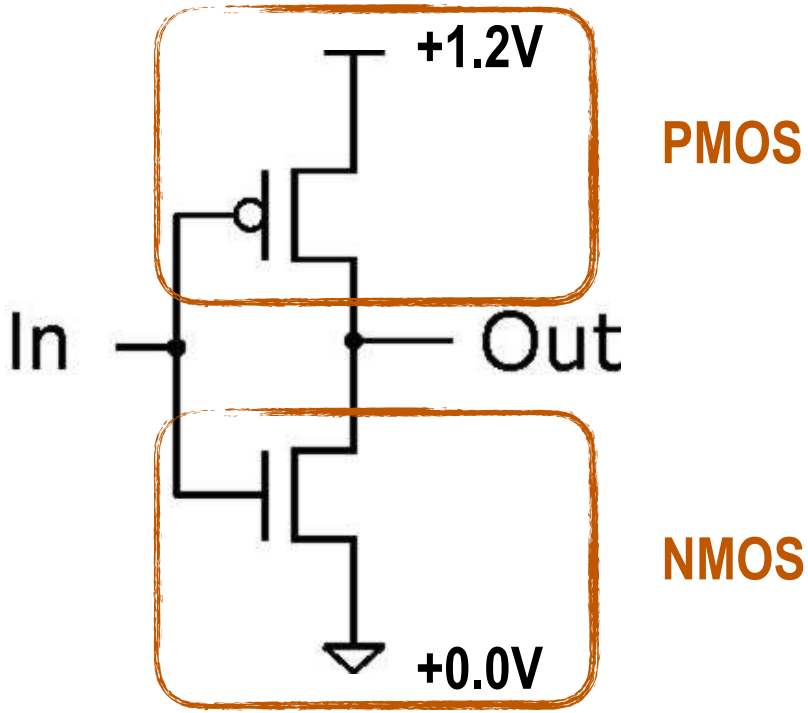

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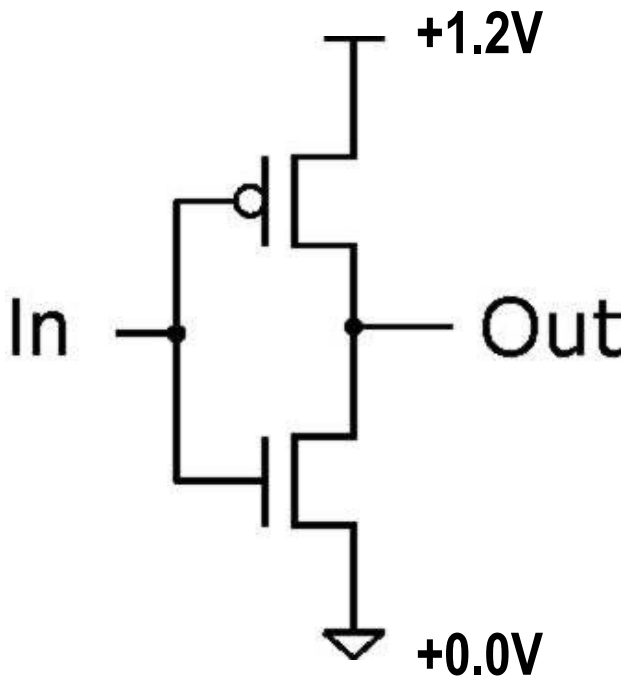

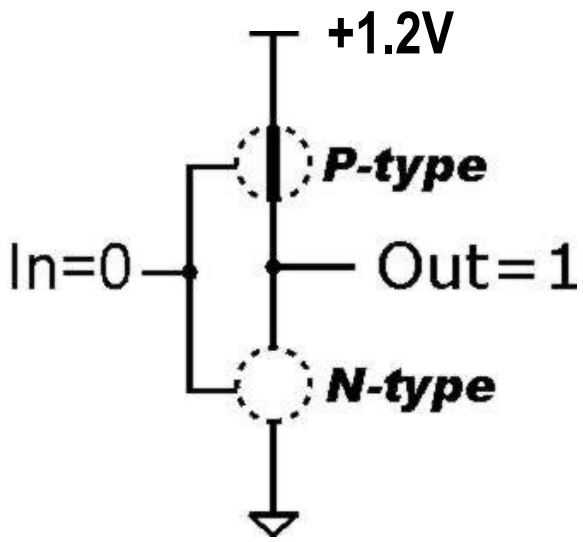

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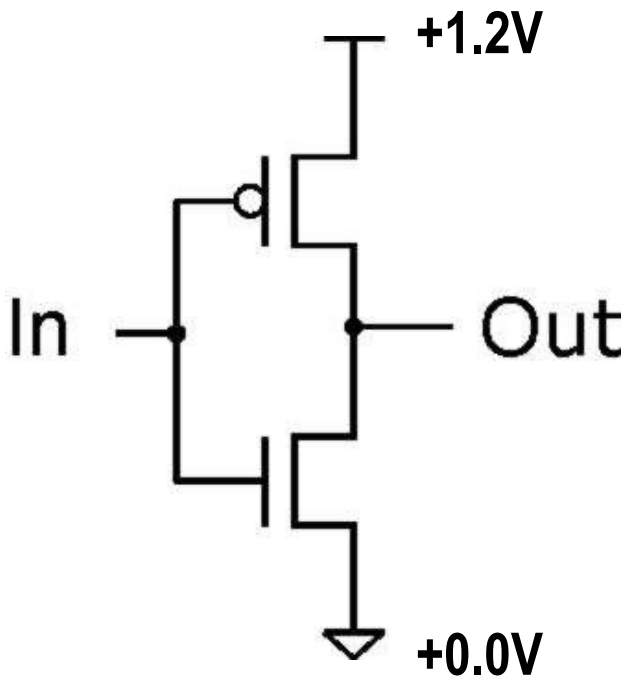

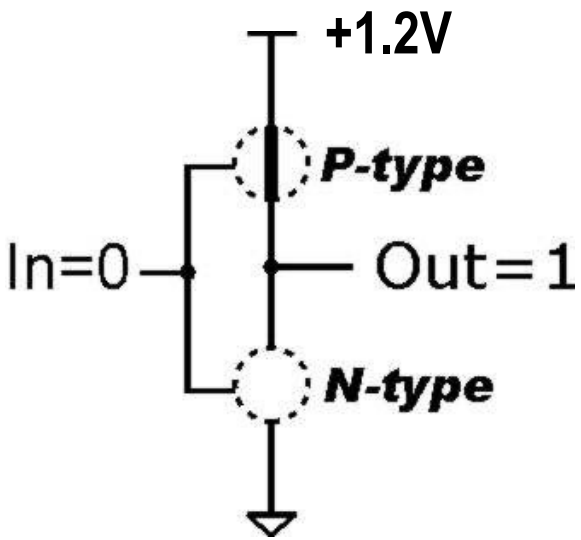

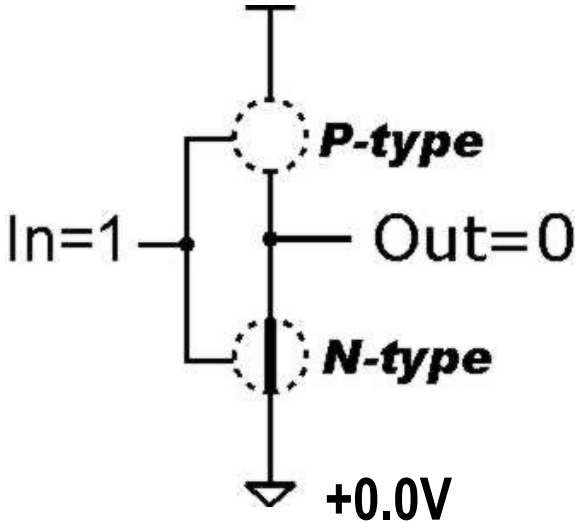

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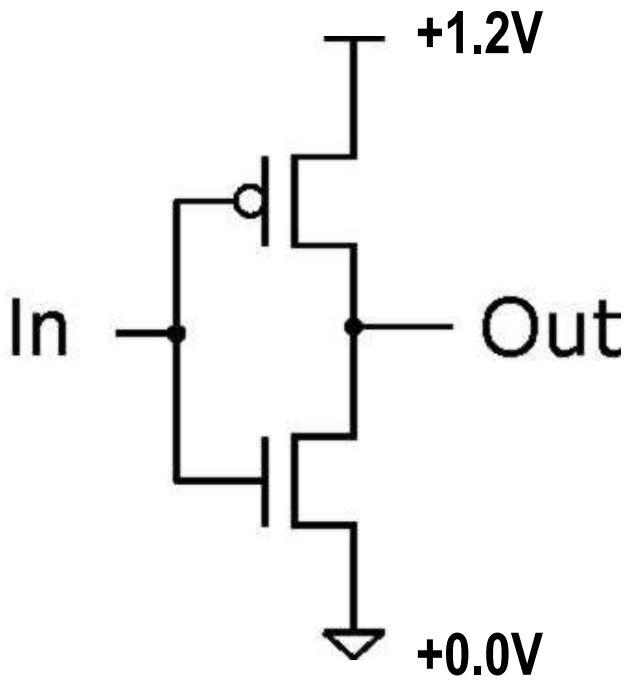
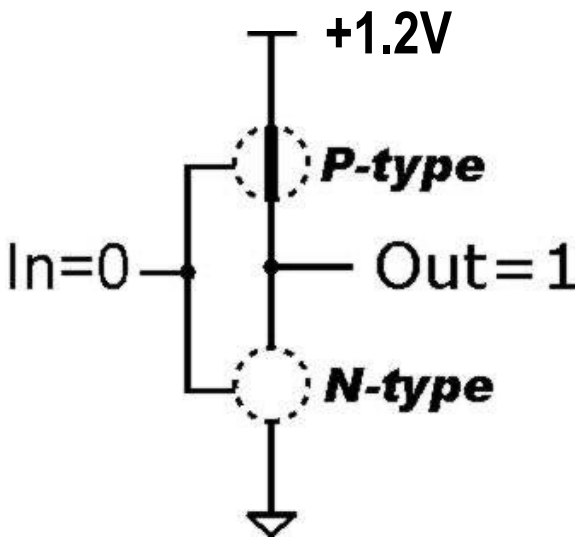
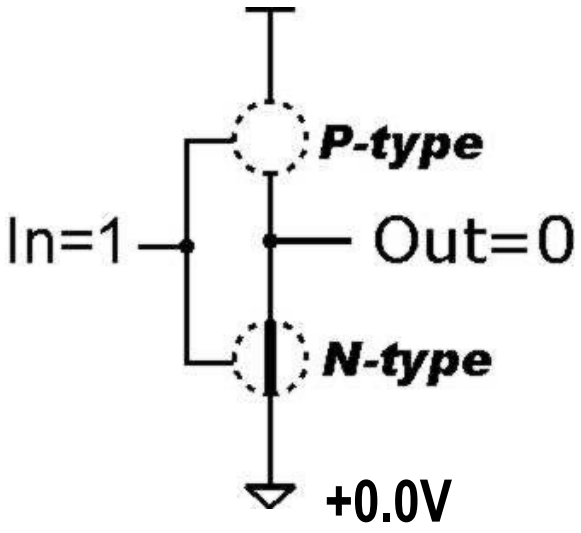
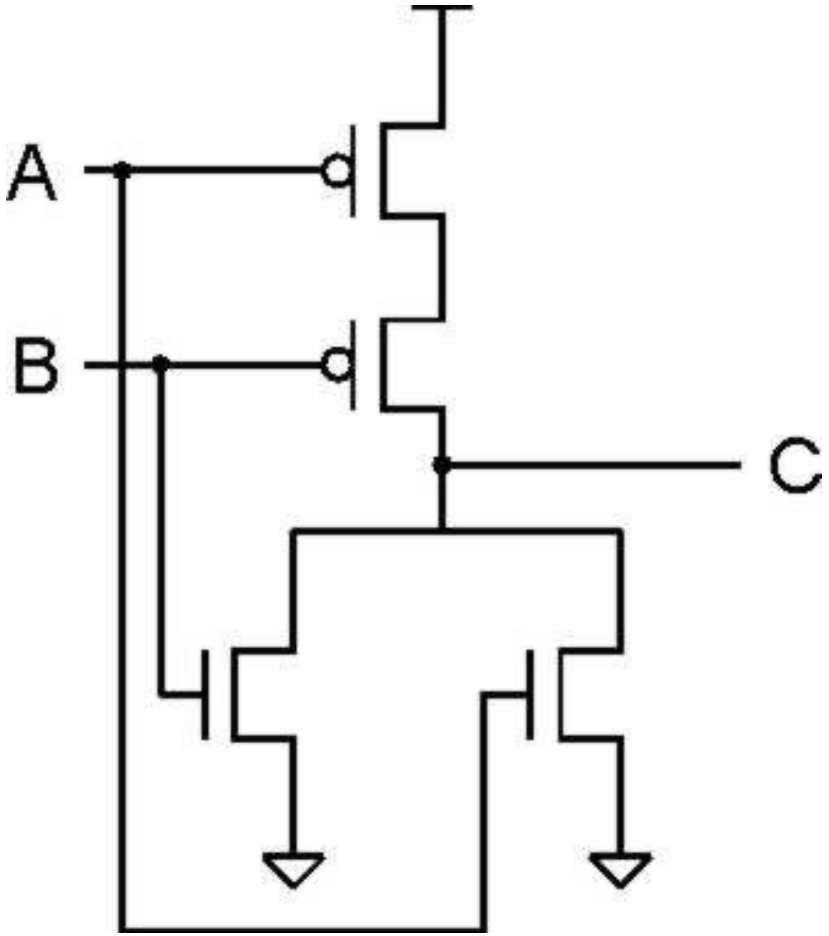


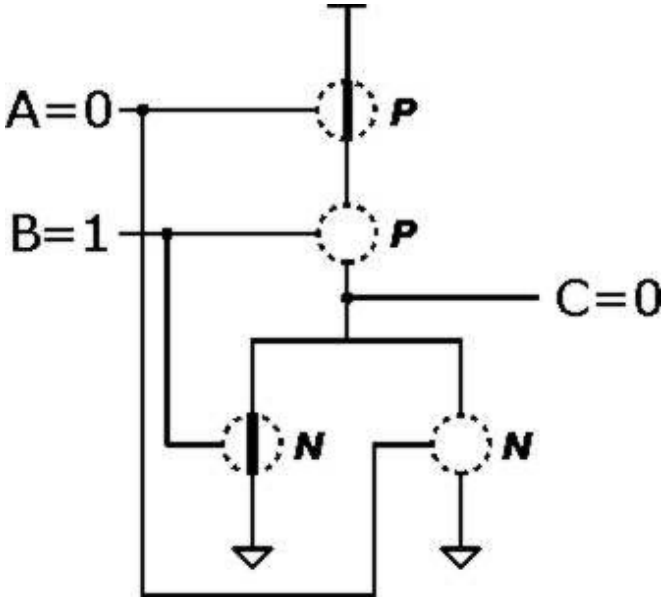
In	Out
0	1
1	0





NOR Gate (NOT + OR)

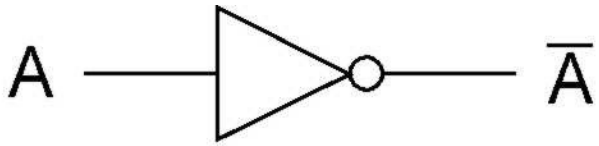




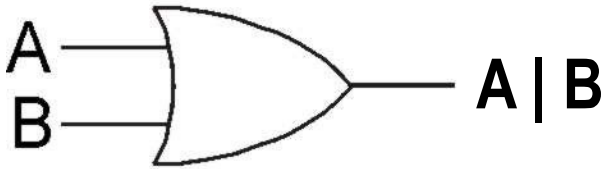
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Note: Serial structure on top, parallel on bottom.

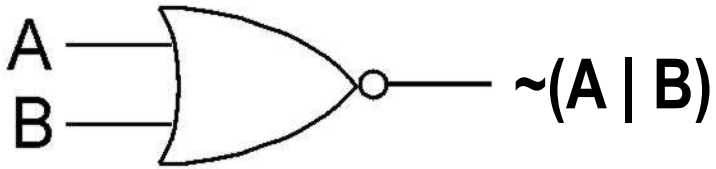
Basic Logic Gates



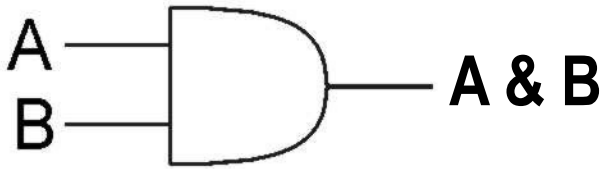
NOT



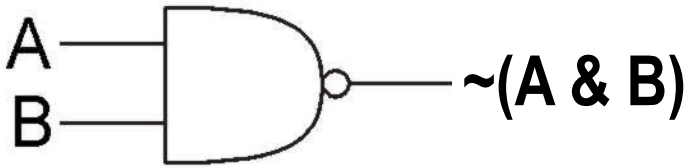
OR



NOR

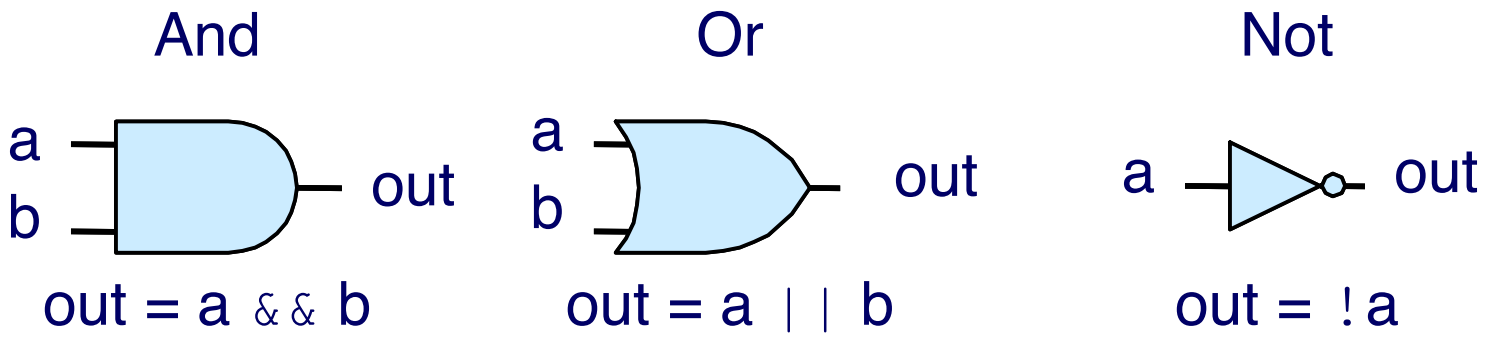


AND

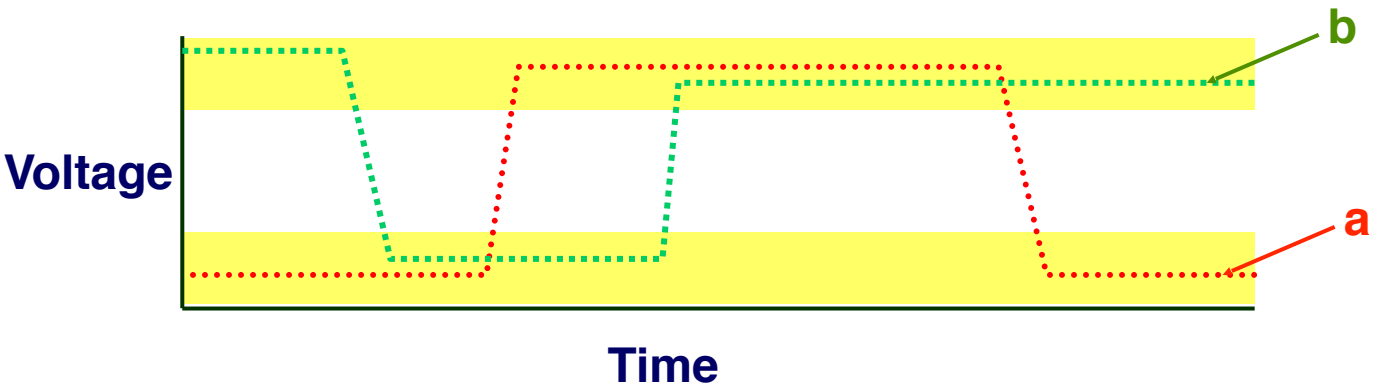


NAND

Computing with Logic Gates



- Outputs are Boolean functions of inputs
- Respond continuously to changes in inputs with some small delay
- Different gates have different delays (b/c different transistor combinations)



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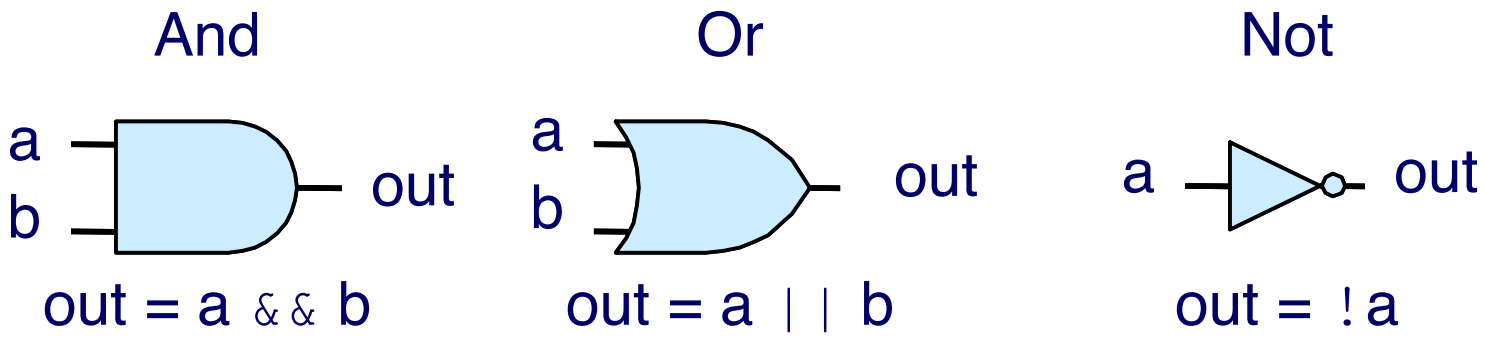

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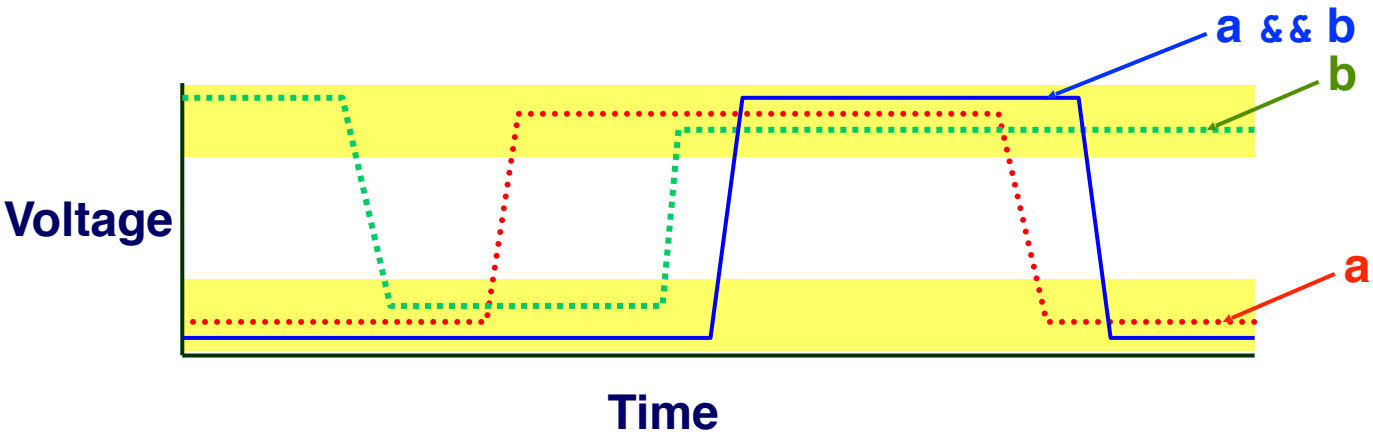

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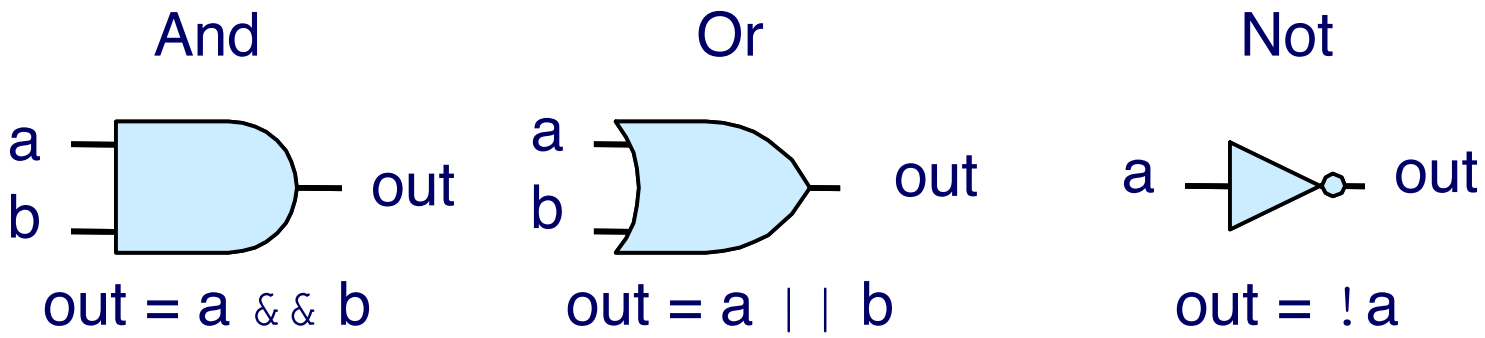

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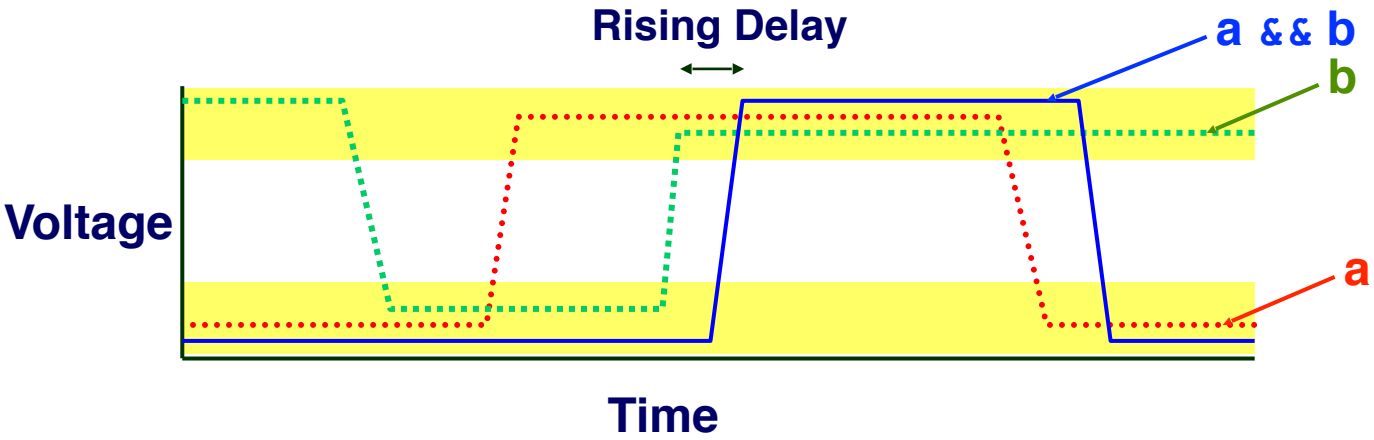

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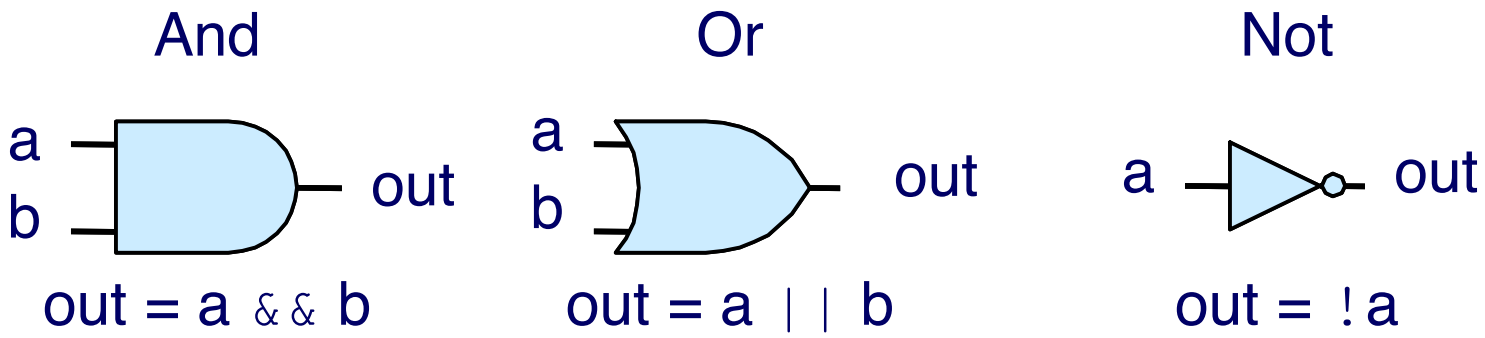

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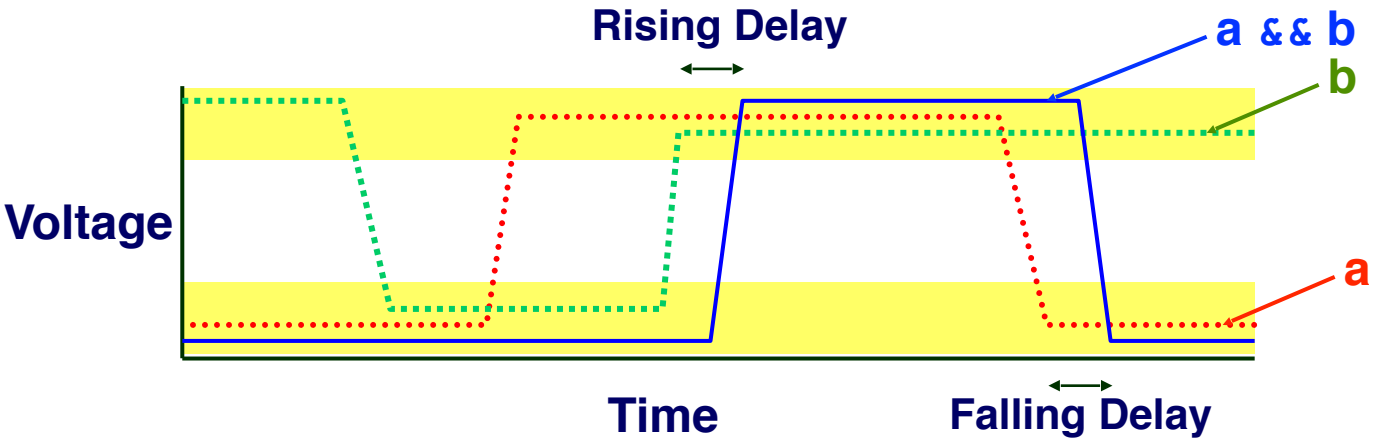
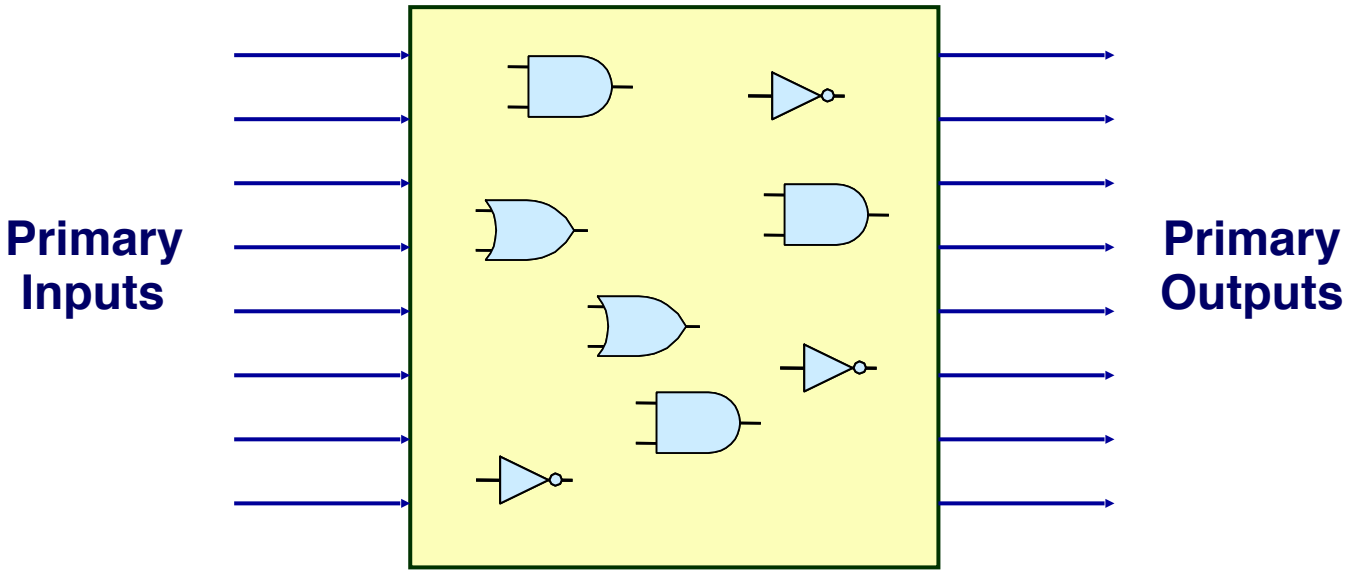


Combinational Circuits



- A Network of Logic Gates
  - Continuously responds to changes on primary inputs
  - Primary outputs become (**after some delay**) Boolean functions of primary inputs

Bit Equality

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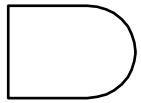

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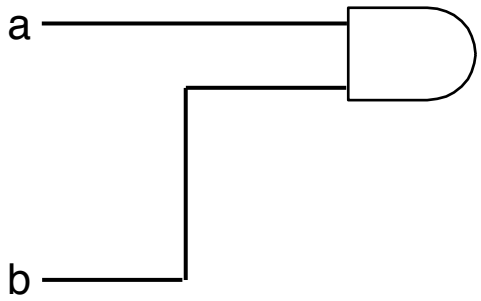

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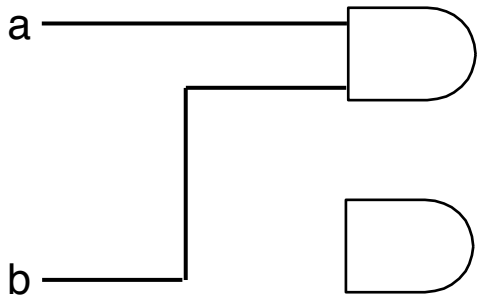

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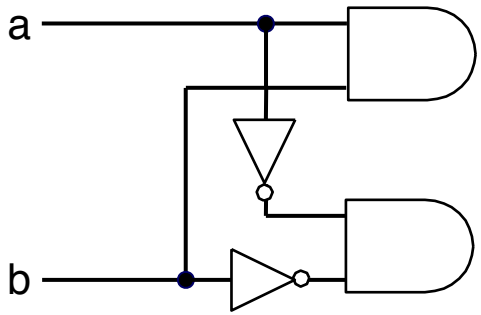

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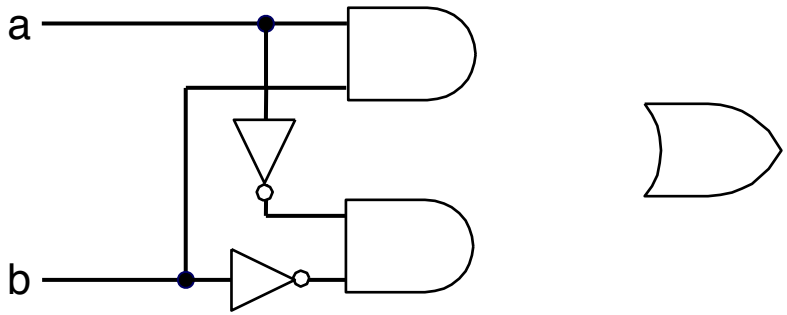

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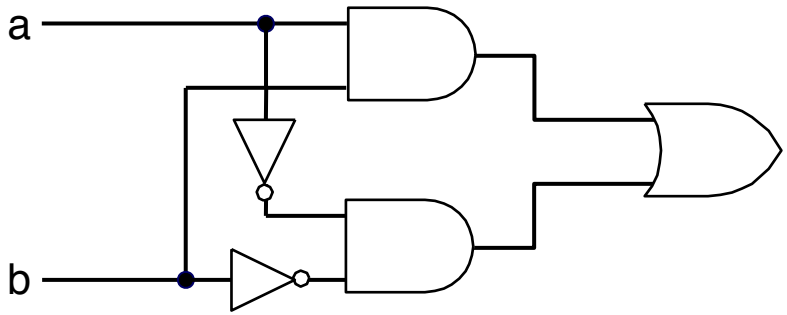

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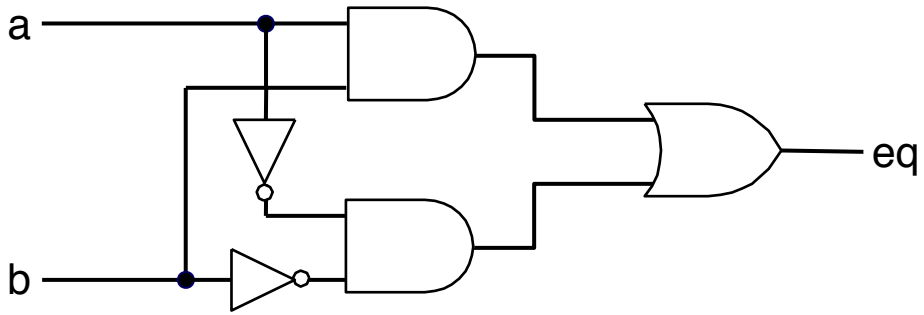

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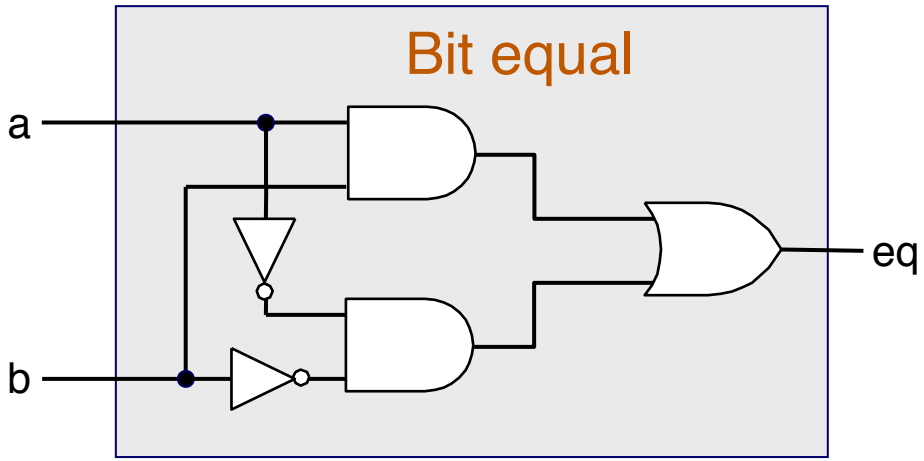
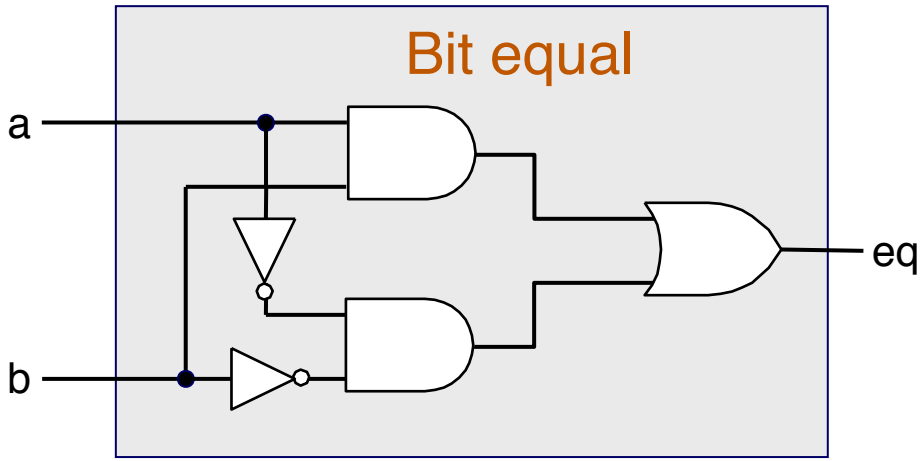


Delay of Bit Equal Circuit



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  - Assuming 1-input NOT takes 1 unit of time, 2-input AND takes 4.3, and 2-input OR takes 4.7

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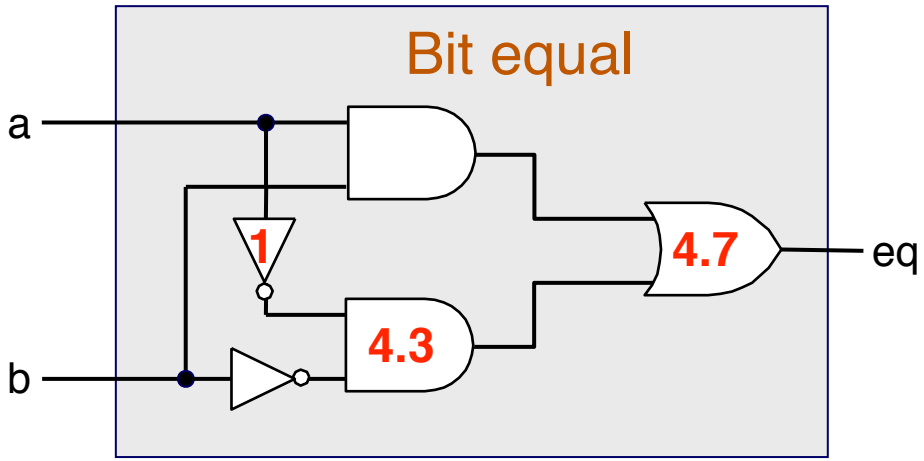

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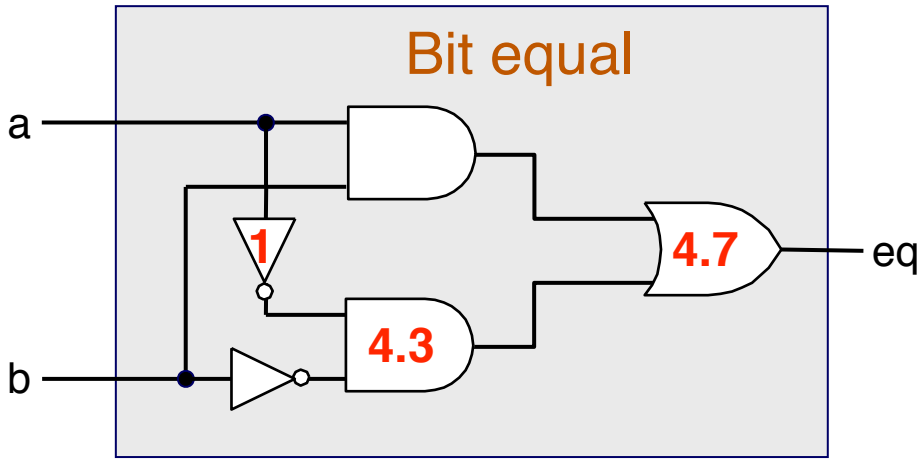

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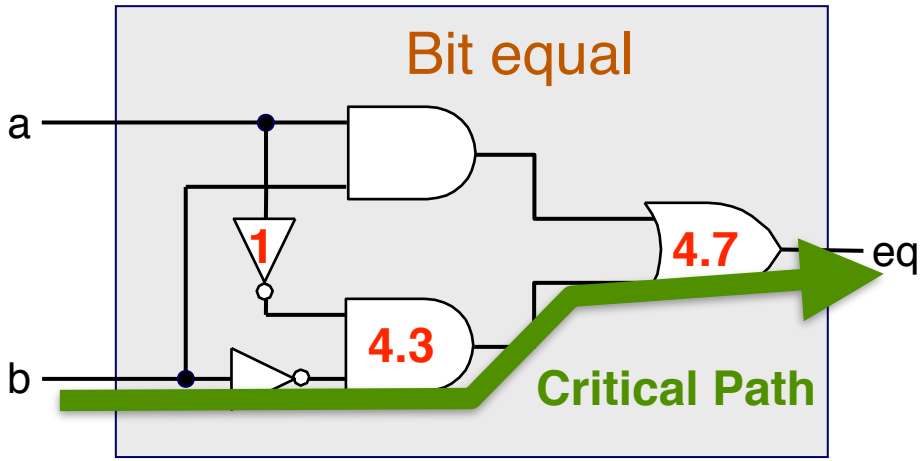

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