1. For each pseudoinstruction below, produce a ***minimal sequence*** of actual MIPS instr. to do the same thing.

	Pseudoinstruction	What it accomplishes
(a)	**bge $t5, $t3, L**	if($t5 >= $t3) goto L
(b)	**bgt $t5, $t3, L**	if($t5 > $t3) goto L

2. What type of format is used for each of instr. below?

   (a) sll (b) **sw** (c) **slt** (d) **beq** (e) **jal**

3. For addresses below in the table and assume PC is at address **0x00000000**

(i) 0x0005 0000	(ii) 0xFFFF FF00

   (a) how many **branch** instr. do you need to get to each address?

   (b) how many **jump** instr. are required to get to each address?

Ans.

1.

bge $t5, $t3, L	if ($t5 ≧ $t3) go to L	slt $at, $t5, $t3 beq $at, $zero, L
bgt $t5, $t3, L	if ($t5 > $t3) go to L	slt $at, $t3, $t5 bne $at, $zero, L

2. sll: R-type, sw:I-type, slt: R-type, beq:I-type, jal: J-type

3. (a) (i) 3 (ii) 1
   (b) (i) 1 (ii) can't be done