4(b) 答案更正說明如下。

4. (40%) Given the code sequence, please answer questions below.

(a) (10%) How many cycles will each of the following 2 schemes take to *complete the execution* of the code sequence? (Note: Assume the Beq is *Taken*, and no prediction is made for the branch outcome)

A. the single-cycle CPU

B. the pipelined MIPS CPU **with** forwarding and branch h/w modified (i.e., decision is made at the end of **ID** stage)

(b) (10%) For the pipeline scheme above, what instructions are at IF, ID, EXE, MEM, and WB stages respectively, during the 5th cycle?

(c) (20%) please list the values of 7 control signals at the 5th cycle. (Please fill your answers in the table below)

```
        add   $t3, $s1, $s2
        lw    $t1, 0($t3)
        lw    $t2, 4($t3)
        add   $s1, $t1, $t2
        sw    $t1, 4($t3)
        beq   $t1, $t2, label
        add   $t4, $t1, $t2
        sub   $t5, $t1, $t2
        or    $t6, $t4, $t5
label:  sub   $t6, $t1, $t2
```

上次檢討時 (b) 題的答案為

IF	ID	EXE	MEM	WB
add	Stall cycle	lw	lw	Add

更正為

IF	ID	EXE	MEM	WB
sw	add	lw	lw	Add

因為在 cycle5 時，add 指令還在 ID，還沒變成 stall cycle，要在 cycle6 時才變成 stall，而 sw, add 會分別在 IF, ID 多停留一個 cycle，如下圖顯示。

cycle	1	2	3	4	5	6	7	
add	IF	ID	EXE	MEM	WB			
lw		IF	ID	EXE	MEM	WB		
lw			IF	ID	EXE	MEM	**WB**	
add				IF	ID(add)	**Stall**	Stall	
sw					IF(sw)	ID (add)	EXE(add)	
						IF(sw)	ID (sw)	
beq							IF (beq)	