1. How many cycles will each of the following 3 schemes take to execute the code sequence below, respectively? (Note: Assume the reads and writes of register file can occur in the same cycle.)
   (a) single-cycle
   (b) pipeline without both forwarding and branch h/w modified (i.e., decision made at the end of MEM stage).
   (c) pipeline with forwarding and branch h/w modified (i.e., decision made at the end of ID stage)
2. For each scheme above, list the values of 9 control signals when the code executes at the 5th cycle.

```
      add $t3, $s1, $s2
      lw    $t1, 0($t3)
      lw    $t2, 4($t3)
      sw    $t2, 0($t3)
      sw    $t1, 4($t3)
      beq $t1, $t2, L1 -> taken
      add $t4, $t1, $t2
      sub  $t5, $t1, $t2
      or    $t6, $t4, $t5
L1 : sub $t6, $t1, $t2
```

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1. How many cycles will each of the following 3 schemes take to execute the code sequence below, respectively? (Note: Assume the reads and writes of register file can occur in the same cycle.)
   (d) single-cycle
   (e) pipeline without both forwarding and branch h/w modified (i.e., decision made at the end of MEM stage).
   (f) pipeline with forwarding and branch h/w modified (i.e., decision made at the end of ID stage)
2. For each scheme above, list the values of 9 control signals when the code executes at the 5th cycle.

```
      add $t3, $s1, $s2
      lw    $t1, 0($t3)
      lw    $t2, 4($t3)
      sw    $t2, 0($t3)
      sw    $t1, 4($t3)
      beq $t1, $t2, L1 -> taken
      add $t4, $t1, $t2
      sub  $t5, $t1, $t2
      or    $t6, $t4, $t5
L1 : sub $t6, $t1, $t2
```