Computer Organization Quiz4

總分 100/100

Quiz of chapter4

0 分，共 **0** 分

你的學號 *

123456789

你的姓名 *

練習ing

Computer Organization Quiz4 **100** 分，共 **100** 分

Quiz of chapter4

(30%) Assume that a 5-stage pipelined MIPS CPU is used. Consider the code sequence on the right side, where assume the branch instructions are predicted taken, but actually it is “NOT” taken. To complete the execution of this code sequence, which of following statements are true? (Note: register reads/writes can happen in the same cycle) *

```
lw $s0, 0($t0)
lw $s1, 0($t0)
bne $s0, $s1, L
add $s2, $s0, $s1
sub $s3, $s1, $s0
addi $t1, $s2, 10
```

	True	False	分數	
Assume the CPU supports data forwarding and the branch outcome is determined at MEM stage. At the 6th cycle, the instruction at EXE stage is bne	◉	○	5/5	✓
Assume the CPU supports data forwarding and the branch outcome is determined at ID stage. At the 6th cycle, the instruction at EXE stage is bne	○	◉	5/5	✓
Assume the CPU supports data forwarding and the branch outcome is determined at	◉	○	5/5	✓

MEM stage. It will take 14 clock cycles to complete the code execution.				
Assume the CPU supports data forwarding and the branch outcome is determined at ID stage. It will take 12 cycles to complete the code execution	○	◉	5/5	✓
Assume the CPU does not implement data forwarding and the branch outcome is determined at MEM stage. It will take 15 clock cycles to complete the code execution.	○	◉	5/5	✓
Assume the CPU does not implement data forwarding and the branch outcome is determined at MEM stage. At the 11th cycle, the instruction at EXE stage is add.	◉	○	5/5	✓

(30%) Consider the following sequence of actual outcomes for a branch. T means the branch is taken. N means not taken. Assume both predictors are initialized to predict “not taken”. Branch: N-T-N-T-T-T-N *

	True	False	分數	
If the same branch pattern repeats thousands of times, the accuracy rate is 3/7 when 1-bit predictor is used.	◉	○	5/5	✓
If the same branch pattern repeats thousands of times, the accuracy rate is 2/7 when 2-bit predictor is used	◉	○	5/5	✓
If 1-bit predictor is used, the 5th prediction is “taken”.	◉	○	5/5	✓
If 1-bit predictor is used, the prediction accuracy rate is 3/7	◉	○	5/5	✓
If 2-bit predictor is used, the accuracy rate is 4/7.	○	◉	5/5	✓
If 2-bit predictor is used, the 5th prediction is “taken”.	○	◉	5/5	✓

(20%) According to the five-stage MIPS pipeline described in the textbook. For the code sequence and the definition of forwarding control signals below, which of following statements are correct? (Note: assume that “ForwardA” controls the first input of ALU, and “ForwardB” the second input). *

1. addi $3, $2, 0x10
2. add $3, $4, $2
3. sub $2, $1, $3
4. lw $4, 200($3)
5. add $3, $1, $4

Mux control	Source
ForwardA = 00	ID/EX
ForwardA = 10	EX/MEM
ForwardA = 01	MEM/WB
ForwardB = 00	ID/EX
ForwardB = 10	EX/MEM
ForwardB = 01	MEM/WB

	True	False	分數	
For the 5th instruction add, forwardA = 00 and forwardB = 10	○	◉	5/5	✓
For the 3rd instruction sub, forwardA = 00 and forwardB = 10	◉	○	5/5	✓
For the 4th instruction lw, forwardA = 00 and forwardB = 01	○	◉	5/5	✓
For the 2nd instruction add, forwardA = 00 and forwardB = 00	◉	○	5/5	✓

(20%) For the static 2-issue pipelined processor given in the textbook and the code sequence below. If we unroll 1 more copy of the code (i.e., 2 copies in total) and schedule it again in the table using minimum number of cycles. To complete the table for the scheduled code, which of following statements are correct? *

```
Loop:  lw    $t0, 0($s1)
       addu  $t0, $t0, $s2
       sw    $t0, 0($s1)
       addi  $s1, $s1, -4
       bne   $s1, $zero, Loop
```

Clock cycle	ALU or branch instr.	Data transfer instr.
1	addi $s1, $s1, -8	lw $t0, 0($s1)
2		
3		
:	:	:

	True	False	分數	
There are two nop (no operation) in the scheduled code.	◉	○	5/5	✓
It will take 5 cycles to schedule the unrolled code.	◉	○	5/5	✓
The 3rd issue packet contain instructions: addu and sw.	○	◉	5/5	✓

The IPC is 5/8 for the scheduled code (if we ignore the remaining 4 stages for the last instruction.)	○	◉	5/5	✓