M8

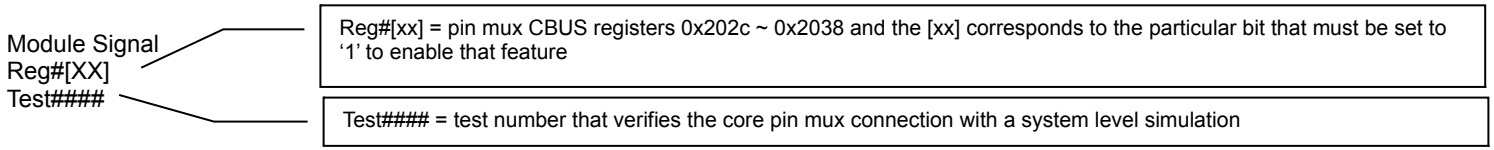
Core Pin Mux

Revision: September 7, 2016

Date	Author	Change
2013-04-11	Chris Maslyar	Initial Release
2013-04-29	Chris Maslyar	Fixed I2S Out (channels 67)
2013-05-14	Chris Maslyar	Added VGA outputs and new Audio outputs
2013-06-18	Chris Maslyar	Updated from SVN $top/doc/M8-Signoff-core_pin_mux.odt (r9149)
2013-08-12	Chris Maslyar	Fixed gpioDV GPIO controls
2013-09-09	Chris Maslyar	Added comments for BSD_EN as a gpio

M8 Core Pin Mux Signoff

This document lists the pin mux registers and the VLSI simulation that tests the core pin mux condition. The format of each cell is as follows:



GPIOAO_9	0xc8100024 bit[9]	0xc8100024 bit[25]	0xc8100028 bit[9]	JTAG_TMS Secure register Test536	I2S_AO_CLK_OUT Reg[29] Test304			
GPIOAO_10	0xc8100024 bit[10]	0xc8100024 bit[26]	0xc8100028 bit[10]	JTAG_ Secure register Test536	I2S_LR_CLK_OUT Reg[28] Test304			
GPIOAO_11	0xc8100024 bit[11]	0xc8100024 bit[27]	0xc8100028 bit[11]	JTAG_ Secure register Test536	I2S_OUT_01 Reg[27] Test304			
GPIOAO_12	0xc8100024 bit[12]	0xc8100024 bit[28]	0xc8100028 bit[12]	HDMI_CEC Reg[17] test599				
GPIOAO_13	0xc8100024 bit[13]	0xc8100024 bit[29]	0xc8100028 bit[13]	REMOTE_OUTPUT Reg[31] test599				
TEST_N	See below	0xc8100024 bit[31]		PWM_F Reg[19]				
BSD_EN	See below 0x200d bit[30]	0x200d bit[31]						

BSD_EN / TEST_N:

To make the BSD_EN and TEST_N pins outputs, you must write the following registers in the order given below. This will prevent the chip from entering a production test mode if there is noise near the BSD_EN or TEST_N pin.

1. Set Bit[29]=0 of 0x200d (PREG_PAD_GPIO0_O) to block the BSD_EN signal from entering the TAP controller
2. Set bit[0]=1 of 0xDA004000 (AO_SECURE_REG0) to prevent the TEST_N pin from

Once these two steps are complete, you can enable the BSD_EN pin as an output by writing bit[30]=0 of CBUS 0x200d (PREG_PAD_GPIO0_O)

You can set the level on the BSD_EN pin using bit[31] of CBUS 0x200d (PREG_PAD_GPIO0_O). 1 =output high. 0 = output low