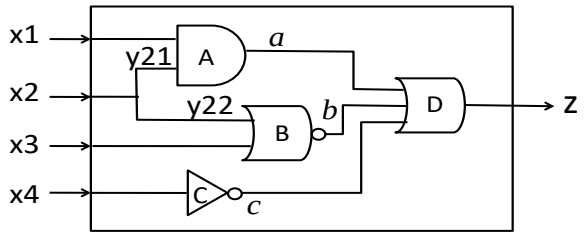
國立清華大學 電機工程學系
112 學年度第二學期
EE-6250 超大型積體電路測試 VLSI Testing
Homework #1 (佔學期總成績 10 分)
(可兩人一組) Due on April 29, 2024
Submission to https://eeclass.nthu.edu.tw/ 作業區

1. Consider the fault simulation of the following gate-level netlist. The primary input signals are {x1, x2, x3, x4} and the primary output signal is {z}. The output signals of logic gates {A, B, C, D} are denoted as {a, b, c, z}. Note that signal x2 has two branch signals {y21, y22}.



(a) (40%) Write a C or C++ program that can **simulate the logic behavior of the given netlist** under any arbitrary input vector. Note that this can be done by executing the following Boolean expressions in sequence:

a = x1 and x2;
b = x2 nor x3;
c = ~x4;
z = a or b or c;

Show the result of your program as a truth table. In the resulting truth table, list not only the value of the primary output signal z but also values of internal signals {a, b, c}.

(b) (40%) Enhance your C or C++ program so that it can perform **deductive fault simulation**. Report the number of stuck-at faults detected by each of the 16 input vectors. Consider all the stuck-at-0 faults and stuck-at-1 faults for {x1, x2, x3, x4, y21, y22, a, b, c, z}.

(c) (5%) Report the average number of stuck-at faults detected by an input vector.

(d) (5%) Report the input vector that detects the maximum number of faults. List the faults detected.

(e) (5%) Report the average number of test patterns for a fault.

(f) (5%) Report the hardest-to-detect fault(s) – i.e., the faults that are detected by the least number of input vectors.

繳交資料: Combine the following documents as a single PDF file before submitting to our【清華大學-數位學習平台】(https://eeclass.nthu.edu.tw/).

(1) A cover page with your 系所，中英文姓名，學號等資訊.
(2) 各個組員的負責項目或實作貢獻的一段簡述. (無實際【實作】貢獻之組員將零分計算)
(3) Your answers to the above questions (a)-(f) into a single PDF file.
(4) The source codes of your C or C++ programs.