

## Introduction

This document is addressed to application developers. It provides complete information on how to use the memory and peripherals of STM32F446xx microcontrollers.

The STM32F446xx constitute a family of microcontrollers with different memory sizes, packages and peripherals.

For ordering information, mechanical and electrical device characteristics refer to the corresponding datasheets.

For information on the Arm<sup>®</sup> Cortex<sup>®</sup>-M4 with FPU core refer to the Cortex<sup>®</sup>-M4 Technical Reference Manual.

STM32F446xx microcontrollers include ST state-of-the-art patented technology.

## Related documents

Available from STMicroelectronics web site [www.st.com](http://www.st.com):

- STM32F446xx datasheets

For information on the Cortex<sup>®</sup>-M4 with FPU, refer to *STM32 Cortex<sup>®</sup>-M4 MCUs and MPUs programming manual* (PM0214).

# Contents

<b>1</b>	<b>Documentation conventions</b>	<b>51</b>
1.1	General information	51
1.2	List of abbreviations for registers	51
1.3	Glossary	52
1.4	Availability of peripherals	52
<b>2</b>	<b>Memory and bus architecture</b>	<b>53</b>
2.1	System architecture	53
2.1.1	I-bus	54
2.1.2	D-bus	54
2.1.3	S-bus	54
2.1.4	DMA memory bus	54
2.1.5	DMA peripheral bus	55
2.1.6	USB OTG HS DMA bus	55
2.1.7	BusMatrix	55
2.1.8	AHB/APB bridges (APB)	55
2.2	Memory organization	56
2.2.1	Introduction	56
2.2.2	Memory map and register boundary addresses	57
2.2.3	Embedded SRAM	60
2.2.4	Flash memory overview	60
2.2.5	Bit banding	60
2.3	Boot configuration	61
<b>3</b>	<b>Embedded Flash memory interface</b>	<b>64</b>
3.1	Introduction	64
3.2	Main features	64
3.3	Embedded Flash memory	65
3.4	Read interface	66
3.4.1	Relation between CPU clock frequency and Flash memory read time	66
3.4.2	Adaptive real-time memory accelerator (ART Accelerator™)	67
3.5	Erase and program operations	69
3.5.1	Unlocking the Flash control register	69

3.5.2	Program/erase parallelism	70
3.5.3	Erase	70
3.5.4	Programming	71
3.5.5	Interrupts	72
3.6	Option bytes	72
3.6.1	Description of user option bytes	72
3.6.2	Programming user option bytes	74
3.6.3	Read protection (RDP)	74
3.6.4	Write protections	77
3.6.5	Proprietary code readout protection (PCROP)	78
3.7	One-time programmable bytes	79
3.8	Flash interface registers	80
3.8.1	Flash access control register (FLASH_ACR)	80
3.8.2	Flash key register (FLASH_KEYR)	81
3.8.3	Flash option key register (FLASH_OPTKEYR)	81
3.8.4	Flash status register (FLASH_SR)	82
3.8.5	Flash control register (FLASH_CR)	83
3.8.6	Flash option control register (FLASH_OPTCR)	85
3.8.7	Flash interface register map	87
<b>4</b>	<b>CRC calculation unit</b>	<b>88</b>
4.1	CRC introduction	88
4.2	CRC main features	88
4.3	CRC functional description	88
4.4	CRC registers	89
4.4.1	Data register (CRC_DR)	89
4.4.2	Independent data register (CRC_IDR)	90
4.4.3	Control register (CRC_CR)	90
4.4.4	CRC register map	91
<b>5</b>	<b>Power controller (PWR)</b>	<b>92</b>
5.1	Power supplies	92
5.1.1	Independent A/D converter supply and reference voltage	93
5.1.2	Battery backup domain	93
5.1.3	Voltage regulator	95
5.2	Power supply supervisor	98

5.2.1	Power-on reset (POR) / power-down reset (PDR) . . . . .	98
5.2.2	Brownout reset (BOR) . . . . .	99
5.2.3	Programmable voltage detector (PVD) . . . . .	99
5.3	Low-power modes . . . . .	100
5.3.1	Slowing down system clocks . . . . .	101
5.3.2	Peripheral clock gating . . . . .	101
5.3.3	Low power mode . . . . .	102
5.3.4	Sleep mode . . . . .	102
5.3.5	Stop mode . . . . .	103
5.3.6	Standby mode . . . . .	106
5.3.7	Programming the RTC alternate functions to wake up the device from the Stop and Standby modes . . . . .	108
5.4	Power control registers . . . . .	111
5.4.1	PWR power control register (PWR_CR) . . . . .	111
5.4.2	PWR power control/status register (PWR_CSR) . . . . .	113
5.5	PWR register map . . . . .	115
<b>6</b>	<b>Reset and clock control (RCC) . . . . .</b>	<b>116</b>
6.1	Reset . . . . .	116
6.1.1	System reset . . . . .	116
6.1.2	Power reset . . . . .	116
6.1.3	Backup domain reset . . . . .	117
6.2	Clocks . . . . .	117
6.2.1	HSE clock . . . . .	120
6.2.2	HSI clock . . . . .	121
6.2.3	PLL configuration . . . . .	121
6.2.4	LSE clock . . . . .	122
6.2.5	LSI clock . . . . .	122
6.2.6	System clock (SYSCLK) selection . . . . .	122
6.2.7	Clock security system (CSS) . . . . .	123
6.2.8	RTC/AWU clock . . . . .	123
6.2.9	Watchdog clock . . . . .	124
6.2.10	Clock-out capability . . . . .	124
6.2.11	Internal/external clock measurement using TIM5/TIM11 . . . . .	125
6.3	RCC registers . . . . .	127
6.3.1	RCC clock control register (RCC_CR) . . . . .	127
6.3.2	RCC PLL configuration register (RCC_PLLCFGR) . . . . .	129

6.3.3	RCC clock configuration register (RCC_CFGR) . . . . .	131
6.3.4	RCC clock interrupt register (RCC_CIR) . . . . .	133
6.3.5	RCC AHB1 peripheral reset register (RCC_AHB1RSTR) . . . . .	136
6.3.6	RCC AHB2 peripheral reset register (RCC_AHB2RSTR) . . . . .	138
6.3.7	RCC AHB3 peripheral reset register (RCC_AHB3RSTR) . . . . .	138
6.3.8	RCC APB1 peripheral reset register (RCC_APB1RSTR) . . . . .	139
6.3.9	RCC APB2 peripheral reset register (RCC_APB2RSTR) . . . . .	142
6.3.10	RCC AHB1 peripheral clock enable register (RCC_AHB1ENR) . . . . .	144
6.3.11	RCC AHB2 peripheral clock enable register (RCC_AHB2ENR) . . . . .	145
6.3.12	RCC AHB3 peripheral clock enable register (RCC_AHB3ENR) . . . . .	146
6.3.13	RCC APB1 peripheral clock enable register (RCC_APB1ENR) . . . . .	146
6.3.14	RCC APB2 peripheral clock enable register (RCC_APB2ENR) . . . . .	149
6.3.15	RCC AHB1 peripheral clock enable in low power mode register (RCC_AHB1LPENR) . . . . .	151
6.3.16	RCC AHB2 peripheral clock enable in low power mode register (RCC_AHB2LPENR) . . . . .	153
6.3.17	RCC AHB3 peripheral clock enable in low power mode register (RCC_AHB3LPENR) . . . . .	154
6.3.18	RCC APB1 peripheral clock enable in low power mode register (RCC_APB1LPENR) . . . . .	154
6.3.19	RCC APB2 peripheral clock enabled in low power mode register (RCC_APB2LPENR) . . . . .	158
6.3.20	RCC Backup domain control register (RCC_BDCR) . . . . .	159
6.3.21	RCC clock control & status register (RCC_CSR) . . . . .	161
6.3.22	RCC spread spectrum clock generation register (RCC_SSCGR) . . . . .	162
6.3.23	RCC PLLI2S configuration register (RCC_PLLI2SCFGR) . . . . .	163
6.3.24	RCC PLL configuration register (RCC_PLLSAICFGR) . . . . .	166
6.3.25	RCC dedicated clock configuration register (RCC_DCKCFGR) . . . . .	167
6.3.26	RCC clocks gated enable register (CKGATENR) . . . . .	169
6.3.27	RCC dedicated clocks configuration register 2 (DCKCFGR2) . . . . .	170
6.3.28	RCC register map . . . . .	172
<b>7</b>	<b>General-purpose I/Os (GPIO) . . . . .</b>	<b>176</b>
7.1	GPIO introduction . . . . .	176
7.2	GPIO main features . . . . .	176
7.3	GPIO functional description . . . . .	176
7.3.1	General-purpose I/O (GPIO) . . . . .	178
7.3.2	I/O pin multiplexer and mapping . . . . .	178

7.3.3	I/O port control registers	180
7.3.4	I/O port data registers	181
7.3.5	I/O data bitwise handling	181
7.3.6	GPIO locking mechanism	181
7.3.7	I/O alternate function input/output	182
7.3.8	External interrupt/wakeup lines	182
7.3.9	Input configuration	182
7.3.10	Output configuration	183
7.3.11	Alternate function configuration	184
7.3.12	Analog configuration	185
7.3.13	Using the OSC32_IN/OSC32_OUT pins as GPIO PC14/PC15 port pins	185
7.3.14	Using the OSC_IN/OSC_OUT pins as GPIO PH0/PH1 port pins	185
7.3.15	Selection of RTC additional_AF1 and RTC_AF2 alternate functions	186
7.4	GPIO registers	187
7.4.1	GPIO port mode register (GPIOx_MODER) (x = A..H)	187
7.4.2	GPIO port output type register (GPIOx_OTYPER) (x = A..H)	188
7.4.3	GPIO port output speed register (GPIOx_OSPEEDR) (x = A..H)	188
7.4.4	GPIO port pull-up/pull-down register (GPIOx_PUPDR) (x = A..H)	189
7.4.5	GPIO port input data register (GPIOx_IDR) (x = A..H)	189
7.4.6	GPIO port output data register (GPIOx_ODR) (x = A..H)	190
7.4.7	GPIO port bit set/reset register (GPIOx_BSRR) (x = A..H)	190
7.4.8	GPIO port configuration lock register (GPIOx_LCKR) (x = A..H)	190
7.4.9	GPIO alternate function low register (GPIOx_AFR1) (x = A..H)	192
7.4.10	GPIO alternate function high register (GPIOx_AFRH) (x = A..H)	192
7.4.11	GPIO register map	193
<b>8</b>	<b>System configuration controller (SYSCFG)</b>	<b>195</b>
8.1	I/O compensation cell	195
8.2	SYSCFG registers	195
8.2.1	SYSCFG memory remap register (SYSCFG_MEMRMP)	195
8.2.2	SYSCFG peripheral mode configuration register (SYSCFG_PMC)	197
8.2.3	SYSCFG external interrupt configuration register 1 (SYSCFG_EXTICR1)	197
8.2.4	SYSCFG external interrupt configuration register 2 (SYSCFG_EXTICR2)	198
8.2.5	SYSCFG external interrupt configuration register 3 (SYSCFG_EXTICR3)	199

8.2.6	SYSCFG external interrupt configuration register 4 (SYSCFG_EXTICR4) .....	199
8.2.7	Compensation cell control register (SYSCFG_CMPCR) .....	200
8.2.8	SYSCFG configuration register (SYSCFG_CFGR) .....	200
8.2.9	SYSCFG register maps .....	202
<b>9</b>	<b>Direct memory access controller (DMA) .....</b>	<b>203</b>
9.1	DMA introduction .....	203
9.2	DMA main features .....	203
9.3	DMA functional description .....	205
9.3.1	DMA block diagram .....	205
9.3.2	DMA overview .....	205
9.3.3	DMA transactions .....	206
9.3.4	Channel selection .....	206
9.3.5	Arbiter .....	208
9.3.6	DMA streams .....	208
9.3.7	Source, destination and transfer modes .....	208
9.3.8	Pointer incrementation .....	212
9.3.9	Circular mode .....	213
9.3.10	Double-buffer mode .....	213
9.3.11	Programmable data width, packing/unpacking, endianness .....	214
9.3.12	Single and burst transfers .....	215
9.3.13	FIFO .....	216
9.3.14	DMA transfer completion .....	219
9.3.15	DMA transfer suspension .....	220
9.3.16	Flow controller .....	221
9.3.17	Summary of the possible DMA configurations .....	222
9.3.18	Stream configuration procedure .....	222
9.3.19	Error management .....	223
9.4	DMA interrupts .....	224
9.5	DMA registers .....	225
9.5.1	DMA low interrupt status register (DMA_LISR) .....	225
9.5.2	DMA high interrupt status register (DMA_HISR) .....	226
9.5.3	DMA low interrupt flag clear register (DMA_LIFCR) .....	227
9.5.4	DMA high interrupt flag clear register (DMA_HIFCR) .....	227
9.5.5	DMA stream x configuration register (DMA_SxCR) .....	228
9.5.6	DMA stream x number of data register (DMA_SxNDTR) .....	231

9.5.7	DMA stream x peripheral address register (DMA_SxPAR) .....	232
9.5.8	DMA stream x memory 0 address register (DMA_SxM0AR) .....	232
9.5.9	DMA stream x memory 1 address register (DMA_SxM1AR) .....	232
9.5.10	DMA stream x FIFO control register (DMA_SxFCR) .....	233
9.5.11	DMA register map .....	235
<b>10</b>	<b>Interrupts and events .....</b>	<b>239</b>
10.1	Nested vectored interrupt controller (NVIC) .....	239
10.1.1	NVIC features .....	239
10.1.2	SysTick calibration value register .....	239
10.1.3	Interrupt and exception vectors .....	239
10.2	External interrupt/event controller (EXTI) .....	239
10.2.1	EXTI main features .....	243
10.2.2	EXTI block diagram .....	244
10.2.3	Wakeup event management .....	244
10.2.4	Functional description .....	244
10.2.5	External interrupt/event line mapping .....	246
10.3	EXTI registers .....	247
10.3.1	Interrupt mask register (EXTI_IMR) .....	247
10.3.2	Event mask register (EXTI_EMR) .....	247
10.3.3	Rising trigger selection register (EXTI_RTSTR) .....	248
10.3.4	Falling trigger selection register (EXTI_FTSR) .....	248
10.3.5	Software interrupt event register (EXTI_SWIER) .....	249
10.3.6	Pending register (EXTI_PR) .....	249
10.3.7	EXTI register map .....	250
<b>11</b>	<b>Flexible memory controller (FMC) .....</b>	<b>251</b>
11.1	Introduction .....	251
11.2	FMC main features .....	251
11.3	FMC block diagram .....	252
11.4	AHB interface .....	253
11.4.1	Supported memories and transactions .....	253
11.5	External device address mapping .....	255
11.5.1	NOR/PSRAM address mapping .....	255
11.5.2	NAND Flash memory address mapping .....	256



11.5.3	SDRAM address mapping	257
11.6	NOR Flash/PSRAM controller	259
11.6.1	External memory interface signals	261
11.6.2	Supported memories and transactions	262
11.6.3	General timing rules	264
11.6.4	NOR Flash/PSRAM controller asynchronous transactions	264
11.6.5	Synchronous transactions	281
11.6.6	NOR/PSRAM controller registers	288
11.7	NAND Flash controller	295
11.7.1	External memory interface signals	295
11.7.2	NAND Flash supported memories and transactions	297
11.7.3	Timing diagrams for NAND Flash memory	297
11.7.4	NAND Flash operations	298
11.7.5	NAND Flash prewait functionality	299
11.7.6	Computation of the error correction code (ECC) in NAND Flash memory	300
11.7.7	NAND Flash controller registers	301
11.8	SDRAM controller	307
11.8.1	SDRAM controller main features	307
11.8.2	SDRAM External memory interface signals	307
11.8.3	SDRAM controller functional description	308
11.8.4	Low-power modes	314
11.8.5	SDRAM controller registers	316
11.8.6	FMC register map	323
<b>12</b>	<b>Quad-SPI interface (QUADSPI)</b>	<b>326</b>
12.1	Introduction	326
12.2	QUADSPI main features	326
12.3	QUADSPI functional description	326
12.3.1	QUADSPI block diagram	326
12.3.2	QUADSPI pins	327
12.3.3	QUADSPI command sequence	328
12.3.4	QUADSPI signal interface protocol modes	330
12.3.5	QUADSPI indirect mode	332
12.3.6	QUADSPI status flag polling mode	334
12.3.7	QUADSPI memory-mapped mode	334
12.3.8	QUADSPI Flash memory configuration	335

12.3.9	QUADSPI delayed data sampling	335
12.3.10	QUADSPI configuration	335
12.3.11	QUADSPI usage	336
12.3.12	Sending the instruction only once	338
12.3.13	QUADSPI error management	338
12.3.14	QUADSPI busy bit and abort functionality	338
12.3.15	nCS behavior	339
12.4	QUADSPI interrupts	340
12.5	QUADSPI registers	342
12.5.1	QUADSPI control register (QUADSPI_CR)	342
12.5.2	QUADSPI device configuration register (QUADSPI_DCR)	345
12.5.3	QUADSPI status register (QUADSPI_SR)	346
12.5.4	QUADSPI flag clear register (QUADSPI_FCR)	347
12.5.5	QUADSPI data length register (QUADSPI_DLR)	347
12.5.6	QUADSPI communication configuration register (QUADSPI_CCR)	348
12.5.7	QUADSPI address register (QUADSPI_AR)	350
12.5.8	QUADSPI alternate bytes registers (QUADSPI_ABR)	351
12.5.9	QUADSPI data register (QUADSPI_DR)	351
12.5.10	QUADSPI polling status mask register (QUADSPI_PSMKR)	352
12.5.11	QUADSPI polling status match register (QUADSPI_PSMAR)	352
12.5.12	QUADSPI polling interval register (QUADSPI_PIR)	353
12.5.13	QUADSPI low-power timeout register (QUADSPI_LPTR)	353
12.5.14	QUADSPI register map	354
<b>13</b>	<b>Analog-to-digital converter (ADC)</b>	<b>355</b>
13.1	ADC introduction	355
13.2	ADC main features	355
13.3	ADC functional description	355
13.3.1	ADC on-off control	357
13.3.2	ADC1/2 and ADC3 connectivity	358
13.3.3	ADC clock	361
13.3.4	Channel selection	361
13.3.5	Single conversion mode	362
13.3.6	Continuous conversion mode	362
13.3.7	Timing diagram	362
13.3.8	Analog watchdog	363
13.3.9	Scan mode	364

13.3.10	Injected channel management	364
13.3.11	Discontinuous mode	365
13.4	Data alignment	366
13.5	Channel-wise programmable sampling time	367
13.6	Conversion on external trigger and trigger polarity	368
13.7	Fast conversion mode	369
13.8	Data management	370
13.8.1	Using the DMA	370
13.8.2	Managing a sequence of conversions without using the DMA	370
13.8.3	Conversions without DMA and without overrun detection	371
13.9	Multi ADC mode	371
13.9.1	Injected simultaneous mode	374
13.9.2	Regular simultaneous mode	375
13.9.3	Interleaved mode	376
13.9.4	Alternate trigger mode	378
13.9.5	Combined regular/injected simultaneous mode	380
13.9.6	Combined regular simultaneous + alternate trigger mode	380
13.10	Temperature sensor	381
13.11	Battery charge monitoring	383
13.12	ADC interrupts	383
13.13	ADC registers	384
13.13.1	ADC status register (ADC_SR)	384
13.13.2	ADC control register 1 (ADC_CR1)	385
13.13.3	ADC control register 2 (ADC_CR2)	387
13.13.4	ADC sample time register 1 (ADC_SMPR1)	389
13.13.5	ADC sample time register 2 (ADC_SMPR2)	390
13.13.6	ADC injected channel data offset register x (ADC_JOFRx) (x=1..4)	390
13.13.7	ADC watchdog higher threshold register (ADC_HTR)	390
13.13.8	ADC watchdog lower threshold register (ADC_LTR)	391
13.13.9	ADC regular sequence register 1 (ADC_SQR1)	391
13.13.10	ADC regular sequence register 2 (ADC_SQR2)	392
13.13.11	ADC regular sequence register 3 (ADC_SQR3)	393
13.13.12	ADC injected sequence register (ADC_JSQR)	394
13.13.13	ADC injected data register x (ADC_JDRx) (x= 1..4)	394
13.13.14	ADC regular data register (ADC_DR)	395
13.13.15	ADC Common status register (ADC_CSR)	395

13.13.16	ADC common control register (ADC_CCR)	396
13.13.17	ADC common regular data register for dual and triple modes (ADC_CDR)	399
13.14	ADC register map	399
<b>14</b>	<b>Digital-to-analog converter (DAC)</b>	<b>402</b>
14.1	DAC introduction	402
14.2	DAC main features	402
14.3	DAC functional description	403
14.3.1	DAC channel enable	403
14.3.2	DAC output buffer enable	404
14.3.3	DAC data format	404
14.3.4	DAC conversion	405
14.3.5	DAC output voltage	406
14.3.6	DAC trigger selection	406
14.3.7	DMA request	407
14.3.8	Noise generation	407
14.3.9	Triangle-wave generation	408
14.4	Dual DAC channel conversion	409
14.4.1	Independent trigger without wave generation	410
14.4.2	Independent trigger with single LFSR generation	410
14.4.3	Independent trigger with different LFSR generation	410
14.4.4	Independent trigger with single triangle generation	411
14.4.5	Independent trigger with different triangle generation	411
14.4.6	Simultaneous software start	411
14.4.7	Simultaneous trigger without wave generation	412
14.4.8	Simultaneous trigger with single LFSR generation	412
14.4.9	Simultaneous trigger with different LFSR generation	412
14.4.10	Simultaneous trigger with single triangle generation	413
14.4.11	Simultaneous trigger with different triangle generation	413
14.5	DAC registers	414
14.5.1	DAC control register (DAC_CR)	414
14.5.2	DAC software trigger register (DAC_SWTRIGR)	417
14.5.3	DAC channel1 12-bit right-aligned data holding register (DAC_DHR12R1)	417
14.5.4	DAC channel1 12-bit left aligned data holding register (DAC_DHR12L1)	418

14.5.5	DAC channel1 8-bit right aligned data holding register (DAC_DHR8R1) .....	418
14.5.6	DAC channel2 12-bit right aligned data holding register (DAC_DHR12R2) .....	419
14.5.7	DAC channel2 12-bit left aligned data holding register (DAC_DHR12L2) .....	419
14.5.8	DAC channel2 8-bit right-aligned data holding register (DAC_DHR8R2) .....	419
14.5.9	Dual DAC 12-bit right-aligned data holding register (DAC_DHR12RD) .....	420
14.5.10	DUAL DAC 12-bit left aligned data holding register (DAC_DHR12LD) .....	420
14.5.11	DUAL DAC 8-bit right aligned data holding register (DAC_DHR8RD) .....	421
14.5.12	DAC channel1 data output register (DAC_DOR1) .....	421
14.5.13	DAC channel2 data output register (DAC_DOR2) .....	421
14.5.14	DAC status register (DAC_SR) .....	422
14.5.15	DAC register map .....	423
<b>15</b>	<b>Digital camera interface (DCMI) .....</b>	<b>424</b>
15.1	Introduction .....	424
15.2	DCMI main features .....	424
15.3	DCMI functional description .....	424
15.3.1	DCMI block diagram .....	425
15.3.2	DCMI pins .....	425
15.3.3	DCMI clocks .....	425
15.3.4	DCMI DMA interface .....	426
15.3.5	DCMI physical interface .....	426
15.3.6	DCMI synchronization .....	428
15.3.7	DCMI capture modes .....	430
15.3.8	DCMI crop feature .....	431
15.3.9	DCMI JPEG format .....	432
15.3.10	DCMI FIFO .....	432
15.3.11	DCMI data format description .....	433
15.4	DCMI interrupts .....	435
15.5	DCMI registers .....	436
15.5.1	DCMI control register (DCMI_CR) .....	436
15.5.2	DCMI status register (DCMI_SR) .....	438
15.5.3	DCMI raw interrupt status register (DCMI_RIS) .....	439

15.5.4	DCMI interrupt enable register (DCMI_IER) . . . . .	440
15.5.5	DCMI masked interrupt status register (DCMI_MIS) . . . . .	441
15.5.6	DCMI interrupt clear register (DCMI_ICR) . . . . .	442
15.5.7	DCMI embedded synchronization code register (DCMI_ESCR) . . . . .	442
15.5.8	DCMI embedded synchronization unmask register (DCMI_ESUR) . . . . .	444
15.5.9	DCMI crop window start (DCMI_CWSTRT) . . . . .	444
15.5.10	DCMI crop window size (DCMI_CWSIZE) . . . . .	445
15.5.11	DCMI data register (DCMI_DR) . . . . .	445
15.5.12	DCMI register map . . . . .	447
<b>16</b>	<b>Advanced-control timers (TIM1&amp;TIM8) . . . . .</b>	<b>448</b>
16.1	TIM1&TIM8 introduction . . . . .	448
16.2	TIM1&TIM8 main features . . . . .	448
16.3	TIM1&TIM8 functional description . . . . .	450
16.3.1	Time-base unit . . . . .	450
16.3.2	Counter modes . . . . .	452
16.3.3	Repetition counter . . . . .	461
16.3.4	Clock selection . . . . .	464
16.3.5	Capture/compare channels . . . . .	467
16.3.6	Input capture mode . . . . .	470
16.3.7	PWM input mode . . . . .	471
16.3.8	Forced output mode . . . . .	471
16.3.9	Output compare mode . . . . .	472
16.3.10	PWM mode . . . . .	473
16.3.11	Complementary outputs and dead-time insertion . . . . .	476
16.3.12	Using the break function . . . . .	478
16.3.13	Clearing the OCxREF signal on an external event . . . . .	481
16.3.14	6-step PWM generation . . . . .	482
16.3.15	One-pulse mode . . . . .	483
16.3.16	Encoder interface mode . . . . .	484
16.3.17	Timer input XOR function . . . . .	487
16.3.18	Interfacing with Hall sensors . . . . .	487
16.3.19	TIMx and external trigger synchronization . . . . .	489
16.3.20	Timer synchronization . . . . .	492
16.3.21	Debug mode . . . . .	492
16.4	TIM1&TIM8 registers . . . . .	493
16.4.1	TIM1&TIM8 control register 1 (TIMx_CR1) . . . . .	493

16.4.2	TIM1&TIM8 control register 2 (TIMx_CR2) .....	494
16.4.3	TIM1&TIM8 slave mode control register (TIMx_SMCR) .....	496
16.4.4	TIM1&TIM8 DMA/interrupt enable register (TIMx_DIER) .....	498
16.4.5	TIM1&TIM8 status register (TIMx_SR) .....	500
16.4.6	TIM1&TIM8 event generation register (TIMx_EGR) .....	501
16.4.7	TIM1&TIM8 capture/compare mode register 1 (TIMx_CCMR1) .....	503
16.4.8	TIM1&TIM8 capture/compare mode register 2 (TIMx_CCMR2) .....	506
16.4.9	TIM1&TIM8 capture/compare enable register (TIMx_CCER) .....	507
16.4.10	TIM1&TIM8 counter (TIMx_CNT) .....	511
16.4.11	TIM1&TIM8 prescaler (TIMx_PSC) .....	511
16.4.12	TIM1&TIM8 auto-reload register (TIMx_ARR) .....	511
16.4.13	TIM1&TIM8 repetition counter register (TIMx_RCR) .....	512
16.4.14	TIM1&TIM8 capture/compare register 1 (TIMx_CCR1) .....	512
16.4.15	TIM1&TIM8 capture/compare register 2 (TIMx_CCR2) .....	513
16.4.16	TIM1&TIM8 capture/compare register 3 (TIMx_CCR3) .....	513
16.4.17	TIM1&TIM8 capture/compare register 4 (TIMx_CCR4) .....	514
16.4.18	TIM1&TIM8 break and dead-time register (TIMx_BDTR) .....	514
16.4.19	TIM1&TIM8 DMA control register (TIMx_DCR) .....	516
16.4.20	TIM1&TIM8 DMA address for full transfer (TIMx_DMAR) .....	517
16.4.21	TIM1&TIM8 register map .....	518
<b>17</b>	<b>General-purpose timers (TIM2 to TIM5) .....</b>	<b>520</b>
17.1	TIM2 to TIM5 introduction .....	520
17.2	TIM2 to TIM5 main features .....	520
17.3	TIM2 to TIM5 functional description .....	521
17.3.1	Time-base unit .....	521
17.3.2	Counter modes .....	523
17.3.3	Clock selection .....	532
17.3.4	Capture/compare channels .....	535
17.3.5	Input capture mode .....	537
17.3.6	PWM input mode .....	538
17.3.7	Forced output mode .....	539
17.3.8	Output compare mode .....	540
17.3.9	PWM mode .....	541
17.3.10	One-pulse mode .....	544
17.3.11	Clearing the OCxREF signal on an external event .....	545
17.3.12	Encoder interface mode .....	546

17.3.13	Timer input XOR function	549
17.3.14	Timers and external trigger synchronization	549
17.3.15	Timer synchronization	552
17.3.16	Debug mode	557
17.4	TIM2 to TIM5 registers	558
17.4.1	TIMx control register 1 (TIMx_CR1)	558
17.4.2	TIMx control register 2 (TIMx_CR2)	560
17.4.3	TIMx slave mode control register (TIMx_SMCR)	561
17.4.4	TIMx DMA/Interrupt enable register (TIMx_DIER)	563
17.4.5	TIMx status register (TIMx_SR)	564
17.4.6	TIMx event generation register (TIMx_EGR)	566
17.4.7	TIMx capture/compare mode register 1 (TIMx_CCMR1)	567
17.4.8	TIMx capture/compare mode register 2 (TIMx_CCMR2)	570
17.4.9	TIMx capture/compare enable register (TIMx_CCER)	571
17.4.10	TIMx counter (TIMx_CNT)	573
17.4.11	TIMx prescaler (TIMx_PSC)	573
17.4.12	TIMx auto-reload register (TIMx_ARR)	573
17.4.13	TIMx capture/compare register 1 (TIMx_CCR1)	574
17.4.14	TIMx capture/compare register 2 (TIMx_CCR2)	574
17.4.15	TIMx capture/compare register 3 (TIMx_CCR3)	575
17.4.16	TIMx capture/compare register 4 (TIMx_CCR4)	575
17.4.17	TIMx DMA control register (TIMx_DCR)	576
17.4.18	TIMx DMA address for full transfer (TIMx_DMAR)	576
17.4.19	TIM2 option register (TIM2_OR)	577
17.4.20	TIM5 option register (TIM5_OR)	578
17.4.21	TIMx register map	579
<b>18</b>	<b>General-purpose timers (TIM9 to TIM14)</b>	<b>581</b>
18.1	TIM9 to TIM14 introduction	581
18.2	TIM9 to TIM14 main features	581
18.2.1	TIM9/TIM12 main features	581
18.2.2	TIM10/TIM11 and TIM13/TIM14 main features	582
18.3	TIM9 to TIM14 functional description	584
18.3.1	Time-base unit	584
18.3.2	Counter modes	586
18.3.3	Clock selection	589
18.3.4	Capture/compare channels	591



18.3.5	Input capture mode .....	592
18.3.6	PWM input mode (only for TIM9/12) .....	593
18.3.7	Forced output mode .....	594
18.3.8	Output compare mode .....	595
18.3.9	PWM mode .....	596
18.3.10	One-pulse mode .....	597
18.3.11	TIM9/12 external trigger synchronization .....	599
18.3.12	Timer synchronization (TIM9/12) .....	602
18.3.13	Debug mode .....	602
18.4	TIM9 and TIM12 registers .....	602
18.4.1	TIM9/12 control register 1 (TIMx_CR1) .....	602
18.4.2	TIM9/12 slave mode control register (TIMx_SMCR) .....	604
18.4.3	TIM9/12 Interrupt enable register (TIMx_DIER) .....	605
18.4.4	TIM9/12 status register (TIMx_SR) .....	606
18.4.5	TIM9/12 event generation register (TIMx_EGR) .....	608
18.4.6	TIM9/12 capture/compare mode register 1 (TIMx_CCMR1) .....	608
18.4.7	TIM9/12 capture/compare enable register (TIMx_CCER) .....	612
18.4.8	TIM9/12 counter (TIMx_CNT) .....	613
18.4.9	TIM9/12 prescaler (TIMx_PSC) .....	613
18.4.10	TIM9/12 auto-reload register (TIMx_ARR) .....	613
18.4.11	TIM9/12 capture/compare register 1 (TIMx_CCR1) .....	614
18.4.12	TIM9/12 capture/compare register 2 (TIMx_CCR2) .....	614
18.4.13	TIM9/12 register map .....	615
18.5	TIM10/11/13/14 registers .....	617
18.5.1	TIM10/11/13/14 control register 1 (TIMx_CR1) .....	617
18.5.2	TIM10/11/13/14 Interrupt enable register (TIMx_DIER) .....	618
18.5.3	TIM10/11/13/14 status register (TIMx_SR) .....	618
18.5.4	TIM10/11/13/14 event generation register (TIMx_EGR) .....	619
18.5.5	TIM10/11/13/14 capture/compare mode register 1 (TIMx_CCMR1) .....	620
18.5.6	TIM10/11/13/14 capture/compare enable register (TIMx_CCER) .....	623
18.5.7	TIM10/11/13/14 counter (TIMx_CNT) .....	624
18.5.8	TIM10/11/13/14 prescaler (TIMx_PSC) .....	624
18.5.9	TIM10/11/13/14 auto-reload register (TIMx_ARR) .....	624
18.5.10	TIM10/11/13/14 capture/compare register 1 (TIMx_CCR1) .....	625
18.5.11	TIM11 option register 1 (TIM11_OR) .....	625

18.5.12	TIM10/11/13/14 register map	626
<b>19</b>	<b>Basic timers (TIM6&amp;TIM7)</b>	<b>628</b>
19.1	TIM6&TIM7 introduction	628
19.2	TIM6&TIM7 main features	628
19.3	TIM6&TIM7 functional description	629
19.3.1	Time-base unit	629
19.3.2	Counting mode	631
19.3.3	Clock source	633
19.3.4	Debug mode	634
19.4	TIM6&TIM7 registers	634
19.4.1	TIM6&TIM7 control register 1 (TIMx_CR1)	634
19.4.2	TIM6&TIM7 control register 2 (TIMx_CR2)	636
19.4.3	TIM6&TIM7 DMA/Interrupt enable register (TIMx_DIER)	636
19.4.4	TIM6&TIM7 status register (TIMx_SR)	637
19.4.5	TIM6&TIM7 event generation register (TIMx_EGR)	637
19.4.6	TIM6&TIM7 counter (TIMx_CNT)	637
19.4.7	TIM6&TIM7 prescaler (TIMx_PSC)	638
19.4.8	TIM6&TIM7 auto-reload register (TIMx_ARR)	638
19.4.9	TIM6&TIM7 register map	639
<b>20</b>	<b>Independent watchdog (IWDG)</b>	<b>640</b>
20.1	IWDG introduction	640
20.2	IWDG main features	640
20.3	IWDG functional description	640
20.3.1	Hardware watchdog	640
20.3.2	Register access protection	640
20.3.3	Debug mode	641
20.4	IWDG registers	642
20.4.1	Key register (IWDG_KR)	642
20.4.2	Prescaler register (IWDG_PR)	643
20.4.3	Reload register (IWDG_RLR)	644
20.4.4	Status register (IWDG_SR)	644
20.4.5	IWDG register map	645
<b>21</b>	<b>Window watchdog (WWDG)</b>	<b>646</b>

21.1	WWDG introduction .....	646
21.2	WWDG main features .....	646
21.3	WWDG functional description .....	646
21.4	How to program the watchdog timeout .....	648
21.5	Debug mode .....	649
21.6	WWDG registers .....	650
21.6.1	Control register (WWDG_CR) .....	650
21.6.2	Configuration register (WWDG_CFR) .....	651
21.6.3	Status register (WWDG_SR) .....	651
21.6.4	WWDG register map .....	652
<b>22</b>	<b>Real-time clock (RTC) .....</b>	<b>653</b>
22.1	Introduction .....	653
22.2	RTC main features .....	653
22.3	RTC functional description .....	655
22.3.1	Clock and prescalers .....	655
22.3.2	Real-time clock and calendar .....	655
22.3.3	Programmable alarms .....	656
22.3.4	Periodic auto-wakeup .....	656
22.3.5	RTC initialization and configuration .....	657
22.3.6	Reading the calendar .....	659
22.3.7	Resetting the RTC .....	660
22.3.8	RTC synchronization .....	660
22.3.9	RTC reference clock detection .....	661
22.3.10	RTC coarse digital calibration .....	661
22.3.11	RTC smooth digital calibration .....	662
22.3.12	Timestamp function .....	664
22.3.13	Tamper detection .....	665
22.3.14	Calibration clock output .....	667
22.3.15	Alarm output .....	667
22.4	RTC and low power modes .....	668
22.5	RTC interrupts .....	668
22.6	RTC registers .....	670
22.6.1	RTC time register (RTC_TR) .....	670
22.6.2	RTC date register (RTC_DR) .....	671
22.6.3	RTC control register (RTC_CR) .....	672

22.6.4	RTC initialization and status register (RTC_ISR) . . . . .	674
22.6.5	RTC prescaler register (RTC_PRER) . . . . .	676
22.6.6	RTC wakeup timer register (RTC_WUTR) . . . . .	677
22.6.7	RTC calibration register (RTC_CALIBR) . . . . .	677
22.6.8	RTC alarm A register (RTC_ALRMAR) . . . . .	679
22.6.9	RTC alarm B register (RTC_ALRMBR) . . . . .	680
22.6.10	RTC write protection register (RTC_WPR) . . . . .	681
22.6.11	RTC sub second register (RTC_SSR) . . . . .	681
22.6.12	RTC shift control register (RTC_SHIFTR) . . . . .	682
22.6.13	RTC time stamp time register (RTC_TSTR) . . . . .	683
22.6.14	RTC time stamp date register (RTC_TSDR) . . . . .	683
22.6.15	RTC timestamp sub second register (RTC_TSSSR) . . . . .	684
22.6.16	RTC calibration register (RTC_CALR) . . . . .	684
22.6.17	RTC tamper and alternate function configuration register (RTC_TAFCR) . . . . .	685
22.6.18	RTC alarm A sub second register (RTC_ALRMASR) . . . . .	687
22.6.19	RTC alarm B sub second register (RTC_ALRMBSSR) . . . . .	688
22.6.20	RTC backup registers (RTC_BKPxR) . . . . .	689
22.6.21	RTC register map . . . . .	690
<b>23</b>	<b>Fast-mode Plus Inter-integrated circuit (FMPI2C) interface . . . . .</b>	<b>692</b>
23.1	Introduction . . . . .	692
23.2	FMPI2C main features . . . . .	692
23.3	FMPI2C implementation . . . . .	693
23.4	FMPI2C functional description . . . . .	693
23.4.1	FMPI2C block diagram . . . . .	694
23.4.2	FMPI2C pins and internal signals . . . . .	695
23.4.3	FMPI2C clock requirements . . . . .	695
23.4.4	Mode selection . . . . .	696
23.4.5	FMPI2C initialization . . . . .	696
23.4.6	Software reset . . . . .	701
23.4.7	Data transfer . . . . .	702
23.4.8	FMPI2C slave mode . . . . .	704
23.4.9	FMPI2C master mode . . . . .	713
23.4.10	FMPI2C_TIMINGR register configuration examples . . . . .	725
23.4.11	SMBus specific features . . . . .	726
23.4.12	SMBus initialization . . . . .	729

23.4.13	SMBus: FMPI2C_TIMEOUTR register configuration examples . . . . .	731
23.4.14	SMBus slave mode . . . . .	731
23.4.15	Error conditions . . . . .	738
23.4.16	DMA requests . . . . .	740
23.4.17	Debug mode . . . . .	741
23.5	FMPI2C low-power modes . . . . .	741
23.6	FMPI2C interrupts . . . . .	742
23.7	FMPI2C registers . . . . .	743
23.7.1	FMPI2C control register 1 (FMPI2C_CR1) . . . . .	743
23.7.2	FMPI2C control register 2 (FMPI2C_CR2) . . . . .	745
23.7.3	FMPI2C own address 1 register (FMPI2C_OAR1) . . . . .	747
23.7.4	FMPI2C own address 2 register (FMPI2C_OAR2) . . . . .	749
23.7.5	FMPI2C timing register (FMPI2C_TIMINGR) . . . . .	750
23.7.6	FMPI2C timeout register (FMPI2C_TIMEOUTR) . . . . .	751
23.7.7	FMPI2C interrupt and status register (FMPI2C_ISR) . . . . .	752
23.7.8	FMPI2C interrupt clear register (FMPI2C_ICR) . . . . .	754
23.7.9	FMPI2C PEC register (FMPI2C_PECR) . . . . .	755
23.7.10	FMPI2C receive data register (FMPI2C_RXDR) . . . . .	756
23.7.11	FMPI2C transmit data register (FMPI2C_TXDR) . . . . .	756
23.7.12	FMPI2C register map . . . . .	757
<b>24</b>	<b>Inter-integrated circuit (I<sup>2</sup>C) interface . . . . .</b>	<b>759</b>
24.1	I <sup>2</sup> C introduction . . . . .	759
24.2	I <sup>2</sup> C main features . . . . .	760
24.3	I <sup>2</sup> C functional description . . . . .	761
24.3.1	Mode selection . . . . .	761
24.3.2	I2C slave mode . . . . .	762
24.3.3	I2C master mode . . . . .	765
24.3.4	Error conditions . . . . .	771
24.3.5	Programmable noise filter . . . . .	772
24.3.6	SDA/SCL line control . . . . .	773
24.3.7	SMBus . . . . .	773
24.3.8	DMA requests . . . . .	776
24.3.9	Packet error checking . . . . .	777
24.4	I <sup>2</sup> C interrupts . . . . .	778
24.5	I <sup>2</sup> C debug mode . . . . .	780

24.6	I <sup>2</sup> C registers	780
24.6.1	I <sup>2</sup> C control register 1 (I2C_CR1)	780
24.6.2	I <sup>2</sup> C control register 2 (I2C_CR2)	782
24.6.3	I <sup>2</sup> C own address register 1 (I2C_OAR1)	784
24.6.4	I <sup>2</sup> C own address register 2 (I2C_OAR2)	784
24.6.5	I <sup>2</sup> C data register (I2C_DR)	785
24.6.6	I <sup>2</sup> C status register 1 (I2C_SR1)	785
24.6.7	I <sup>2</sup> C status register 2 (I2C_SR2)	789
24.6.8	I <sup>2</sup> C clock control register (I2C_CCR)	790
24.6.9	I <sup>2</sup> C TRISE register (I2C_TRISE)	791
24.6.10	I <sup>2</sup> C FLTR register (I2C_FLTR)	792
24.6.11	I2C register map	793
<b>25</b>	<b>Universal synchronous receiver transmitter (USART) /universal asynchronous receiver transmitter (UART)</b>	<b>794</b>
25.1	USART introduction	794
25.2	USART main features	795
25.3	USART implementation	796
25.4	USART functional description	796
25.4.1	USART character description	799
25.4.2	Transmitter	800
25.4.3	Receiver	803
25.4.4	Fractional baud rate generation	808
25.4.5	USART receiver tolerance to clock deviation	817
25.4.6	Multiprocessor communication	818
25.4.7	Parity control	820
25.4.8	LIN (local interconnection network) mode	821
25.4.9	USART synchronous mode	823
25.4.10	Single-wire half-duplex communication	825
25.4.11	Smartcard	826
25.4.12	IrDA SIR ENDEC block	828
25.4.13	Continuous communication using DMA	830
25.4.14	Hardware flow control	832
25.5	USART interrupts	834
25.6	USART registers	835
25.6.1	Status register (USART_SR)	835
25.6.2	Data register (USART_DR)	838

	25.6.3	Baud rate register (USART_BRR) .....	838
	25.6.4	Control register 1 (USART_CR1) .....	839
	25.6.5	Control register 2 (USART_CR2) .....	841
	25.6.6	Control register 3 (USART_CR3) .....	842
	25.6.7	Guard time and prescaler register (USART_GTPR) .....	844
	25.6.8	USART register map .....	845
<b>26</b>		<b>Serial peripheral interface/ inter-IC sound (SPI/I2S) .....</b>	<b>846</b>
	26.1	Introduction .....	846
	26.1.1	SPI main features .....	846
	26.1.2	SPI extended features .....	847
	26.1.3	I2S features .....	847
	26.2	SPI/I2S implementation .....	847
	26.3	SPI functional description .....	848
	26.3.1	General description .....	848
	26.3.2	Communications between one master and one slave .....	849
	26.3.3	Standard multi-slave communication .....	852
	26.3.4	Multi-master communication .....	853
	26.3.5	Slave select (NSS) pin management .....	853
	26.3.6	Communication formats .....	855
	26.3.7	SPI configuration .....	857
	26.3.8	Procedure for enabling SPI .....	857
	26.3.9	Data transmission and reception procedures .....	858
	26.3.10	Procedure for disabling the SPI .....	860
	26.3.11	Communication using DMA (direct memory addressing) .....	861
	26.3.12	SPI status flags .....	863
	26.3.13	SPI error flags .....	864
	26.4	SPI special features .....	865
	26.4.1	TI mode .....	865
	26.4.2	CRC calculation .....	866
	26.5	SPI interrupts .....	868
	26.6	I <sup>2</sup> S functional description .....	869
	26.6.1	I <sup>2</sup> S general description .....	869
	26.6.2	I2S full-duplex .....	870
	26.6.3	Supported audio protocols .....	871
	26.6.4	Clock generator .....	878

26.6.5	I <sup>2</sup> S master mode	880
26.6.6	I <sup>2</sup> S slave mode	882
26.6.7	I <sup>2</sup> S status flags	883
26.6.8	I <sup>2</sup> S error flags	884
26.6.9	I <sup>2</sup> S interrupts	885
26.6.10	DMA features	885
26.7	SPI and I <sup>2</sup> S registers	886
26.7.1	SPI control register 1 (SPI_CR1) (not used in I <sup>2</sup> S mode)	886
26.7.2	SPI control register 2 (SPI_CR2)	888
26.7.3	SPI status register (SPI_SR)	889
26.7.4	SPI data register (SPI_DR)	891
26.7.5	SPI CRC polynomial register (SPI_CRCPR) (not used in I <sup>2</sup> S mode)	891
26.7.6	SPI RX CRC register (SPI_RXCRCR) (not used in I <sup>2</sup> S mode)	892
26.7.7	SPI TX CRC register (SPI_TXCRCR) (not used in I <sup>2</sup> S mode)	892
26.7.8	SPI_I <sup>2</sup> S configuration register (SPI_I2SCFGR)	893
26.7.9	SPI_I <sup>2</sup> S prescaler register (SPI_I2SPR)	894
26.7.10	SPI register map	896
<b>27</b>	<b>SPDIF receiver interface (SPDIFRX)</b>	<b>897</b>
27.1	SPDIFRX interface introduction	897
27.2	SPDIFRX main features	897
27.3	SPDIFRX functional description	897
27.3.1	S/PDIF protocol (IEC-60958)	898
27.3.2	SPDIFRX decoder (SPDIFRX_DC)	901
27.3.3	SPDIFRX tolerance to clock deviation	905
27.3.4	SPDIFRX synchronization	905
27.3.5	SPDIFRX handling	907
27.3.6	Data reception management	909
27.3.7	Dedicated control flow	911
27.3.8	Reception errors	912
27.3.9	Clocking strategy	914
27.3.10	DMA interface	914
27.3.11	Interrupt generation	915
27.3.12	Register protection	916
27.4	Programming procedures	917
27.4.1	Initialization phase	917



27.4.2	Handling of interrupts coming from SPDIFRX	918
27.4.3	Handling of interrupts coming from DMA	919
27.5	SPDIFRX interface registers	919
27.5.1	Control register (SPDIFRX_CR)	919
27.5.2	Interrupt mask register (SPDIFRX_IMR)	922
27.5.3	Status register (SPDIFRX_SR)	923
27.5.4	Interrupt flag clear register (SPDIFRX_IFCR)	925
27.5.5	Data input register (SPDIFRX_FMT0_DR)	926
27.5.6	Data input register (SPDIFRX_FMT1_DR)	927
27.5.7	Data input register (SPDIFRX_FMT2_DR)	928
27.5.8	Channel status register (SPDIFRX_CSR)	929
27.5.9	Debug information register (SPDIFRX_DIR)	929
27.5.10	SPDIFRX interface register map	931
<b>28</b>	<b>Serial audio interface (SAI)</b>	<b>932</b>
28.1	Introduction	932
28.2	SAI main features	932
28.3	SAI functional description	933
28.3.1	SAI block diagram	933
28.3.2	SAI pins and internal signals	934
28.3.3	Main SAI modes	935
28.3.4	SAI synchronization mode	936
28.3.5	Audio data size	937
28.3.6	Frame synchronization	937
28.3.7	Slot configuration	940
28.3.8	SAI clock generator	942
28.3.9	Internal FIFOs	944
28.3.10	AC'97 link controller	946
28.3.11	SPDIF output	948
28.3.12	Specific features	951
28.3.13	Error flags	955
28.3.14	Disabling the SAI	958
28.3.15	SAI DMA interface	958
28.4	SAI interrupts	959
28.5	SAI registers	961
28.5.1	SAI global configuration register (SAI_GCR)	961

28.5.2	SAI configuration register 1 (SAI_ACR1) .....	961
28.5.3	SAI configuration register 1 (SAI_BCR1) .....	964
28.5.4	SAI configuration register 2 (SAI_ACR2) .....	967
28.5.5	SAI configuration register 2 (SAI_BCR2) .....	969
28.5.6	SAI frame configuration register (SAI_AFRCR) .....	971
28.5.7	SAI frame configuration register (SAI_BFRCR) .....	972
28.5.8	SAI slot register (SAI_ASLOTR) .....	973
28.5.9	SAI slot register (SAI_BSLOTR) .....	974
28.5.10	SAI interrupt mask register (SAI_AIM) .....	975
28.5.11	SAI interrupt mask register (SAI_BIM) .....	977
28.5.12	SAI status register (SAI_ASR) .....	978
28.5.13	SAI status register (SAI_BSR) .....	980
28.5.14	SAI clear flag register (SAI_ACLRFR) .....	982
28.5.15	SAI clear flag register (SAI_BCLRFR) .....	983
28.5.16	SAI data register (SAI_ADR) .....	984
28.5.17	SAI data register (SAI_BDR) .....	985
28.5.18	SAI register map .....	985
<b>29</b>	<b>Secure digital input/output interface (SDIO) .....</b>	<b>987</b>
29.1	SDIO main features .....	987
29.2	SDIO bus topology .....	987
29.3	SDIO functional description .....	989
29.3.1	SDIO adapter .....	991
29.3.2	SDIO APB2 interface .....	1002
29.4	Card functional description .....	1003
29.4.1	Card identification mode .....	1003
29.4.2	Card reset .....	1004
29.4.3	Operating voltage range validation .....	1004
29.4.4	Card identification process .....	1004
29.4.5	Block write .....	1005
29.4.6	Block read .....	1006
29.4.7	Stream access, stream write and stream read (MultiMediaCard only) .....	1006
29.4.8	Erase: group erase and sector erase .....	1008
29.4.9	Wide bus selection or deselection .....	1008
29.4.10	Protection management .....	1008
29.4.11	Card status register .....	1012

29.4.12	SD status register	1015
29.4.13	SD I/O mode	1019
29.4.14	Commands and responses	1020
29.5	Response formats	1023
29.5.1	R1 (normal response command)	1024
29.5.2	R1b	1024
29.5.3	R2 (CID, CSD register)	1024
29.5.4	R3 (OCR register)	1025
29.5.5	R4 (Fast I/O)	1025
29.5.6	R4b	1025
29.5.7	R5 (interrupt request)	1026
29.5.8	R6	1026
29.6	SDIO I/O card-specific operations	1027
29.6.1	SDIO I/O read wait operation by SDIO_D2 signalling	1027
29.6.2	SDIO read wait operation by stopping SDIO_CLK	1028
29.6.3	SDIO suspend/resume operation	1028
29.6.4	SDIO interrupts	1028
29.7	HW flow control	1028
29.8	SDIO registers	1029
29.8.1	SDIO power control register (SDIO_POWER)	1029
29.8.2	SDIO clock control register (SDIO_CLKCR)	1029
29.8.3	SDIO argument register (SDIO_ARG)	1031
29.8.4	SDIO command register (SDIO_CMD)	1031
29.8.5	SDIO command response register (SDIO_RESPCMD)	1032
29.8.6	SDIO response 1..4 register (SDIO_RESPx)	1032
29.8.7	SDIO data timer register (SDIO_DTIMER)	1033
29.8.8	SDIO data length register (SDIO_DLEN)	1034
29.8.9	SDIO data control register (SDIO_DCTRL)	1034
29.8.10	SDIO data counter register (SDIO_DCOUNT)	1037
29.8.11	SDIO status register (SDIO_STA)	1037
29.8.12	SDIO interrupt clear register (SDIO_ICR)	1038
29.8.13	SDIO mask register (SDIO_MASK)	1040
29.8.14	SDIO FIFO counter register (SDIO_FIFOCNT)	1042
29.8.15	SDIO data FIFO register (SDIO_FIFO)	1043
29.8.16	SDIO register map	1044

## 30      **Controller area network (bxCAN) . . . . . 1046**

30.1	Introduction	1046
30.2	bxCAN main features	1046
30.3	bxCAN general description	1047
30.3.1	CAN 2.0B active core	1047
30.3.2	Control, status and configuration registers	1047
30.3.3	Tx mailboxes	1047
30.3.4	Acceptance filters	1048
30.4	bxCAN operating modes	1049
30.4.1	Initialization mode	1049
30.4.2	Normal mode	1049
30.4.3	Sleep mode (low-power)	1050
30.5	Test mode	1051
30.5.1	Silent mode	1051
30.5.2	Loop back mode	1051
30.5.3	Loop back combined with silent mode	1052
30.6	Behavior in debug mode	1052
30.7	bxCAN functional description	1052
30.7.1	Transmission handling	1052
30.7.2	Time triggered communication mode	1054
30.7.3	Reception handling	1054
30.7.4	Identifier filtering	1056
30.7.5	Message storage	1060
30.7.6	Error management	1061
30.7.7	Bit timing	1061
30.8	bxCAN interrupts	1065
30.9	CAN registers	1066
30.9.1	Register access protection	1066
30.9.2	CAN control and status registers	1066
30.9.3	CAN mailbox registers	1077
30.9.4	CAN filter registers	1082
30.9.5	bxCAN register map	1086
<b>31</b>	<b>USB on-the-go full-speed/high-speed (OTG_FS/OTG_HS)</b>	<b>1090</b>
31.1	Introduction	1090
31.2	OTG_FS/OTG_HS main features	1092
31.2.1	General features	1092

31.2.2	Host-mode features .....	1093
31.2.3	Peripheral-mode features .....	1093
31.3	OTG_FS/OTG_HS implementation .....	1094
31.4	OTG_FS/OTG_HS functional description .....	1095
31.4.1	OTG_FS/OTG_HS block diagram .....	1095
31.4.2	OTG_FS/OTG_HS pin and internal signals .....	1096
31.4.3	OTG_FS/OTG_HS core .....	1097
31.4.4	Embedded full-speed OTG PHY connected to OTG_FS .....	1097
31.4.5	Embedded full-speed OTG PHY connected to OTG_HS .....	1098
31.4.6	OTG detections .....	1098
31.4.7	High-speed OTG PHY connected to OTG_HS .....	1098
31.5	OTG_FS/OTG_HS dual role device (DRD) .....	1099
31.5.1	ID line detection .....	1099
31.5.2	HNP dual role device .....	1099
31.5.3	SRP dual role device .....	1100
31.6	OTG_FS/OTG_HS as a USB peripheral .....	1100
31.6.1	SRP-capable peripheral .....	1101
31.6.2	Peripheral states .....	1101
31.6.3	Peripheral endpoints .....	1102
31.7	OTG_FS/OTG_HS as a USB host .....	1104
31.7.1	SRP-capable host .....	1105
31.7.2	USB host states .....	1105
31.7.3	Host channels .....	1107
31.7.4	Host scheduler .....	1108
31.8	OTG_FS/OTG_HS SOF trigger .....	1109
31.8.1	Host SOFs .....	1109
31.8.2	Peripheral SOFs .....	1109
31.9	OTG_FS/OTG_HS low-power modes .....	1110
31.10	OTG_FS/OTG_HS Dynamic update of the OTG_HFIR register .....	1111
31.11	OTG_FS/OTG_HS data FIFOs .....	1111
31.11.1	Peripheral FIFO architecture .....	1112
31.11.2	Host FIFO architecture .....	1113
31.11.3	FIFO RAM allocation .....	1114
31.12	OTG_FS system performance .....	1116
31.13	OTG_FS/ <b>OTG_HS</b> interrupts .....	1116
31.14	OTG_FS/ <b>OTG_HS</b> control and status registers .....	1118

31.14.1	CSR memory map	1118
31.15	OTG_FS/OTG_HS registers	1124
31.15.1	OTG control and status register (OTG_GOTGCTL)	1124
31.15.2	OTG interrupt register (OTG_GOTGINT)	1127
31.15.3	OTG AHB configuration register (OTG_GAHBCFG)	1129
31.15.4	OTG USB configuration register (OTG_GUSBCFG)	1131
31.15.5	OTG reset register (OTG_GRSTCTL)	1134
31.15.6	OTG core interrupt register (OTG_GINTSTS)	1137
31.15.7	OTG interrupt mask register (OTG_GINTMSK)	1142
31.15.8	OTG receive status debug read register (OTG_GRXSTSR)	1145
31.15.9	OTG receive status debug read [alternate] (OTG_GRXSTSR)	1146
31.15.10	OTG status read and pop registers (OTG_GRXSTSP)	1147
31.15.11	OTG status read and pop registers [alternate] (OTG_GRXSTSP)	1148
31.15.12	OTG receive FIFO size register (OTG_GRXFSIZ)	1149
31.15.13	OTG host non-periodic transmit FIFO size register (OTG_HNPTXFSIZ)/Endpoint 0 Transmit FIFO size (OTG_DIEPTXF0)	1150
31.15.14	OTG non-periodic transmit FIFO/queue status register (OTG_HNPTXSTS)	1151
31.15.15	OTG general core configuration register (OTG_GCCFG)	1152
31.15.16	OTG core ID register (OTG_CID)	1153
31.15.17	OTG core LPM configuration register (OTG_GLPMCFG)	1153
31.15.18	OTG host periodic transmit FIFO size register (OTG_HPTXFSIZ)	1157
31.15.19	OTG device IN endpoint transmit FIFO x size register (OTG_DIEPTXFx)	1157
31.15.20	Host-mode registers	1158
31.15.21	OTG host configuration register (OTG_HCFG)	1158
31.15.22	OTG host frame interval register (OTG_HFIR)	1159
31.15.23	OTG host frame number/frame time remaining register (OTG_HFNUM)	1160
31.15.24	OTG_Host periodic transmit FIFO/queue status register (OTG_HPTXSTS)	1160
31.15.25	OTG host all channels interrupt register (OTG_HAINT)	1161
31.15.26	OTG host all channels interrupt mask register (OTG_HAINTMSK)	1162
31.15.27	OTG host port control and status register (OTG_HPRT)	1163
31.15.28	OTG host channel x characteristics register (OTG_HCCHARx)	1165
31.15.29	OTG host channel x split control register (OTG_HCSPLTx)	1166

31.15.30 OTG host channel x interrupt register (OTG_HCINTx) . . . . .	1167
31.15.31 OTG host channel x interrupt mask register (OTG_HCINTMSKx) . .	1169
31.15.32 OTG host channel x transfer size register (OTG_HCTSIZx) . . . . .	1170
31.15.33 OTG host channel x DMA address register (OTG_HCDMAx) . . . . .	1171
31.15.34 Device-mode registers . . . . .	1172
31.15.35 OTG device configuration register (OTG_DCFG) . . . . .	1172
31.15.36 OTG device control register (OTG_DCTL) . . . . .	1174
31.15.37 OTG device status register (OTG_DSTS) . . . . .	1176
31.15.38 OTG device IN endpoint common interrupt mask register (OTG_DIEPMSK) . . . . .	1177
31.15.39 OTG device OUT endpoint common interrupt mask register (OTG_DOEPMSK) . . . . .	1178
31.15.40 OTG device all endpoints interrupt register (OTG_DAINTE) . . . . .	1180
31.15.41 OTG all endpoints interrupt mask register (OTG_DAINTEMSK) . . . . .	1180
31.15.42 OTG device $V_{BUS}$ discharge time register (OTG_DVBUSDIS) . . . . .	1181
31.15.43 OTG device $V_{BUS}$ pulsing time register (OTG_DVBUSPULSE) . . . . .	1181
31.15.44 OTG device threshold control register (OTG_DTHRCTL) . . . . .	1182
31.15.45 OTG device IN endpoint FIFO empty interrupt mask register (OTG_DIEPEMPMSK) . . . . .	1183
31.15.46 OTG device each endpoint interrupt register (OTG_DEACHINT) . . .	1184
31.15.47 OTG device each endpoint interrupt mask register (OTG_DEACHINTMSK) . . . . .	1184
31.15.48 OTG device each IN endpoint-1 interrupt mask register (OTG_HS_DIEPEACHMSK1) . . . . .	1185
31.15.49 OTG device each OUT endpoint-1 interrupt mask register (OTG_HS_DOEPEACHMSK1) . . . . .	1186
31.15.50 OTG device control IN endpoint 0 control register (OTG_DIEPCTL0) . . . . .	1187
31.15.51 OTG device IN endpoint x control register (OTG_DIEPCTLx) . . . .	1189
31.15.52 OTG device IN endpoint x interrupt register (OTG_DIEPINTx) . . . .	1191
31.15.53 OTG device IN endpoint 0 transfer size register (OTG_DIEPTSIZ0) . . . . .	1193
31.15.54 OTG device IN endpoint x DMA address register (OTG_DIEPDMAx) . . . . .	1194
31.15.55 OTG device IN endpoint transmit FIFO status register (OTG_DTXFSTSx) . . . . .	1194
31.15.56 OTG device IN endpoint x transfer size register (OTG_DIEPTSIZx) .	1195

31.15.57	OTG device control OUT endpoint 0 control register (OTG_DOEPCTL0) .....	1196
31.15.58	OTG device OUT endpoint x interrupt register (OTG_DOEPINTx) ..	1197
31.15.59	OTG device OUT endpoint 0 transfer size register (OTG_DOEPSIZ0) .....	1199
31.15.60	OTG device OUT endpoint x DMA address register (OTG_DOEPDMAx) .....	1200
31.15.61	OTG device OUT endpoint x control register (OTG_DOEPCTLx) .....	1201
31.15.62	OTG device OUT endpoint x transfer size register (OTG_DOEPSIZx) .....	1203
31.15.63	OTG power and clock gating control register (OTG_PCGCCTL) ...	1204
31.15.64	OTG_FS/OTG_HS register map .....	1205
31.16	OTG_FS/OTG_HS programming model .....	1218
31.16.1	Core initialization .....	1218
31.16.2	Host initialization .....	1219
31.16.3	Device initialization .....	1220
31.16.4	DMA mode .....	1220
31.16.5	Host programming model .....	1220
31.16.6	Device programming model .....	1254
31.16.7	Worst case response time .....	1274
31.16.8	OTG programming model .....	1276
<b>32</b>	<b>HDMI-CEC controller (CEC) .....</b>	<b>1283</b>
32.1	Introduction .....	1283
32.2	HDMI-CEC controller main features .....	1283
32.3	HDMI-CEC functional description .....	1284
32.3.1	HDMI-CEC pin .....	1284
32.3.2	HDMI-CEC block diagram .....	1284
32.3.3	Message description .....	1284
32.3.4	Bit timing .....	1285
32.4	Arbitration .....	1286
32.4.1	SFT option bit .....	1287
32.5	Error handling .....	1288
32.5.1	Bit error .....	1288
32.5.2	Message error .....	1288
32.5.3	Bit rising error (BRE) .....	1288
32.5.4	Short bit period error (SBPE) .....	1289



32.5.5	Long bit period error (LBPE) . . . . .	1289
32.5.6	Transmission error detection (TXERR) . . . . .	1290
32.6	HDMI-CEC interrupts . . . . .	1292
32.7	HDMI-CEC registers . . . . .	1293
32.7.1	CEC control register (CEC_CR) . . . . .	1293
32.7.2	CEC configuration register (CEC_CFGR) . . . . .	1294
32.7.3	CEC Tx data register (CEC_TXDR) . . . . .	1296
32.7.4	CEC Rx data register (CEC_RXDR) . . . . .	1296
32.7.5	CEC interrupt and status register (CEC_ISR) . . . . .	1296
32.7.6	CEC interrupt enable register (CEC_IER) . . . . .	1298
32.7.7	HDMI-CEC register map . . . . .	1300
<b>33</b>	<b>Debug support (DBG) . . . . .</b>	<b>1301</b>
33.1	Overview . . . . .	1301
33.2	Reference Arm® documentation . . . . .	1302
33.3	SWJ debug port (serial wire and JTAG) . . . . .	1302
33.3.1	Mechanism to select the JTAG-DP or the SW-DP . . . . .	1303
33.4	Pinout and debug port pins . . . . .	1303
33.4.1	SWJ debug port pins . . . . .	1304
33.4.2	Flexible SWJ-DP pin assignment . . . . .	1304
33.4.3	Internal pull-up and pull-down on JTAG pins . . . . .	1304
33.4.4	Using serial wire and releasing the unused debug pins as GPIOs . . . . .	1305
33.5	STM32F446xx JTAG TAP connection . . . . .	1305
33.6	ID codes and locking mechanism . . . . .	1307
33.6.1	MCU device ID code . . . . .	1307
33.6.2	Boundary scan TAP . . . . .	1307
33.6.3	Cortex®-M4 with FPU TAP . . . . .	1307
33.6.4	Cortex®-M4 with FPU JEDEC-106 ID code . . . . .	1308
33.7	JTAG debug port . . . . .	1308
33.8	SW debug port . . . . .	1310
33.8.1	SW protocol introduction . . . . .	1310
33.8.2	SW protocol sequence . . . . .	1310
33.8.3	SW-DP state machine (reset, idle states, ID code) . . . . .	1311
33.8.4	DP and AP read/write accesses . . . . .	1312
33.8.5	SW-DP registers . . . . .	1312
33.8.6	SW-AP registers . . . . .	1313

33.9	AHB-AP (AHB access port) - valid for both JTAG-DP and SW-DP	1314
33.10	Core debug	1315
33.11	Capability of the debugger host to connect under system reset	1316
33.12	FPB (Flash patch breakpoint)	1316
33.13	DWT (data watchpoint trigger)	1317
33.14	ITM (instrumentation trace macrocell)	1317
33.14.1	General description	1317
33.14.2	Time stamp packets, synchronization and overflow packets	1317
33.15	ETM (Embedded trace macrocell)	1319
33.15.1	General description	1319
33.15.2	Signal protocol, packet types	1319
33.15.3	Main ETM registers	1320
33.15.4	Configuration example	1320
33.16	MCU debug component (DBGMCU)	1320
33.16.1	Debug support for low-power modes	1321
33.16.2	Debug support for timers, watchdog, bxCAN and I <sup>2</sup> C	1321
33.16.3	Debug MCU configuration register	1321
33.16.4	Debug MCU APB1 freeze register (DBGMCU_APB1_FZ)	1324
33.16.5	Debug MCU APB2 Freeze register (DBGMCU_APB2_FZ)	1326
33.17	TPIU (trace port interface unit)	1327
33.17.1	Introduction	1327
33.17.2	TRACE pin assignment	1328
33.17.3	TPUI formatter	1330
33.17.4	TPUI frame synchronization packets	1330
33.17.5	Transmission of the synchronization frame packet	1330
33.17.6	Synchronous mode	1331
33.17.7	Asynchronous mode	1331
33.17.8	TRACECLKIN connection in STM32F446xx	1331
33.17.9	TPIU registers	1331
33.17.10	Example of configuration	1332
33.18	DBG register map	1333
<b>34</b>	<b>Device electronic signature</b>	<b>1334</b>
34.1	Unique device ID register (96 bits)	1334
34.2	Flash memory size register	1335

	34.3	Package data register .....	1335
<b>35</b>		<b>Revision history .....</b>	<b>1337</b>

## List of tables

Table 1.	STM32F446xx register boundary addresses .....	57
Table 2.	Boot modes .....	61
Table 3.	Memory mapping vs. Boot mode/physical remap in STM32F446xx .....	62
Table 4.	Flash module organization .....	65
Table 5.	Number of wait states according to CPU clock (HCLK) frequency .....	66
Table 6.	Program/erase parallelism .....	70
Table 7.	Flash interrupt request .....	72
Table 8.	Option byte organization .....	72
Table 9.	Description of the option bytes .....	73
Table 10.	Access versus read protection level .....	76
Table 11.	OTP area organization .....	79
Table 12.	Flash register map and reset value .....	87
Table 13.	CRC calculation unit register map and reset values .....	91
Table 14.	Voltage regulator configuration mode versus device operating mode .....	96
Table 15.	Low-power mode summary .....	101
Table 16.	Sleep-now entry and exit .....	103
Table 17.	Stop operating modes .....	104
Table 18.	Stop mode entry and exit for STM32F446xx .....	106
Table 19.	Standby mode entry and exit .....	107
Table 20.	PWR - register map and reset values .....	115
Table 21.	RCC register map and reset values .....	172
Table 22.	Port bit configuration table .....	177
Table 23.	Flexible SWJ-DP pin assignment .....	179
Table 24.	RTC_AF1 pin .....	186
Table 25.	RTC_AF2 pin .....	187
Table 26.	GPIO register map and reset values .....	193
Table 27.	SYSCFG register map and reset values .....	202
Table 28.	DMA1 request mapping .....	207
Table 29.	DMA2 request mapping .....	207
Table 30.	Source and destination address .....	208
Table 31.	Source and destination address registers in double-buffer mode (DBM = 1) .....	214
Table 32.	Packing/unpacking and endian behavior (bit PINC = MINC = 1) .....	215
Table 33.	Restriction on NDT versus PSIZE and MSIZE .....	215
Table 34.	FIFO threshold configurations .....	218
Table 35.	Possible DMA configurations .....	222
Table 36.	DMA interrupt requests .....	224
Table 37.	DMA register map and reset values .....	235
Table 38.	Vector table for STM32F446xx .....	239
Table 39.	External interrupt/event controller register map and reset values .....	250
Table 40.	NOR/PSRAM bank selection .....	256
Table 41.	NOR/PSRAM External memory address .....	256
Table 42.	NAND memory mapping and timing registers .....	256
Table 43.	NAND bank selection .....	256
Table 44.	SDRAM bank selection .....	257
Table 45.	SDRAM address mapping .....	257
Table 46.	SDRAM address mapping with 8-bit data bus width .....	258
Table 47.	SDRAM address mapping with 16-bit data bus width .....	259
Table 48.	Programmable NOR/PSRAM access parameters .....	260

Table 49.	Non-multiplexed I/O NOR Flash memory	261
Table 50.	16-bit multiplexed I/O NOR Flash memory	261
Table 51.	Non-multiplexed I/Os PSRAM/SRAM	262
Table 52.	16-Bit multiplexed I/O PSRAM	262
Table 53.	NOR Flash/PSRAM: example of supported memories and transactions	263
Table 54.	FMC_BCRx bitfields (mode 1)	266
Table 55.	FMC_BTRx bitfields (mode 1)	266
Table 56.	FMC_BCRx bitfields (mode A)	268
Table 57.	FMC_BTRx bitfields (mode A)	268
Table 58.	FMC_BWTRx bitfields (mode A)	269
Table 59.	FMC_BCRx bitfields (mode 2/B)	271
Table 60.	FMC_BTRx bitfields (mode 2/B)	271
Table 61.	FMC_BWTRx bitfields (mode 2/B)	272
Table 62.	FMC_BCRx bitfields (mode C)	273
Table 63.	FMC_BTRx bitfields (mode C)	274
Table 64.	FMC_BWTRx bitfields (mode C)	274
Table 65.	FMC_BCRx bitfields (mode D)	276
Table 66.	FMC_BTRx bitfields (mode D)	276
Table 67.	FMC_BWTRx bitfields (mode D)	277
Table 68.	FMC_BCRx bitfields (Muxed mode)	278
Table 69.	FMC_BTRx bitfields (Muxed mode)	279
Table 70.	FMC_BCRx bitfields (Synchronous multiplexed read mode)	284
Table 71.	FMC_BTRx bitfields (Synchronous multiplexed read mode)	285
Table 72.	FMC_BCRx bitfields (Synchronous multiplexed write mode)	286
Table 73.	FMC_BTRx bitfields (Synchronous multiplexed write mode)	287
Table 74.	Programmable NAND Flash access parameters	295
Table 75.	8-bit NAND Flash	295
Table 76.	16-bit NAND Flash	296
Table 77.	Supported memories and transactions	297
Table 78.	ECC result relevant bits	306
Table 79.	SDRAM signals	307
Table 80.	FMC register map and reset values	323
Table 81.	QUADSPI pins	327
Table 82.	QUADSPI interrupt requests	341
Table 83.	QUADSPI register map and reset values	354
Table 84.	ADC pins	357
Table 85.	Analog watchdog channel selection	363
Table 86.	Configuring the trigger polarity	368
Table 87.	External trigger for regular channels	368
Table 88.	External trigger for injected channels	369
Table 89.	ADC interrupts	383
Table 90.	ADC global register map	399
Table 91.	ADC register map and reset values for each ADC	399
Table 92.	ADC register map and reset values (common ADC registers)	401
Table 93.	DAC pins	403
Table 94.	External triggers	406
Table 95.	DAC register map	423
Table 96.	DCMI input/output pins	425
Table 97.	Positioning of captured data bytes in 32-bit words (8-bit width)	427
Table 98.	Positioning of captured data bytes in 32-bit words (10-bit width)	427
Table 99.	Positioning of captured data bytes in 32-bit words (12-bit width)	427

Table 100.	Positioning of captured data bytes in 32-bit words (14-bit width)	428
Table 101.	Data storage in monochrome progressive video format	433
Table 102.	Data storage in RGB progressive video format	434
Table 103.	Data storage in YCbCr progressive video format	434
Table 104.	Data storage in YCbCr progressive video format - Y extraction mode	435
Table 105.	DCMI interrupts	435
Table 106.	DCMI register map and reset values	447
Table 107.	Counting direction versus encoder signals	485
Table 108.	TIMx Internal trigger connection	498
Table 109.	Output control bits for complementary OCx and OCxN channels with break feature	510
Table 110.	TIM1&TIM8 register map and reset values	518
Table 111.	Counting direction versus encoder signals	547
Table 112.	TIMx internal trigger connections	562
Table 113.	Output control bit for standard OCx channels	572
Table 114.	TIM2 to TIM5 register map and reset values	579
Table 115.	TIMx internal trigger connections	605
Table 116.	Output control bit for standard OCx channels	613
Table 117.	TIM9/12 register map and reset values	615
Table 118.	Output control bit for standard OCx channels	623
Table 119.	TIM10/11/13/14 register map and reset values	626
Table 120.	TIM6&TIM7 register map and reset values	639
Table 121.	Min/max IWDG timeout period at 32 kHz (LSI)	641
Table 122.	IWDG register map and reset values	645
Table 123.	WWDG register map and reset values	652
Table 124.	Effect of low power modes on RTC	668
Table 125.	Interrupt control bits	669
Table 126.	RTC register map and reset values	690
Table 127.	STM32F446xx FMPI2C implementation	693
Table 128.	FMPI2C input/output pins	695
Table 129.	FMPI2C internal input/output signals	695
Table 130.	Comparison of analog vs. digital filters	697
Table 131.	I2C-SMBus specification data setup and hold times	700
Table 132.	FMPI2C configuration	704
Table 133.	I2C-SMBus specification clock timings	715
Table 134.	Examples of timing settings for fI2CCLK = 8 MHz	725
Table 135.	Examples of timings settings for fI2CCLK = 16 MHz	725
Table 136.	SMBus timeout specifications	728
Table 137.	SMBus with PEC configuration	730
Table 138.	Examples of TIMEOUTA settings for various FMPI2CCLK frequencies (max t <sub>TIMEOUT</sub> = 25 ms)	731
Table 139.	Examples of TIMEOUTB settings for various FMPI2CCLK frequencies	731
Table 140.	Examples of TIMEOUTA settings for various FMPI2CCLK frequencies (max t <sub>IDLE</sub> = 50 µs)	731
Table 141.	Effect of low-power modes on the FMPI2C	741
Table 142.	FMPI2C Interrupt requests	742
Table 143.	FMPI2C register map and reset values	757
Table 144.	Maximum DNF[3:0] value to be compliant with Thd:dat(max)	772
Table 145.	SMBus vs. I2C	774
Table 146.	I2C Interrupt requests	778
Table 147.	I2C register map and reset values	793
Table 148.	USART features	796

Table 149.	Noise detection from sampled data . . . . .	807
Table 150.	Error calculation for programmed baud rates at $f_{PCLK} = 8\text{ MHz}$ or $f_{PCLK} = 12\text{ MHz}$ , oversampling by 16. . . . .	810
Table 151.	Error calculation for programmed baud rates at $f_{PCLK} = 8\text{ MHz}$ or $f_{PCLK} = 12\text{ MHz}$ , oversampling by 8. . . . .	810
Table 152.	Error calculation for programmed baud rates at $f_{PCLK} = 16\text{ MHz}$ or $f_{PCLK} = 24\text{ MHz}$ , oversampling by 16. . . . .	811
Table 153.	Error calculation for programmed baud rates at $f_{PCLK} = 16\text{ MHz}$ or $f_{PCLK} = 24\text{ MHz}$ , oversampling by 8. . . . .	812
Table 154.	Error calculation for programmed baud rates at $f_{PCLK} = 8\text{ MHz}$ or $f_{PCLK} = 16\text{ MHz}$ , oversampling by 16. . . . .	812
Table 155.	Error calculation for programmed baud rates at $f_{PCLK} = 8\text{ MHz}$ or $f_{PCLK} = 16\text{ MHz}$ , oversampling by 8. . . . .	813
Table 156.	Error calculation for programmed baud rates at $f_{PCLK} = 30\text{ MHz}$ or $f_{PCLK} = 60\text{ MHz}$ , oversampling by 16. . . . .	814
Table 157.	Error calculation for programmed baud rates at $f_{PCLK} = 30\text{ MHz}$ or $f_{PCLK} = 60\text{ MHz}$ , oversampling by 8 . . . . .	814
Table 158.	Error calculation for programmed baud rates at $f_{PCLK} = 42\text{ MHz}$ or $f_{PCLK} = 84\text{ Hz}$ , oversampling by 16. . . . .	815
Table 159.	Error calculation for programmed baud rates at $f_{PCLK} = 42\text{ MHz}$ or $f_{PCLK} = 84\text{ MHz}$ , oversampling by 8. . . . .	816
Table 160.	USART receiver tolerance when DIV fraction is 0 . . . . .	817
Table 161.	USART receiver tolerance when DIV_Fraction is different from 0 . . . . .	818
Table 162.	Frame formats . . . . .	820
Table 163.	USART interrupt requests. . . . .	834
Table 164.	USART register map and reset values . . . . .	845
Table 165.	STM32F446xx SPI implementation . . . . .	847
Table 166.	SPI interrupt requests . . . . .	868
Table 167.	Audio-frequency precision using standard 8 MHz HSE . . . . .	879
Table 168.	I <sup>2</sup> S interrupt requests . . . . .	885
Table 169.	SPI register map and reset values . . . . .	896
Table 170.	Transition sequence for preamble . . . . .	904
Table 171.	Minimum SPDIFRX_CLK frequency versus audio sampling rate. . . . .	914
Table 172.	Bit field property versus SPDIFRX state. . . . .	916
Table 173.	SPDIFRX interface register map and reset values . . . . .	931
Table 174.	SAI internal input/output signals . . . . .	934
Table 175.	SAI input/output pins. . . . .	934
Table 176.	External synchronization selection . . . . .	937
Table 177.	Example of possible audio frequency sampling range . . . . .	943
Table 178.	SOPD pattern . . . . .	949
Table 179.	Parity bit calculation . . . . .	949
Table 180.	Audio sampling frequency versus symbol rates . . . . .	950
Table 181.	SAI interrupt sources . . . . .	959
Table 182.	SAI register map and reset values . . . . .	985
Table 183.	SDIO I/O definitions . . . . .	990
Table 184.	Command format . . . . .	995
Table 185.	Short response format . . . . .	996
Table 186.	Long response format. . . . .	996
Table 187.	Command path status flags . . . . .	996
Table 188.	Data token format . . . . .	999
Table 189.	DPSM flags. . . . .	1000
Table 190.	Transmit FIFO status flags . . . . .	1001



Table 191.	Receive FIFO status flags	1001
Table 192.	Card status	1012
Table 193.	SD status	1015
Table 194.	Speed class code field	1016
Table 195.	Performance move field	1017
Table 196.	AU_SIZE field	1017
Table 197.	Maximum AU size	1017
Table 198.	Erase size field	1018
Table 199.	Erase timeout field	1018
Table 200.	Erase offset field	1018
Table 201.	Block-oriented write commands	1021
Table 202.	Block-oriented write protection commands	1022
Table 203.	Erase commands	1022
Table 204.	I/O mode commands	1022
Table 205.	Lock card	1023
Table 206.	Application-specific commands	1023
Table 207.	R1 response	1024
Table 208.	R2 response	1024
Table 209.	R3 response	1025
Table 210.	R4 response	1025
Table 211.	R4b response	1025
Table 212.	R5 response	1026
Table 213.	R6 response	1027
Table 214.	Response type and SDIO_RESPx registers	1033
Table 215.	SDIO register map	1044
Table 216.	Transmit mailbox mapping	1060
Table 217.	Receive mailbox mapping	1060
Table 218.	bxCAN register map and reset values	1086
Table 219.	OTG_HS speeds supported	1091
Table 220.	OTG_FS speeds supported	1091
Table 221.	OTG_FS/OTG_HS implementation	1094
Table 222.	OTG_FS input/output pins	1096
Table 223.	OTG_HS input/output pins	1096
Table 224.	OTG_FS/OTG_HS input/output signals	1097
Table 225.	Compatibility of STM32 low power modes with the OTG	1110
Table 226.	Core global control and status registers (CSRs)	1118
Table 227.	Host-mode control and status registers (CSRs)	1119
Table 228.	Device-mode control and status registers	1121
Table 229.	Data FIFO (DFIFO) access register map	1124
Table 230.	Power and clock gating control and status registers	1124
Table 231.	TRDT values (FS)	1134
Table 232.	TRDT values (HS)	1134
Table 233.	Minimum duration for soft disconnect	1175
Table 234.	OTG_FS/OTG_HS register map and reset values	1205
Table 235.	HDMI pin	1284
Table 236.	Error handling timing parameters	1290
Table 237.	TXERR timing parameters	1291
Table 238.	HDMI-CEC interrupts	1292
Table 239.	HDMI-CEC register map and reset values	1300
Table 240.	SWJ debug port pins	1304
Table 241.	Flexible SWJ-DP pin assignment	1304
Table 242.	JTAG debug port data registers	1308



Table 243.	32-bit debug port registers addressed through the shifted value A[3:2] . . . . .	1310
Table 244.	Packet request (8-bits) . . . . .	1311
Table 245.	ACK response (3 bits). . . . .	1311
Table 246.	DATA transfer (33 bits). . . . .	1311
Table 247.	SW-DP registers . . . . .	1312
Table 248.	Cortex <sup>®</sup> -M4 with FPU AHB-AP registers . . . . .	1314
Table 249.	Core debug registers . . . . .	1315
Table 250.	Main ITM registers . . . . .	1318
Table 251.	Main ETM registers. . . . .	1320
Table 252.	Asynchronous TRACE pin assignment. . . . .	1328
Table 253.	Synchronous TRACE pin assignment . . . . .	1328
Table 254.	Flexible TRACE pin assignment . . . . .	1329
Table 255.	Important TPIU registers. . . . .	1332
Table 256.	DBG register map and reset values . . . . .	1333
Table 257.	Document revision history . . . . .	1337

## List of figures

Figure 1.	System architecture for STM32F446xx devices . . . . .	54
Figure 2.	Memory map . . . . .	57
Figure 3.	Flash memory interface connection inside system architecture . . . . .	64
Figure 4.	Sequential 32-bit instruction execution . . . . .	68
Figure 5.	RDP levels . . . . .	77
Figure 6.	PCROP levels . . . . .	79
Figure 7.	CRC calculation unit block diagram . . . . .	88
Figure 8.	Power supply overview for STM32F446xx . . . . .	92
Figure 9.	Backup domain . . . . .	95
Figure 10.	Power-on reset/power-down reset waveform . . . . .	98
Figure 11.	BOR thresholds . . . . .	99
Figure 12.	PVD thresholds . . . . .	100
Figure 13.	Simplified diagram of the reset circuit . . . . .	117
Figure 14.	Clock tree . . . . .	118
Figure 15.	HSE/ LSE clock sources (hardware configuration) . . . . .	120
Figure 16.	Frequency measurement with TIM5 in Input capture mode . . . . .	125
Figure 17.	Frequency measurement with TIM11 in Input capture mode . . . . .	126
Figure 18.	Basic structure of a 5 V tolerant I/O port bit . . . . .	177
Figure 19.	Selecting an alternate function on STM32F446xx . . . . .	180
Figure 20.	Input floating/pull up/pull down configurations . . . . .	183
Figure 21.	Output configuration . . . . .	184
Figure 22.	Alternate function configuration . . . . .	184
Figure 23.	High impedance-analog configuration . . . . .	185
Figure 24.	DMA block diagram . . . . .	205
Figure 25.	Channel selection . . . . .	206
Figure 26.	Peripheral-to-memory mode . . . . .	210
Figure 27.	Memory-to-peripheral mode . . . . .	211
Figure 28.	Memory-to-memory mode . . . . .	212
Figure 29.	FIFO structure . . . . .	217
Figure 30.	External interrupt/event controller block diagram . . . . .	244
Figure 31.	External interrupt/event GPIO mapping . . . . .	246
Figure 32.	FMC block diagram . . . . .	252
Figure 33.	FMC memory banks . . . . .	255
Figure 34.	Mode 1 read access waveforms . . . . .	265
Figure 35.	Mode 1 write access waveforms . . . . .	265
Figure 36.	Mode A read access waveforms . . . . .	267
Figure 37.	Mode A write access waveforms . . . . .	267
Figure 38.	Mode 2 and mode B read access waveforms . . . . .	269
Figure 39.	Mode 2 write access waveforms . . . . .	270
Figure 40.	Mode B write access waveforms . . . . .	270
Figure 41.	Mode C read access waveforms . . . . .	272
Figure 42.	Mode C write access waveforms . . . . .	273
Figure 43.	Mode D read access waveforms . . . . .	275
Figure 44.	Mode D write access waveforms . . . . .	275
Figure 45.	Muxed read access waveforms . . . . .	277
Figure 46.	Muxed write access waveforms . . . . .	278
Figure 47.	Asynchronous wait during a read access waveforms . . . . .	280
Figure 48.	Asynchronous wait during a write access waveforms . . . . .	281

Figure 49.	Wait configuration waveforms . . . . .	283
Figure 50.	Synchronous multiplexed read mode waveforms - NOR, PSRAM (CRAM) . . . . .	284
Figure 51.	Synchronous multiplexed write mode waveforms - PSRAM (CRAM) . . . . .	286
Figure 52.	NAND Flash controller waveforms for common memory access . . . . .	298
Figure 53.	Access to non 'CE don't care' NAND-Flash . . . . .	299
Figure 54.	Burst write SDRAM access waveforms . . . . .	309
Figure 55.	Burst read SDRAM access . . . . .	310
Figure 56.	Logic diagram of Read access with RBURST bit set (CAS=1, RPIPE=0) . . . . .	311
Figure 57.	Read access crossing row boundary . . . . .	313
Figure 58.	Write access crossing row boundary . . . . .	313
Figure 59.	Self-refresh mode . . . . .	315
Figure 60.	Power-down mode . . . . .	316
Figure 61.	QUADSPI block diagram when dual-flash mode is disabled . . . . .	326
Figure 62.	QUADSPI block diagram when dual-flash mode is enabled . . . . .	327
Figure 63.	An example of a read command in quad mode . . . . .	328
Figure 64.	An example of a DDR command in quad mode . . . . .	331
Figure 65.	nCS when CKMODE = 0 (T = CLK period) . . . . .	339
Figure 66.	nCS when CKMODE = 1 in SDR mode (T = CLK period) . . . . .	339
Figure 67.	nCS when CKMODE = 1 in DDR mode (T = CLK period) . . . . .	340
Figure 68.	nCS when CKMODE = 1 with an abort (T = CLK period) . . . . .	340
Figure 69.	Single ADC block diagram . . . . .	356
Figure 70.	ADC1 connectivity . . . . .	358
Figure 71.	ADC2 connectivity . . . . .	359
Figure 72.	ADC3 connectivity . . . . .	360
Figure 73.	Timing diagram . . . . .	363
Figure 74.	Analog watchdog's guarded area . . . . .	363
Figure 75.	Injected conversion latency . . . . .	365
Figure 76.	Right alignment of 12-bit data . . . . .	367
Figure 77.	Left alignment of 12-bit data . . . . .	367
Figure 78.	Left alignment of 6-bit data . . . . .	367
Figure 79.	Multi ADC block diagram <sup>(1)</sup> . . . . .	372
Figure 80.	Injected simultaneous mode on 4 channels: dual ADC mode . . . . .	375
Figure 81.	Injected simultaneous mode on 4 channels: triple ADC mode . . . . .	375
Figure 82.	Regular simultaneous mode on 16 channels: dual ADC mode . . . . .	376
Figure 83.	Regular simultaneous mode on 16 channels: triple ADC mode . . . . .	376
Figure 84.	Interleaved mode on 1 channel in continuous conversion mode: dual ADC mode . . . . .	377
Figure 85.	Interleaved mode on 1 channel in continuous conversion mode: triple ADC mode . . . . .	378
Figure 86.	Alternate trigger: injected group of each ADC . . . . .	379
Figure 87.	Alternate trigger: 4 injected channels (each ADC) in discontinuous mode . . . . .	379
Figure 88.	Alternate trigger: injected group of each ADC . . . . .	380
Figure 89.	Alternate + regular simultaneous . . . . .	381
Figure 90.	Case of trigger occurring during injected conversion . . . . .	381
Figure 91.	Temperature sensor and VREFINT channel block diagram . . . . .	382
Figure 92.	DAC channel block diagram . . . . .	403
Figure 93.	DAC output buffer connection . . . . .	404
Figure 94.	Data registers in single DAC channel mode . . . . .	405
Figure 95.	Data registers in dual DAC channel mode . . . . .	405
Figure 96.	Timing diagram for conversion with trigger disabled TEN = 0 . . . . .	406
Figure 97.	DAC LFSR register calculation algorithm . . . . .	408
Figure 98.	DAC conversion (SW trigger enabled) with LFSR wave generation . . . . .	408
Figure 99.	DAC triangle wave generation . . . . .	409
Figure 100.	DAC conversion (SW trigger enabled) with triangle wave generation . . . . .	409

Figure 101. DCMI block diagram	425
Figure 102. Top-level block diagram	425
Figure 103. DCMI signal waveforms	426
Figure 104. Timing diagram	428
Figure 105. Frame capture waveforms in snapshot mode	430
Figure 106. Frame capture waveforms in continuous grab mode	431
Figure 107. Coordinates and size of the window after cropping	431
Figure 108. Data capture waveforms	432
Figure 109. Pixel raster scan order	433
Figure 110. Advanced-control timer block diagram	449
Figure 111. Counter timing diagram with prescaler division change from 1 to 2	451
Figure 112. Counter timing diagram with prescaler division change from 1 to 4	451
Figure 113. Counter timing diagram, internal clock divided by 1	452
Figure 114. Counter timing diagram, internal clock divided by 2	453
Figure 115. Counter timing diagram, internal clock divided by 4	453
Figure 116. Counter timing diagram, internal clock divided by N	453
Figure 117. Counter timing diagram, update event when ARPE=0 (TIMx_ARR not preloaded)	454
Figure 118. Counter timing diagram, update event when ARPE=1 (TIMx_ARR preloaded)	454
Figure 119. Counter timing diagram, internal clock divided by 1	456
Figure 120. Counter timing diagram, internal clock divided by 2	456
Figure 121. Counter timing diagram, internal clock divided by 4	457
Figure 122. Counter timing diagram, internal clock divided by N	457
Figure 123. Counter timing diagram, update event when repetition counter is not used	458
Figure 124. Counter timing diagram, internal clock divided by 1, TIMx_ARR = 0x6	459
Figure 125. Counter timing diagram, internal clock divided by 2	459
Figure 126. Counter timing diagram, internal clock divided by 4, TIMx_ARR=0x36	460
Figure 127. Counter timing diagram, internal clock divided by N	460
Figure 128. Counter timing diagram, update event with ARPE=1 (counter underflow)	461
Figure 129. Counter timing diagram, update event with ARPE=1 (counter overflow)	461
Figure 130. Update rate examples depending on mode and TIMx_RCR register settings	463
Figure 131. Control circuit in normal mode, internal clock divided by 1	464
Figure 132. TI2 external clock connection example	465
Figure 133. Control circuit in external clock mode 1	466
Figure 134. External trigger input block	466
Figure 135. Control circuit in external clock mode 2	467
Figure 136. Capture/compare channel (example: channel 1 input stage)	468
Figure 137. Capture/compare channel 1 main circuit	468
Figure 138. Output stage of capture/compare channel (channels 1 to 3)	469
Figure 139. Output stage of capture/compare channel (channel 4)	469
Figure 140. PWM input mode timing	471
Figure 141. Output compare mode, toggle on OC1	473
Figure 142. Edge-aligned PWM waveforms (ARR=8)	474
Figure 143. Center-aligned PWM waveforms (ARR=8)	475
Figure 144. Complementary output with dead-time insertion	477
Figure 145. Dead-time waveforms with delay greater than the negative pulse	477
Figure 146. Dead-time waveforms with delay greater than the positive pulse	477
Figure 147. Output behavior in response to a break	480
Figure 148. Clearing TIMx_OCxREF	481
Figure 149. 6-step generation, COM example (OSSR=1)	482
Figure 150. Example of one pulse mode	483

Figure 151. Example of counter operation in encoder interface mode. ....	486
Figure 152. Example of encoder interface mode with TI1FP1 polarity inverted. ....	486
Figure 153. Example of Hall sensor interface . ....	488
Figure 154. Control circuit in reset mode . ....	489
Figure 155. Control circuit in gated mode . ....	490
Figure 156. Control circuit in trigger mode . ....	491
Figure 157. Control circuit in external clock mode 2 + trigger mode . ....	492
Figure 158. General-purpose timer block diagram . ....	521
Figure 159. Counter timing diagram with prescaler division change from 1 to 2 . ....	522
Figure 160. Counter timing diagram with prescaler division change from 1 to 4 . ....	523
Figure 161. Counter timing diagram, internal clock divided by 1 . ....	524
Figure 162. Counter timing diagram, internal clock divided by 2 . ....	524
Figure 163. Counter timing diagram, internal clock divided by 4 . ....	524
Figure 164. Counter timing diagram, internal clock divided by N . ....	525
Figure 165. Counter timing diagram, Update event when ARPE=0 (TIMx_ARR not preloaded). ....	525
Figure 166. Counter timing diagram, Update event when ARPE=1 (TIMx_ARR preloaded). ....	526
Figure 167. Counter timing diagram, internal clock divided by 1 . ....	527
Figure 168. Counter timing diagram, internal clock divided by 2 . ....	527
Figure 169. Counter timing diagram, internal clock divided by 4 . ....	527
Figure 170. Counter timing diagram, internal clock divided by N . ....	528
Figure 171. Counter timing diagram, Update event . ....	528
Figure 172. Counter timing diagram, internal clock divided by 1, TIMx_ARR=0x6 . ....	529
Figure 173. Counter timing diagram, internal clock divided by 2 . ....	530
Figure 174. Counter timing diagram, internal clock divided by 4, TIMx_ARR=0x36 . ....	530
Figure 175. Counter timing diagram, internal clock divided by N . ....	530
Figure 176. Counter timing diagram, Update event with ARPE=1 (counter underflow). ....	531
Figure 177. Counter timing diagram, Update event with ARPE=1 (counter overflow). ....	531
Figure 178. Control circuit in normal mode, internal clock divided by 1 . ....	532
Figure 179. TI2 external clock connection example. ....	533
Figure 180. Control circuit in external clock mode 1 . ....	534
Figure 181. External trigger input block . ....	534
Figure 182. Control circuit in external clock mode 2 . ....	535
Figure 183. Capture/compare channel (example: channel 1 input stage) . ....	536
Figure 184. Capture/compare channel 1 main circuit . ....	536
Figure 185. Output stage of capture/compare channel (channel 1). ....	537
Figure 186. PWM input mode timing . ....	539
Figure 187. Output compare mode, toggle on OC1. ....	541
Figure 188. Edge-aligned PWM waveforms (ARR=8) . ....	542
Figure 189. Center-aligned PWM waveforms (ARR=8) . ....	543
Figure 190. Example of one-pulse mode . ....	544
Figure 191. Clearing TIMx_OCxREF . ....	546
Figure 192. Example of counter operation in encoder interface mode . ....	548
Figure 193. Example of encoder interface mode with TI1FP1 polarity inverted . ....	548
Figure 194. Control circuit in reset mode . ....	549
Figure 195. Control circuit in gated mode . ....	550
Figure 196. Control circuit in trigger mode . ....	551
Figure 197. Control circuit in external clock mode 2 + trigger mode . ....	552
Figure 198. Master/Slave timer example . ....	552
Figure 199. Gating timer 2 with OC1REF of timer 1 . ....	553
Figure 200. Gating timer 2 with Enable of timer 1 . ....	554
Figure 201. Triggering timer 2 with update of timer 1 . ....	555
Figure 202. Triggering timer 2 with Enable of timer 1 . ....	556

Figure 203. Triggering timer 1 and 2 with timer 1 TI1 input . . . . .	557
Figure 204. General-purpose timer block diagram (TIM9 and TIM12) . . . . .	582
Figure 205. General-purpose timer block diagram (TIM10/11/13/14) . . . . .	583
Figure 206. Counter timing diagram with prescaler division change from 1 to 2 . . . . .	585
Figure 207. Counter timing diagram with prescaler division change from 1 to 4 . . . . .	585
Figure 208. Counter timing diagram, internal clock divided by 1 . . . . .	586
Figure 209. Counter timing diagram, internal clock divided by 2 . . . . .	587
Figure 210. Counter timing diagram, internal clock divided by 4 . . . . .	587
Figure 211. Counter timing diagram, internal clock divided by N . . . . .	587
Figure 212. Counter timing diagram, update event when ARPE=0 (TIMx_ARR not preloaded) . . . . .	588
Figure 213. Counter timing diagram, update event when ARPE=1 (TIMx_ARR preloaded) . . . . .	588
Figure 214. Control circuit in normal mode, internal clock divided by 1 . . . . .	589
Figure 215. TI2 external clock connection example . . . . .	590
Figure 216. Control circuit in external clock mode 1 . . . . .	590
Figure 217. Capture/compare channel (example: channel 1 input stage) . . . . .	591
Figure 218. Capture/compare channel 1 main circuit . . . . .	592
Figure 219. Output stage of capture/compare channel (channel 1) . . . . .	592
Figure 220. PWM input mode timing . . . . .	594
Figure 221. Output compare mode, toggle on OC1 . . . . .	596
Figure 222. Edge-aligned PWM waveforms (ARR=8) . . . . .	597
Figure 223. Example of one pulse mode . . . . .	598
Figure 224. Control circuit in reset mode . . . . .	600
Figure 225. Control circuit in gated mode . . . . .	601
Figure 226. Control circuit in trigger mode . . . . .	601
Figure 227. Basic timer block diagram . . . . .	628
Figure 228. Counter timing diagram with prescaler division change from 1 to 2 . . . . .	630
Figure 229. Counter timing diagram with prescaler division change from 1 to 4 . . . . .	630
Figure 230. Counter timing diagram, internal clock divided by 1 . . . . .	631
Figure 231. Counter timing diagram, internal clock divided by 2 . . . . .	632
Figure 232. Counter timing diagram, internal clock divided by 4 . . . . .	632
Figure 233. Counter timing diagram, internal clock divided by N . . . . .	632
Figure 234. Counter timing diagram, update event when ARPE = 0 (TIMx_ARR not preloaded) . . . . .	633
Figure 235. Counter timing diagram, update event when ARPE=1 (TIMx_ARR preloaded) . . . . .	633
Figure 236. Control circuit in normal mode, internal clock divided by 1 . . . . .	634
Figure 237. Independent watchdog block diagram . . . . .	641
Figure 238. Watchdog block diagram . . . . .	647
Figure 239. Window watchdog timing diagram . . . . .	648
Figure 240. RTC block diagram . . . . .	654
Figure 241. FMPI2C block diagram . . . . .	694
Figure 242. I2C bus protocol . . . . .	696
Figure 243. Setup and hold timings . . . . .	698
Figure 244. FMPI2C initialization flowchart . . . . .	701
Figure 245. Data reception . . . . .	702
Figure 246. Data transmission . . . . .	703
Figure 247. Slave initialization flowchart . . . . .	706
Figure 248. Transfer sequence flowchart for FMPI2C slave transmitter, NOSTRETCH= 0 . . . . .	708
Figure 249. Transfer sequence flowchart for FMPI2C slave transmitter,	



NOSTRETCH= 1	709
Figure 250. Transfer bus diagrams for FMPI2C slave transmitter	710
Figure 251. Transfer sequence flowchart for slave receiver with NOSTRETCH=0	711
Figure 252. Transfer sequence flowchart for slave receiver with NOSTRETCH=1	712
Figure 253. Transfer bus diagrams for FMPI2C slave receiver	712
Figure 254. Master clock generation	714
Figure 255. Master initialization flowchart	716
Figure 256. 10-bit address read access with HEAD10R=0	716
Figure 257. 10-bit address read access with HEAD10R=1	717
Figure 258. Transfer sequence flowchart for FMPI2C master transmitter for $N \leq 255$ bytes	718
Figure 259. Transfer sequence flowchart for FMPI2C master transmitter for $N > 255$ bytes	719
Figure 260. Transfer bus diagrams for FMPI2C master transmitter	720
Figure 261. Transfer sequence flowchart for FMPI2C master receiver for $N \leq 255$ bytes	722
Figure 262. Transfer sequence flowchart for FMPI2C master receiver for $N > 255$ bytes	723
Figure 263. Transfer bus diagrams for FMPI2C master receiver	724
Figure 264. Timeout intervals for $t_{\text{LOW:SEXT}}$ , $t_{\text{LOW:MEXT}}$	728
Figure 265. Transfer sequence flowchart for SMBus slave transmitter N bytes + PEC	732
Figure 266. Transfer bus diagrams for SMBus slave transmitter (SBC=1)	733
Figure 267. Transfer sequence flowchart for SMBus slave receiver N Bytes + PEC	734
Figure 268. Bus transfer diagrams for SMBus slave receiver (SBC=1)	735
Figure 269. Bus transfer diagrams for SMBus master transmitter	736
Figure 270. Bus transfer diagrams for SMBus master receiver	738
Figure 271. I2C bus protocol	761
Figure 272. I2C block diagram	762
Figure 273. Transfer sequence diagram for slave transmitter	764
Figure 274. Transfer sequence diagram for slave receiver	765
Figure 275. Transfer sequence diagram for master transmitter	768
Figure 276. Transfer sequence diagram for master receiver	770
Figure 277. I2C interrupt mapping diagram	779
Figure 278. USART block diagram	798
Figure 279. Word length programming	799
Figure 280. Configurable stop bits	801
Figure 281. TC/TXE behavior when transmitting	802
Figure 282. Start bit detection when oversampling by 16 or 8	803
Figure 283. Data sampling when oversampling by 16	806
Figure 284. Data sampling when oversampling by 8	807
Figure 285. Mute mode using Idle line detection	819
Figure 286. Mute mode using address mark detection	819
Figure 287. Break detection in LIN mode (11-bit break length - LBDL bit is set)	822
Figure 288. Break detection in LIN mode vs. Framing error detection	823
Figure 289. USART example of synchronous transmission	824
Figure 290. USART data clock timing diagram (M=0)	824
Figure 291. USART data clock timing diagram (M=1)	825
Figure 292. RX data setup/hold time	825
Figure 293. ISO 7816-3 asynchronous protocol	826
Figure 294. Parity error detection using the 1.5 stop bits	827
Figure 295. IrDA SIR ENDEC- block diagram	829
Figure 296. IrDA data modulation (3/16) -Normal mode	829
Figure 297. Transmission using DMA	831
Figure 298. Reception using DMA	832
Figure 299. Hardware flow control between 2 USARTs	832
Figure 300. RTS flow control	833

Figure 301. CTS flow control . . . . .	833
Figure 302. USART interrupt mapping diagram . . . . .	835
Figure 303. SPI block diagram. . . . .	848
Figure 304. Full-duplex single master/ single slave application. . . . .	849
Figure 305. Half-duplex single master/ single slave application . . . . .	850
Figure 306. Simplex single master/single slave application (master in transmit-only/ slave in receive-only mode) . . . . .	851
Figure 307. Master and three independent slaves. . . . .	852
Figure 308. Multi-master application . . . . .	853
Figure 309. Hardware/software slave select management . . . . .	854
Figure 310. Data clock timing diagram . . . . .	856
Figure 311. TXE/RXNE/BSY behavior in master / full-duplex mode (BIDIMODE=0, RXONLY=0) in the case of continuous transfers . . . . .	859
Figure 312. TXE/RXNE/BSY behavior in slave / full-duplex mode (BIDIMODE=0, RXONLY=0) in the case of continuous transfers . . . . .	860
Figure 313. Transmission using DMA . . . . .	862
Figure 314. Reception using DMA. . . . .	863
Figure 315. TI mode transfer . . . . .	866
Figure 316. I <sup>2</sup> S block diagram . . . . .	869
Figure 317. Full-duplex communication. . . . .	871
Figure 318. I <sup>2</sup> S Philips protocol waveforms (16/32-bit full accuracy, CPOL = 0). . . . .	872
Figure 319. I <sup>2</sup> S Philips standard waveforms (24-bit frame with CPOL = 0). . . . .	872
Figure 320. Transmitting 0x8EAA33 . . . . .	873
Figure 321. Receiving 0x8EAA33 . . . . .	873
Figure 322. I <sup>2</sup> S Philips standard (16-bit extended to 32-bit packet frame with CPOL = 0) . . . . .	873
Figure 323. Example of 16-bit data frame extended to 32-bit channel frame . . . . .	874
Figure 324. MSB Justified 16-bit or 32-bit full-accuracy length with CPOL = 0 . . . . .	874
Figure 325. MSB justified 24-bit frame length with CPOL = 0 . . . . .	874
Figure 326. MSB justified 16-bit extended to 32-bit packet frame with CPOL = 0 . . . . .	875
Figure 327. LSB justified 16-bit or 32-bit full-accuracy with CPOL = 0 . . . . .	875
Figure 328. LSB justified 24-bit frame length with CPOL = 0. . . . .	875
Figure 329. Operations required to transmit 0x3478AE. . . . .	876
Figure 330. Operations required to receive 0x3478AE . . . . .	876
Figure 331. LSB justified 16-bit extended to 32-bit packet frame with CPOL = 0 . . . . .	876
Figure 332. Example of 16-bit data frame extended to 32-bit channel frame . . . . .	877
Figure 333. PCM standard waveforms (16-bit) . . . . .	877
Figure 334. PCM standard waveforms (16-bit extended to 32-bit packet frame). . . . .	877
Figure 335. Audio sampling frequency definition . . . . .	878
Figure 336. I <sup>2</sup> S clock generator architecture . . . . .	878
Figure 337. SPDIFRX block diagram. . . . .	898
Figure 338. S/PDIF sub-frame format . . . . .	899
Figure 339. S/PDIF block format . . . . .	899
Figure 340. S/PDIF Preambles . . . . .	900
Figure 341. Channel coding example . . . . .	900
Figure 342. SPDIFRX decoder . . . . .	902
Figure 343. Noise filtering and edge detection . . . . .	902
Figure 344. Thresholds . . . . .	904
Figure 345. Synchronization flowchart. . . . .	906
Figure 346. Synchronization process scheduling . . . . .	907
Figure 347. SPDIFRX States . . . . .	908
Figure 348. SPDIFRX_FMTx_DR register format . . . . .	910
Figure 349. Channel/user data format . . . . .	911



Figure 350.	S/PDIF overrun error when RXSTEO = 0	913
Figure 351.	S/PDIF overrun error when RXSTEO = 1	914
Figure 352.	SPDIFRX interface interrupt mapping diagram	915
Figure 353.	SAI functional block diagram	933
Figure 354.	Audio frame	937
Figure 355.	FS role is start of frame + channel side identification (FSDEF = TRIS = 1)	939
Figure 356.	FS role is start of frame (FSDEF = 0)	940
Figure 357.	Slot size configuration with FBOFF = 0 in SAI_xSLOTR	941
Figure 358.	First bit offset	941
Figure 359.	Audio block clock generator overview	942
Figure 360.	AC'97 audio frame	946
Figure 361.	Example of typical AC'97 configuration on devices featuring at least 2 embedded SAI (three external AC'97 decoders)	947
Figure 362.	SPDIF format	948
Figure 363.	SAI_xDR register ordering	949
Figure 364.	Data companding hardware in an audio block in the SAI	953
Figure 365.	Tristate strategy on SD output line on an inactive slot	954
Figure 366.	Tristate on output data line in a protocol like I2S	955
Figure 367.	Overrun detection error	956
Figure 368.	FIFO underrun event	956
Figure 369.	"No response" and "no data" operations	988
Figure 370.	(Multiple) block read operation	988
Figure 371.	(Multiple) block write operation	988
Figure 372.	Sequential read operation	989
Figure 373.	Sequential write operation	989
Figure 374.	SDIO block diagram	989
Figure 375.	SDIO adapter	991
Figure 376.	Control unit	992
Figure 377.	SDIO_CK clock dephasing (BYPASS = 0)	992
Figure 378.	SDIO adapter command path	993
Figure 379.	Command path state machine (SDIO)	994
Figure 380.	SDIO command transfer	995
Figure 381.	Data path	997
Figure 382.	Data path state machine (DPSM)	998
Figure 383.	CAN network topology	1047
Figure 384.	Dual-CAN block diagram	1048
Figure 385.	bxCAN operating modes	1050
Figure 386.	bxCAN in silent mode	1051
Figure 387.	bxCAN in loop back mode	1051
Figure 388.	bxCAN in combined mode	1052
Figure 389.	Transmit mailbox states	1054
Figure 390.	Receive FIFO states	1055
Figure 391.	Filter bank scale configuration - Register organization	1057
Figure 392.	Example of filter numbering	1058
Figure 393.	Filtering mechanism example	1059
Figure 394.	CAN error state diagram	1061
Figure 395.	Bit timing	1063
Figure 396.	CAN frames	1064
Figure 397.	Event flags and interrupt generation	1065
Figure 398.	CAN mailbox registers	1077
Figure 399.	OTG_FS full-speed block diagram	1095
Figure 400.	OTG_HS high-speed block diagram	1096

Figure 401. OTG_FS/OTG_HS A-B device connection . . . . .	1099
Figure 402. OTG_FS/OTG_HS peripheral-only connection . . . . .	1101
Figure 403. OTG_FS/OTG_HS host-only connection . . . . .	1105
Figure 404. SOF connectivity (SOF trigger output to TIM and ITR1 connection) . . . . .	1109
Figure 405. Updating OTG_HFIR dynamically (RLDCTRL = 1) . . . . .	1111
Figure 406. Device-mode FIFO address mapping and AHB FIFO access mapping . . . . .	1112
Figure 407. Host-mode FIFO address mapping and AHB FIFO access mapping . . . . .	1113
Figure 408. Interrupt hierarchy . . . . .	1117
Figure 409. Transmit FIFO write task . . . . .	1223
Figure 410. Receive FIFO read task . . . . .	1224
Figure 411. Normal bulk/control OUT/SETUP . . . . .	1226
Figure 412. Bulk/control IN transactions . . . . .	1230
Figure 413. Normal interrupt OUT . . . . .	1233
Figure 414. Normal interrupt IN . . . . .	1238
Figure 415. Isochronous OUT transactions . . . . .	1240
Figure 416. Isochronous IN transactions . . . . .	1243
Figure 417. Normal bulk/control OUT/SETUP transactions - DMA . . . . .	1245
Figure 418. Normal bulk/control IN transaction - DMA . . . . .	1247
Figure 419. Normal interrupt OUT transactions - DMA mode . . . . .	1248
Figure 420. Normal interrupt IN transactions - DMA mode . . . . .	1249
Figure 421. Normal isochronous OUT transaction - DMA mode . . . . .	1250
Figure 422. Normal isochronous IN transactions - DMA mode . . . . .	1251
Figure 423. Receive FIFO packet read . . . . .	1257
Figure 424. Processing a SETUP packet . . . . .	1259
Figure 425. Bulk OUT transaction . . . . .	1266
Figure 426. TRDT max timing case . . . . .	1276
Figure 427. A-device SRP . . . . .	1277
Figure 428. B-device SRP . . . . .	1278
Figure 429. A-device HNP . . . . .	1279
Figure 430. B-device HNP . . . . .	1281
Figure 431. HDMI-CEC block diagram . . . . .	1284
Figure 432. Message structure . . . . .	1285
Figure 433. Blocks . . . . .	1285
Figure 434. Bit timings . . . . .	1286
Figure 435. Signal free time . . . . .	1286
Figure 436. Arbitration phase . . . . .	1287
Figure 437. SFT of three nominal bit periods . . . . .	1287
Figure 438. Error bit timing . . . . .	1288
Figure 439. Error handling . . . . .	1289
Figure 440. TXERR detection . . . . .	1291
Figure 441. Block diagram of STM32 MCU and Cortex®-M4 with FPU-level debug support . . . . .	1301
Figure 442. SWJ debug port . . . . .	1303
Figure 443. JTAG TAP connections . . . . .	1306
Figure 444. TPIU block diagram . . . . .	1327