SoC Design Lab3 Report

312551174 張祐誠

GitHub

Overview

Lab3 和 Lab2 都是實作 FIR 濾波器，不同的地方在於 Lab3 的 Kernel Function 是要直接用 Verilog 完成的，本次 Lab 需要實作 fir.v 和 fir_tb.v，fir.v 利用 FSM 的觀念完成整體的控制判斷，而 testbench 作為本次的 host 端負責傳送資料和發起 ap 的控制訊號，另外，此實驗的 design specification 如下所示。

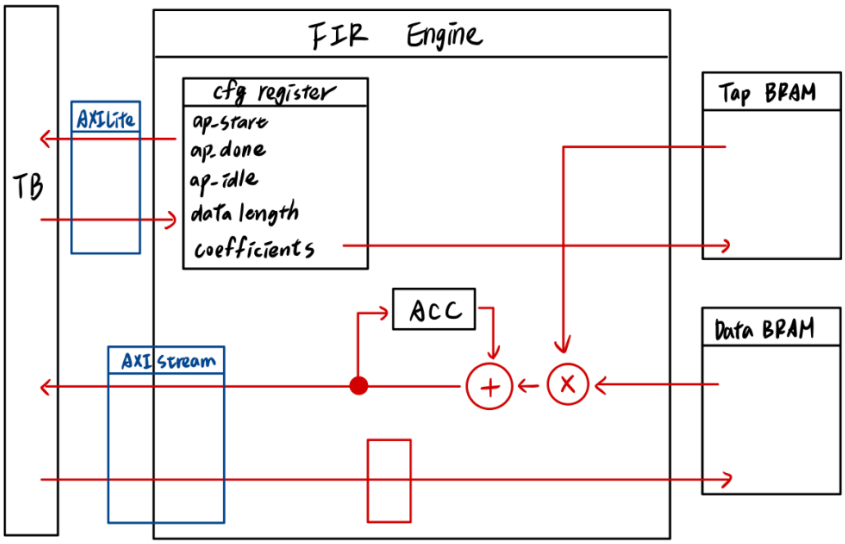
- Interface

Data	Protocol
data_in	axi-stream
data_out	axi-stream
coef	axilite
len	axilite
ap_start	axilite
ap_done	axilite

- AP control

Address	Bit	Description
0x00	0	ap_start
	1	ap_done
	2	ap_idle
0x10-0x14	31:0	data length
0x20-0xff	31:0	coef

System Architecture



System Description

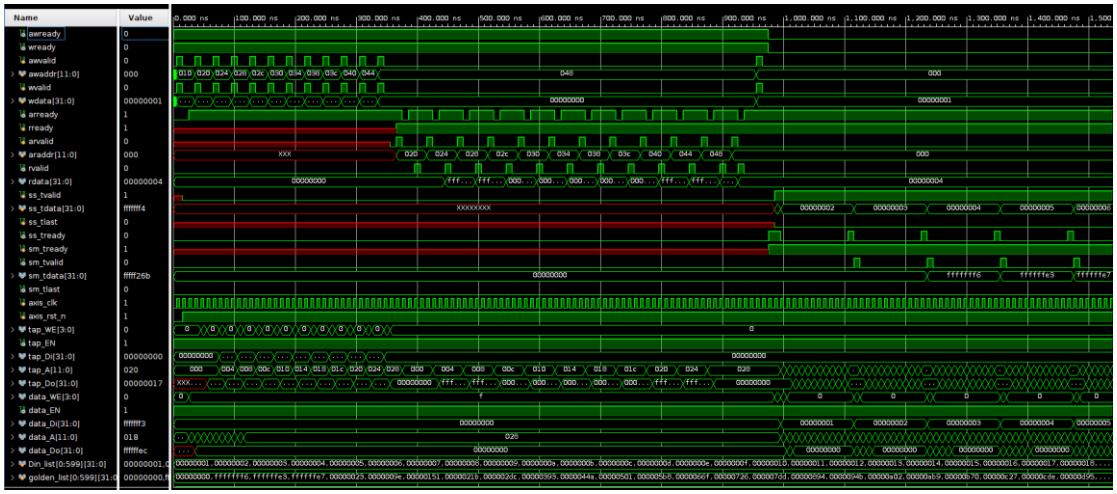
- AXI-Lite control
  1. 在傳輸 coefficient 之前，先檢查 ap_idle 訊號，若是 enable 的時候才開始啟用
  2. ap_start 由 testbech 設定，並由 FIR engine reset
- AXI-Stream control
  1. 當 FIR 需要資料的時候，ss_tready 設為 1
  2. 當 FIR 完成計算的時候，sm_tvalid 設為 1 並設定 sm_tdata 為輸出。

BRAM

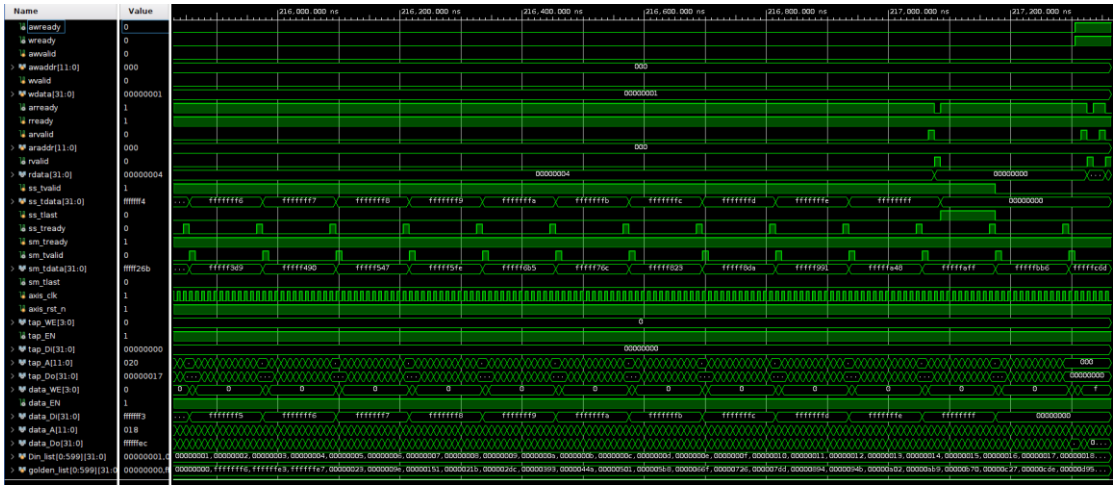
1. 由於只有一個加法器，所以需要一個暫存器用於累加 result
2. 從 data_ram 讀取的第一筆資料位址為 0，之後，位址會按遞減順序讀取
3. 從 tap_ram 讀取的第一筆資料位址為 0，之後，位址會按遞增順序讀取
4. 經過 11 個計算後將結果輸出至 output stream

Simulation

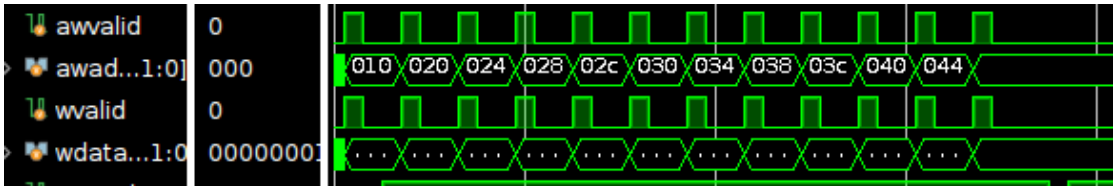
- 一開始



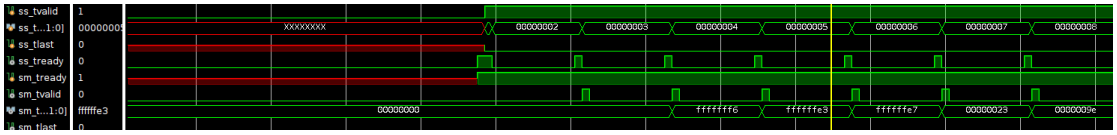
- 結束



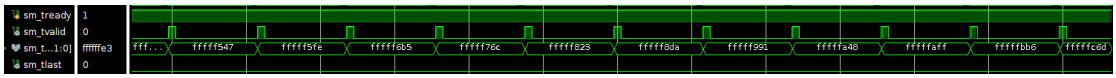
- AXILITE Coef



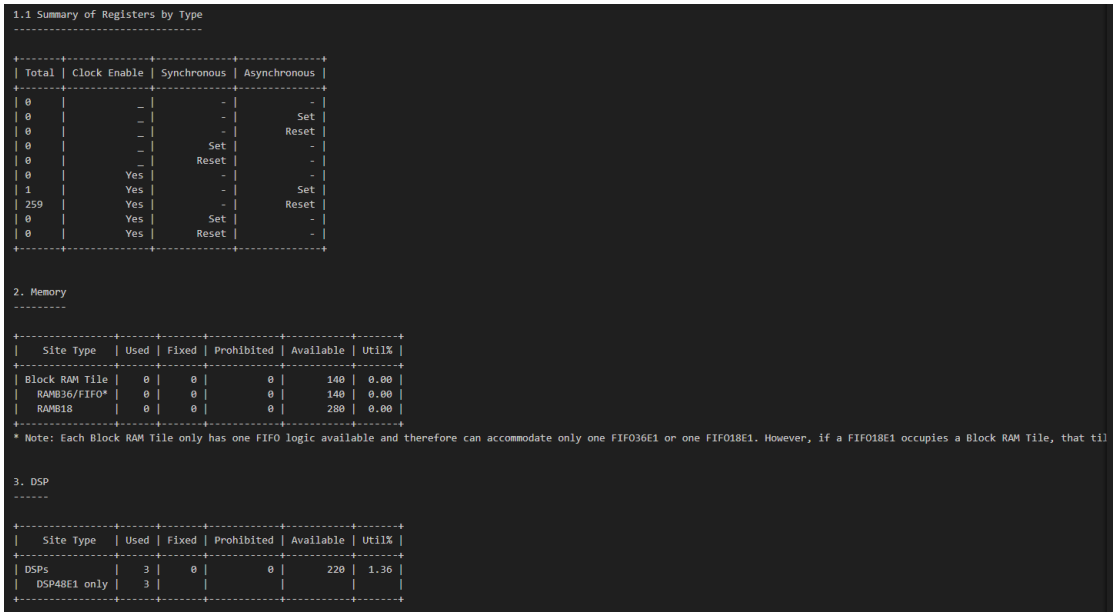
- AXI-STREAM Data In



- AXI-STREAM Data Out



Synthesis Report



1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
1	Yes	-	Set
259	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that til

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	220	1.36
DSP48E1 only	3				

Delay Path

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack (MET) :             1.767ns  (required time - arrival time)
  Source:                 tap_A_r_reg[5]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Destination:            sum_r_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@7.500ns period=15.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            15.000ns  (axis_clk rise@15.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        13.096ns  (logic 8.684ns (66.308%)  route 4.412ns (33.692%))
  Logic Levels:           12  (CARRY4=5 DSP48E1=2 LUT2=3 LUT3=1 LUT6=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 17.128 - 15.000 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock axis_clk rise edge)
                                                    0.000     0.000 r
                                                    0.000     0.000 r  axis_clk (IN)
                         net (fo=0)                 0.000     0.000    axis_clk
                                                                       r  axis_clk_IBUF_inst/I
                         IBUF (Prop_ibuf_I_O)       0.972     0.972 r  axis_clk_IBUF_inst/O
                         net (fo=1, unplaced)       0.800     1.771    axis_clk_IBUF
                                                                       r  axis_clk_IBUF_BUFG_inst/I
                         BUFG (Prop_bufg_I_O)       0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                         net (fo=260, unplaced)     0.584     2.456    axis_clk_IBUF_BUFG
                         FDCE                                          r  tap_A_r_reg[5]/C
  -------------------------------------------------------------------    -------------------
```

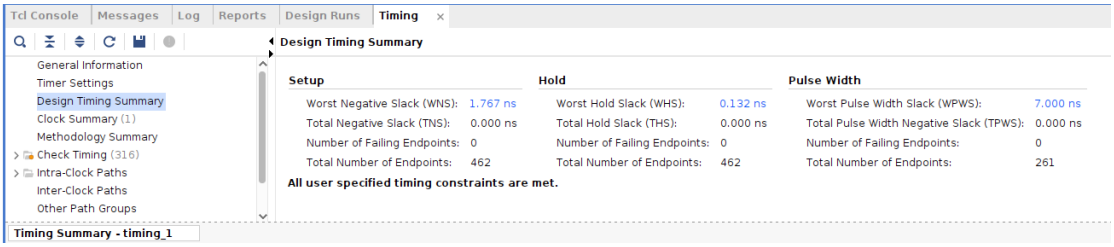
```
                                                                    -------------------
FDCE (Prop_fdce_C_Q)         0.478     2.934 r  tap_A_r_reg[5]/Q
net (fo=5, unplaced)         0.993     3.927    tap_A_OBUF[5]
                                                r  sum_w1_i_18/I0
LUT6 (Prop_lut6_I0_O)        0.295     4.222 r  sum_w1_i_18/O
net (fo=32, unplaced)        0.520     4.742    sum_w1_i_18_n_0
                                                r  sum_w1_i_1/I1
LUT3 (Prop_lut3_I1_O)        0.124     4.866 r  sum_w1_i_1/O
net (fo=2, unplaced)         0.800     5.666    sum_w1_i_1_n_0
                                                r  sum_w1__0/B[16]
DSP48E1 (Prop_dsp48e1_B[16]_PCOUT[47])
                             3.851     9.517 r  sum_w1__0/PCOUT[47]
net (fo=1, unplaced)         0.055     9.572    sum_w1__0_n_106
                                                r  sum_w1__1/PCIN[47]
DSP48E1 (Prop_dsp48e1_PCIN[47]_P[0])
                             1.518    11.090 r  sum_w1__1/P[0]
net (fo=2, unplaced)         0.800    11.890    sum_w1__1_n_105
                                                r  sum_r[19]_i_10/I0
LUT2 (Prop_lut2_I0_O)        0.124    12.014 r  sum_r[19]_i_10/O
net (fo=1, unplaced)         0.000    12.014    sum_r[19]_i_10_n_0
                                                r  sum_r_reg[19]_i_7/S[1]
CARRY4 (Prop_carry4_S[1]_CO[3])
                             0.533    12.547 r  sum_r_reg[19]_i_7/CO[3]
net (fo=1, unplaced)         0.009    12.556    sum_r_reg[19]_i_7_n_0
                                                r  sum_r_reg[23]_i_7/CI
CARRY4 (Prop_carry4_CI_CO[3])
                             0.117    12.673 r  sum_r_reg[23]_i_7/CO[3]
net (fo=1, unplaced)         0.000    12.673    sum_r_reg[23]_i_7_n_0
                                                r  sum_r_reg[27]_i_7/CI
CARRY4 (Prop_carry4_CI_O[3])
                             0.331    13.004 r  sum_r_reg[27]_i_7/O[3]
net (fo=1, unplaced)         0.618    13.622    sum_r_reg[27]_i_7_n_4
                                                r  sum_r[27]_i_3/I1
LUT2 (Prop_lut2_I1_O)        0.307    13.929 r  sum_r[27]_i_3/O
net (fo=1, unplaced)         0.000    13.929    sum_r[27]_i_3_n_0
                                                r  sum_r_reg[27]_i_2/S[3]
CARRY4 (Prop_carry4_S[3]_CO[3])
                             0.376    14.305 r  sum_r_reg[27]_i_2/CO[3]
net (fo=1, unplaced)         0.000    14.305    sum_r_reg[27]_i_2_n_0
                                                r  sum_r_reg[31]_i_3/CI
CARRY4 (Prop_carry4_CI_O[3])
                             0.331    14.636 r  sum_r_reg[31]_i_3/O[3]
net (fo=1, unplaced)         0.618    15.254    sum_r_reg[31]_i_3_n_4
                                                r  sum_r[31]_i_2/I0
LUT2 (Prop_lut2_I0_O)        0.299    15.553 r  sum_r[31]_i_2/O
net (fo=1, unplaced)         0.000    15.553    sum_w[31]
FDCE                                            r  sum_r_reg[31]/D
```

```
FDCE                                            r  sum_r_reg[31]/D
-------------------------------------------------------------------    -------------------

(clock axis_clk rise edge)
                            15.000    15.000 r
                             0.000    15.000 r  axis_clk (IN)
net (fo=0)                   0.000    15.000    axis_clk
                                                r  axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)         0.838    15.838 r  axis_clk_IBUF_inst/O
net (fo=1, unplaced)         0.760    16.598    axis_clk_IBUF
                                                r  axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)         0.091    16.689 r  axis_clk_IBUF_BUFG_inst/O
net (fo=260, unplaced)       0.439    17.128    axis_clk_IBUF_BUFG
FDCE                                            r  sum_r_reg[31]/C
clock pessimism              0.184    17.311
clock uncertainty           -0.035    17.276
FDCE (Setup_fdce_C_D)        0.044    17.320    sum_r_reg[31]
-------------------------------------------------------------------
required time                         17.320
arrival time                         -15.553
-------------------------------------------------------------------
slack                                  1.767
```

Resource Usage

- Timing Report



- Constraint

```
create_clock -period 15 -name axis_clk -waveform {0.000 7.500} [get_ports axis_clk]
```

感想

本次 LAB 隨然跟之前的流程差不多，但是須完成 Verilog 的實作，但由於本身並非本科系，所以花了好多時間才了解 FSM 的實作跟 Testbench 的撰寫，最後也是參考眾多他人的實作，完成本次的實驗，另外，由於缺乏相關開發經驗，所以本次 LAB 有與其他同一同討論系統框架，所以部分內容會有相似部分，謝謝。