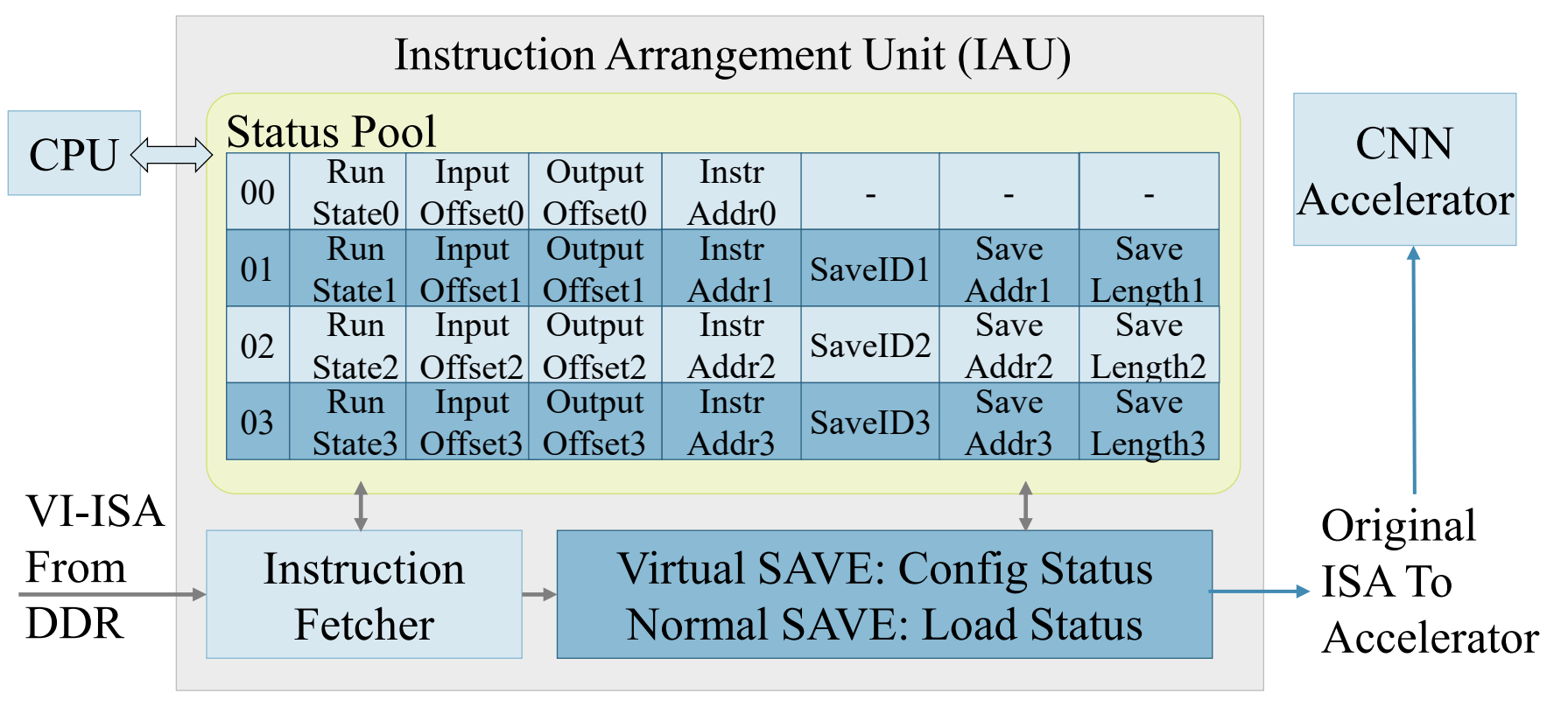
Instruction Arrangement Unit (IAU)
CPU
Status Pool
00
Run State0
Input Offset0
Output Offset0
Instr Addr0
-
-
-
01
Run State1
Input Offset1
Output Offset1
Instr Addr1
SaveID1
Save Addr1
Save Length1
02
Run State2
Input Offset2
Output Offset2
Instr Addr2
SaveID2
Save Addr2
Save Length2
03
Run State3
Input Offset3
Output Offset3
Instr Addr3
SaveID3
Save Addr3
Save Length3
CNN Accelerator
VI-ISA From DDR
Instruction Fetcher
Virtual SAVE: Config Status
Normal SAVE: Load Status
Original ISA To Accelerator