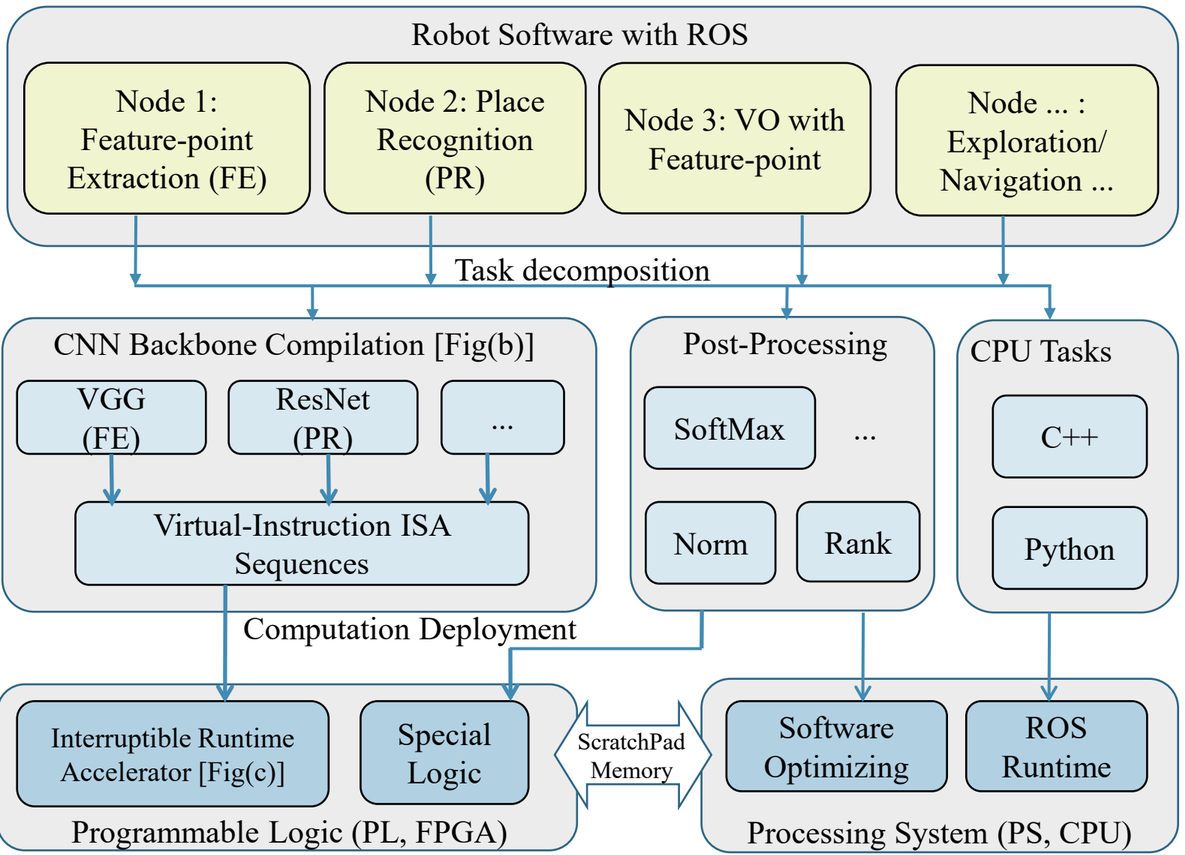
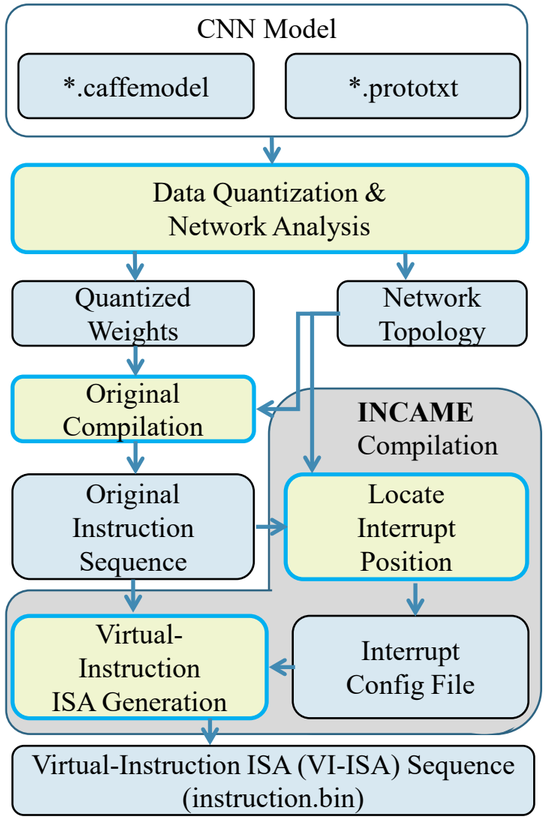
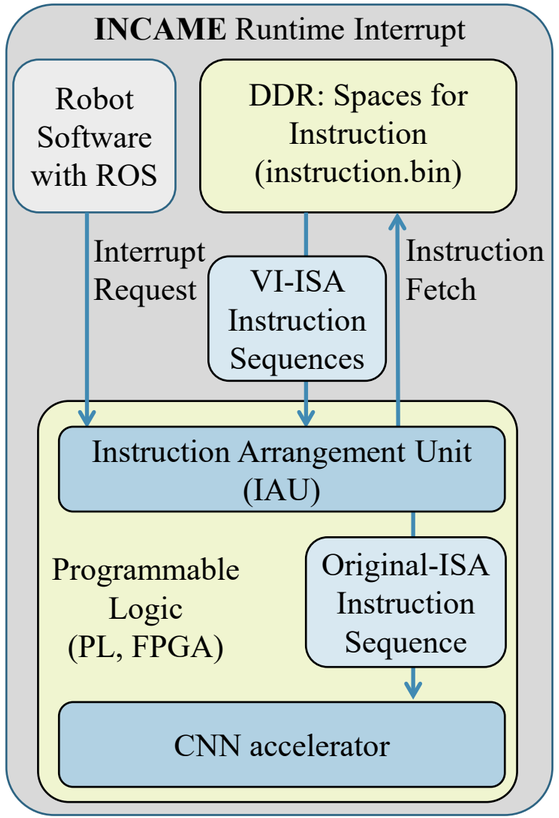


(a) At **task decomposition** step, the operations in different ROS nodes are separated to CNN backbones, CNN Post-Processing, and Other CPU Tasks. At **computation deployment**, the CNN backbone and Post-Processing are deployed with hardware modules and software optimizing.



(b) At **compilation** step, INCAME locates the interrupt location, adds virtual instructions, and generates the virtual-instruction ISA (VI-ISA) sequence.



(c) At **runtime**, IAU fetches VI-ISA instructions from DDR and translates the VI-ISA sequence to original ISA sequence executed on the accelerator.