

Lab 1: Introduction to High-Level Synthesis

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PART I: Vector Addition Example

pl_vecadd.cpp

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"

void pl_vecadd(float a[1024], float b[1024], float c[1024])
{
    #pragma HLS INTERFACE m_axi port=a offset=slave bundle=data0
    #pragma HLS INTERFACE s_axilite register port=a bundle=ctrl
    #pragma HLS INTERFACE m_axi port=b offset=slave bundle=data1
    #pragma HLS INTERFACE s_axilite register port=b bundle=ctrl
    #pragma HLS INTERFACE m_axi port=c offset=slave bundle=data2
    #pragma HLS INTERFACE s_axilite register port=c bundle=ctrl
    #pragma HLS INTERFACE s_axilite register port=return bundle=ctrl
    for (int i = 0; i < 1024; i += 1)
    {
        #pragma HLS pipeline
        c[i] = a[i] + b[i];
    }
}
```

Vitis HLS synthesis summary

The screenshot shows the Vitis HLS synthesis summary report for the project 'pl_vecadd'. The report is divided into several sections: General Information, Timing Estimate, Performance & Resource Estimates, and Performance Pragma.

General Information

- Date: Tue Nov 7 20:23:04 2023
- Version: 2023.1 (Build 3854077 on May 4 2023)
- Project: soc_lab1
- Solution: solution1 (Vivado IP Flow Target)
- Product family: zynqplus
- Target device: xck26-stvc784-21V-c

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Intensity	Trip Count	Pipelines	BRAM	DSF	FF	LU	URAM
pl_vecadd					1045	1.045E4		1046		no	12	2	3684	3004	0
VITIS_LOOP_14_1					1042	1.042E4	20	1	1024	yes	-	-	-	-	-

Performance Pragma

Vitis HLS Console

```
INFO: [HLS 200-111] Finished Generating all RTL models: CPU user time: 1 seconds, CPU system time: 0 seconds, Elapsed time: 1.227 seconds, current allocated memory: 154.324 MB.
INFO: [HLS 200-111] Finished Updating report files: CPU user time: 2 seconds, CPU system time: 1 seconds, Elapsed time: 2.533 seconds, current allocated memory: 162.289 MB.
INFO: [VHDL 288-304] Generating VHDL RTL for pl_vecadd.
INFO: [VLOG 209-307] Generating Verilog RTL for pl_vecadd.
INFO: [HLS 200-796] **** Loop Constraint Status: All loop constraints were satisfied.
INFO: [HLS 200-789] **** Estimated Fmax: 136.99 MHz.
INFO: [HLS 200-111] Finished Command csynth design CPU user time: 5 seconds, CPU system time: 1 seconds, Elapsed time: 52.354 seconds, current allocated memory: 50.262 MB.
INFO: [HLS 200-112] Total CPU user time: 7 seconds, Total CPU system time: 2 seconds, Total elapsed time: 59.847 seconds, peak allocated memory: 162.359 MB.
Finished C synthesis.
```

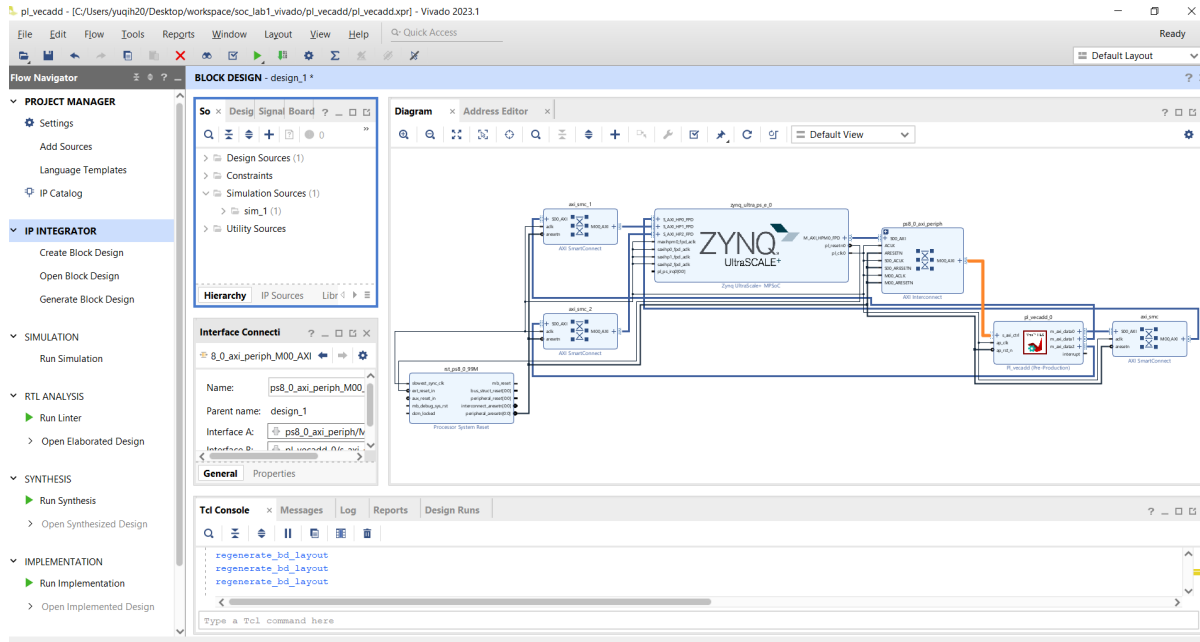
Latency(Cycles): 1045

Latency(ns): 1.045E4

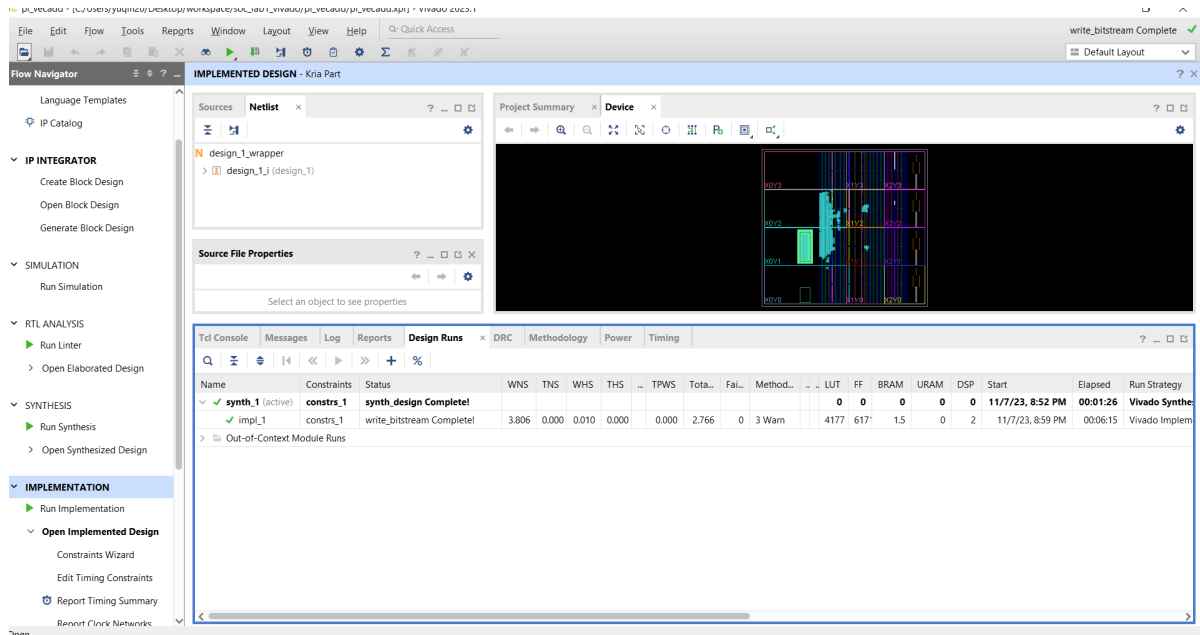
LUT:3004

Vivado post-implementation summary

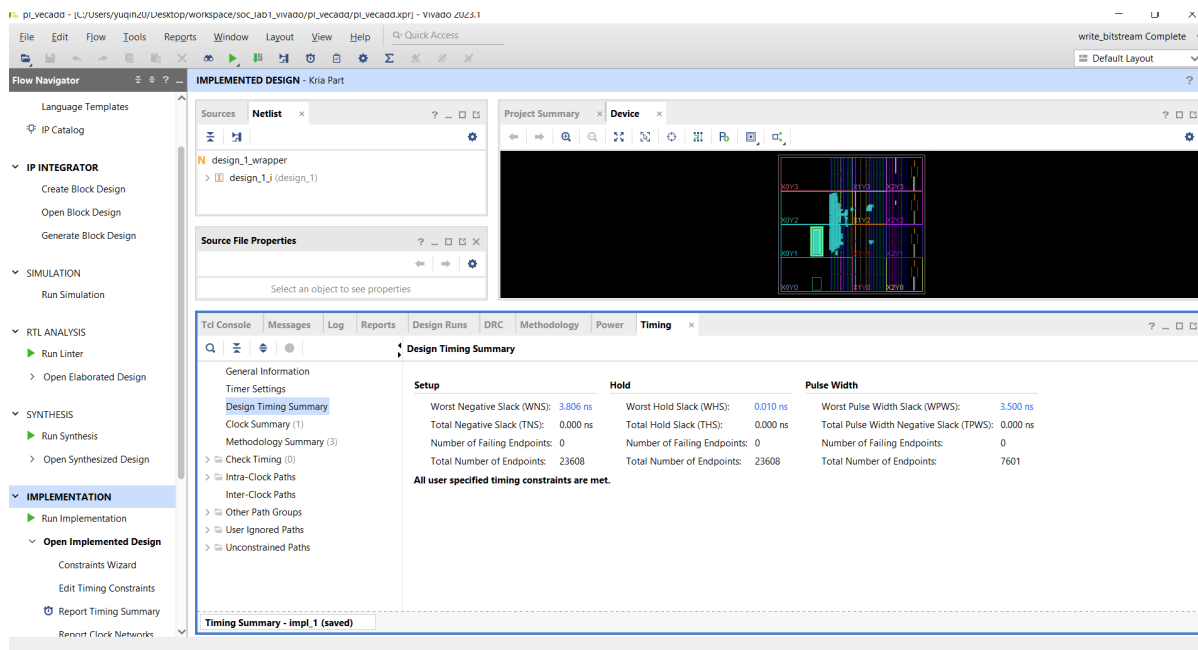
Block Design:



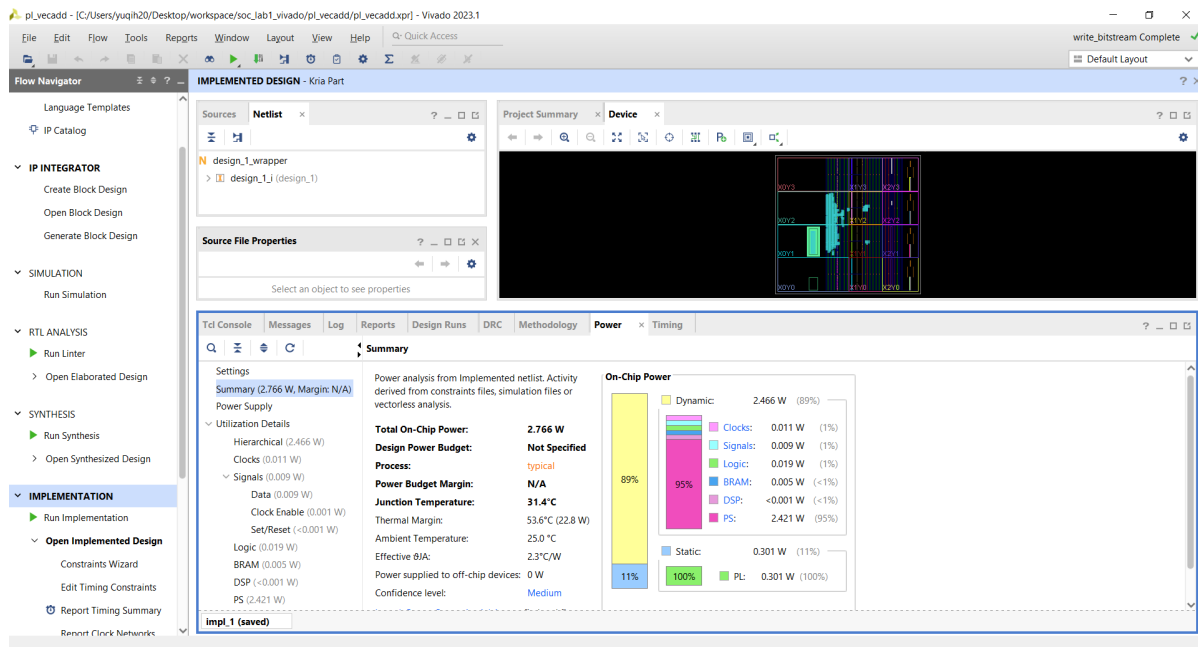
Runs:



Timing:



Power:



PART II: Matrix Multiplication

Plain:

matmual_plain.cpp

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"

#define M 16
#define K 16
#define N 16

void matmul_plain(int A[M][K], int B[K][N], int AB[M][N]) {
    #pragma HLS INTERFACE m_axi port=A offset=slave bundle=data0
```

```
#pragma HLS INTERFACE s_axilite register port=A bundle=ctrl1
#pragma HLS INTERFACE m_axi port=B offset=slave bundle=data1
#pragma HLS INTERFACE s_axilite register port=B bundle=ctrl1
#pragma HLS INTERFACE m_axi port=AB offset=slave bundle=data2
#pragma HLS INTERFACE s_axilite register port=AB bundle=ctrl1
#pragma HLS INTERFACE s_axilite register port=return bundle=ctrl1
```

```
for (int i = 0; i < M; i++) {
    for (int j = 0; j < N; j++) {
        int sum = 0;
        for (int k = 0; k < K; k++) {
            sum += A[i][k] * B[k][j];
        }
        AB[i][j] = sum;
    }
}
```

Vitis HLS synthesis summary

Vitis HLS 2023.1 - matrix_mult (C:\Users\yuqih20\Desktop\eeecs298_soc\soc_lab1\matrix_mult)

File Edit Project Solution Window Help

Explorer x Module Hierarchy x matmul_plain.cpp x Synthesis Summary(solution1) x

matrix_mult

- Includes
 - matmul_plain.cpp
 - Test Bench
 - solution1

Synthesis Summary Report of 'matmul_plain'

General Information

Date: Fri Nov 10 18:59:43 2023
Version: 2023.1 (Build 3854077 on May 4 2023)
Project: matrix_mult

Solution: solution1 (Vivado IP Flow Target)
Product family: zynqplus
Target device: xck26-slvc/84-2LV-c

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSF	FF	LUT	URAM	
matmul_plain	!! Violation			-	4114	4.114E4		-	4115	-	no	12	3	5117	4574	0
VITIS_LOOP_19_1_VITIS_LOOP_20_2	!! Violation	Memory Dependen 1		-	4111	4.111E4		32	16	256	yes	-	-	-	-	-

Performance Pragma

Vitis HLS Console

INFO: [HLS 200-1603] Design has inferred MAXI bursts and missed bursts, see Vitis HLS GUI synthesis summary report for detailed information.
INFO: [HLS 200-111] Finished Updating report files: CPU user time: 1 seconds. CPU system time: 0 seconds. Elapsed time: 2.623 seconds; current allocated memory: 164.984 MB.
INFO: [VHDL 208-384] Generating VHDL RTL for matmul_plain.
INFO: [VLOG 209-387] Generating Verilog RTL for matmul_plain.
INFO: [HLS 200-790] **** Loop Constraint Status: All loop constraints were NOT satisfied.
INFO: [HLS 200-789] **** Estimated Fmax: 136.99 MHz
INFO: [HLS 200-111] Finished Command csynth_design CPU user time: 6 seconds. CPU system time: 1 seconds. Elapsed time: 42.927 seconds; current allocated memory: 57.805 MB.
INFO: [HLS 200-112] Total CPU user time: 8 seconds. Total CPU system time: 2 seconds. Total elapsed time: 45.437 seconds; peak allocated memory: 165.062 MB.
Finished C synthesis.

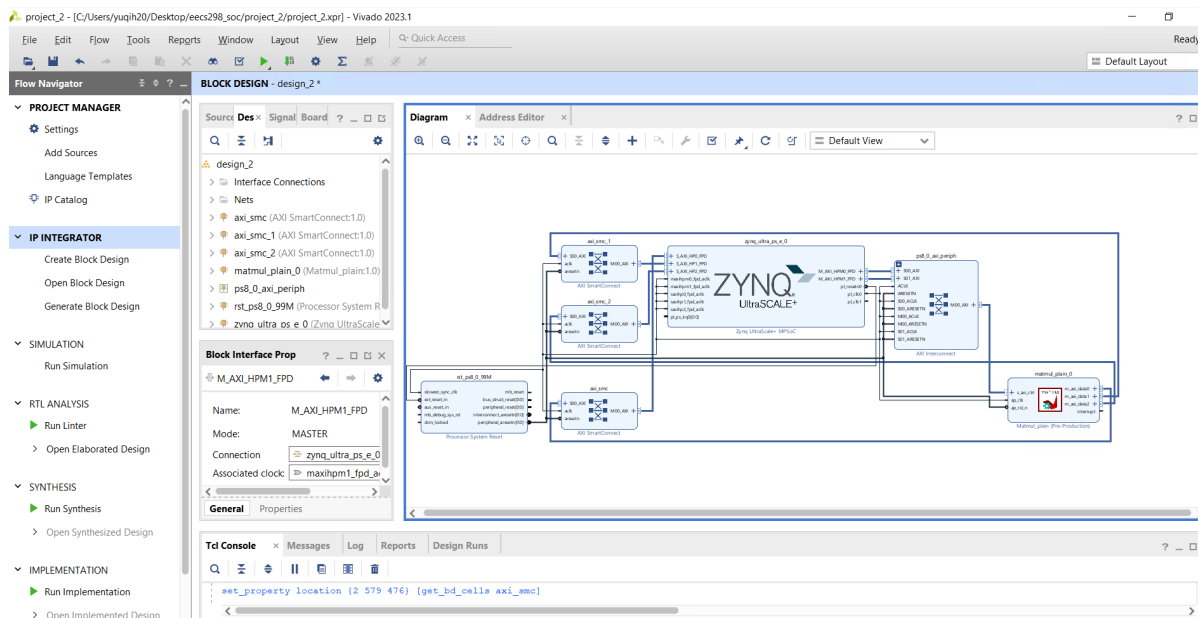
Latency(Cycles): 4114

Latency(ns): 4.114E4

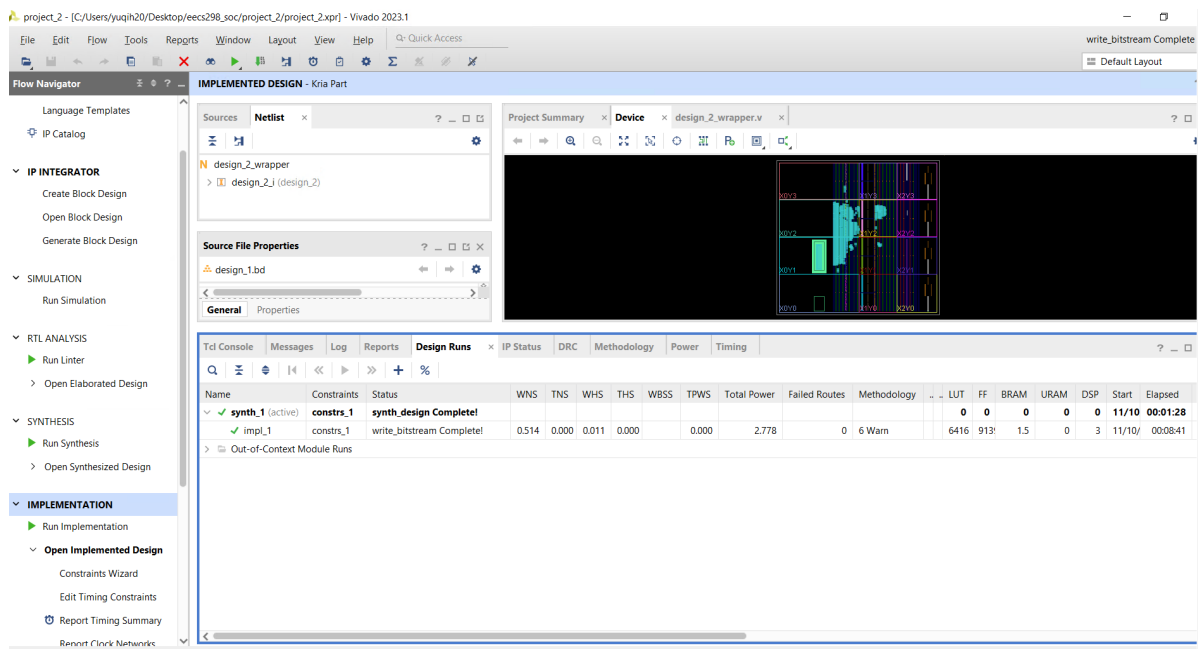
LUT:4574

Vivado post-implementation summary

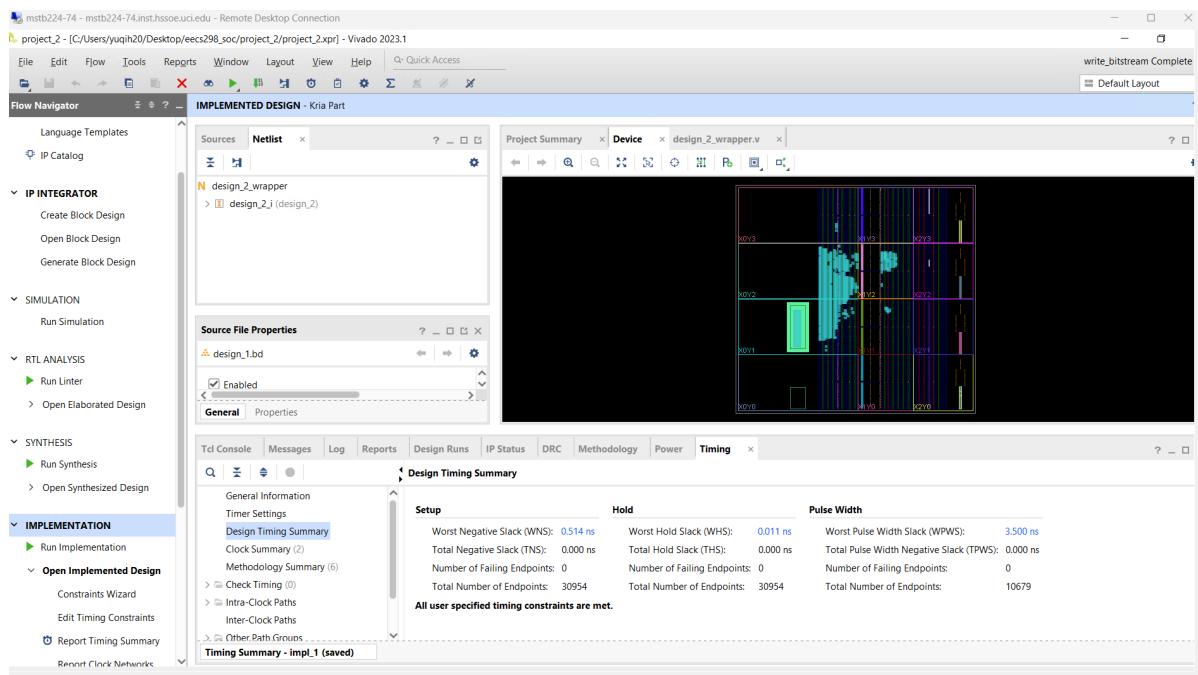
Block Design:



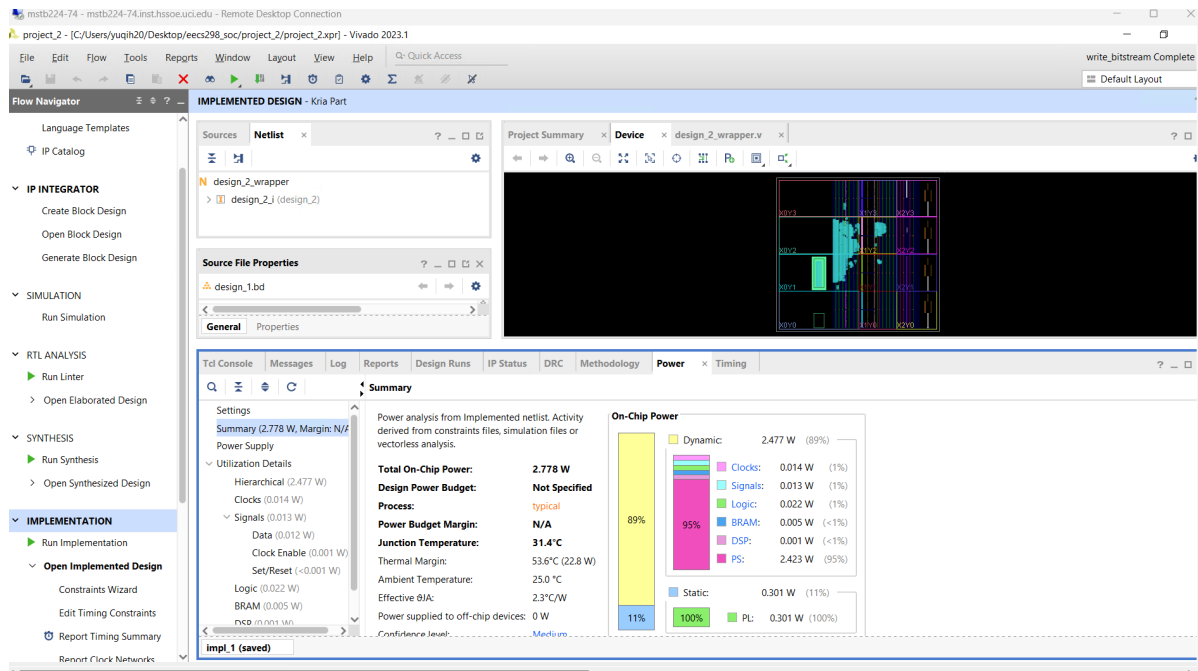
Runs:



Timing:



Power:



Optimized:

matmul_optimized.cpp

```
#include "ap_int.h"
#include "ap_fixed.h"
#include "hls_math.h"

#define M 16
#define K 16
#define N 16

void matmul_optimized(int A[M][K], int B[K][N], int AB[M][N]) {
    #pragma HLS INTERFACE m_axi port=A offset=slave bundle=data0
    #pragma HLS INTERFACE s_axilite port=A bundle=ctrl
    #pragma HLS INTERFACE m_axi port=B offset=slave bundle=data1
    #pragma HLS INTERFACE s_axilite port=B bundle=ctrl
    #pragma HLS INTERFACE m_axi port=AB offset=slave bundle=data2
    #pragma HLS INTERFACE s_axilite port=AB bundle=ctrl
    #pragma HLS INTERFACE s_axilite port=return bundle=ctrl

    #pragma HLS ARRAY_PARTITION variable=A complete dim=2
    #pragma HLS ARRAY_PARTITION variable=B complete dim=1

    // Main matrix multiplication loop
    for (int i = 0; i < M; i++) {
        for (int j = 0; j < N; j++) {
            #pragma HLS PIPELINE
            int sum = 0;
            for (int k = 0; k < K; k++) {
                sum += A[i][k] * B[k][j];
            }
        }
    }
}
```

```

        AB[i][j] = sum;
    }
}

```

Vitis HLS synthesis summary

Vitis HLS 2023.1 - matrix_mult (C:\Users\yuqih20\Desktop\eees29oc_soc_lab1\matrix_mult)

File Edit Project Solution Window Help

Explorer Module Hierarchy

- matrix_mult
 - Includes
 - Source
 - matmul_optimized.cpp
 - matmul_plain.cpp
 - Test Bench
 - solution1

Synthesis Summary Report of 'matmul_optimized'

General Information

Date: Fri Nov 10 19:56:06 2023
Version: 2023.1 (Build 3854077 on May 4 2023)
Project: matrix_mult

Solution: solution1 (Vivado IP Flow Target)
Product family: zynquplus
Target device: xck26-stvc784-2LV-c

Timing Estimate

Target	Estimated	Uncertainty
10.00 ns	7.300 ns	2.70 ns

Performance & Resource Estimates

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency/cycles	Latency/ns	Iteration Latency	Interval	Trip Count	Pipelined	BRA#	DSP	F#	LUT	URAM
* @ matmul_optimized			-	-	510	5.100E3	-	511	-	no	132	48	34011	29193	0
↳ VITIS_LOOP_23_1			-	-	496	4.960E3	31	-	16	no	-	-	-	-	-

Performance Pragma

Vitis HLS Console

```
INFO: [HLS 200-111] Finished generating all RTL models: CPU user time: 1 seconds, CPU system time: 0 seconds, Elapsed time: 2.943 seconds; current allocated memory: 190.7 MB
INFO: [HLS 200-1603] Design has inferred MAXI bursts and missed bursts, see Vitis HLS GUI synthesis summary report for detailed information.
INFO: [HLS 200-111] Finished Updating report files: CPU user time: 47 seconds, CPU system time: 1 seconds, Elapsed time: 50.279 seconds; current allocated memory: 231.508 MB
INFO: [WDL 208-304] Generating VHDL RTL for matmul_optimized.
INFO: [VLOG 209-307] Generating Verilog RTL for matmul_optimized.
INFO: [HLS 200-790] **** Loop Constraint Status: All loop constraints were satisfied.
INFO: [HLS 200-789] **** Estimated Fmax: 136.99 MHz
INFO: [HLS 200-111] Finished Command csynth_design CPU user time: 55 seconds, CPU system time: 2 seconds, Elapsed time: 131.343 seconds; current allocated memory: 121.824 MB
INFO: [HLS 200-112] Total CPU user time: 57 seconds. Total CPU system time: 3 seconds. Total elapsed time: 134.103 seconds; peak allocated memory: 231.508 MB.
Finished C synthesis.
```

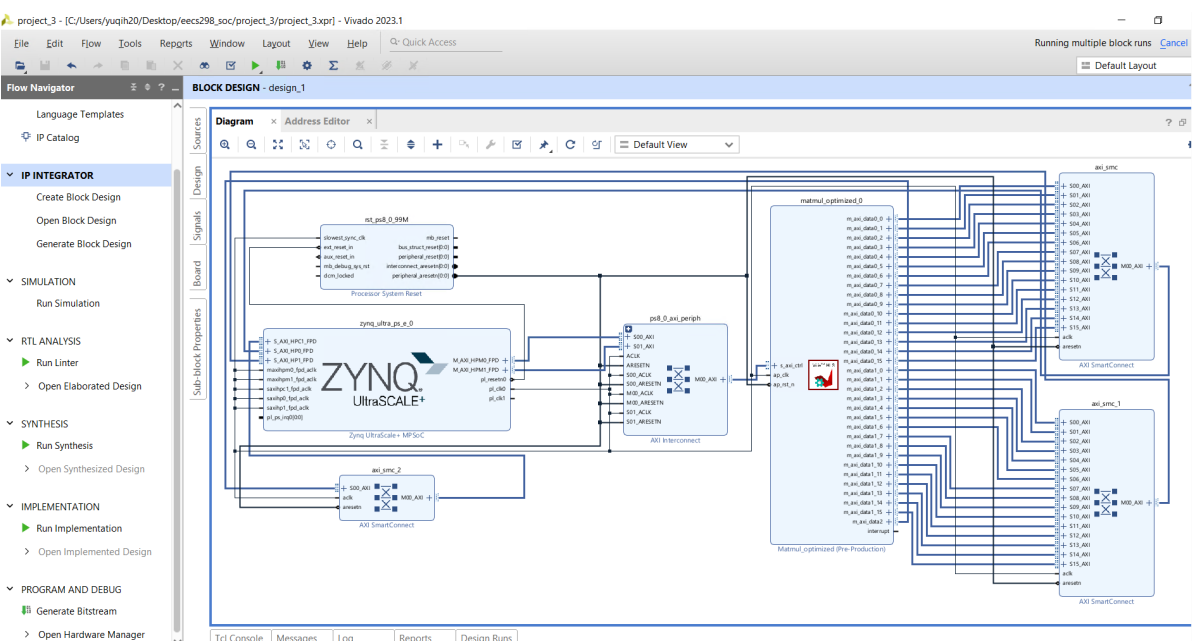
Latency(Cycles): 510

Latency(ns): 5.100E3

LUT:29193

Vivado post-implementation summary

Block Design:



Runs:

project_3 - [C:/Users/yuqih20/Desktop/eecs298_soc/project_3/project_3.xpr] - Vivado 2023.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

Flow Navigator

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Run Linter

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

IMPLEMENTATION

Run Implementation

Open Implemented Design

Constraints Wizard

Edit Timing Constraints

Report Timing Summary

Sources

Netlist

design_1_wrapper

design_1_j (design_1)

Sub-block Properties

Select an object to see properties

Project Summary

Device

Tcl Console

Messages

Log

Reports

Design Runs

DRC

Methodology

Power

Timing

Name	Constraints	Status	WNS	TNS	WHS	THS	...	Tot..	Methodology	F...	...	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1 (active)	constrs_1	synth_design Complete!	2.107	0.000	0.010	0.000	0.00	3.219	7 Warn	0		40649	660	16.5	0	0	11/10	00:01:48	Vivado Synthesis
impl_1	constrs_1	write_bitstream Complete!															11/10/	00:28:35	Vivado Implementa

Out-of-Context Module Runs

Timing:

project_3 - [C:/Users/yuqih20/Desktop/eecs298_soc/project_3/project_3.xpr] - Vivado 2023.1

File Edit Flow Tools Reports Window Layout View Help Quick Access

write_bitstream Complete

Default Layout

Flow Navigator

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Run Linter

Open Elaborated Design

SYNTHESIS

Run Synthesis

Open Synthesized Design

IMPLEMENTATION

Run Implementation

Open Implemented Design

Constraints Wizard

Edit Timing Constraints

Report Timing Summary

Report Clock Networks

Sources

Netlist

design_1_wrapper

design_1_j (design_1)

Sub-block Properties

Select an object to see properties

Project Summary

Device

Tcl Console

Messages

Log

Reports

Design Runs

DRC

Methodology

Power

Timing

Design Timing Summary

General Information

Timer Settings

Design Timing Summary

Clock Summary (2)

Methodology Summary (7)

Check Timing (0)

Intra-Clock Paths

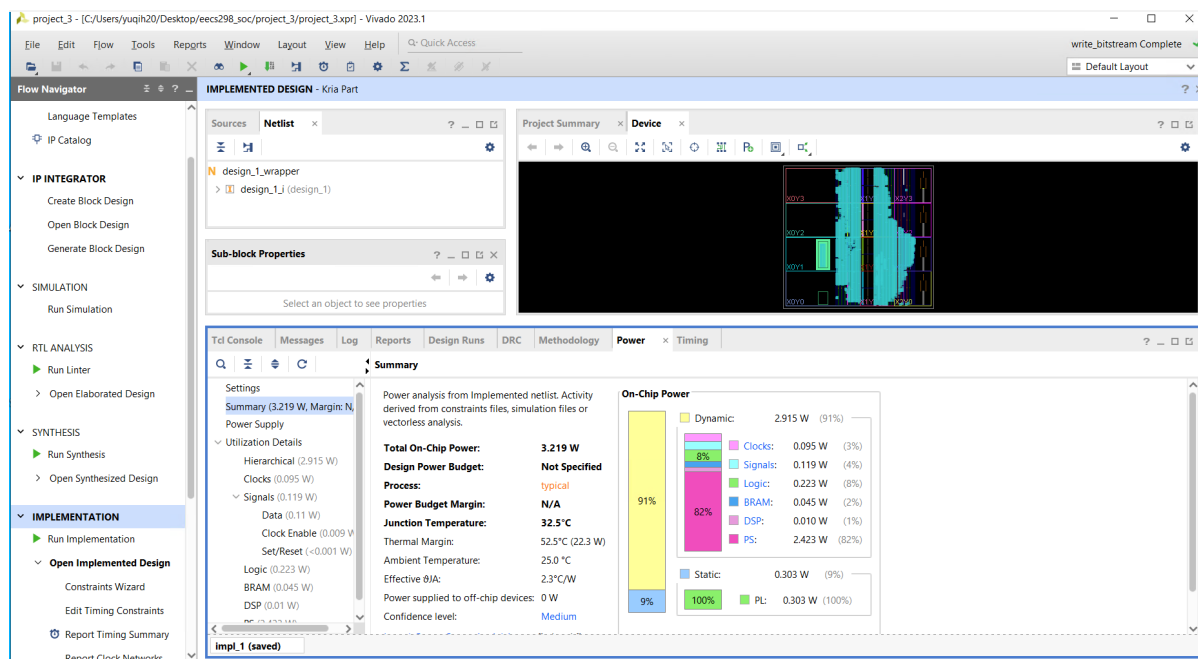
Inter-Clock Paths

Timing Summary - impl_1 (saved)

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.107 ns	Worst Hold Slack (WHS): 0.010 ns	Worst Pulse Width Slack (WPWS): 3.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 247798	Total Number of Endpoints: 247798	Total Number of Endpoints: 79893

All user specified timing constraints are met.

Power:



Comparison:

Vitis C synthesis

Metric	Plain Version	Optimized Version
Latency (Cycles)	4114	510
Latency (ns)	4.114E4	5.100E3
LUT	4574	29193
FF	5117	34011

Vivado post-implementation:

Metric	Plain Version	Optimized Version
WNS	0.514	2.107
Total Power	2.778	3.219
LUT	6416	40649
FF	9139	66071
BRAM	1.5	16.5