

數位系統導論既實習

班級:資工一乙

學號:CBB113234

姓名:詹幼綺

程式碼內容:

```
module fulladd4(sum,c_out,a,b,c_in);
output [3:0]sum;
output c_out;
input [3:0]a,b;
input c_in;
wire c1,c2,c3;
fulladd fa0(sum[0],c1,a[0],b[0],c_in);
fulladd fa1(sum[1],c2,a[1],b[1],c1);
fulladd fa2(sum[2],c3,a[2],b[2],c2);
fulladd fa3(sum[3],c_out,a[3],b[3],c3);
endmodule

module mux2_1(res,in0,in1,S);
output res;
input in0,in1;
input S;
wire S_n;
not not1(S_n,S);
and and1(S_n,in0,S,in0);
and and2(S,in1,S,in1);
or or1(res,S_n,in0,S,in1);
endmodule

module fulladd(sum,c_out);
output sum,c_out;
input a,b,c_in;
wire s1,c1,c2;
xor(s1,a,b);
and(c1,a,b);
xor(sum,s1,c_in);
and(c2,s1,c_in);
or(c_out,c2,c1);
endmodule

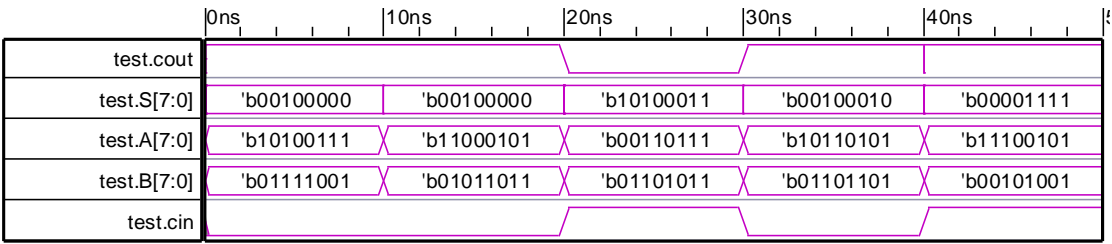
module mux2_1_4bit(res,in0,in1,S);
output [3:0]res;
input [3:0]in0,in1;
input S;
assign res=S?in1:in0;
endmodule

module carry(Cout,S,A,B,Cin);
output Cout;
output [7:0]S;
input [7:0]A,B;
input Cin;
wire C_out,Cout0,Cout1;
wire [3:0]a,b;
fulladd4 fa0(S[3:0],C_out,A[3:0],B[3:0],Cin);
fulladd4 fa1(a,Cout0,A[7:4],B[7:4],1'b0);
fulladd4 fa2(b,Cout1,A[7:4],B[7:4],1'b1);
mux2_1_4bit mux0(S[7:4],a,b,C_out);
mux2_1 mux1(Cout,Cout0,Cout1,C_out);
endmodule
```

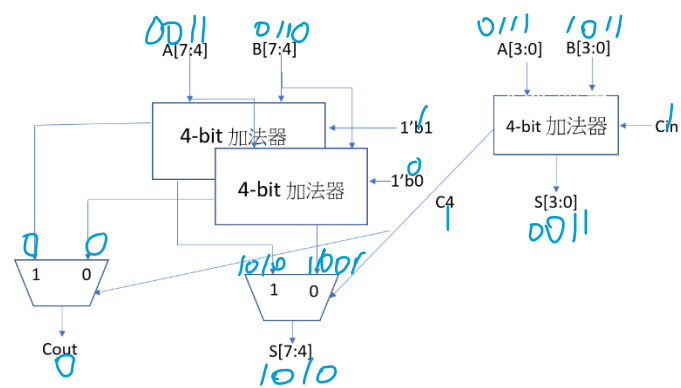
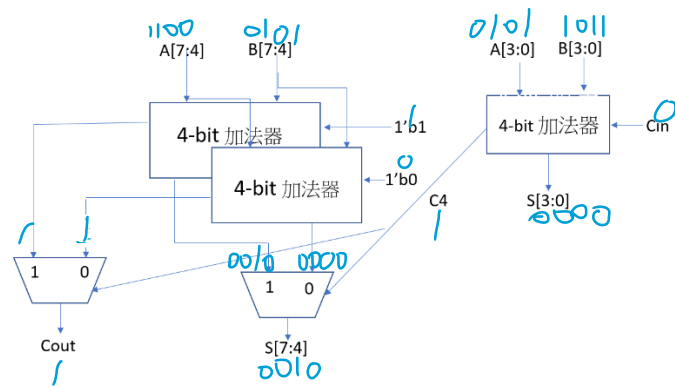
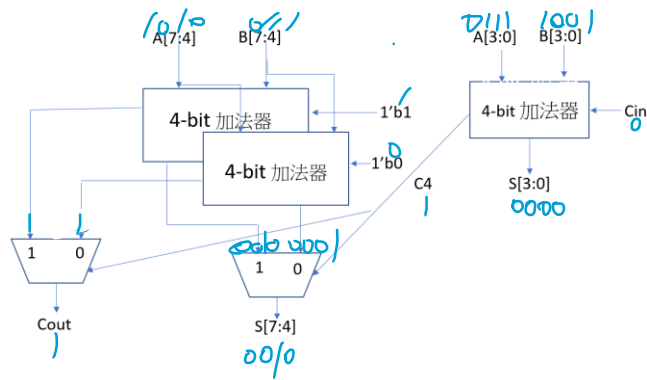
測試檔內容:

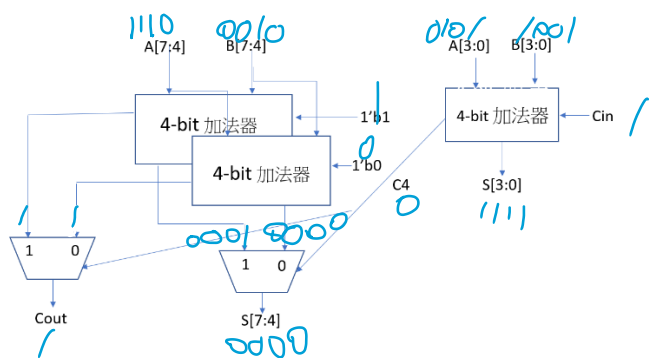
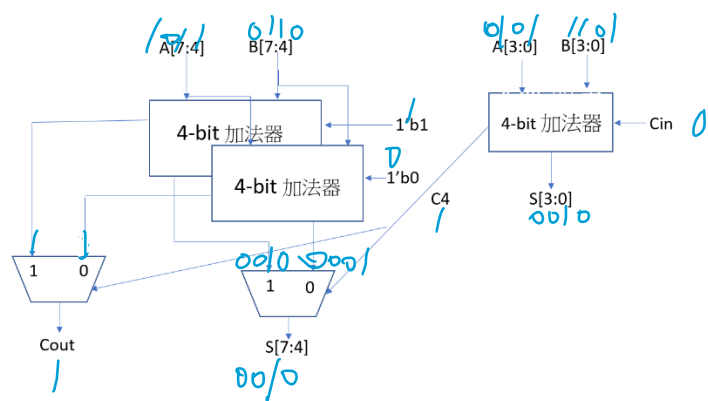
```
module test;
wire cout;
wire [7:0]S;
reg [7:0]A,B;
reg cin;
carry carry1(cout,S,A,B,cin);
initial begin
    A[7:0]=8'b10100111;
    B[7:0]=8'b01111001;
    cin=0;
#10
    A[7:0]=8'b11000101;
    B[7:0]=8'b01011011;
    cin=0;
#10
    A[7:0]=8'b00110111;
    B[7:0]=8'b01101011;
    cin=1;
#10
    A[7:0]=8'b10110101;
    B[7:0]=8'b01101101;
    cin=0;
#10
    A[7:0]=8'b11100101;
    B[7:0]=8'b00101001;
    cin=1;
#10
end
```

波形圖：



手寫測試檔:





心得:

OK!