Internals-01

Microcontroller and Embedded System.

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(2b).

RISC	CISC
Instruction size fixed	Instruction size varies
4 bytes of instruction length.	1,2,3 or 4 bytes of instruction length.
Less number of instructions	More number of instructions
It is easy and quick to decode.	It slow & serial to decode.
It has medium instruction execution speed.	It is slow instruction execution.
It has simple hardware	It has complicated hardware.
Rarely accessing memory	frequent access of memory
It has many registers, general purpose registers.	It has few and special purpose registers.
Complex addressing modes are synthesized in software	supports complex addressing modes.
Ex:- Inter X86, Motorola 68000 series	Ex: ARM, 8051, ATMEL

2a). Banked Registers:-

All 37 registers in the register file of those 20 registers are hidden from a program at different times they are available only when the processor is in a particular mode. These registers are called banked registers.

These are identified by the shading the diagram. for EX: Abort mode has banked register, registers of a particular ~~Characteristic pos~~ mode are denoted by an underline character post fixed to the mode mnemonic / mode.

All processor modes except System mode have a set of associated bank registers that are subset of main 16 registers.

~~[illegible]~~ Interrupt request mode - r13 and r14 are accessed. r13 is changed to r13-irq and r14 → r14-irq in IR mode. The user mode registers r13-usr and r14-usr are not affected.

3a). ~~ARM~~ ARM CORE DATA FLOW:

The figure show Non-Neumann architecture ARM core data flow model. Here Data & instruction share same Bus. ~~ARM~~ ARM processor uses load-store architecture.

Load - Instruction copies data from memory to register.

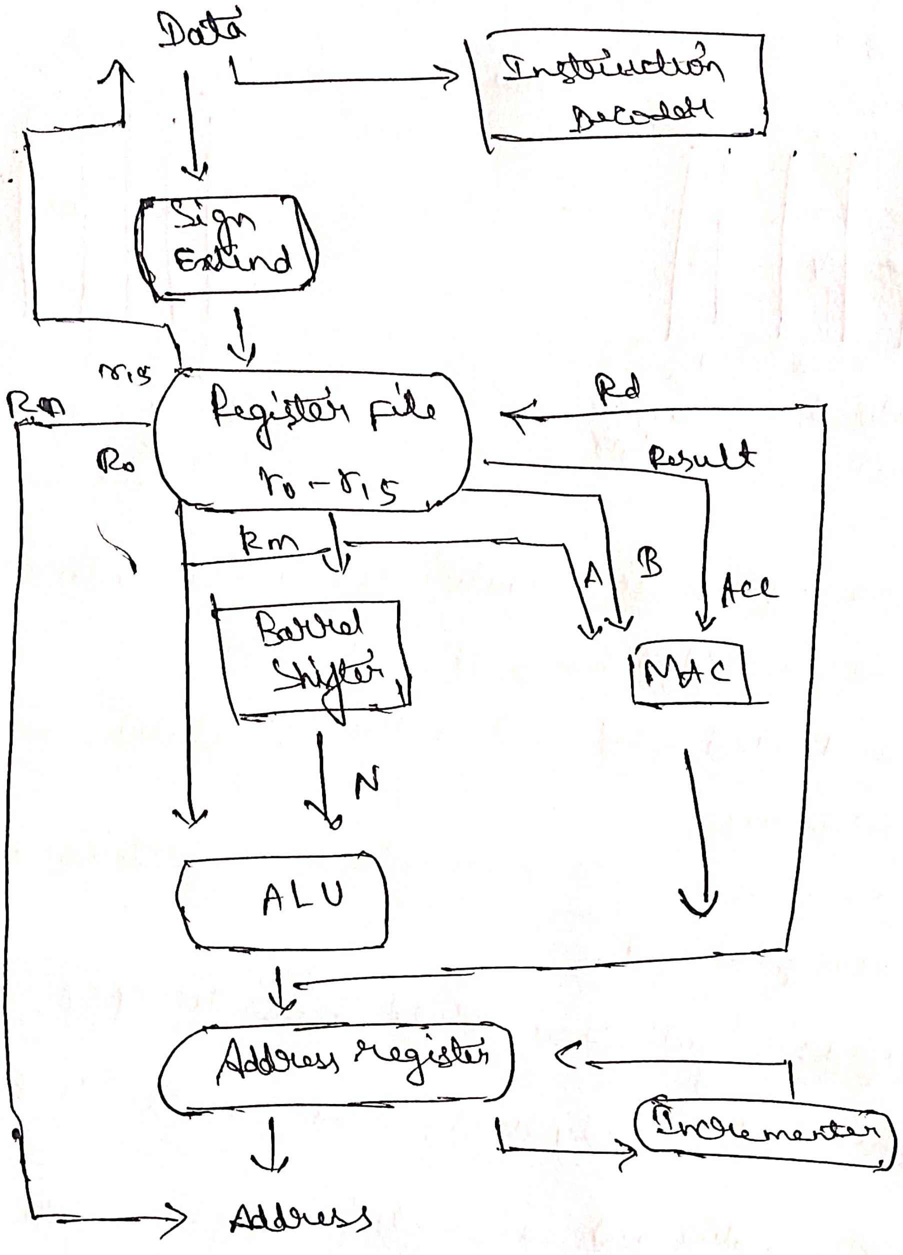
Store - copies data from register to memory.

Register file - It is a store bank of 32 bit register r0-r15

Sign Extend - It converts a signed 8 bit & 16 bit numbers to 32 bit values.

Instruction decoder:-

It translates instructions before they executed.



ARM has 2 sources registers Rm & Rn read from register file using Internal buses A & B.

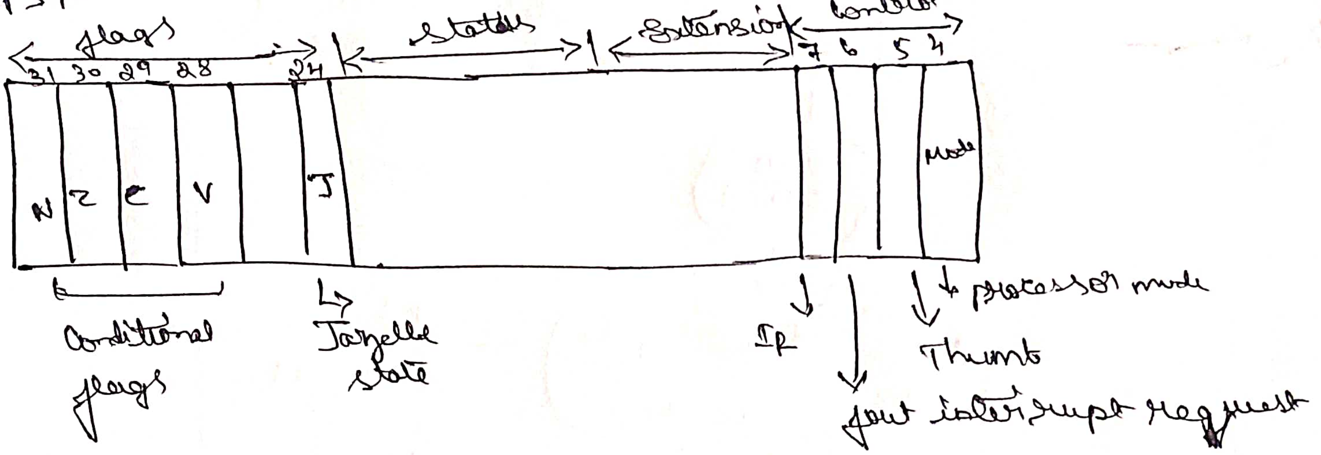
Data processing instruction write the result in Destination Register Rd. to the register file.

LOAD & STOR instructions use ALU to generate address.

The Contents of registers Rn is pre-processed in Barrel register before it enters ALU.

*The instruction updates the address register before the core reads or writes the next register value.

(3b) CPSR



- ARM uses CPSR to monitor and control internally operations
- CPSR is dedicated has 32 bit register
- It is divided into → controls, status, conditional flags and extensions.
- process modes :- Determines which registers are active priviliged and non priviliged.
- priviliged :- full read, write, acces to CPSR.
- Non - priviliged :- only read, read - write (conditional).
- processor status and instruction sets :- State of core determines which instruction set is executed.
- ~~IR~~ Interrupt mode :- ~~[illegible]~~ used to stop a specific instructions.
- Conditional flags :- N - negative : Results in negative.

  Z - Zero : Results in Zero.

  C - carry : carries a unsigned overflow.

  V - overflow : Carries a signed overflow.