Progress Report (4/12-5/1)

This week, we worked on completing our advanced features. The advanced features that were implemented, as well as the division of labor is as follows:

- Parameterized Cache (sets and ways): Neha (6)
- L2 Cache: Neha (implementation+testing), Mitchell (performance analysis) (2)
- OBL Prefetching: Neha (4)
- Victim Cache: Mitchell (6)
- Local Branch History: Yu (2)
- Global Branch History: Yu (3)
- Tournament Branch Predictor: Yu (1)
- BTB Jump support: Yu (1)
- 4-way set associative or higher BTB: Yu (3)
- Software Branch Prediction: Yu (2)

Since some of these features are mutually exclusive, there is no one processor performance number, but the performance of each of these features independently is available as part of the performance analysis.

For testing, we created a comprehensive test bench to test each of the advanced features as a DUT. In addition, for some of the features, we added additional assembly tests to test the added feature alongside the rest of the processor. We also verified that all the provided test code runs correctly with the additional features.

Roadmap:

Our next steps are to use our analysis to determine which of the advanced features best improved the performance of our processor and integrate those for the final competition runs. In addition, we will need to prepare our presentation and lab report.