

Progress Report (3/29-4/12)

Over the last two weeks, the main addition to our code was to integrate our MP3 cache into our design and add support for coremark. As of now, CMP 1-3 and Coremark all successfully run. The fmax and total power for our design as of now is given below. The current datapath for our design is given at the end of this document.

slack = 5.14

fmax = $1/(10\text{-slack}) * 1000 = 205.76 \text{ MHz}$

Clock cycle = $1/(205.76 \text{ MHz}) * 1000 = 4.86$

total power = $4.65\text{e}+03 \text{ uW}$

In addition, we worked on the designs for the advanced features. The division of work matches the implementation details described below. Mitchell also researched an improved control hazard detection implementation but came to the conclusion that the power increase of doing so will be substantial. As a result, this feature was put on hold.

Roadmap (4/12-4/26)

As our next step, we plan to start building and verifying the advanced features. The division of work is as follows:

Neha: L2+ cache system, 4-way set associative cache, parameterized cache

Mitchell: Victim cache

Yu: Local branch history table, global 2-level branch history table, tournament branch predictor software branch predictor model

Each member is responsible for the implementation and verification of their respective part. For verification, we intend to create a DUT for each of the added components in order to separate testing. Additionally, we will add performance counters where necessary.